# Wishbone bus arbiter and address decoder

Sébastien Bourdeauducq

December 2009

## 1 Specifications

This core allows up to several masters to communicate with up to several slaves on a shared Wishbone bus.

It takes care of bus arbitration and remapping of the slave base addresses. It is very simple and does not take care of priorities. Scheduling occurs when a master releases the bus, and then the next master which requested the bus takes ownership.

It is based on `wb_conbus` from OpenCores.

## 2 Using the core

All parameters and ports should be self-explanatory. No special care should be taken.

## Copyright notice