GEp SBS trigger and electronics update

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1 Experiment overview

2 Electronics inventory

2.1 Pipelined electronics

2.1.1 JLab Flash ADC 250

The JLab Flash ADC 250 is a VME 12 bit 250 MHZ Flash ADC with 16 channels. It can transfer data through the VME64X backplane in 2eSST protocol which can reach up to 200 MB/s, it can also transfer data through the VXS backplane which is serial multiline point to point protocol with data transfer up to 8 GBit/s per lane. Each FADC has 4 VXS lanes. It has 8 microsecond pipeline. It will be used for the Hadron Calorimeter readout to allow to produce a HCAL trigger by doing clustering of the FADC data in a dedicated logic module the VXS Trigger Processor (VTP).

2.1.2 F1 TDC

The JLAB F1 TDC is base on the F1 chip, it is a pipelined multihit pipelined TDC with 64 channels in low resolution mode 120 ps and 32 channel in high resolution mode of 60ps. It can be readout using the VME backplane also using the 2eSST transfer protocol for data rates up to 200 MB/s. It will be used for Neutron Form Factor experiment where the neutron momentum is measured by time of flight. The F1 TDC will supplement the FADC which typically can give a timing resolution of 0.3 ns.

2.1.3 SubSystem Processor

The SubSystem Processor is part of the standard JLAB pipeline electronics system. It is a VME64X board with 8 QSFP optical port with VME 2eSST capability (200 MB/s) and VXS connectivity. The initial goal of the SSP was to gather data from different crates of FADC to concentrate the data to a single logic module Global Trigger Processor (GTP) which is superseded by the VXS Trigger Processor (VTP). Each optical link can transfer up 6.25 Gb/s giving a

25 GBit/s bandwidth for each QSFP connector the board can send data to the VTP using up to 4 VXS lines with each line having a 6.25 Gbit/s bandwith. Since this module is capable of reading a lot of data in parallel it will also be used to readout the GEM electronics using their optical cable. Data processing for improved zero suppression will be done by the SSP FPGA.

2.1.4 VETROC

The VXS Electron Trigger Read Out Controller (VETROC) is a board to generate an electron trigger from a silicton strip detector. It was designed as a flexible 192 channels pipelined input output/register compatible with JLAB pipeline electornics system. It allows to have the status of each of its input at 250 MHz sampling which can be used for trigger purpose in conjunction with the FADC data.

2.1.5 VXS Trigger Processor

The JLAB pipeline system relies on the VXS bus to transfer the FADC data to a central module called General Trigger Processor (GTP) where the logic involving all the FADC channels can be processed. A new version of this module with additionnal optical link on the front panel and VXS lines on the back was designed and called VXS Trigger Processor (VTP).

2.2 Fastbus electronics

2.2.1 Lecroy 1881M ADC

The electromagnetic calorimeter having a large number of channel will be readout using the Fastbus 1881M. It is a high Density, 64 Channels Per FASTBUS Slot 13 bit integrating ADC. It has a conversion Time of 12 sec in 13-Bit Mode (9 sec in 12-Bit Mode) a fast clear is possible to allow a L1 L2 logic reducing the dead time due to conversion. It can be programmed to perform online pedestal suppression. It has a buffer up 64 Events. Theoretical data transfer is up to 40 MB/s with an actual sustained rate of 15 MB/s. A fast clear can be issued and the module is ready to register another trigger after 1 μs.

2.2.2 Lecroy 1877S TDC

All other hit based detectors (CDET, GRINCH) will be read with Fastubs 1877S Multihit Time-to-Digital Converter with Data Supression.It is a High Density, 96 Channels Per FASTBUS Slotwith 0.5 ns resolution. It is a multhit TDC with up to 16 Hits/Channel and it can detect rising and/or falling edge which will allow to measure the amplitude of the signal with time over threshold information. It can hold up to 8 events in its buffer. The module can define windows for signal to be recorded in 4ns steps reducing the amount of data from accidentals. It can hold up to 8 Events in its buffer. Fast clear after 1 μs 300 ns after stop.

3 Proton Form Factor

3.0.1 ECAL trigger

In Fig. 1, the left plot shows the distribution of events at the front of the ECal and overlayed on the individual blocks. The middle plot shows the groups of 2x4 blocks (outlined in red) which will go into the sum of 8 modules. Around the edges the groups include less than 8 blocks (outlined in green). There are a total of 219 sum of 8 modules needed. The sum of 8 modules pass the individual analog signal of each block to a connector in the back of the module. A cable goes from this connector goes to a nearby patch panel on the ECal platform. The patch panel goes to a long 500ns delay cable which brings the signal to another patch panel in the electronics hut. This patch panel changes from the individual BNC cables into a 16 channel ribbon cable which goes into the 1881M ADC. Table 1 gives the total propagation time of the individual signal from each block along with the breakdown into the different components.

For the formation of the trigger, the sum of 8 modules have 6 outputs of the summed signal. In the right plot of Fig. 1, the groups of 32 blocks which sum 4 groups of 8 blocks are indicated by purple filled circles at the intersection of 4 groups of 8. The group of 32 blocks overlap by two groups of 8 in both horizontal and vertical directions. So most of the groups of 8 have to go to 4 groups of 32. At the edges the groups of 8 feed into two groups of 32. There are 192 groups of 32. The output of the groups of 32 would go into 16 channel discriminators. A total of twelve 16-channel discriminators would be needed. The outputs of the discriminator would go into a 16-channel mixed logic unit to produce an "OR" for each set of 16 inputs. The 12 "OR" signals would go into a final 16-channel mixed logic unit to a trigger that needs to be sent to the Trigger Supervisor as the Level One trigger. A 50m fast R8 cable will bring the trigger from the ECal platform to the Trigger Supervisor which will be located in a VXS crate in the electronics hut. The Trigger Supervisor takes 40ns to produce the ADC gate and the cable from the Trigger Supervisor to the trigger distribution card in the back of the FASTBUS crate takes 25ns. The total time is 391ns which is 180ns less than the 571ns for the propagation time of the individual signals to the ADC.

Cable length from PMT to sum of 8 module	40ns
Sum of 8 module transit time	10ns
Cable from back of the Sum of 8 module to patch panel on ECal	6ns
Cable from ECal patch panel to patch panel in electronics hut	500ns
Ribbon Cable from patch panel on ECal	15ns
Total time	571ns

Table 1: The contributions to total propagation time of the ECal calorimeter signals.

Cable length from PMT to sum of 8 module	40ns
Sum of 8 module transit time	10ns
Cable from Sum of 8 module to FI/FO for group of 32	24ns
FI/FO module transit time	10ns
Cable from FI/FO to the 16 channel discriminator	4ns
16 channel discriminator transit time	10ns
Cable from the 16 channel discriminator to 16 channel mixed logic unit	4ns
16 channel mixed logic unit transit time	10ns
Cable from the 16 channel mixed logic units to final 16 channel mixed logic unit	4ns
16 channel mixed logic unit transit time	10ns
50M fast cable from the ECal platform to Trigger Supervisor	200ns
Transit time in TS to produce the ADC gate	40ns
Cable from TS to logic fan	6ns
Logic fan	10ns
Logic fan to FASTBUS crate	25ns
Total time	407 ns

Table 2: The contributions to total time formation of the ECal Level One trigger sued as the ADC gate.

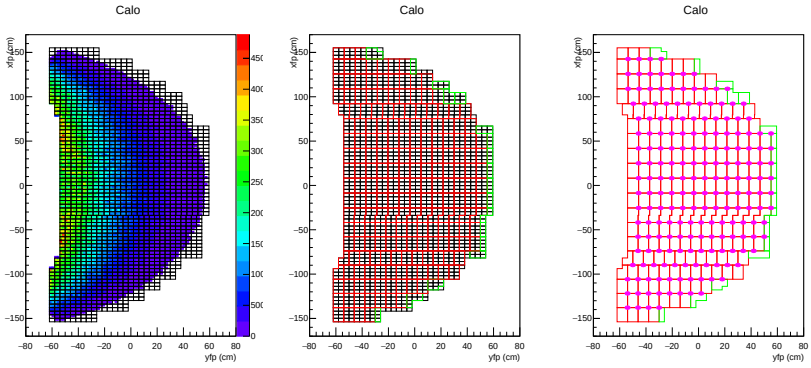
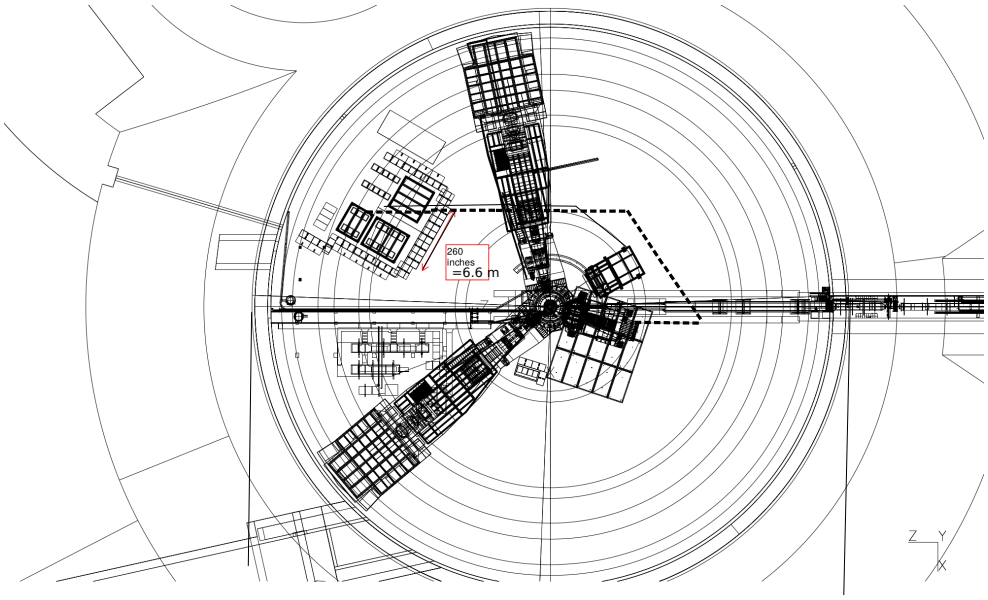


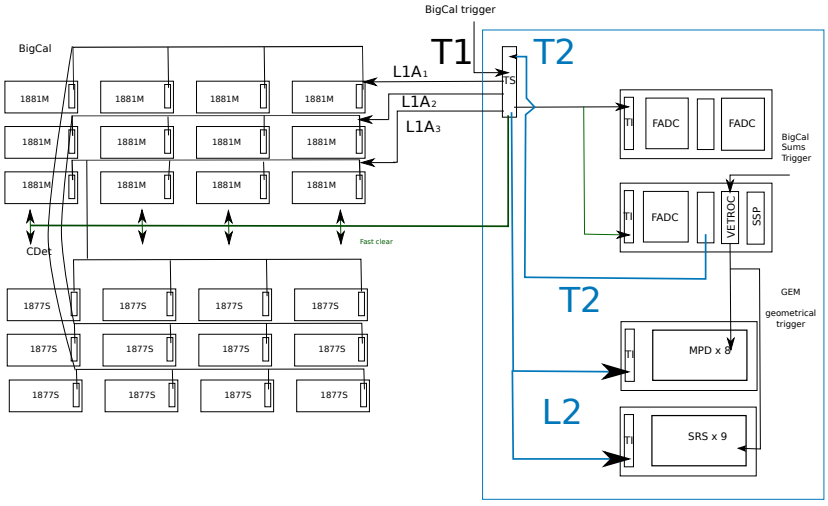
Figure 1: The left plot is the distribution of elastic electrons in ECAL with the black rectangles representing groups of 2x4 lead glass blocks. The right plot demonstrates the scheme for make overlapping groups of 32 lead glass blocks to be used in the ECAL trigger with details explained in text.

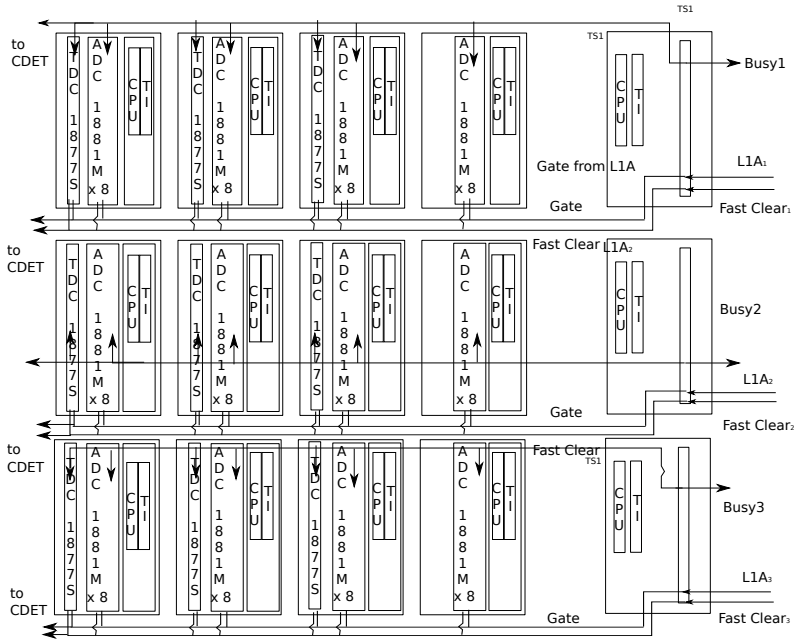
3.1 Hall layout



174 ft = 53 m diameter

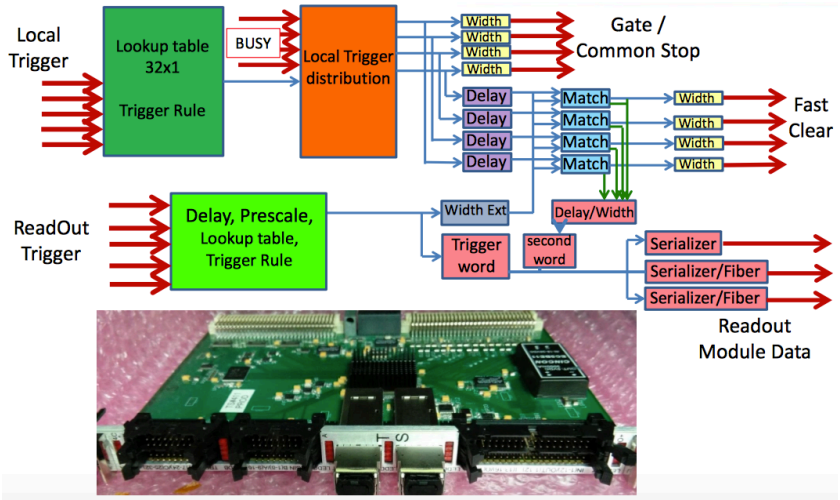
3.2 Electronics layout

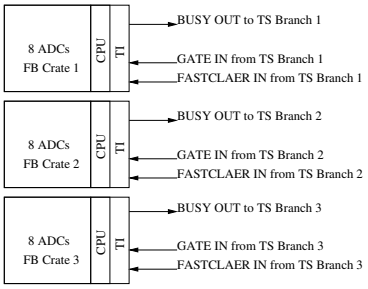




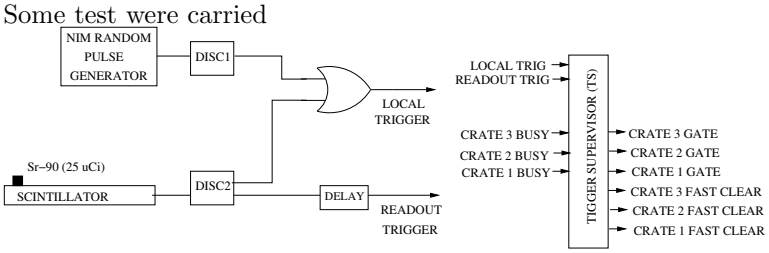
3.3 Fastbus

A special version of the trigger supervisor firmware was developped for SBS to be able to use the event switching to different crates to reduce the dead time.



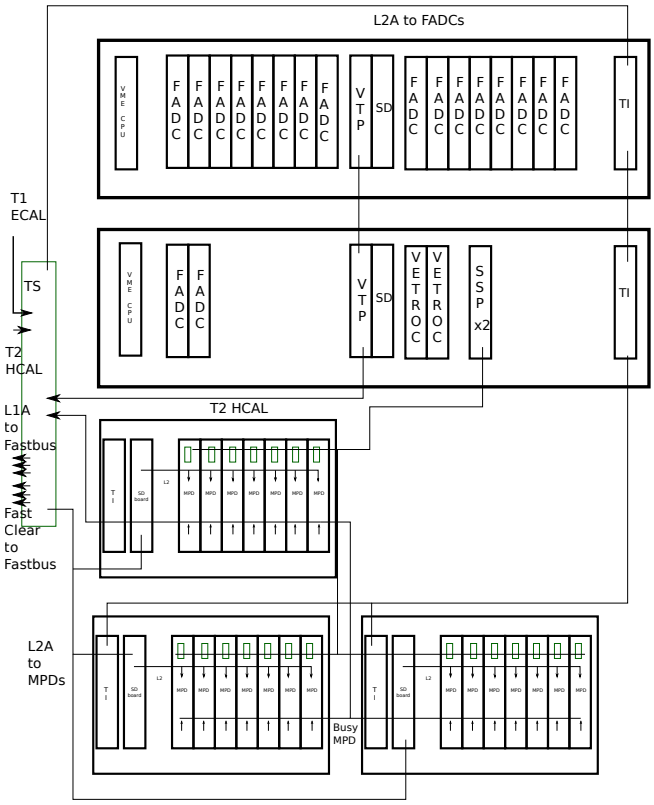


Some test were carried

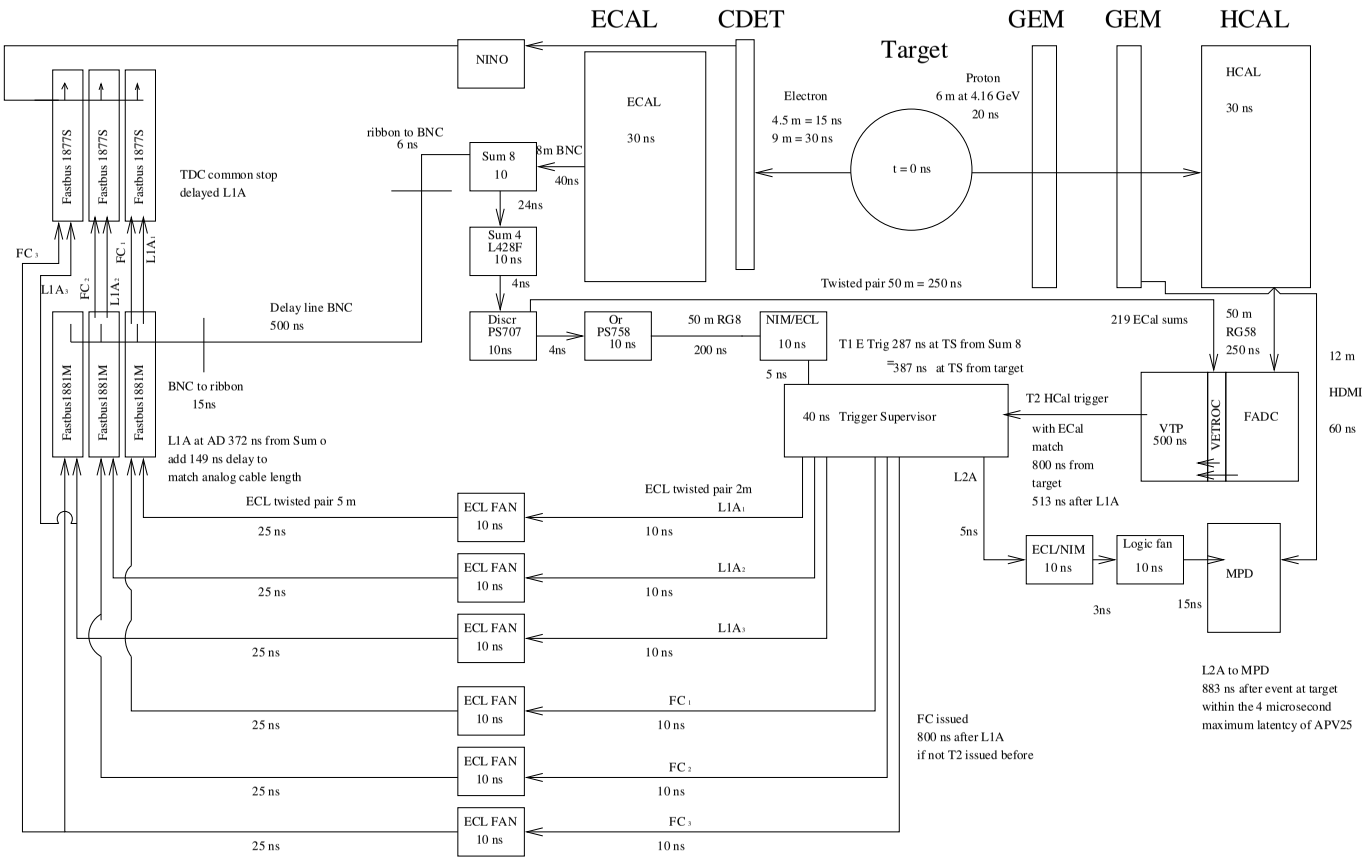


As expected the deadtime is scaling

3.4 GEM readout



3.5 Experiment timing


ECAL
CDET
Target
GEM
GEM
HCAL
NINO
ECAL
30 ns
HCAL
30 ns
Electron
4.5 m = 15 ns
9 m = 30 ns
Proton
6 m at 4.16 GeV
20 ns
t = 0 ns
ribbon to BNC
6 ns
Sum 8
10
8m BNC
40ns
24ns
Sum 4
L428F
10 ns
4ns
Fastbus 1877S
Fastbus 1877S
Fastbus 1877S
TDC common stop
delayed L1A
FC 3
L1A 3
FC 2
L1A 2
FC 1
L1A 1
Delay line BNC
500 ns
Twisted pair 50 m = 250 ns
Discr
PS707
10ns
4ns
Or
PS758
10 ns
50 m RG8
200 ns
NIM/ECL
10 ns
T1 E Trig 287 ns at TS from Sum 8
=387 ns at TS from target
5 ns
219 ECal sums
50 m
RG58
250 ns
12 m
HDMI
60 ns
Fastbus1881M
Fastbus1881M
Fastbus1881M
BNC to ribbon
15ns
L1A at AD 372 ns from Sum o
add 149 ns delay to
match analog cable length
40 ns Trigger Supervisor
T2 HCal trigger
with ECal
match
800 ns from
target
513 ns after L1A
VTP
500 ns
VETROC
FADC
L2A
5ns
ECL/NIM
10 ns
Logic fan
10 ns
MPD
3ns
15ns
L2A to MPD
883 ns after event at target
within the 4 microsecond
maximum latency of APV25
ECL twisted pair 5 m
ECL twisted pair 2m
L1A 1
ECL FAN
10 ns
25 ns
10 ns
L1A 2
L1A 3
FC 1
FC 2
FC 3
FC issued
800 ns after L1A
if not T2 issued before

3.6 Expected data rate