THE IMAGINATION UNIVERSITY PROGRAMME

Overview of the RVfpgaEH1 Materials

0. STRUCTURE OF THE RVfpgaEH1 MATERIALS

IMPORTANT: You should read this **ReadmeSecond_EH1** document completely before starting to use RVfpgaEH1.

IMPORTANT: We will identify the absolute path to the RVfpgaEH1 folder as: ***[RVfpgaPath]***

The [RVfpgaPath]/RVfpga folder includes the following elements:

1. **Documents** (folder): contains:
    a. **RVfpga_GettingStartedGuide** (GSG), which introduces the system and tools used in the RVfpgaEH course. It is briefly described below (Section 2).
    b. **RVfpga_Slides**, which are the slides for the GSG and the Labs.
    c. **Workshop_Guide**, which includes the instructions that the attendees of a one-day RVfpga Workshop should follow.
    d. **IUP_Brochure** and **TeachingMaterial_LicenseAgreement**, which describe Imagination Technologies' teaching materials packages and license.
    e. **Figures_GSG** (folder): Figures used in the GSG document.

2. **examples** (folder): contains example programs that you will run in PlatformIO while using the Getting Started Guide.

3. **src** (folder): contains the source code (Verilog and SystemVerilog) for the RVfpgaEH1 System.

4. **verilatorSIM** (folder): contains the scripts for running the simulation of RVfpgaEH1 in Verilator. It generates a trace of the different internal signals of the SoC while executing a given program and then uses GTKWave for visualizing the waveform of this trace.

5. **NewSimulators** (folder): contains scripts for running the simulation of the RVfpgaEH1 System using Verilator. Two new simulators are provided:
    a. **RVfpgaEH1-ViDBo** uses a virtual board (i.e., an image of an FPGA board using a web browser) to perform a simulation of the RVfpgaEH1 System and communicate with the peripherals of the simulated board. The following peripherals are supported in RVfpgaEH1-ViDBo: switches, LEDs, UART, pushbuttons, 7-Segment Displays, and tricolor LED (the latter peripheral is not available on the Basys 3 board).
    b. **RVfpgaEH1-Pipeline** uses a VeeR EH1 Pipeline Simulator for analysing the evolution of the instructions through the pipeline.

IMPORTANT: RVfpga v2.2 only included one Verilator-based simulation tool (the one included in folder **verilatorSIM**).

In RVfpga v3.0 we include two new simulation tools for the VeeR EH1-based SoC: **RVfpgaEH1-ViDBo** and **RVfpgaEH1-Pipeline**. An extra appendix (Appendix G) has been included in the RVfpgaEH1 Getting Started Guide with instructions on how to use these new simulators. If you want to install the simulators natively in your machine, look at the instructions provided at RVfpgaEL2.
Note that the websockets library for Windows is only provided in the RVfpgaEL2 package for the NexysA7-DDR configuration (you can find it at *[RVfpgaEL2NexysA7DDRPath]/Simulators/verilatorSIM_ViDBo/libwebsockets*).

6. **driversLinux_NexysA7** (folder): contains the Linux drivers for the Nexys A7 FPGA board.

7. **Labs** (folder): contains instructions, programs, and solutions that you will use during RVfpgaEH1 Labs 1-20. This folder contains several subfolders:
    a. **Lab1, Lab2, … , Lab19, Lab20** (folders): Instructions and resources to be used while completing the labs in PlatformIO. Note that each of the 20 labs has an instruction document that is located within the Labs directory under the specific lab's folder. For example, the instructions for Lab 1 are in [RVfpgaPath]/Labs/Lab01/RVfpga_Lab01. These lab documents give the instructions, examples, tasks, exercises, and figures for each of the 20 RVfpgaEH1 Labs.
    b. **RVfpgaLabsFigures** (folder): Figures used in the lab documents.
    c. **RVfpgaLabsSolutions** (folder): A subset of exercise solutions for each of the labs.
        i. **ProgramsAndDocuments** (folder): documents and software with the solutions for the proposed tasks and exercises.
        ii. **Modified_RVfpgaSystem** (folder): Modified RVfpgaEH1 System source code (Verilog and SystemVerilog) extended as guided by the exercises in Labs 6-10 and in Lab 18. Both different platformIO projects and the source code and the bitstreams for the SoC (that you can directly use on the FPGA) are provided.

IMPORTANT: Instructors should remove folder **RVfpgaLabsSolutions** before distributing RVfpgaEH1 to students.

Videos: In addition to the RVfpga folder and the Virtual Machine, in the Imagination's YouTube channel we provide videos demonstrating different sections of the GSG and the Labs. These videos are a very good complement to the text explanations and the examples provided throughout the course.

2. RVfpgaEH1 GSG OVERVIEW

The RVfpgaEH1 Getting Started Guide (GSG) is the introductory document of the RVfpgaEH1 materials. It is available at:

[RVfpgaPath]/RVfpga/Documents/RVfpga_GettingStartedGuide.docx

IMPORTANT: Before starting to work with the RVfpgaEH1 Labs, you should complete the RVfpgaEH1 Getting Started Guide.

The GSG is an extensive document that includes a Quick Start Guide, software installation instructions, an overview of the RISC-V architecture and RVfpgaEH1 (including in-depth descriptions of the SweRVolf SoC and SweRV EH1 core), and instructions about how to write, simulate, and run programs on RVfpgaEH1 both in simulation and, optionally, in hardware on the Nexys A7 FPGA board.

- **Section 1** An overview of the GSG contents, RVfpgaEH1 System, required software and optional hardware, and expected prior knowledge.
- **Section 2** A Quick Start Guide, which describes the minimal software

installation needed for RVfpgaEH1 and then shows how to download and execute a simple example program on RVfpgaEH1.

- **Sections 3 and 4** A brief introduction to the RISC-V computer architecture, the RVfpgaEH1 SoC (similar to Section II.C of this document), and the organization of the Verilog and SystemVerilog files that make up the RVfpgaEH1 system.
- **Section 5** Shows how to install all of the software tools needed to use RVfpgaEH1 both in simulation and hardware.
- **Section 6** Shows how to use PlatformIO to both download the RVfpgaEH1 SoC onto the Nexys A7 FPGA board and download and run several example programs on RVfpgaEH1.
- **Sections 7 and 8** Show how to simulate RVfpgaEH1 source code (Verilog and SystemVerilog) using Verilator and how to simulate RISC-V code on the Whisper instruction set simulator (ISS), respectively.
- **Appendices:** The Getting Started Guide also includes appendices that show additional features such as how to use RVfpgaEH1 at the command prompt in Linux and how to install the required tools on Windows and macOS machines.

3. RVfpgaEH1 LABS OVERVIEW

The RVfpgaEH1 Labs, listed in Table 1, provide hands-on understanding of RISC-V hardware and software. Before starting RVfpgaEH1 Labs, you must complete the RVfpgaEH1 Getting Started Guide. The RVfpgaEH1 Labs materials are provided in the following folders:

- *[RVfpgaPath]/RVfpga/**Labs*** contains resources for each of the 20 labs, including a instructions document for each lab. These lab resources are contained within each of the subfolders: *Lab01*, *Lab02*, etc.
- *[RVfpgaPath]/RVfpga/Labs/**RVfpgaLabsSolutions*** contains a subset of exercise solutions for each of the 20 RVfpgaEH1 Labs. This folder should be deleted before distributing the RVfpgaEH1 package to students.

Table 1. RVfpgaEH1 Labs

	#	Title
Part 1	1	C Programming
	2	RISC-V Assembly Language
	3	Function Calls
	4	Image Processing: Projects with C & Assembly
	5	Creating a Vivado Project
	6	Introduction to I/O
	7	7-Segment Displays
	8	Timers
	9	Interrupt-Driven I/O
	10	Serial Buses
Part 2	11	SweRV EH1 Configuration and Organization. Performance Monitoring
		SweRV EH1 Reference
	12	Arithmetic/Logical Instructions: `add`
	13	Memory Instructions: the `lw` and `sw` Instructions
	14	Structural Hazards
	15	Data Hazards
	16	Control Hazards. Branch Instructions: `beq` and the Branch Predictor
	17	Superscalar Execution
	18	Adding New Features (Instructions, Hardware Counters) to the Core
	19	Memory Hierarchy: The Instruction Cache (I$)
	20	I$, ICCM, DCCM, and Benchmarking

The labs are divided into two parts. Part 1 shows how to program RVfpgaEH1, build the source code in Vivado, and extend the RVfpgaEH1 System to include additional peripherals. Part 2 focuses on the RISC-V core and memory system.

Specifically, Labs 1-10 (Part 1) show how to use the RISC-V SoC and toolchain (compilers and simulators), and they show how to add peripherals to the SoC. Specifically, Labs 1-4 show how to run C and RISC-V Assembly programs on the board and on simulation, Lab 5 shows how to analyse the SweRVolfX SoC source code, create an RTL project and generate a bitstream for the RVfpgaEH1 System on the FPGA board, and Labs 6-10 show how to modify the RVfpgaEH1 System to add new peripherals.

IMPORTANT: Lab 05 shows how to generate the SoC bitstream using Vivado 2019.2. This version of Vivado is not currently available, but you can use Vivado 2022.2 (the version that we use in RVfpgaEL2) following the exact same steps.

Labs 11-20 (Part 2) focus on microarchitecture and memory hierarchy; they show how to understand the RISC-V pipeline and use or add features to the RISC-V core, including additional instructions, other branch predictors, and memory features. The RVfpga_SweRVref document is provided inside *[RVfpgaPath]/RVfpga/Labs/Lab11* and gives extra instructions on several topics: Sigasi Studio, Configuration of the SweRV EH1 processor, RVfpgaEH1 System hierarchy of modules and their most relevant signals, Main structures/types for grouping control bits, RISC-V compressed instructions, Real Benchmarks.

These labs are well-suited for two-semester course for undergraduates. Labs 11-20 could also be taught to master's level students. Prior to completing this RVfpgaEH1 course, students should understand the fundamentals of logic design, computer architecture, processor design, input/output systems and C/assembly programming. This material is covered in the textbook *Digital Design and Computer Architecture: RISC-V Edition*, Harris & Harris, © Morgan Kaufmann 2021.

4. RVfpgaEH1 SOFTWARE AND HARDWARE

Table 2 lists the required software and optional hardware needed to use these labs. All of the software is free. The Nexys A7 FPGA board (or, equivalently, Nexys DDR FPGA board) is not required to complete the labs. Instead, all labs can be completed using Whisper (Western Digital's Instruction Set Simulator) and Verilator (an open-source HDL simulator).

Table 2. Required Software and Optional Hardware

Software	
Vivado 2022.2 WebPACK*	https://www.xilinx.com/support/download/index.html/content/xilinx/en/downloadNav/vivado-design-tools/2022-2.html
VS Code	https://code.visualstudio.com/Download
PlatformIO	https://platformio.org/ (Installed within VSCode)
Verilator and GTKWave	https://github.com/verilator/verilator http://gtkwave.sourceforge.net/
Whisper (Western Digital's RISC-V Instruction Set Simulator)	https://github.com/chipsalliance/SweRV-ISS (Installed within PlatformIO)
RISC-V Toolchain and OpenOCD	https://github.com/riscv/riscv-gnu-toolchain, https://github.com/riscv/riscv-openocd (Installed within PlatformIO)
Hardware	
Nexys A7 FPGA Board*	https://store.digilentinc.com/nexys-a7-fpga-trainer-board-recommended-for-ece-curriculum/
RISC-V Core and System-on-Chip (SoC)	
Western Digital's SweRV EH1	https://github.com/chipsalliance/Cores-SweRV (included in RVfpgaEH1 package)
SweRVolf	https://github.com/chipsalliance/Cores-SweRVolf (included in RVfpgaEH1 package)

* RVfpga v2.2 used Vivado 2019.2; however, this version of Vivado is not currently available. Fortunately, you can use Vivado 2022.2 (the version that we use in RVfpgaEL2) following the exact same steps. Remember that Vivado is optional and only must be used if you want to modify the SoC and test it in hardware.

5. RVfpgaEH1 1-DAY WORKSHOP OVERVIEW

Two additional documents are included in the RVfpgaEH1 package that can be used by instructors to help an instructor run an RVfpgaEH1 course or run a 1-day RVfpgaEH1 Workshop:

- *[RVfpgaPath]/RVfpga/Documents/**RVfpga_Slides.pptx***: These slides describe the entire RVfpgaEH1 package: overview, installation, Getting Started Guide, labs, etc. The trainer should follow these in an RVfpgaEH1 workshop.

- *[RVfpgaPath]/RVfpga/Documents/**Workshop_Guide.docx***: This document is the guide that the instructor will use and the attendees will follow in an RVfpgaEH1 Workshop. It describes the workshop topics, demonstrations, and hands-on activities.