

**THE IMAGINATION UNIVERSITY PROGRAMME**

**RVfpga Lab 8**

**Timers**

# Introduction

Hardware timers are common peripherals found in microcontrollers and SoCs. They are typically used to generate precise timing. Timers increment or decrement a counter at a fixed frequency, which is often configurable, and then interrupt the processor when the counter reaches zero or a predefined value. More sophisticated timers can also perform other functions, such as generating pulse-width modulated (PWM) waveforms to control the speed of a motor or the brightness of a light.

In this lab,using a similar structure to that of previous labs, we first describe the high-level specification of the timer included in the RVfpgaEL2 System and then explain its low-level implementation. Finally, some exercises are proposed that show how to use the timer.

# High-Level Specification of the Timer Included in RVfpgaEL2

In this section, we first analyse the high-level specification of the timer used in the RVfpgaEL2 System and then we propose one exercise that uses this peripheral.

1. **Timer high-level specification**

The timer module used in the RVfpgaEL2 System has been obtained from OpenCores (<https://opencores.org/projects/ptc>). If you download the package, a document is provided that describes the high-level specification of the module (and which we provide at: *[RVfpgaBasysPath]/src/VeeRwolf/Peripherals/ptc/docs/ptc\_spec.pdf*). We summarize the main operation and features of the timer module here; however, the complete information can be found in the above document.

The timer module has the following main features:

* Uses a Wishbone Interconnection
* 32-bit counter/timer facility
* Single-run or continuous run of PWM/Timer/Counter (PTC)
* Programmable PWM (Pulse-width modulation) mode
* System clock and external clock sources for timer functionality
* HI/LO Reference and Capture registers
* Three-state control for PWM output driver
* PTC functionalities can cause an interrupt to the CPU

Section 4 of the timer module specification document describes the control and status registers available inside the timer module, each of which is assigned to a different address (see Table 1). The base address for the timer in the RVfpgaEL2 System is **0x80001200**.

Table 1. Timer registers

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name** | **Address** | **Width** | **Access** | **Description** |
| RPTC\_CNTR | 0x80001200 | 1-32 | R/W | Main PTC counter |
| RPTC\_HRC | 0x80001204 | 1-32 | R/W | PTC HI Reference/Capture register |
| RPTC\_LRC | 0x80001208 | 1-32 | R/W | PTC LO Reference/Capture register |
| RPTC\_CTRL | 0x8000120C | 9 | R/W | Control register |

The RPTC\_CNTR register is the actual counter register, and it is incremented at every counter/timer clock cycle. The RPTC\_CTRL register is used for controlling the timer module; Table 2 shows the function of each of its bits. RPTC\_HRC and RPTC\_LRC are used as reference/capture registers.

Table 2. RPTC\_CTRL bits

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit** | **Access** | **Reset** | **Name & Description** |
| 0 | R/W | 0 | **EN**  When set, RPTC\_CNTR increments. |
| 1 | R/W | 0 | **ECLK**  Selects the clock signal: external clock, through *ptc\_ecgt* (1), or system clock (0). |
| 2 | R/W | 0 | **NEC**  Used for selecting the negative/positive edge and low/high period of the external clock (*ptc\_ecgt*). |
| 3 | R/W | 0 | **OE**  Enables PWM output driver. |
| 4 | R/W | 0 | **SINGLE**  When set, RPTC\_CNTR is not incremented after  it reaches value equal to the RPTC\_LRC value. When cleared, RPTC\_CNTR is restarted after it reaches value in the RPTC\_LCR register. |
| 5 | R/W | 0 | **INTE**  When set, PTC asserts an interrupt when RPTC\_CNTR value is equal to the value of RPTC\_LRC or RPTC\_HRC. When the signal is cleared, interrupts are masked. |
| 6 | R/W | 0 | **INT**  When read, this bit represents pending interrupt. When it is set, an interrupt is pending. When this bit is written with ‘1’, interrupt request is cleared. |
| 7 | R/W | 0 | **CNTRRST**  When set, RPTC\_CNTR is reset. When cleared, normal operation of the counter occurs. |
| 8 | R/W | 0 | **CAPTE**  When set, RPTC\_CNTR is captured into RPTC\_LRC or RPTC\_HRC registers. When cleared, capture function is masked. |

**TASK:** Locate the declaration of registers RPTC\_CNTR, RPTC\_HRC, RPTC\_LRC and RPTC\_CTRL in the timer module, as well as the definition of their addresses (0x80001200, 0x80001204, 0x80001208 and 0x8000120C respectively). The timer module is available inside folder *[RVfpgaBasysPath]/src/VeeRwolf/Peripherals/ptc*.

R

The timer can operate in different modes (we next briefly describe the modes that you will use in this lab; see Section 3 of the timer module specification document for more details):

* **Timer/Counter mode**: In this mode, the system clock or external clock reference increments register RPTC\_CNTR if the counter is enabled (RPTC\_CTRL[EN] = 1). When RPTC\_CNTR equals the RPTC\_LRC, if RPTC\_CTRL[INTE] is set, RPTC\_CTRL[INT] goes high.
* **PWM mode**: A pulse width modulated (PWM) signal is a method for generating an analog signal using a digital source. A PWM signal consists of two values that define its behaviour: the *duty cycle* and *frequency*. The duty cycle describes the amount of time the signal is high as a percentage of the total time of it takes to complete one cycle. The frequency is how often that cycle repeats. By cycling a digital signal off and on at a fast enough rate, and with a certain duty cycle, the output will appear to behave like a constant voltage analog signal when providing power to devices. For example, a signal with a 50% duty cycle (half the cycle time it is high) and a high voltage of 3.3 V would appear to an analog load as 1.67 V (the average voltage across the cycle). The same signal with a 33% duty cycle would appear to be 1.1V. To operate in PWM mode, RPTC\_CTRL[OE] should be set. Registers RPTC\_HRC and RPTC\_LRC should be set with the value of high and low periods of the PWM output signal: the PWM signal should go high RPTC\_HRC clock cycles after reset (of RPTC\_CNTR); and the PWM signal should go low RPTC\_LRC clock cycles after reset (of the RPTC\_CNTR).

# Exercise

# Exercise 1. Write a program that displays an ascending count on the 8-digit 7-segment displays. The value should change about once per second and, for creating this delay, you must use the timer module.

1. First, write the program in RISC-V assembly language and run it on the Basys 3 Board.
2. Then, perform a simulation in the different RVfpgaEL2 tools.
3. Now write the program in C and run it on the Basys 3 Board.
4. Simulate your C program as in part (b) for the RISC-V assembly program.

# Timer Low-Level Implementation

# In this section, we first describe the low-level implementation of the timer module in the RVfpga System and then propose some exercises where you will first modify the module and then use it in a program for controlling the tri-colour LEDs available on the Basys 3 Board.

1. **Low-level implementation of the timer**

Similarly to the scheme that we followed in previous labs, we divide the analysis of the timer module into phases.

1. Integration of the new module in the VeeRwolfX SoC (left shadowed region in Figure 1)
2. Connection between the new module and the VeeR EL2 Core (right shadowed region in Figure 1).

Note that, as opposed to previous labs, this peripheral (the timer) is not connected physically to the Basys 3 Board. The timer is internal to VeeRwolfX.

A screenshot of a computer

Description automatically generated

Figure 1. Timer module analysis in 2 phases

1. **Integration of the timer module in the SoC**

In module **veerwolf\_core** (*[RVfpgaBasysPath]/src/VeeRwolf/veerwolf\_core.v*) the timer module is instantiated (see Figure 2).

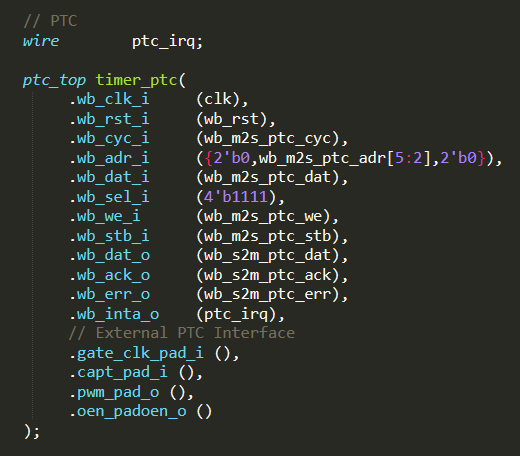


Figure 2. Integration of the timer module (file *veerwolf\_core.v*).

As usual, the interface of the module can be divided in two blocks: Wishbone signals (Table 3) and External I/O signals (Table 4). The Wishbone signals allow the VeeR EL2 Core to communicate with the timer using a controller/peripheral model. The External I/O signals, connect the timer module with external devices; for example, pwm\_pad\_o provides the PWM output signal when operating in the PWM mode described above (you will have to use this signal in Exercise 2 to connect the timer modules with the tri-colour LEDs).

Table 3. Wishbone Signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Port** | **Width** | **Direction** | **Description** |
| wb\_cyc\_i | 1 | Inputs | Indicates valid bus cycle (core select) |
| wb\_adr\_i | 15 | Inputs | Address inputs |
| wb\_dat\_i | 32 | Inputs | Data inputs |
| wb\_dat\_o | 32 | Outputs | Data outputs |
| wb\_sel\_i | 4 | Inputs | Indicates valid bytes on data bus (during valid cycle, this signal must be 0xf) |
| wb\_ack\_o | 1 | Output | Acknowledgment output (indicates normal transaction termination) |
| wb\_err\_o | 1 | Output | Error acknowledgment output (indicates an abnormal transaction termination) |
| wb\_rty\_o | 1 | Output | Not used |
| wb\_we\_i | 1 | Input | Write transaction when asserted high |
| wb\_stb\_i | 1 | Input | Indicates valid data transfer cycle |
| wb\_inta\_o | 1 | Output | Interrupt output |

Table 4. External I/O signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Port** | **Width** | **Direction** | **Description** |
| gate\_clk\_pad\_i | 1 | Input | External clock / Gate input |
| capt\_pad\_i | 1 | Input | Capture input |
| pwm\_pad\_o | 1 | Output | PWM output |
| oen\_padoen\_o | 1 | Output | PWM output driver enable (for three-state or open-drain driver) |

As shown in Figure 2, bits [5:2] of the address provided by the core in the Wishbone bus signal (wb\_m2s\_ptc\_adr[5:2]) are used for selecting one among the 4 available registers (Memory Mapped I/O). Thus, we can access register RPTC\_CNTR at address 0x80001200, register RPTC\_HRC at address 0x80001204, register RPTC\_LRC at address 0x80001208, and register RPTC\_CTRL at address 0x8000120C.

1. **Connection between the timer and the VeeR EL2 Core**

As described in Lab 6, the device controllers are connected to the VeeR EL2 Core using a multiplexer (see Figure 3). Remember that the 6:1 multiplexer is instantiated in file *[RVfpgaBasysPath]/src/VeeRwolf/Interconnect/WishboneInterconnect/wb\_intercon.v*. Then, the **wb\_intercon** module is instantiated in file *[RVfpgaBasysPath]/src/VeeRwolf/Interconnect/WishboneInterconnect/wb\_intercon.vh*. This latter file is included in the **veerwolf\_core** module located here: *[RVfpgaBasysPath]/src/VeeRwolf/veerwolf\_core.v*.

The multiplexer selects which peripheral to read or write, connecting the CPU (wb\_io\_\* signals) with the Wishbone Bus of one peripheral, depending on the address. For example, if the address generated by the CPU is in the range 0x80001200-0x8000123F, the timer module is selected, and thus signals wb\_io\_\* are connected with signals wb\_ptc\_\*.

A computer screen shot of a black screen

Description automatically generated

Figure 3. 6:1 multiplexer that selects the peripheral connected with the CPU (file *wb\_intercon.v*)