

CODE BLOG

```

1  atamal      EQU      0XA0A0F0F0      ;odev icin verilen deger
2  iteration   EQU      16              ;memory ye 16 cycle da kaydedebilecegimiz icin verilen deger
3  adress      EQU      0x20000400      ;soruda verilen ilk adress
4  aranan_eleman EQU      0XA4          ;aramak istedigim deger
5
6              AREA MYCODE, CODE
7              ALIGN
8              ENTRY
9              EXPORT __main
10
11 __main
12      LDR      R0,=iteration      ;R0 registirana iterationa atadim
13      LDR      R1,=adress
14      LDR      R10,=atamal
15      ADD      R7,R0,R0          ;r7 = r0 + r0
16      ADD      R3,R7,R1
17      MOV      R2,R10, LSR #16   ;0X0000A0A0
18      MOV      R5,R10, LSL #16   ;0XF0F00000
19      MOV      R4,R5, LSR #16    ;0X0000F0F0
20
21 L1          STRH      R2,[R1]      ;STRH halfwora biçimde memory e kayıt islemi yapar, adress R1 e R2 degerinin en anlamlı 2 byte ni kaydetti
22          STRH      R4,[R3]      ;R3 adresine r4 ün en anlamlı 4 biti kaydedildi
23          ADD      R1,R1,#2        ;memory de 400 ile baslayan adrese 16 bitlik degerleri yazdirdigimizdan dolayi adres 2 artirildi.
24          ADD      R3,R3,#2        ;memory de 420 ile baslayan adrese 16 bitlik degerleri yazdirdigimizdan dolayi adres 2 artirildi.
25          ADD      R2,R2,#1        ;soruda istenilen degeri birer birer arirarak hafizaya kaydetmemizdi, A0A0----- A1A0 olur
26          ADD      R4,R4,#1        ;soruda istenilen degeri birer birer arirarak hafizaya kaydetmemizdi, F0F0----- F1A0 olur
27          SUBS      R0,R0,#1        ;16 cycle icin donguyu her adimda 1 azaltmasi icin ve R0 degeri 0 oldugunda bayrak ile cikis saglamak icin SUBS kullanildi
28          BNE      L1            ;bayrak aktiflestiginde dongu den cikiyor
29
30
31 ;LINEAR SEARCH
32      LDR      R0,=iteration
33      LDR      R1,=adress
34      MOV      R9,#0              ;R9 a baslangic degeri atadik
35      LDR      R8,=aranan_eleman
36
37
38 L2          CMP      R8,R6          ;CMP komutu R8 ve R6 arasinda karsilastirma yapar
39          BEQ      next            ;Eger R8,R6 esit olursa donguden next ile ciksin
40          LDRB      R6,[R1,R9]      ;LDRB komutu R1 adresine R9 ofset i kadar gider ve o adresteki degerini R6 ya atar
41          ADD      R9,R9,#1
42          B        L2
43
44 next
45      MOV      R12,R9              ;R9 sayisi hangi kosulda saglanir ise biz R12 register ina atamamizi yaptik
46      END

```

Windows'u Ftkir

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1  atamal      EQU      0XA0A0F0F0
2  iteration   EQU      16
3  adress      EQU      0x20000400
4  aranan_eleman EQU      0XA4
5
6              AREA MYCODE, CODE
7              ALIGN
8              ENTRY
9              EXPORT __main
10
11 __main
12      LDR      R0,=iteration
13      LDR      R1,=adress
14      LDR      R10,=atamal
15      ADD      R7,R0,R0
16      ADD      R3,R7,R1
17      MOV      R2,R10, LSR #16
18      MOV      R5,R10, LSL #16
19      MOV      R4,R5, LSR #16
20
21
22 L1          STRH      R2,[R1]
23          STRH      R4,[R3]
24          ADD      R1,R1,#2
25          ADD      R3,R3,#2
26          ADD      R2,R2,#1
27          ADD      R4,R4,#1
28          SUBS      R0,R0,#1
29          BNE      L1
30

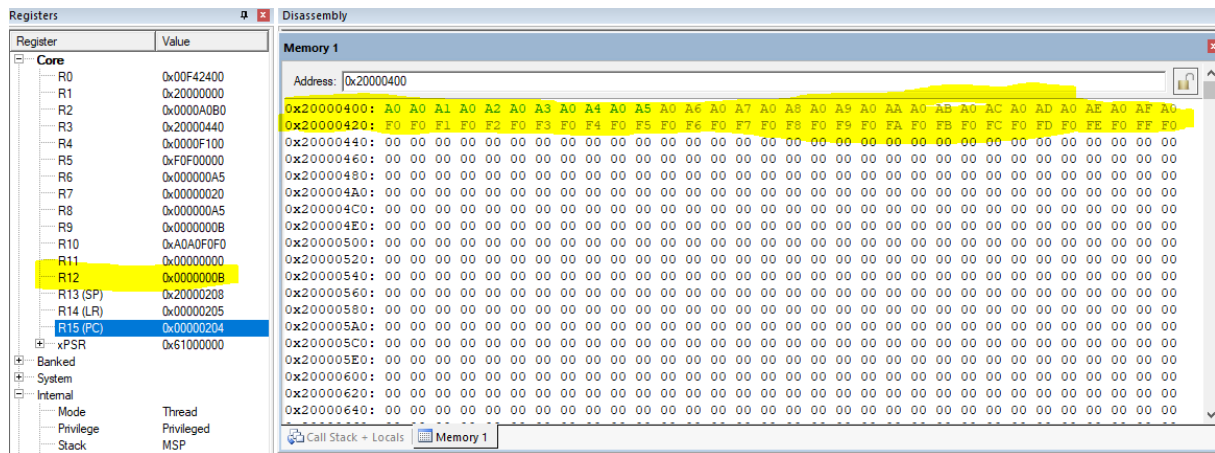
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31 ;LINEAR SEARCH
32      LDR      R0,=iteration
33      LDR      R1,=adress
34      MOV      R9,#0
35      LDR      R8,=aranan_eleman
36
37
38 L2          CMP      R8,R6
39          BEQ      next
40          LDRB      R6,[R1,R9]
41          ADD      R9,R9,#1
42          B        L2
43
44 next
45      MOV      R12,R9
46      END
47

```

MEMORY AND REGISTER



Instructions

- **LSR** : Register x with logical shift left by n bits (0 = n = 31)
- **LSL** : Register x with logical shift right by n bits (1 = n = 32)
- **STRH** : Store unsigned Half Word
- **LDRB** : Load unsigned Byte

ALGORITHM and CODE

First of all, the address information given in the question, the number of cycles and the number of elements I are defined with the EQU instruction. The variables R0, R1, R10 are assigned to registers. Here, 2R0 is added to R3 to define the address that starts with 0x00000420. An important point; Using LSR AND LSL instruction, A0A0F0F0 was converted into 0000A0A0 and 0000F0F0 format.

LOOP 1; The divided values have been saved at 0x00000400 and 0x00000420. The saving was done with STRH, The value of R2 is assigned to the address owned by R1, and the value of R3 is assigned to the address owned by R4. Then A0A0 value is expected to be A1A0, and F0F0 value to be F1F0. For this, 2 is added to the addresses because A0A0 takes 2 bytes of space in memory. We wanted the new value to be added to address 0x00000402. In addition, we increased our value by 1. Before I forget, the reason why there is A1A0 in the memory blog is that it starts from low priority bits while saving to memory. To control the loop, the defined R0 is decremented one by one and if SUBS also changes the flag, the loop exits.

LINEAR SEARCH; Required values for the searched element and its loop are defined before entering freeze. While in loop, the values of R8 and R6 were compared with CMP instructions, If R8 and R6 are equal, use the BEQ instruction to exit the loop. If there is an equality, it is specified to exit the loop, but if there is no equality, we tried to find the value we are looking for by browsing the memory with the LDRB instructions. R6 value in LDRB; At the address R1, R9 is incrementally increased and thus the values starting from 400 to the last position in memory are scanned. R9 is offset value in LDRB.

Lastly I saved the offset value(R9's values) at R12' register.