ANCYWICED008

Hardware Evaluation Board For CYW20735
WICED™ Studio 4

Associated Part Family: CYW20735

This document describes the CYW920735WCDEVAL board and provides various pins, jumpers, switches, ports, and test points to access the CYW20735 to perform development, debug, evaluation, and troubleshooting.

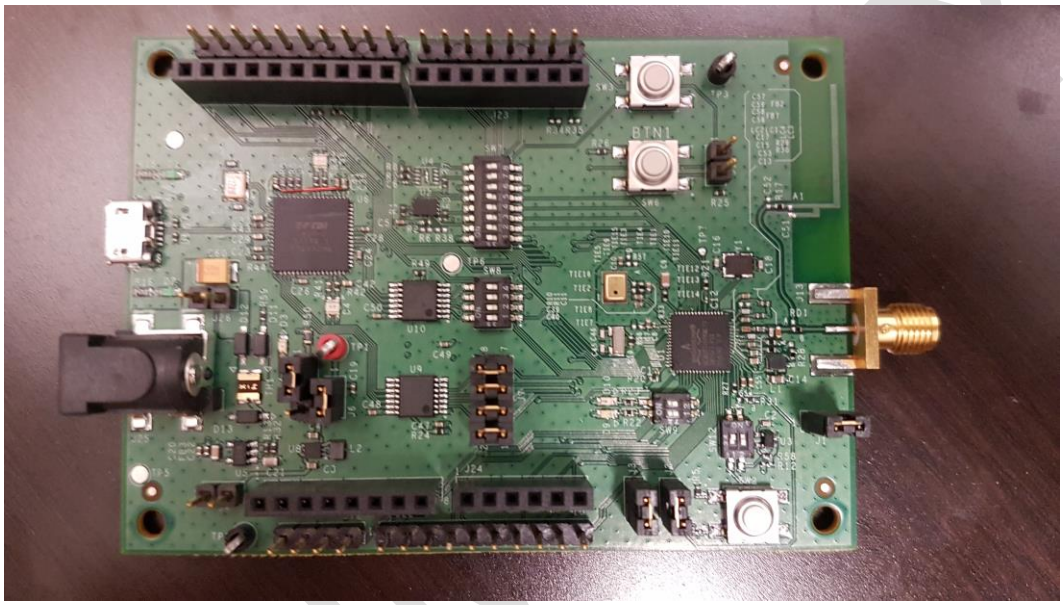
Contents

1 Product Description

The CYW20735 is a monolithic, single chip, Bluetooth dual-mode System-on-a-Chip (SoC) that includes a baseband processor, an ARM® Cortex™-M3 processor and an integrated transceiver.

The Cypress CYW920735WCDEVAL board (Figure 1) is an evaluation board that provides various pins, jumpers, switches, ports, and test points to access the CYW20735 to perform debug, evaluation, and troubleshooting.

Figure 1. CYW920735WCDEVAL Board

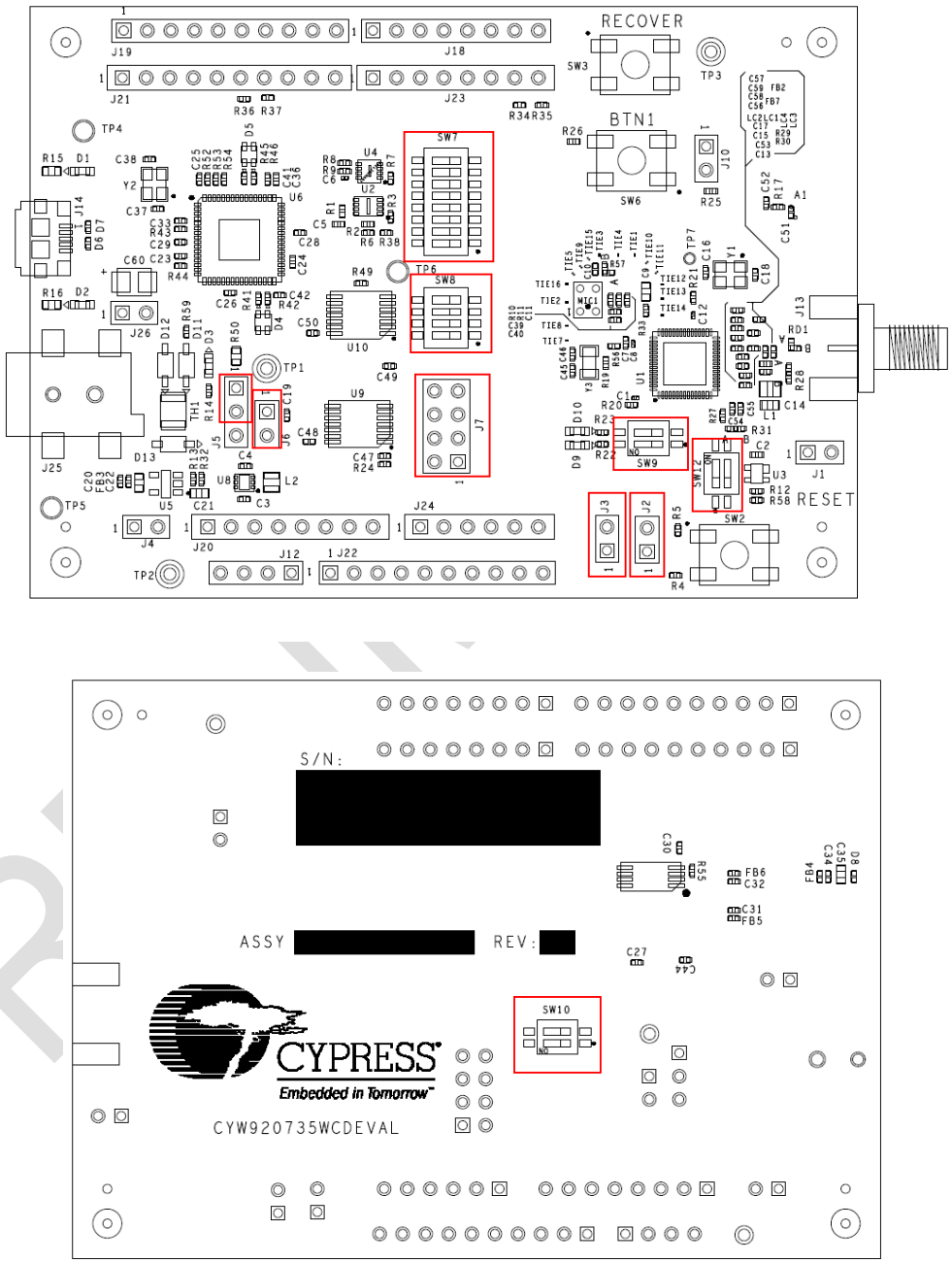


2 Board Layout

Figure 2 shows the location of key jumpers and switches on the CYW920735WCDEVAL board.

Note: Default jumper settings are identified in red.

Figure 2. CYW920735 Evaluation Board Layout and Component Locations



3 DIP Switch Setup

Figure 2 shows the location for SW5, a switch that is used to configure PUART. Settings are shown in Table 1.

Table 1. SW8 DIP Switch Settings

DIP	State	Description
1	OFF	Use P7 as PUART_RX
2	OFF	Use P32 as PUART_TX
3	OFF	Use P9 as PUART_CTS
4	OFF	Use P8 as PUART_RTS

Table 2. SW9 DIP Switch Settings

DIP	State	Description
1	OFF	Use P29 To control LED D9
2	OFF	Use P28 to control LED D10

Table 3. SW12 DIP Switch Settings

DIP	State	Description
1	ON	Use SW2 for RST_N
2	OFF	Use Voltage Detector for RST_N

Table 4. SW10 DIP Switch Settings

DIP	State	Description
1	ON	Enable level shifter for UART
2	ON	Enable level shifter for PUART

Table 5. SW7 DIP Switch Settings

Dip	Default State	Description
1	OFF	Power serial flash from VDDIO
2	OFF	MISO connection between CYW and serial flash

3	OFF	MOSI connection between CYW and serial flash
4	OFF	CS connection between CYW and serial flash
5	OFF	CLK connection between CYW and serial flash
6	OFF	Power authentication IC from VDDIO
7	OFF	SDA connection between CYW and authentication IC
8	OFF	SCL connection between CYW and authentication IC

For applications requiring serial flash memory, enable the on-board serial flash by setting SW7 positions 1-6 to the ON position. For applications that do not require serial flash access, set these to the OFF position.

Authentication IC U4 is DNI by default. If the user decides to install this, then SW7 positions 7-8 should be placed in the ON position for proper connection. If authentication IC is not used, set these to the OFF position.

4 Jumper and Switch Settings

See Figure 2 for the jumpers and switch locations. Table 6 (below) shows the CYW920735WCDEVAL board jumper and switch settings.

Table 6. CYW920735WCD Board Jumper and Switch Settings

Jumper/Switch	State	Comment
J5 1 and 2	Shorted	Select 3.3V main power supply
J6	Shorted	Power supply to the CYW20735
J1	Shorted	Power supply to CBUCK_IN
J2	Shorted	Power supply to PALDO
J10	Shorted	Enables Generic Button SW6
J4	Open	Enables 1.8V Buck
J7		
1 and 2	Shorted	Connects UART_RX to FTDI TX
1 and 2	Shorted	Connects UART_TX to FTDI RX
1 and 2	Shorted	Connects UART_CTS to FTDI RTS
1 and 2	Shorted	Connects UART_RTS to FTDI CTS
J26	Open	Optional: Enables external 5V DC jack for extra current
SW2	–	Reset
SW3	–	Recovery
SW5	Open	See Table 1
SW6	–	Generic button
SW7	Open	See Table 4
SW9	Open	See Table 2

Table 7 shows the CYW920735WCDEVAL board headers.

Table 7. CYW920735WCDEVAL Board Headers

Header	Description
J18	CYW test header - GPIO
J19	CYW test header - GPIO
J20	Arduino shield connection
J21	Arduino shield connection
J22	CYW test header: GPIO, VDDIO, GND
J23	Arduino shield connection
J24	Arduino shield connection
J12	Debug interface

5 Current Consumption Measurement

Table 8 lists the jumper locations for measuring current.

Note: Remove the listed jumper and measure the current across the exposed pins.

Table 8. Current Measurements

To Measure...	Remove the Jumper and Measure Across...
VDDIO	J3
CBUCK Input	J1
PALDO Input	J2
ntire CYW20735	J6

6 Schematics

Figure 3. CYW Baseband Schematic

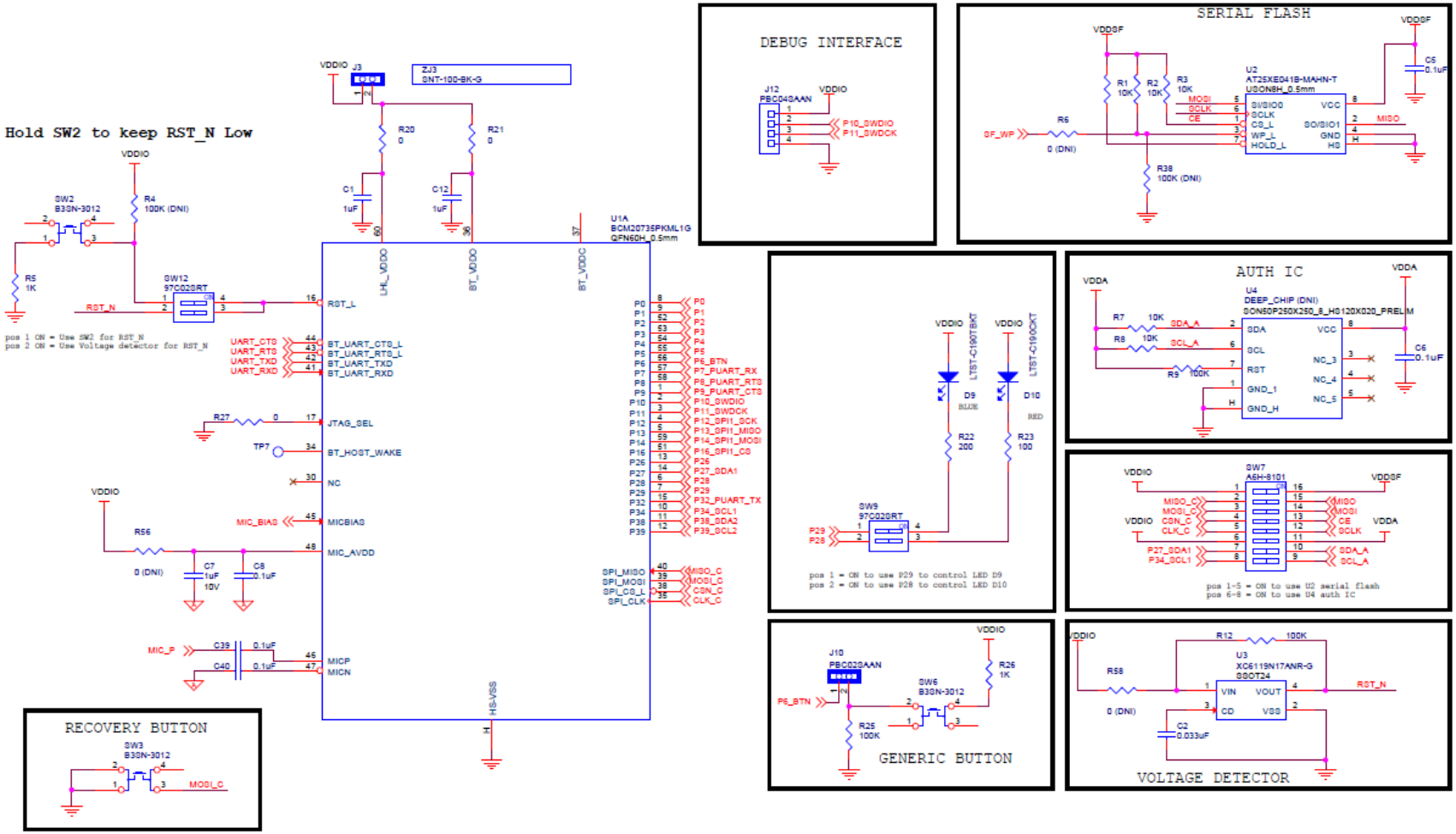


Figure 4. CYW920735 RF Schematic

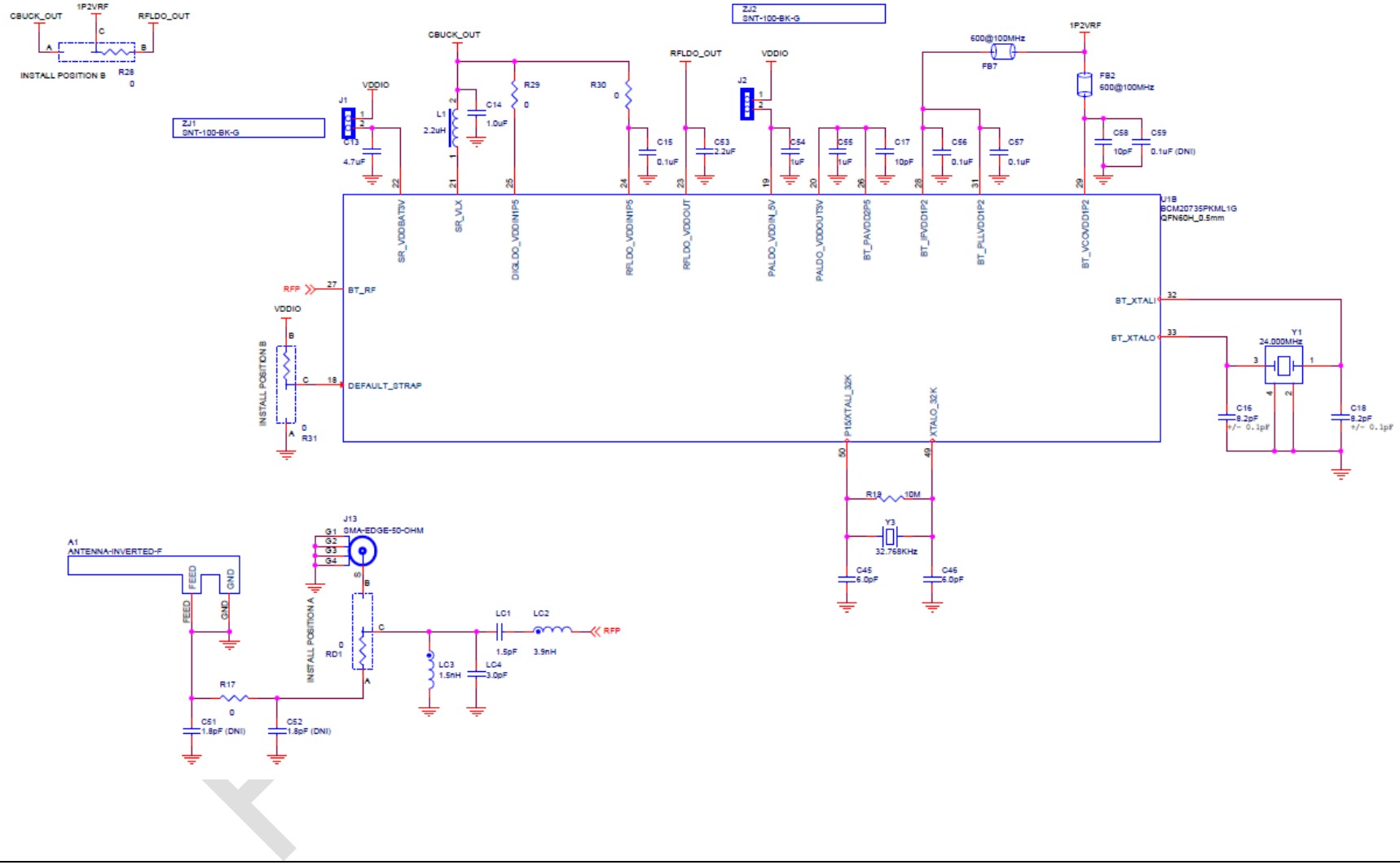
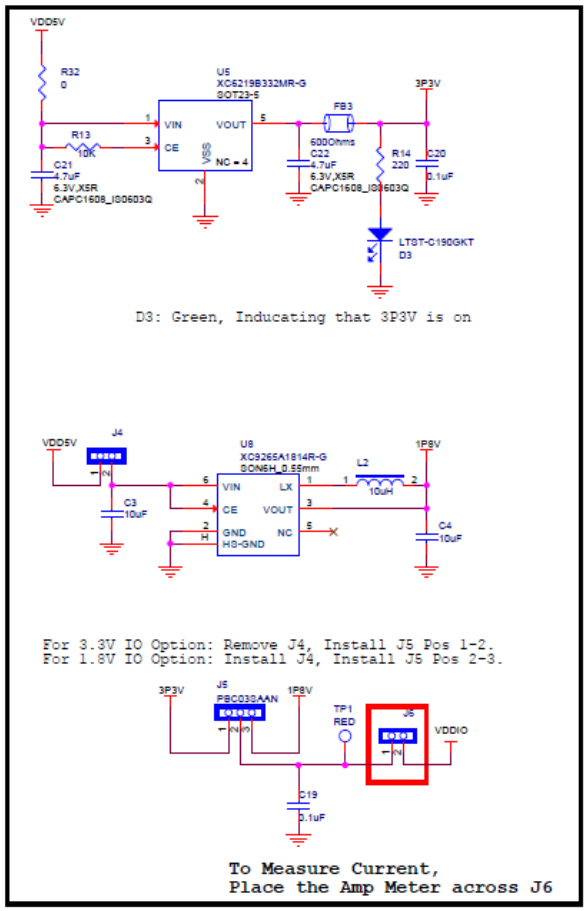
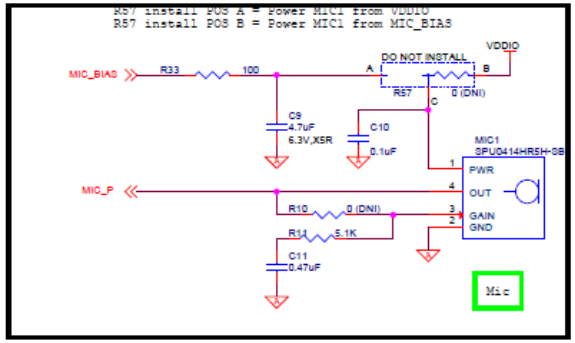
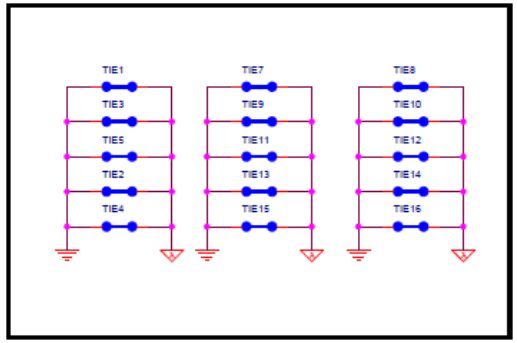
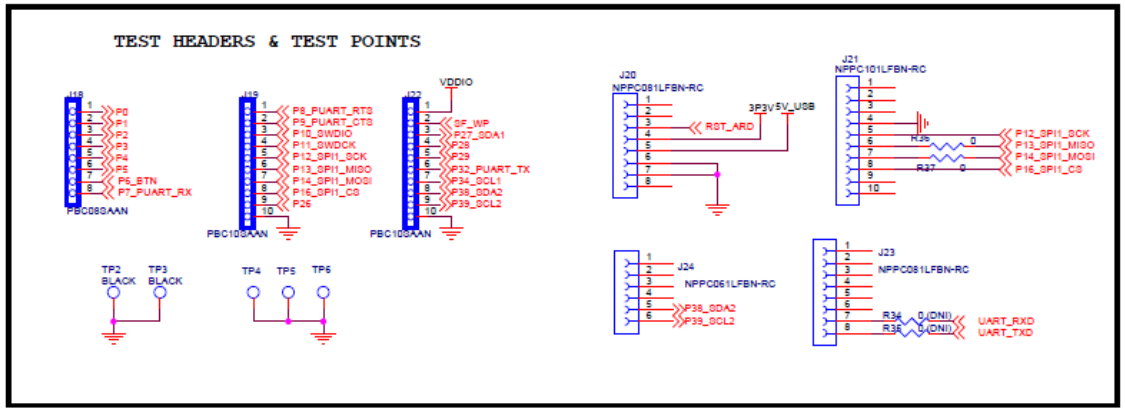


Figure 5. CYW920735 Power and I/O Schematic









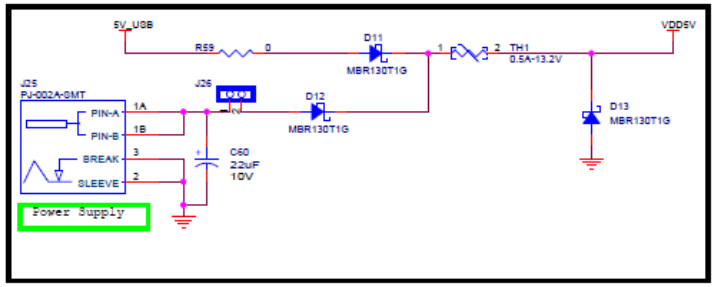
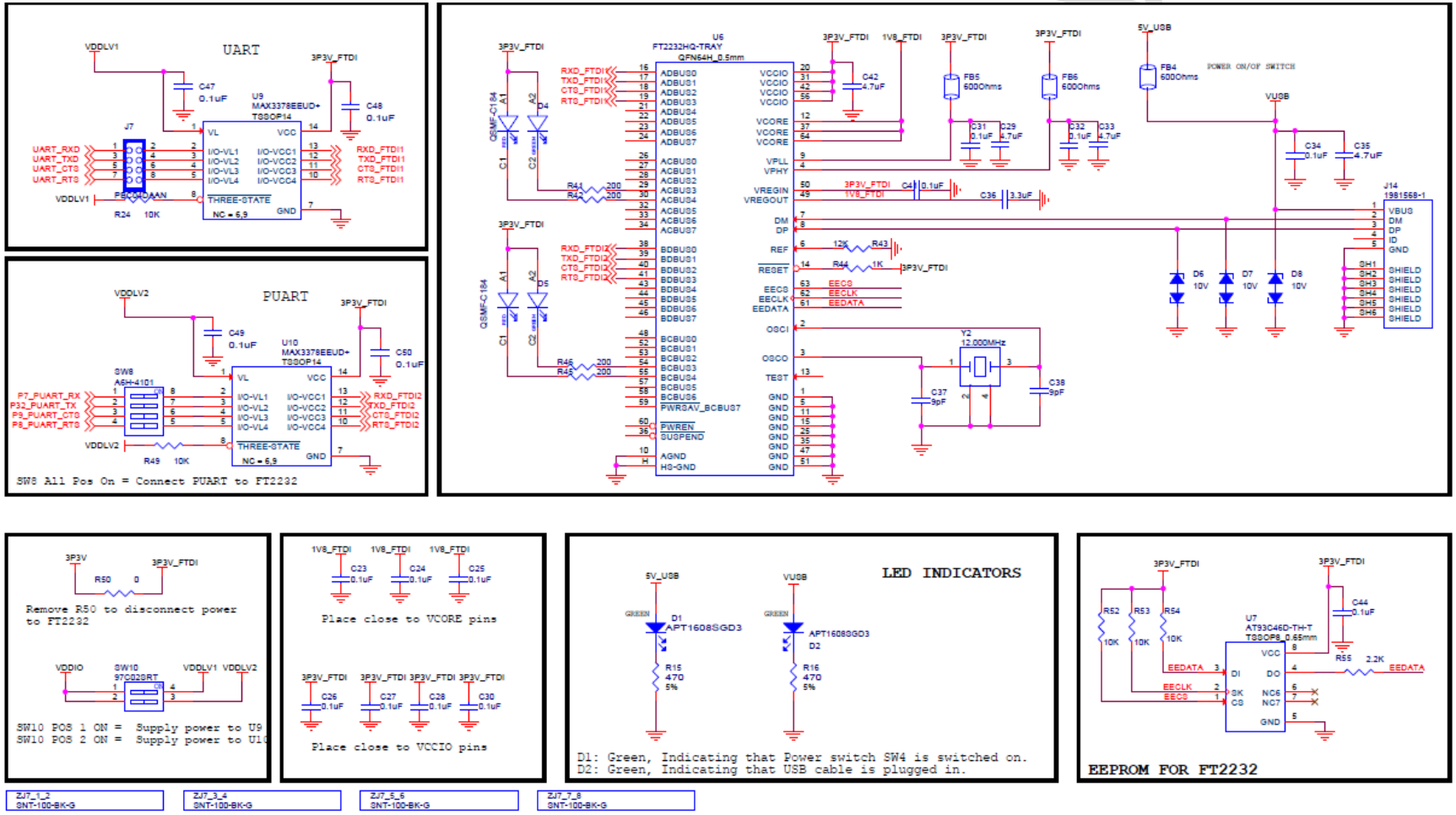


Figure 6.CYW920735 UART Schematic



Document History

Document Title: ANCYWICED008 - Hardware Evaluation Board for CYW20735

Document Number: 001-CYWICED008

Revision	ECN	Submission Date	Description of Change
**	N/A	10/03/2016	Initial revision

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