LOG BOOK [Week 7]
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LAB 5: SCHEMATIC DESIGN ENTRY (Simulation)

1.0 Objectives

- Creating a schematic design entry using Quartus Prime design software.
- Compiling and simulating a simple light circuit and a 1-bit full adder on the FGPA.

2.0 Results and Simulation

A. Schematic Design Entry

The truth table was created from the obtained output from the functional simulation. The value 0 represents OFF and 1 represents ON. The inputs are SW[0] and SW[1]. The output is LEDR[0].

SW[0] / x_1	SW[1] / x_2	LEDR[0] / f
0	0	0
0	1	1
1	0	1
1	1	0

The results obtained from the simulation of the schematic design was the same as that obtained from the Verilog design from Lab 1A.

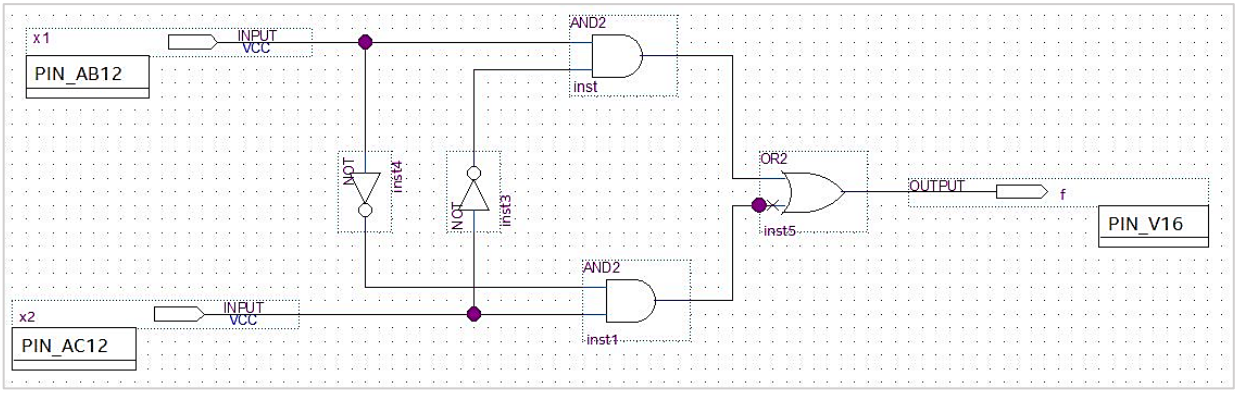


Figure 1: Schematic Design from Quartus_Prime_Schematic.pdf

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✔		in x2	Location	PIN_AC12	Yes			
2	✔		out f	Location	PIN_V16	Yes			
3	✔		in x1	Location	PIN_AB12	Yes			
4		<<new>>	<<new>>	<<new>>					

Figure 2: Pin Assignments for Schematic Design from Quartus_Prime_Schematic.pdf

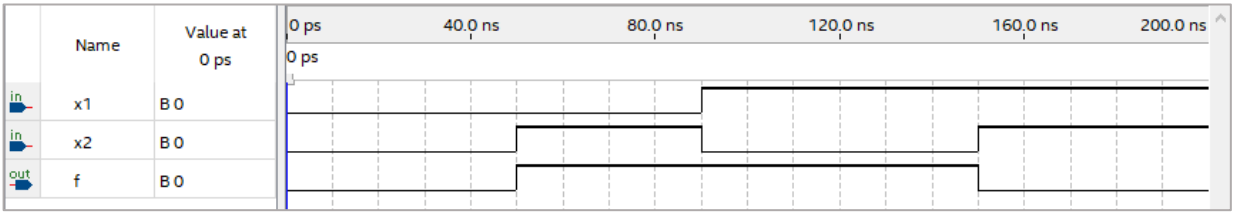


Figure 3: Functional Simulation for Schematic Design rom Quartus_Prime_Schematic.pdf

B. Design of 1-bit Full Adder

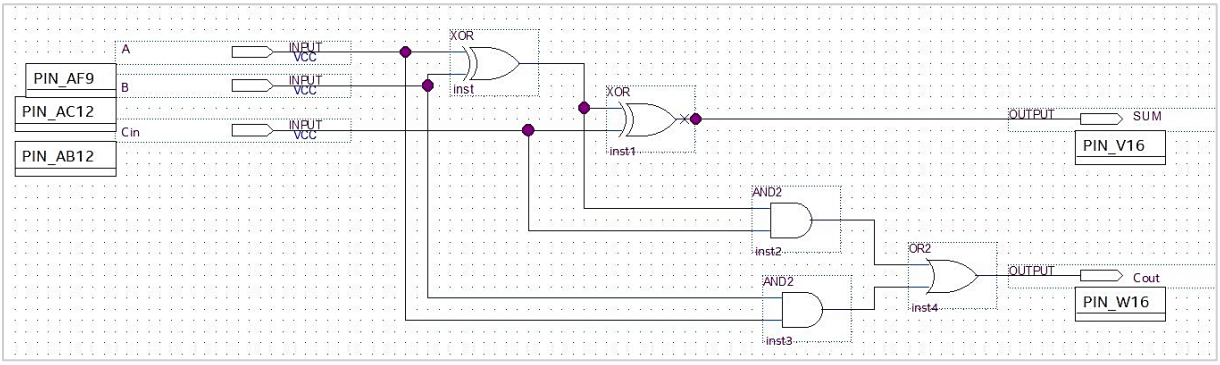


Figure 4: Schematic Design of 1-bit Full Adder

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✔		B	Location	PIN_AC12	Yes			
2	✔		Cin	Location	PIN_AB12	Yes			
3	✔		Cout	Location	PIN_W16	Yes			
4	✔		SUM	Location	PIN_V16	Yes			
5	✔		A	Location	PIN_AF9	Yes			
6		<<new>>	<<new>>	<<new>>					

Figure 5: Pin Assignments for 1-bit Full Adder

Table A: Truth table of 1-bit full adder obtained from the functional simulation.

INPUT			OUTPUT	
SW[2] / *A*	SW[1] / *B*	SW[0] / *Cin*	LEDR[0] / *Sum*	LEDR[1] / *Cout*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table is the same as that of theoretical truth table of a 1-bit full adder.

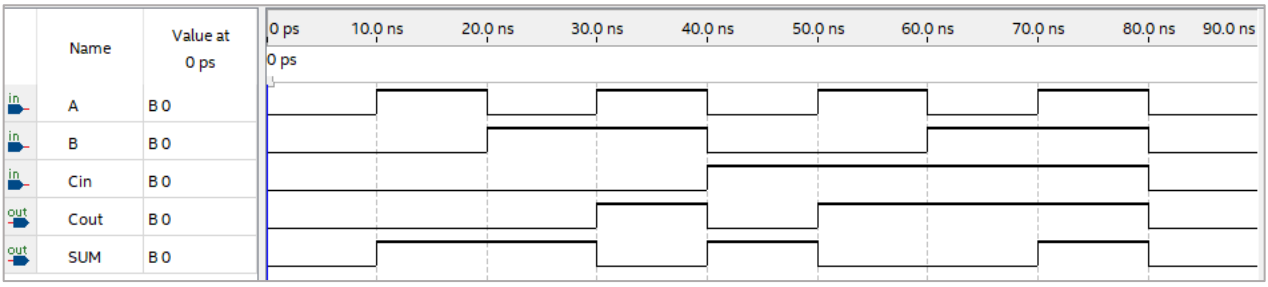


Figure 6: Functional Simulation for 1-bit Full Adder

3.0 Discussion

a) Very complex schematic design circuits tend to become unreadable and difficult to follow. Often these designs are printed on paper and a very complex circuit will be difficult to comprehend in such a scenario.

b) Schematic designs would be best used for simple circuits due to quicker design implementation as well as being very clear and any connection errors can be seen straight away. Verilog design entry would be best suited for more complex circuits where the circuitry would be too 'large' to detect connection errors and instead the behavioural approach would give a better representation for implementation.

4.0 Conclusion

The objectives of the experiment were all successfully fulfilled.

LAB 4 & 5 [Extra]: SCHEMATIC DESIGN (BLOCK DESIGN ENTRY - Simulation)

1.0 Objectives

- Creating a block design entry using Quartus Prime design software.
- Designing and simulating a 4-bit adder.

2.0 Results and Simulation

a) Block Diagram Entry

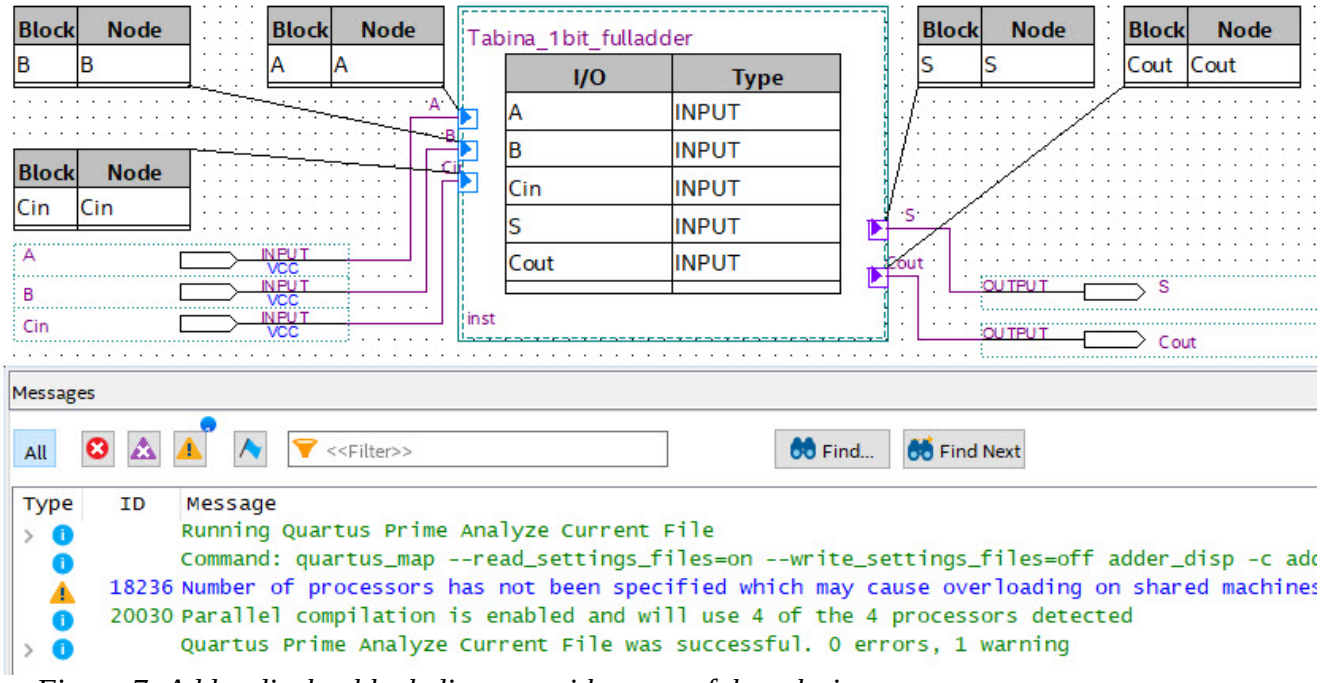


Figure 7: Adder display block diagram with successful analysis

b) Seven-segment Display

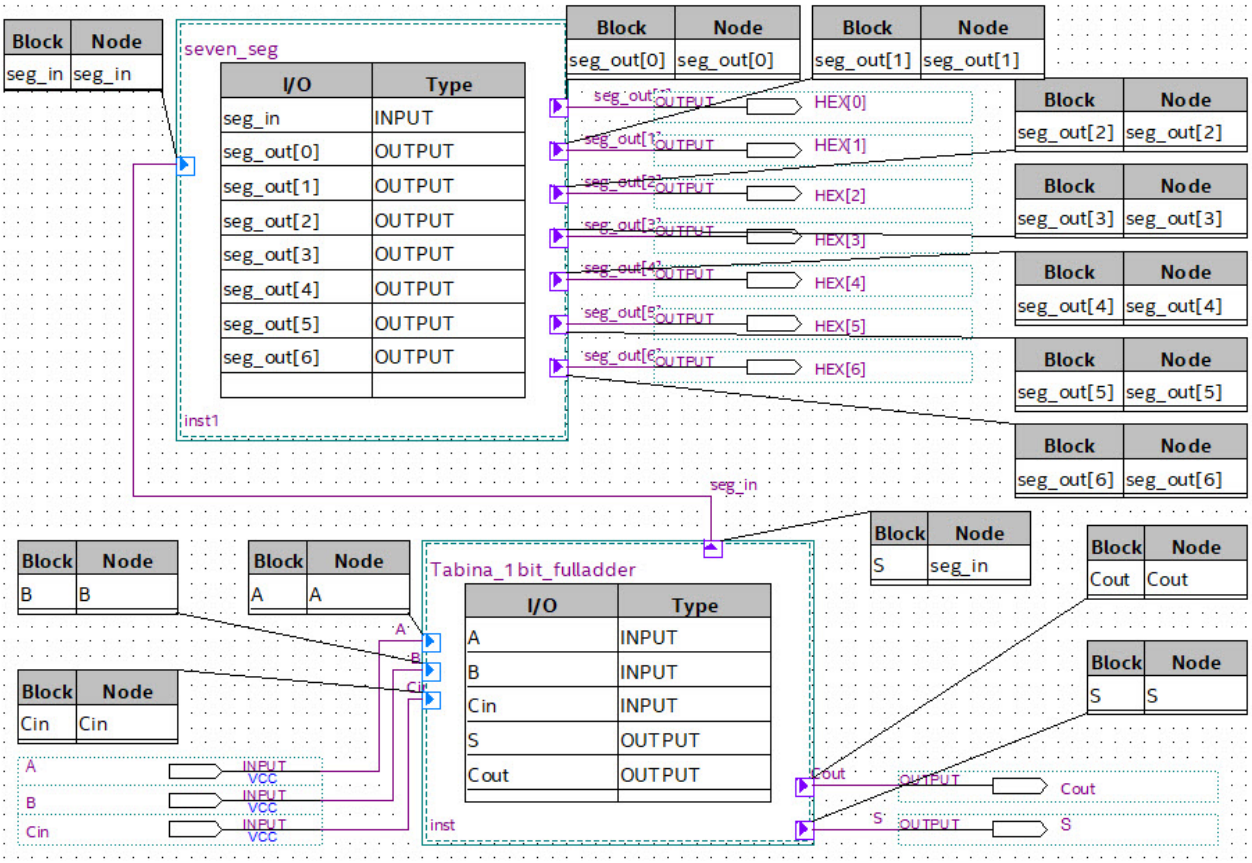
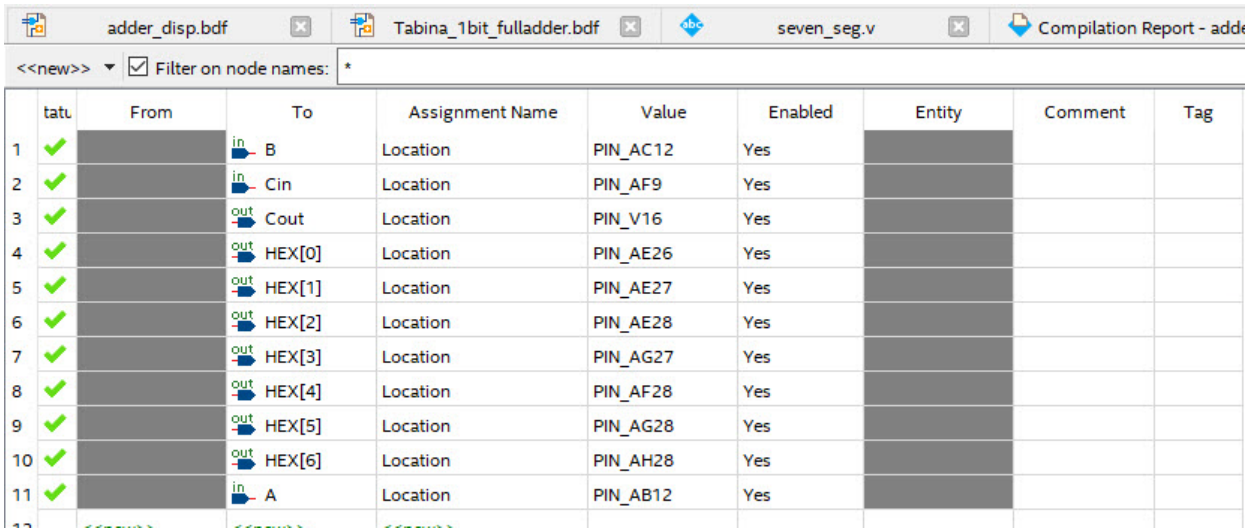


Figure 8: Full-adder with seven-segment display



	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✔		B	Location	PIN_AC12	Yes			
2	✔		Cin	Location	PIN_AF9	Yes			
3	✔		Cout	Location	PIN_V16	Yes			
4	✔		HEX[0]	Location	PIN_AE26	Yes			
5	✔		HEX[1]	Location	PIN_AE27	Yes			
6	✔		HEX[2]	Location	PIN_AE28	Yes			
7	✔		HEX[3]	Location	PIN_AG27	Yes			
8	✔		HEX[4]	Location	PIN_AF28	Yes			
9	✔		HEX[5]	Location	PIN_AG28	Yes			
10	✔		HEX[6]	Location	PIN_AH28	Yes			
11	✔		A	Location	PIN_AB12	Yes			

Figure 9: Pin assignments for adder with seven-segment display

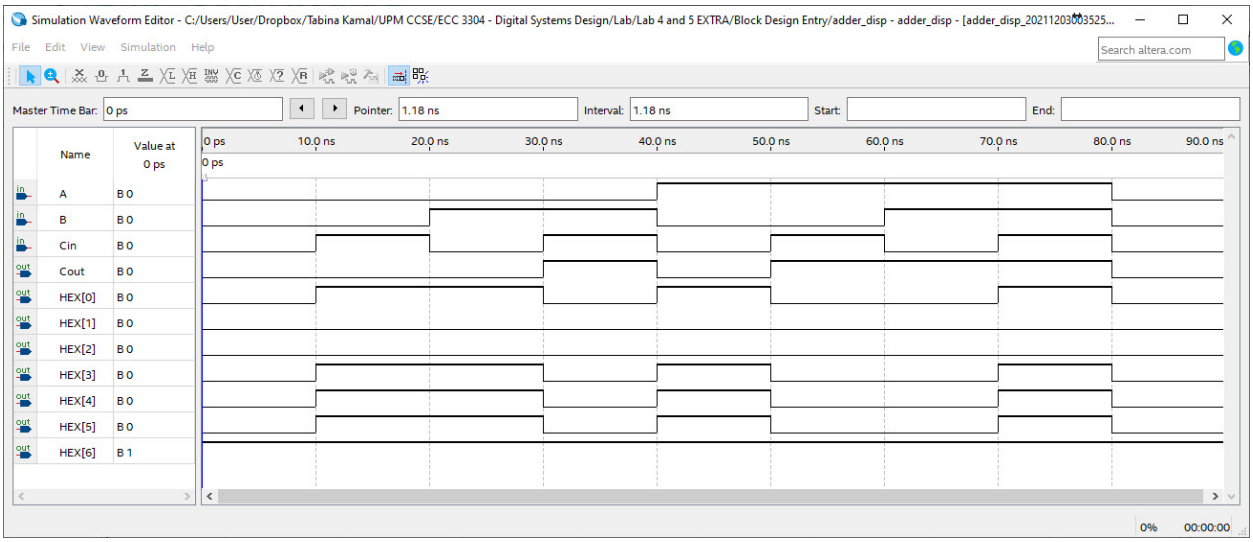


Figure 10: Functional simulation of full-adder with seven-segment display

c) 4-bit Full Adder

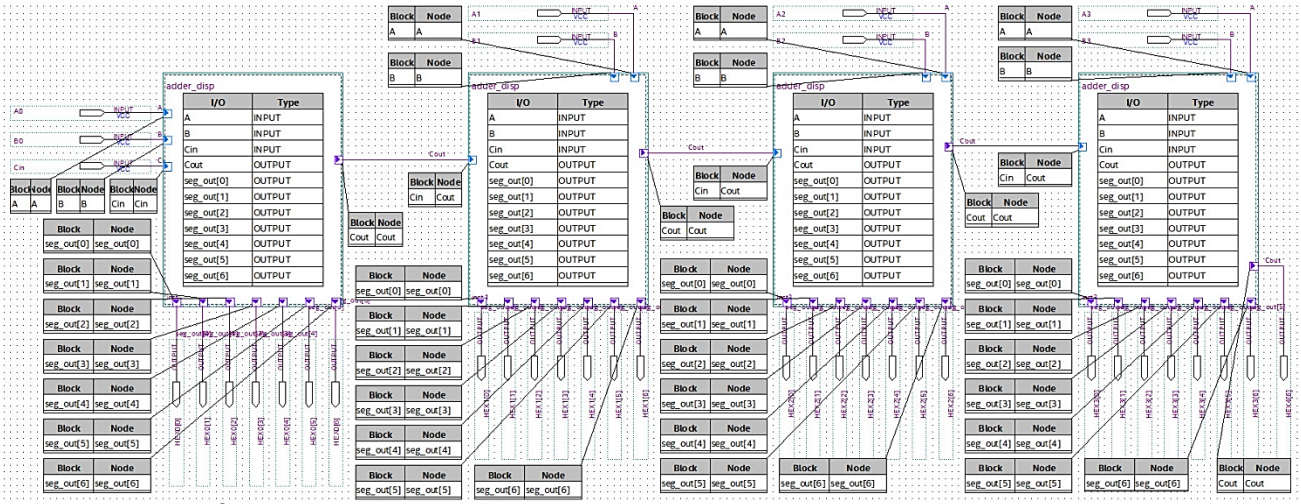


Figure 11: 4-bit full-adder circuit with seven-segment display [Attempt 1]

Type	ID	Message
ℹ	12128	Elaborating entity "seven_seg" for hierarchy "adder_disp:inst3|seven_seg:inst1"
✖	12002	Port "seg_out[0]" does not exist in macrofunction "inst2"
✖	12002	Port "seg_out[1]" does not exist in macrofunction "inst2"
✖	12002	Port "seg_out[2]" does not exist in macrofunction "inst2"
✖	12002	Port "seg_out[3]" does not exist in macrofunction "inst2"
✖	12002	Port "seg_out[4]" does not exist in macrofunction "inst2"
✖	12002	Port "seg_out[5]" does not exist in macrofunction "inst2"
✖	12002	Port "seg_out[6]" does not exist in macrofunction "inst2"
✖	12002	Port "seg_out[0]" does not exist in macrofunction "inst1"
✖	12002	Port "seg_out[1]" does not exist in macrofunction "inst1"
✖	12002	Port "seg_out[2]" does not exist in macrofunction "inst1"
✖	12002	Port "seg_out[3]" does not exist in macrofunction "inst1"
✖	12002	Port "seg_out[4]" does not exist in macrofunction "inst1"
✖	12002	Port "seg_out[5]" does not exist in macrofunction "inst1"
✖	12002	Port "seg_out[6]" does not exist in macrofunction "inst1"
✖	12002	Port "seg_out[0]" does not exist in macrofunction "inst"
✖	12002	Port "seg_out[1]" does not exist in macrofunction "inst"
✖	12002	Port "seg_out[2]" does not exist in macrofunction "inst"
✖	12002	Port "seg_out[3]" does not exist in macrofunction "inst"
✖	12002	Port "seg_out[4]" does not exist in macrofunction "inst"
✖	12002	Port "seg_out[5]" does not exist in macrofunction "inst"
✖	12002	Port "seg_out[6]" does not exist in macrofunction "inst"
✖	12002	Port "seg_out[0]" does not exist in macrofunction "inst3"
✖	12002	Port "seg_out[1]" does not exist in macrofunction "inst3"
✖	12002	Port "seg_out[2]" does not exist in macrofunction "inst3"
✖	12002	Port "seg_out[3]" does not exist in macrofunction "inst3"
✖	12002	Port "seg_out[4]" does not exist in macrofunction "inst3"
✖	12002	Port "seg_out[5]" does not exist in macrofunction "inst3"
✖	12002	Port "seg_out[6]" does not exist in macrofunction "inst3"
✖		Quartus Prime Analysis & Synthesis was unsuccessful. 28 errors, 1 warning
✖	293001	Quartus Prime Full Compilation was unsuccessful. 30 errors, 1 warning

Figure 12: 4-bit full-adder circuit with seven-segment display error messages [Attempt 1]

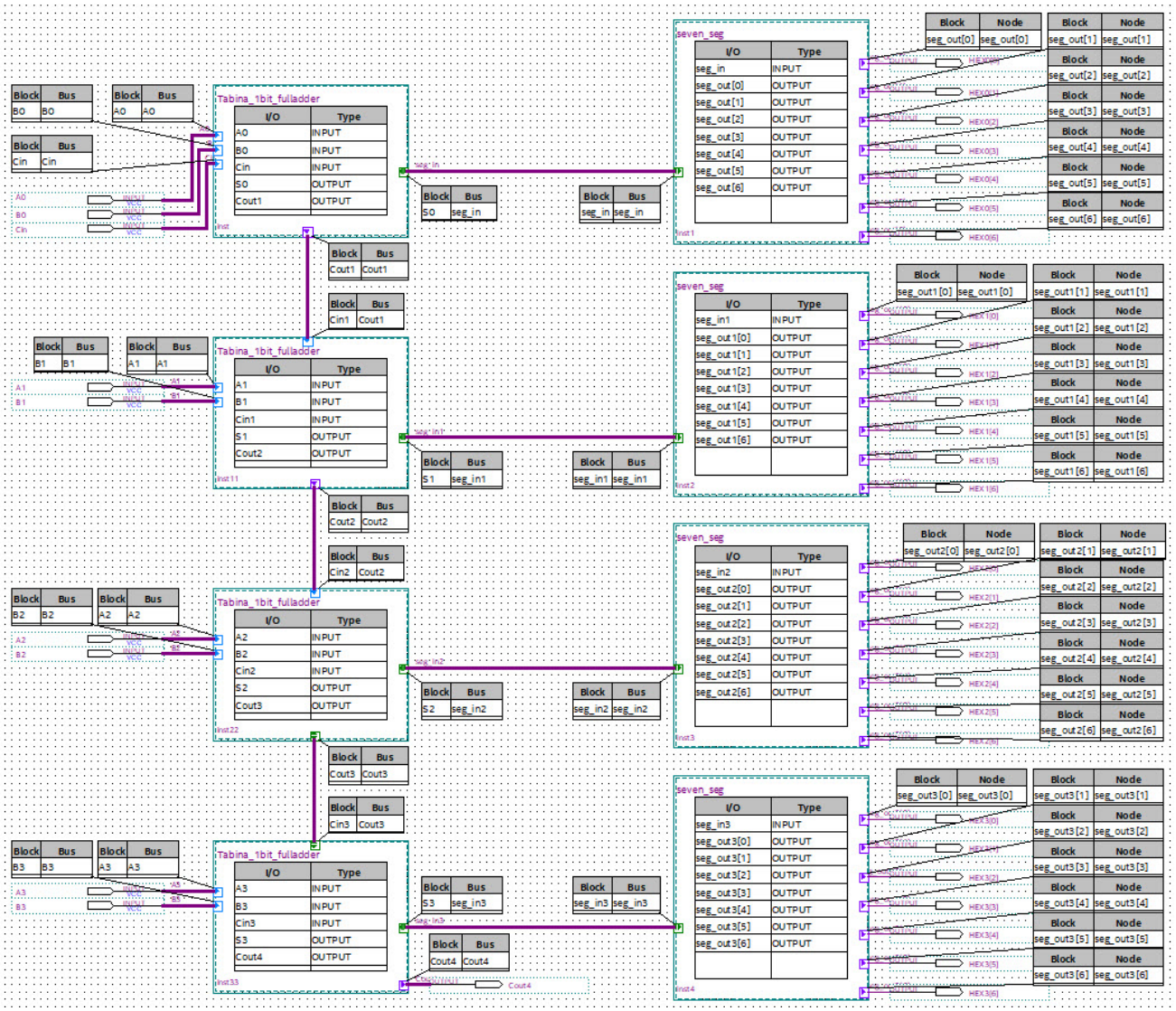


Figure 13: 4-bit full-adder circuit with seven-segment display [Attempt 2]

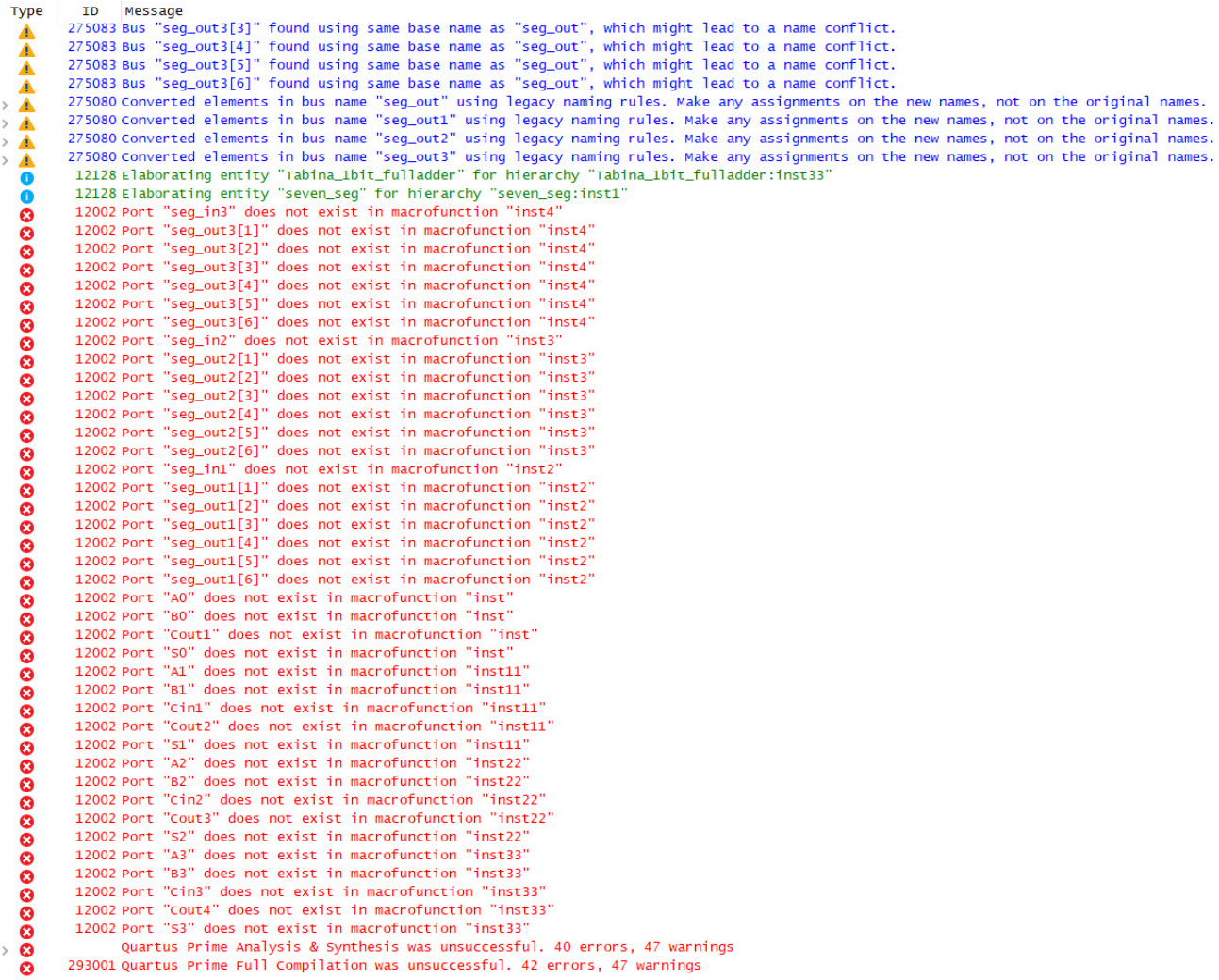


Figure 14: 4-bit full-adder circuit with seven-segment display error messages [Attempt 2]

3.0 Discussion

The expected results were obtained for parts A and B. However, part C was attempted numerous times and the same error messages were obtained in both cases.

4.0 Conclusion

The tasks were partially successful.