LOG BOOK
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LAB 3: VERILOG DESIGN ENTRY

1.0 Objectives

- Creating different models for Verilog HDL design entry using Quartus Prime design software.
- Designing and simulate a 4-bit full subtractor on an FPGA.

2.0 Results and Simulation

A. Verilog Design Entry

i) Structural Design

FullSubstractor_1bit_Struct.v | Assignment Editor

```
//structural Design for 1-bit full subractor

module FullSubstractor_1bit_Struct ( input A, B, Bin,
                                     output D, Bout );

        xor XOR1 ( P, A, B);
        not N1 (Q, B);
        and AND1 ( R, B, Q);
        xor XOR2 ( D, P, Bin);
        not N2 (S, P);
        and AND2 ( T, S, Bin);
        or OR (Bout, T, R);

endmodule
```

Figure 1: Structural design Verilog code

Assignment Editor | FullSubstractor_1bit_Struct.v | Compilation Report -

<<new>> | Filter on node names: *

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✔		in B	Location	PIN_AC12	Yes			
2	✔		in Bin	Location	PIN_AF9	Yes			
3	✔		out D	Location	PIN_V16	Yes			
4	✔		out Bout	Location	PIN_W16	Yes			
5	✔		in A	Location	PIN_AB12	Yes			
6		<<new>>	<<new>>	<<new>>					

Figure 2: Pin Assignments (Structural Design)

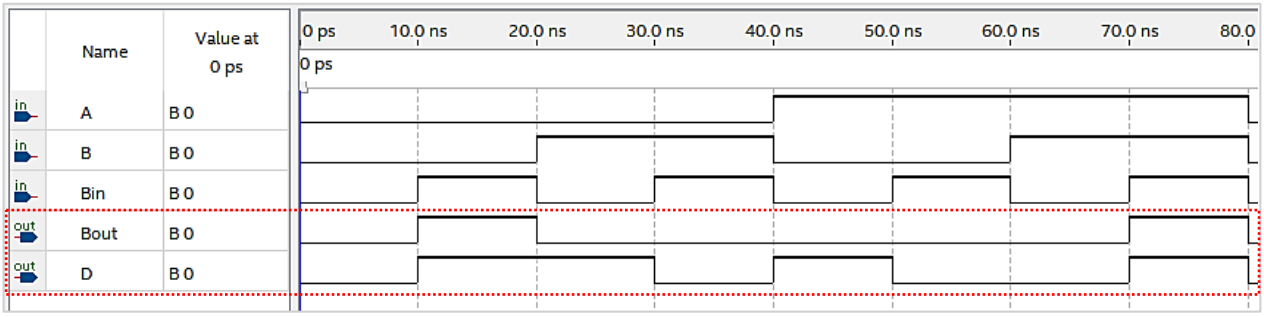

Figure 3: Functional simulation waveform (Structural Design)

ii) Data-flow Design

FullSubtr_1bit_DataFlow.v Compilation Report - F

```
// Data flow design for 1 bit Full Subtractor

module FullSubtr_1bit_DataFlow ( input X, Y, Bin,
                                 output Z, Bout );

    wire P;
    assign P = X^Y;
    assign Z = (P^Bin);
    wire R;
    assign R = (Y & ~Y);
    assign Bout = (R|(~P & Bin));

endmodule
```

Figure 5: Data flow design Verilog code (Data-flow Design)

Assignment Editor FullSubtr_1bit_DataFlow.v Compilation Report - FullSubtr_1bit_DataFlow

<<new>> Filter on node names: *

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓		out Bout	Location	PIN_W16	Yes			
2	✓		in X	Location	PIN_AB12	Yes			
3	✓		in Y	Location	PIN_AC12	Yes			
4	✓		out Z	Location	PIN_V16	Yes			
5	✓		in Bin	Location	PIN_AF9	Yes			
6		<<new>>	<<new>>	<<new>>					

Figure 6: Pin Assignments (Data-flow Design)

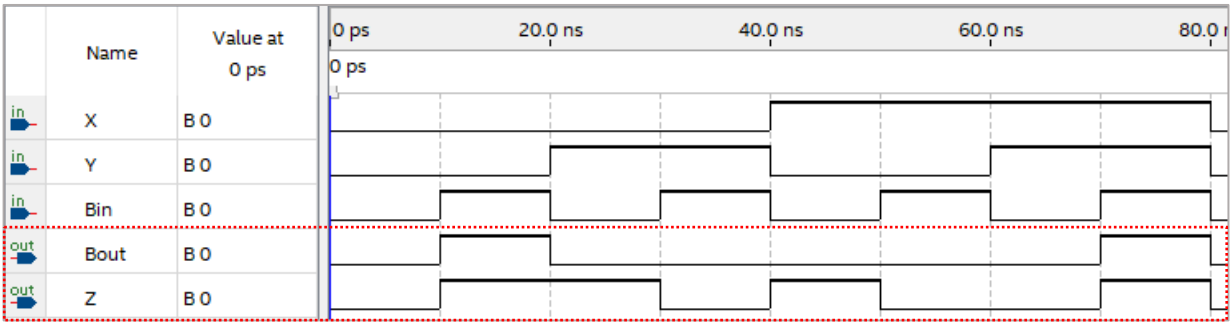

Figure 7: Functional simulation waveform (Data-flow Design)

iii) Behavioural Design

```
// Behavioural Desigm for 1 bit Full Subtractor

module FullSubtr_1bit_Behavr (W, X, Bin, D, Bout);

   input W, X, Bin;
   output reg D, Bout;
   reg P;
   reg R;

   always @*
   begin
      P = W^X;
      D = P^Bin;
      R = X & ~X;
      Bout = R + (Bin & ~P);
   end

endmodule
```

Figure 8: Behavioural design Verilog code

Assignment Editor | FullSubtr_1bit_Behavr.v | Compilation Report - FullSubtr_1bit_Behavr

<<new>> Filter on node names: *

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✓		in X	Location	PIN_AC12	Yes			
2	✓		in Bin	Location	PIN_AF9	Yes			
3	✓		out Bout	Location	PIN_V16	Yes			
4	✓		out D	Location	PIN_W16	Yes			
5	✓		in W	Location	PIN_AB12	Yes			
6		<<new>>	<<new>>	<<new>>					

Figure 9: Pin Assignments (Behavioural Design)

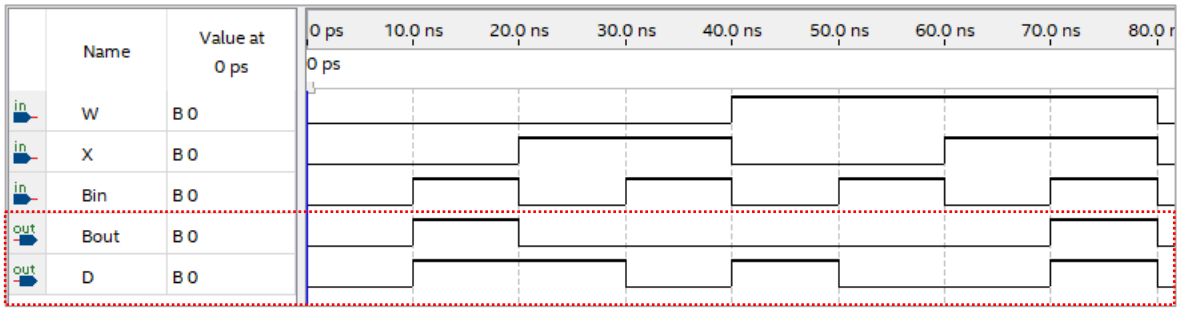

Figure 10: Functional simulation waveform (Behavioural Design)

B. Hierarchical Design

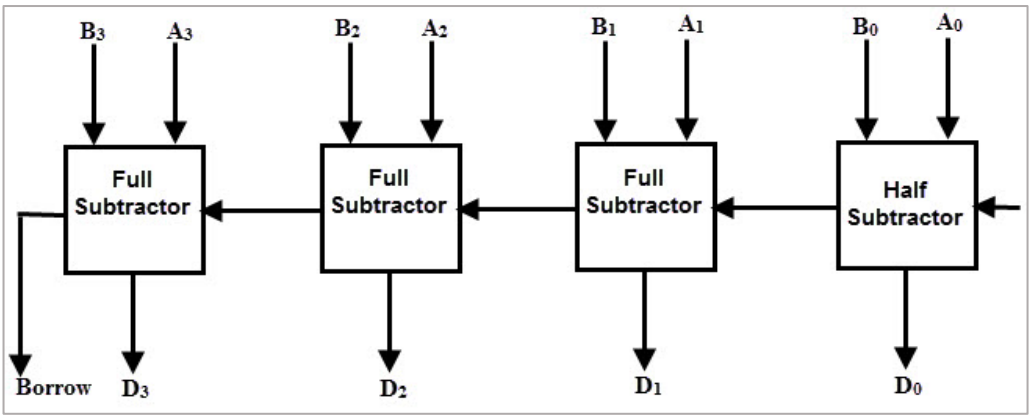

Figure 11: 4-bit Parallel Subtractor Circuit

```
// 4 bit subtractor

module Subtractor_4bit ( input A0, A1, A2, A3, B0, B1, B2, B3,
                         output D0, D1, D2, D3, BOR);

    wire W1, W2, W3;

    L3_HalfSubtr Module_1(.X(A0), .Y(B0), .hBor(W1), .D(D0));
    FullSubstractor_1bit_Struct Module_2 (.A(A1), .B(B1), .Bin(W1), .D(D1), .Bout(W2));
    FullSubstractor_1bit_Struct Module_3 (.A(A2), .B(B3), .Bin(W2), .D(D2), .Bout(W3));
    FullSubstractor_1bit_Struct Module_4 (.A(A3), .B(B3), .Bin(W3), .D(D3), .Bout(BOR));

endmodule
```

Figure 12: 4-bit Parallel Subtractor Verilog code (Use of sub-modules in Fig. 1 and Fig. 13)

```
// Half Subtractor module

module L3_HalfSubtr ( input X, Y,
                      output D, hBor);

    xor XOR1 (D, X, Y);
    not NOT1 (NOTX, X);
    and AND1 (hBor, NOTX, Y);

endmodule
```

Figure 13: Half-subtractor sub-module

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✔		in A1	Location	PIN_AC12	Yes			
2	✔		in A2	Location	PIN_AF9	Yes			
3	✔		in A3	Location	PIN_AF10	Yes			
4	✔		in B0	Location	PIN_AD11	Yes			
5	✔		in B1	Location	PIN_AD12	Yes			
6	✔		in B2	Location	PIN_AE11	Yes			
7	✔		in B3	Location	PIN_AC9	Yes			
8	✔		out BOR	Location	PIN_V16	Yes			
9	✔		out D0	Location	PIN_W16	Yes			
10	✔		out D1	Location	PIN_V17	Yes			
11	✔		out D2	Location	PIN_V18	Yes			
12	✔		out D3	Location	PIN_W19	Yes			
13	✔		in A0	Location	PIN_AB12	Yes			
14		<<new>>	<<new>>	<<new>>					

Figure 14: Pin assignment for 4-bit subtractor

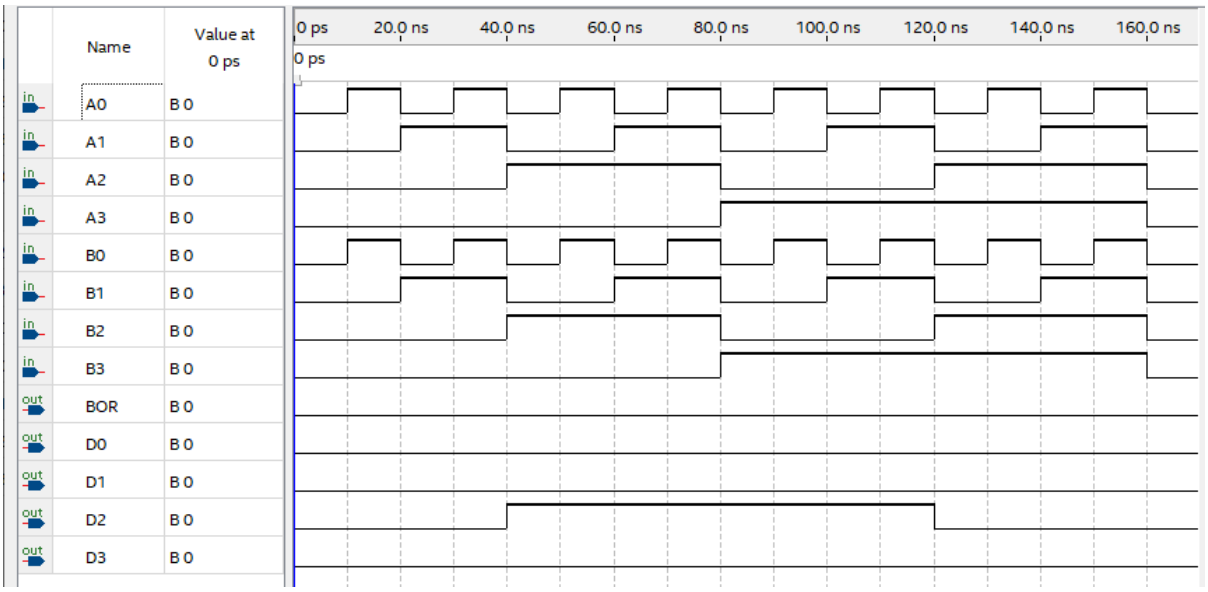

Figure 15: Figure 10: Functional simulation for 4-bit subtractor

3.0 Discussion

a) Design entry methods in Quartus Prime

Design entry type	Method
AHDL	Textual entry using a high-level language
Block Diagram /Schematic Design	A graphical/schematic method of design entry whereby the individual circuit components are represented in a circuit diagram.
EDIF	Design entry using netlist files
SystemVerilog HDL	Textual entry using the verification language used to model, design, simulate, test and implement electronic systems.
Tcl Script	Textual entry using a high-level language
Verilog HDL	
VHDL	

b) Verilog HDL models

- Structural Model: Most effective when designing simple combinational circuits as this model is the textual equivalent of a schematic diagram.
- Data-flow Model: Most effective when designing combinational circuits. It makes use of various operators.
- Behavioural Model: Used for both combinational and sequential circuits. It consists of the description of the output behaviour of the circuit.

c) Preference of Verilog model

The structural and behavioural models are the preferred models. The behavioural model seems to be the most 'versatile' and readable in terms of being closer to human language. The structural model is straight-forward and simple to understand. A combination of these models was used in the hierarchical design of the 4-bit subtractor above.

4.0 Conclusion

The objectives of this simulation experiment have been fulfilled. The functional simulations for each section were successfully obtained.