LOG BOOK [Week 6]
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CONTINUATION FROM LAB 2 [Week 4]

Results and Simulation

- **Part 4**
  The code from Part 3 was modified to turn on and of LED[0] to LED[9] using switches SW[0] to SW[9]. When a switch was turned 'on' the corresponding LED turned on.
  The circuit was successfully demonstrated.

- **Part 5**
  A single 7-segment display was controlled using switches SW[0] to SW[6]. Numerical values were displayed by toggling the switches. The input to the 7-segment display is active-LOW.
  The circuit was successfully demonstrated.

Table 1: Single segment display truth-table

NUMERICAL VALUE	***SW[0]***	***SW[1]***	***SW[2]***	***SW[3]***	***SW[4]***	***SW[5]***	***SW[6]***
0	0	0	0	0	0	0	1
1	1	0	0	1	1	1	1
2	0	0	1	0	0	1	0
3	0	0	0	0	1	1	0
4	1	0	0	1	1	0	0
5	0	1	0	0	1	0	0
6	0	1	0	0	0	0	0
7	0	0	0	1	1	1	1
8	0	0	0	0	0	0	0
9	0	0	0	0	1	0	0

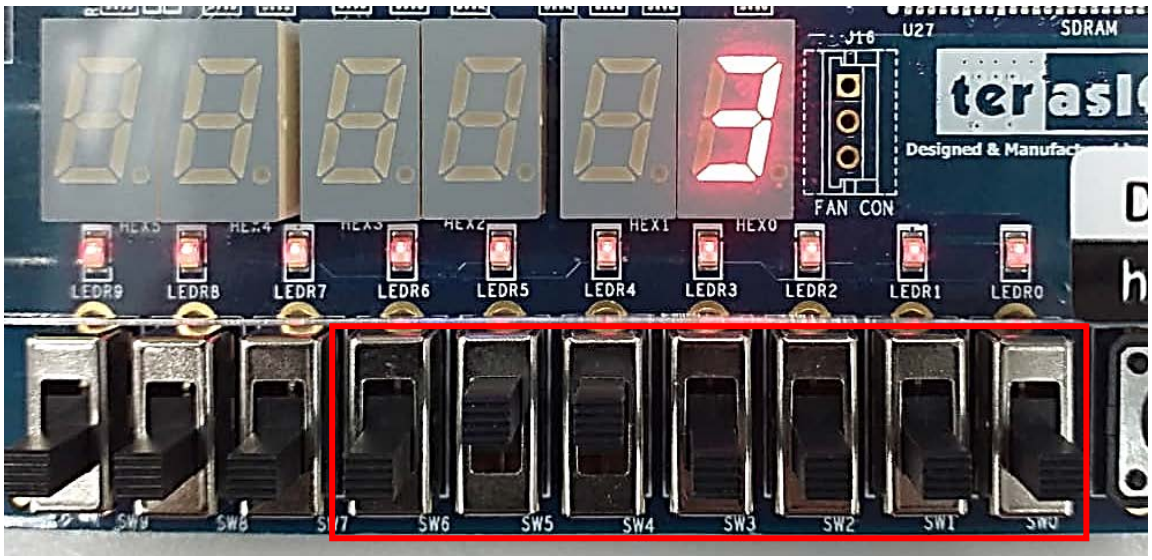

Figure A: Numerical value '3' displayed on a single 7-segment display

- **Part 6**
  Four 7-segment displays from HEX[0] to HEX[3] were coded to display CCSE.
  The circuit was successfully demonstrated.

```
1   //ACTIVE LOW INPUT
2   module DisplayCCSE_Tabina (HEX0, HEX1, HEX2, HEX3);
3   output [6:0] HEX0, HEX1, HEX2, HEX3; // red LEDs
4      assign HEX3[0] = 0;
5      assign HEX3[1] = 1;
6      assign HEX3[2] = 1;
7      assign HEX3[3] = 0;
8      assign HEX3[4] = 0;
9      assign HEX3[5] = 0;
10     assign HEX3[6] = 1;
11
12     assign HEX2[0] = 0;
13     assign HEX2[1] = 1;
14     assign HEX2[2] = 1;
15     assign HEX2[3] = 0;
16     assign HEX2[4] = 0;
17     assign HEX2[5] = 0;
18     assign HEX2[6] = 1;
19
20     assign HEX1[0] = 0;
21     assign HEX1[1] = 1;
22     assign HEX1[2] = 0;
23     assign HEX1[3] = 0;
24     assign HEX1[4] = 1;
25     assign HEX1[5] = 0;
26     assign HEX1[6] = 0;
27
28     assign HEX0[0] = 0;
29     assign HEX0[1] = 1;
30     assign HEX0[2] = 1;
31     assign HEX0[3] = 0;
32     assign HEX0[4] = 0;
33     assign HEX0[5] = 0;
34     assign HEX0[6] = 0;
35  endmodule
```

Figure B: Code for displaying CCSE (from Lab 2 – code modified)

Figure C: 'CCSE' displayed on 7-segment displays HEX[3] to HEX[0].

LAB 4: SCHEMATIC DESIGN ENTRY (Board Testing)

1.0 Objectives

- Creating a schematic design entry using Quartus Prime design software.
- Compiling and testing a simple light circuit and a 1-bit full adder on the FGPA.

2.0 Results and Simulation

A. Schematic Design Entry

The truth table was created from the obtained output on the board. The value 0 represents OFF and 1 represents ON. The inputs are SW[0] and SW[1]. The output is LEDR[0].

SW[0] / x_1	SW[1] / x_2	LEDR[0] / f
0	0	0
0	1	1
1	0	1
1	1	0

The results obtained from the board testing of the schematic design was the same as that obtained from the Verilog design from Lab 2A.

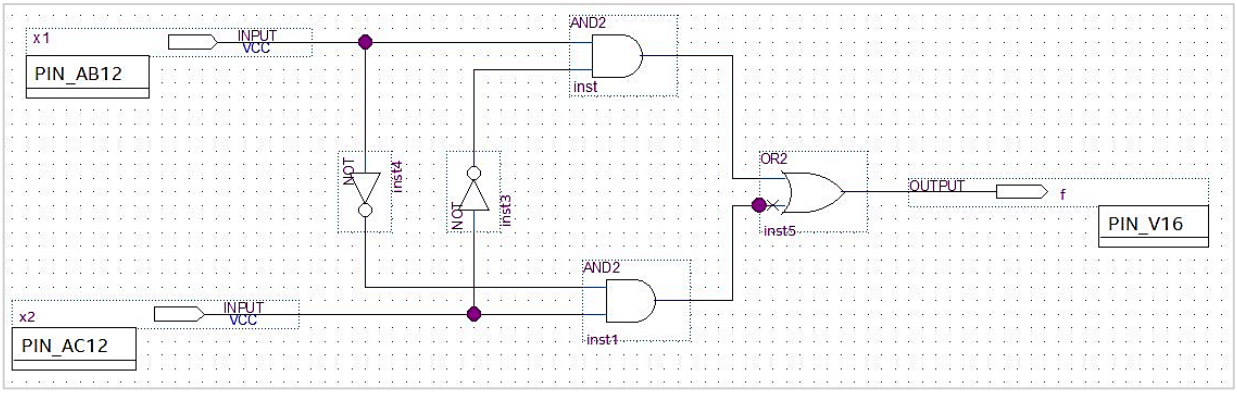

Figure 1: Schematic Design from Quartus_Prime_Schematic.pdf

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✔		in x2	Location	PIN_AC12	Yes			
2	✔		out f	Location	PIN_V16	Yes			
3	✔		in x1	Location	PIN_AB12	Yes			
4		<<new>>	<<new>>	<<new>>					

Figure 2: Pin Assignments for Schematic Design rom Quartus_Prime_Schematic.pdf

B. Design of 1-bit Full Adder

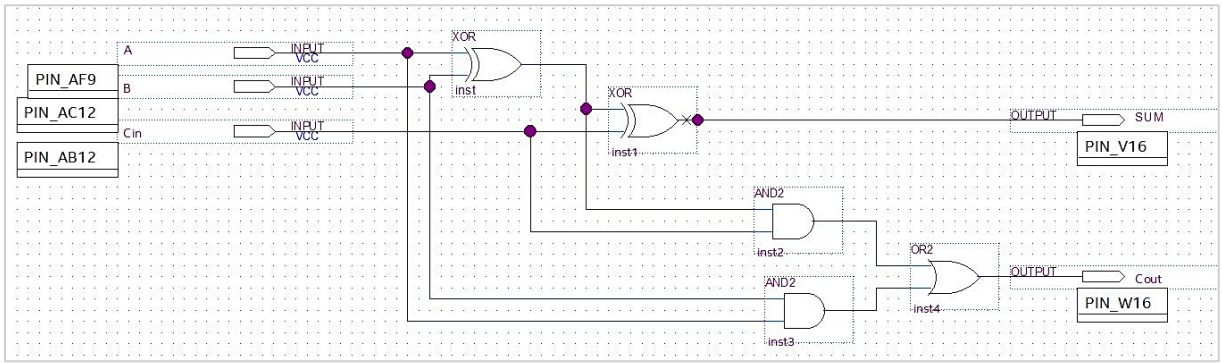

Figure 3: Schematic Design of 1-bit Full Adder

	tatu	From	To	Assignment Name	Value	Enabled	Entity	Comment	Tag
1	✔		in B	Location	PIN_AC12	Yes			
2	✔		in Cin	Location	PIN_AB12	Yes			
3	✔		out Cout	Location	PIN_W16	Yes			
4	✔		out SUM	Location	PIN_V16	Yes			
5	✔		in A	Location	PIN_AF9	Yes			
6		<<new>>	<<new>>	<<new>>					

Figure 4: Pin Assignments for 1-bit Full Adder

Table A: Truth table of 1-bit full adder obtained from the board testing.

INPUT			OUTPUT	
SW[2] / *A*	SW[1] / *B*	SW[0] / *Cin*	LEDR[0] / *Sum*	LEDR[1] / *Cout*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth table is the same as that of theoretical truth table of a 1-bit full adder.

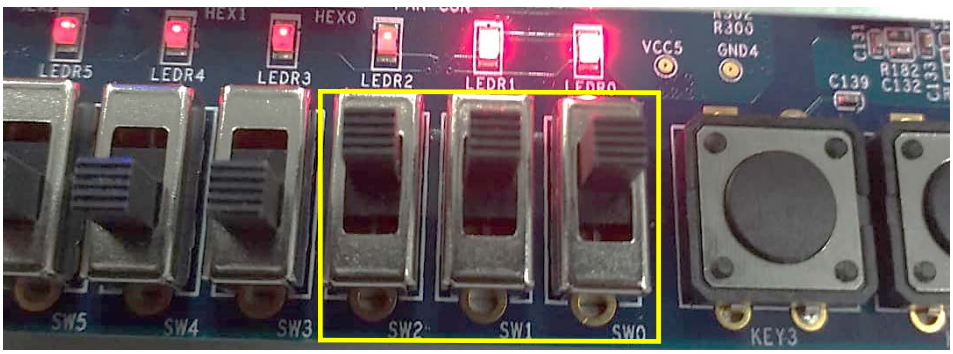

Figure 5: Board testing output of 1-bit Full Adder
(SW[0]=SW[1]=SW[2]=1 and LED[0]=LED[1]=1)

3.0 Discussion

a) No, it is not practical to test for a higher-bit adder using the LEDs and switches as there is a limited number of them on the board. For example, it would not be possible to implement an 8-bit full adder on the board. It would require 8 switches for each addend, requiring a total of 16 switches (not including the required carry in input) whereas the board only has 10 available switches. An alternate method of testing higher-bit adders would be to test the adder circuits on a breadboard using IC chips instead of an FGPA board.

b) For the ***light*** circuit, the schematic design entry is the preferred method rather than the Verilog entry design. The circuit is very simple so the schematic design entry is a very straightforward way to implement the circuit. It is much quicker in terms of design entry time.

4.0 Conclusion

The objectives of the experiment were all successfully fulfilled and the circuits were demonstrated.