LOG BOOK
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Matric No.: 208651
Assigned Date: 04 November 2021

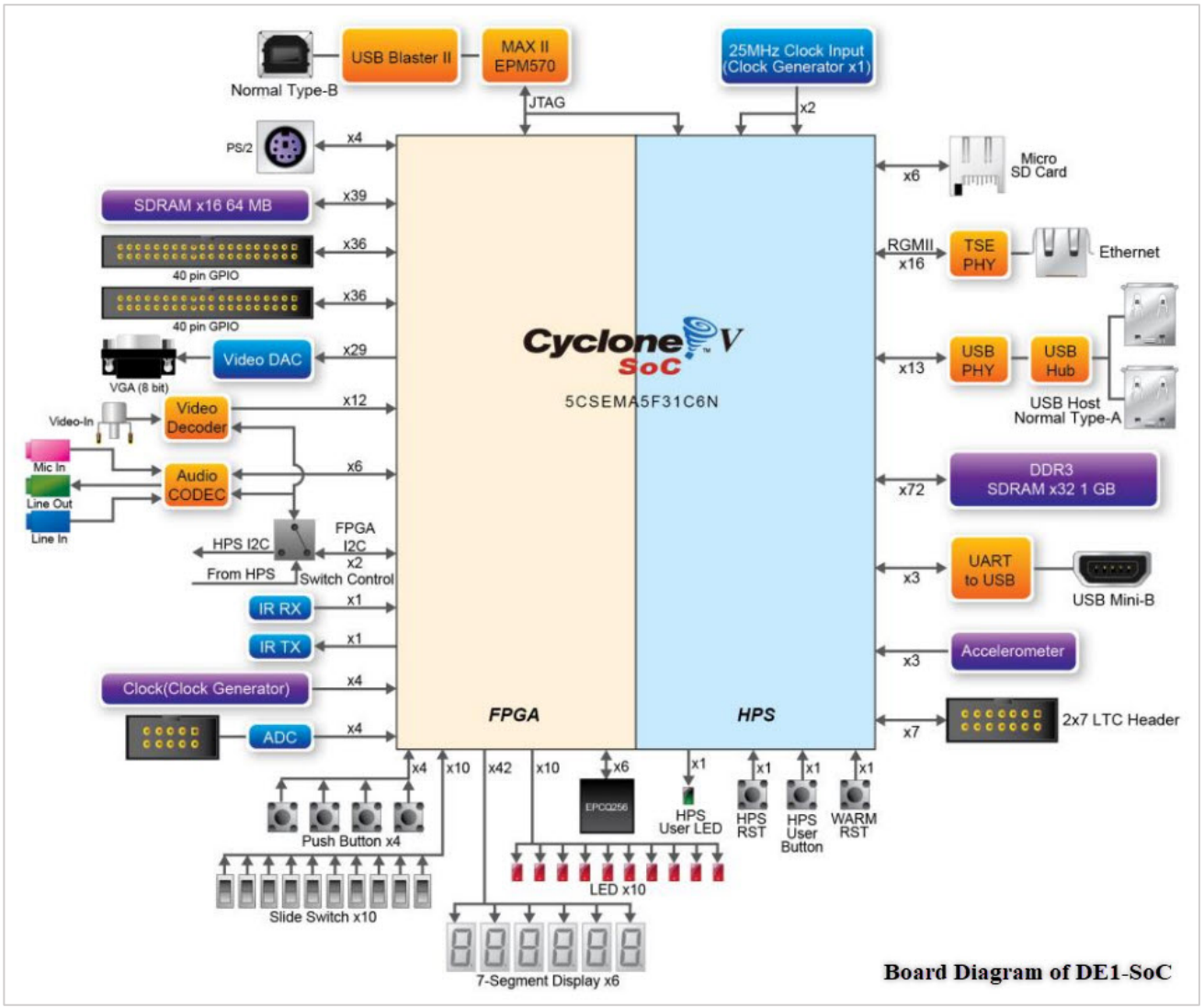
LAB 1: INTRODUCTION TO QUARTUS PRIME USING VERILOG

1.0 Objectives

- Differentiating between the DE1-SoC board and the DE2-SoC boards.
- Understanding the main features in the Quartus Prime software.

2.0 Results and Simulation

- ***Differences between DE1-SoC and DE2-SoC boards***



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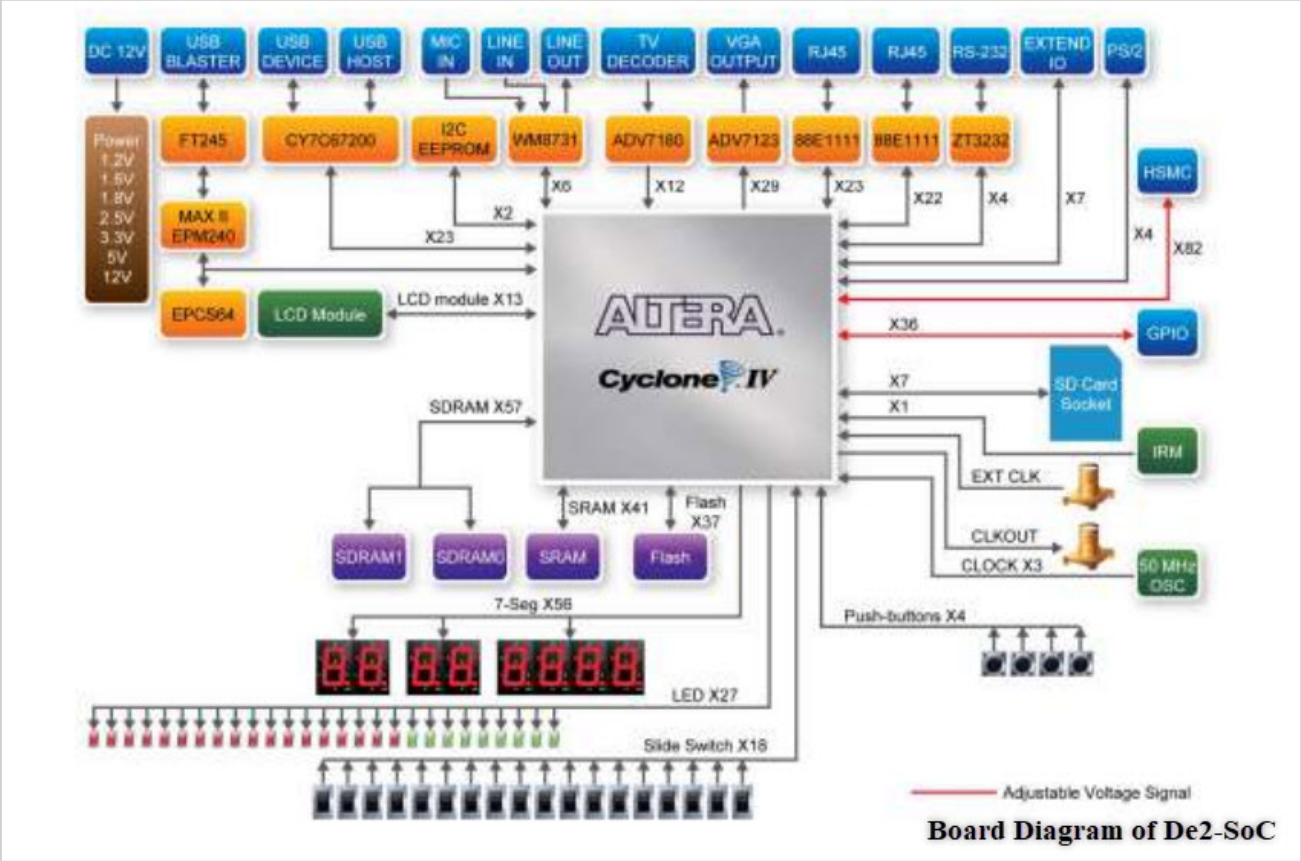

- ***Introduction to Quartus Prime Design Software***

  STEPS USED FOR FGPA DESIGN:

1) Open Quartus Prime and define a new project.
2) Choose an empty project. Then add files if necessary.
3) Choose the correct Device Family and a device from ‘available devices’ In this case the device family ‘Cyclone V’ was used and the device was ‘5CSEMA5F31C6’.
4) EDA tool settings are not chosen as only Quartus tools will be used.
5) A summary will be displayed, if correct, click ‘Yes’.
6) The text editor needs to be used to write the code for Verilog design. Click on File > New > Verilog VHDL file > Ok. A text file with .v extension will be created. The file is to ve saved.
7) To compile, click Processing > Start Compilation. A compilation report is produced, check for errors in the code if any.
8) The pins were assigned according to the ‘DE1-SoC user manual’. Click on Assignment > Assignment Editor. Assign the correct pins to the inputs and outputs and then recompile.
9) For simulation, open the waveform simulator. Set the end time and insert nodes, then adjust the waveform with the inputs and run the functional or timing simulation.

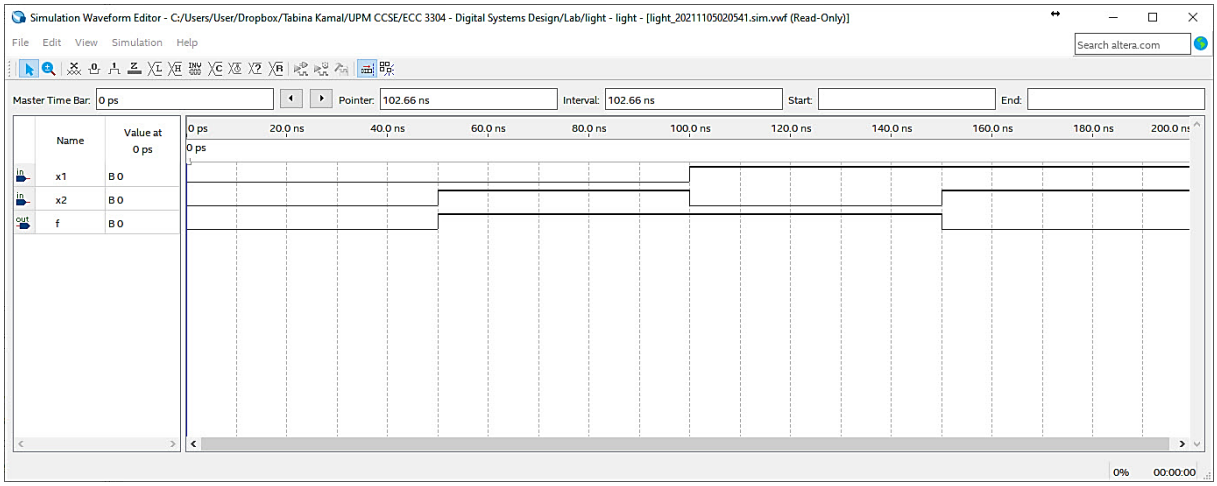

Figure 1: Functional simulation waveform

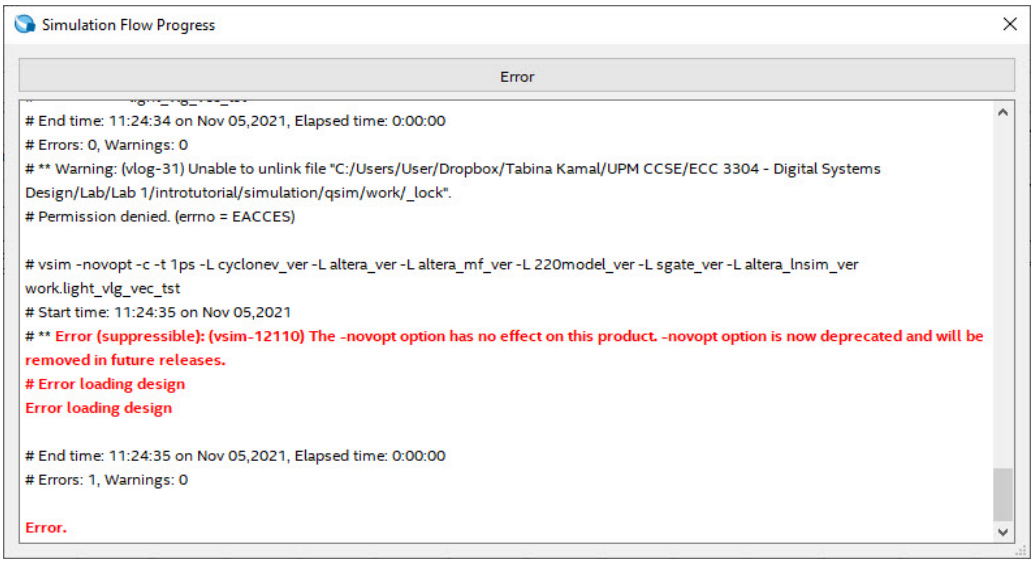

Figure 2: Error message produced after timing simulation

3.0 Discussion

- ***Differences between DE1-SoC and DE2-SoC boards***

  Overall, the DE1-SoC is 'higher' in specifications compared to the DE2-SoC. At first glance, the DE1-Soc has 2 parts to it, the FGPA and the HPS while the DE2-SoC has only the FGPA part. Below is a table summarising the main differences between the boards:

DE1-SoC	DE2-SoC
Cyclone V device	Cyclone IV device
Dual core ARM cortex	No ARM cortex
Larger Memory	Smaller memory
Larger choice of switches, buttons and Indicators	Small choice of switches and indicators. No buttons.
12 DC input	Desktop PC input Switching and step-down regulators
ADC present	No ADC

- ***Introduction to Quartus Prime Design Software***

  The functional simulation was obtained as expected, however there were some errors that occurred due to some software settings. The following errors and their solutions are as below:

  - *Error (199014) Vector Source File*
    Solution: In the simulation waveform editor, click 'Simulation > Simulation Settings > Restore Defaults > Save'

  - *Error (199013) Vector Source File*
    Solution: In the simulation waveform editor, click 'Simulation > Simulation Settings', then delete ' -novopt' following 'vsim'.

  - *Lock file Warning*
    Solution: Delete the 'lock' file in the 'work' folder under the 'simulation' folder in the project folder.

  The timing simulation is not possible with the 'Cyclone V' that is used for this simulation. It is only supported by the Cyclone IV and Stratix IV FGPAs as mentioned in the 'Quartus Prime Introduction' booklet. The error message produced is shown in Figure 2 above.

4.0 Conclusion

The objectives of the experiment have been fulfilled. The differences between the DE1-SoC and the DE2-SoC boards were found. Although the timing simulation was not successful, the expected result was obtained for the functional simulation from running the code provided in the 'Quartus Prime Introduction' booklet.