CSE231 HW2 - REPORT

```
mux_module.v:
       -mux_module (out, a, b, c, d, s0, s1)
        -Find the output for 4*1 mux .
for_xor.v:
       - for_xor (out, a, b)
       -Find the output for XOR operation.
one_bit.v :
        -one_bit (r_i, c_i_plus, a, b, c, alu_op_2, less, alu_op_0, alu_op_1)
       -Find the output for one bit operation.
twenty_two_bit.v :
       -thirty_two_bit (r_i, c_i_plus, a, b, c, alu_op_2, less, alu_op_0, alu_op_1)
       --Find the output for twenty two bit operation.
twenty_two_bit_ALU_test_bench.v :
       -This header same the main.
       -This function do input operation and give the result.
```

-AND First Example

```
Library × sim ×
🖳 Transcript :
 # -- Compiling module thirty_two_bit_ALU_test_bench
 # Top level modules:
       thirty_two_bit_ALU_test_bench
ModelSim > vsim work.thirty_two_bit_ALU_test_bench
 # vsim work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty_two_bit
 # Loading work.one_bit
 # Loading work.for_xor
 # Loading work.mux module
VSIM 8> step -current
 # S0 = 0
  S1 = 0
       a = 10001001001000100001000011100001
  carry out = 10001011001000000000000011100001
 VSIM 9>
Now: 20 ps Delta: 0
                            sim:/thirty_two_bit_ALU_test_bench
```

-OR First Example

```
sim ×
Library ×
Transcript
# -- Compiling module thirty_two_bit_ALU_test_bench
# Top level modules:
       thirty two bit ALU test bench
VSIM 14> vsim work.thirty_two_bit_ALU_test_bench
# vsim work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty two bit ALU test bench
# Loading work.thirty_two_bit
# Loading work.one bit
 # Loading work.for xor
 # Loading work.mux_module
VSIM 15> step -current
 # S0 = 0
 # S1 = 1
        a = 10001001001000100001000011100001
        b = 1100101100100100000100000100001
 # result = 11001011001001100001100011100001
 # carry out = 10001011001000000000000011100001
VSIM 16>
Now: 20 ps Delta: 0
                             sim:/thirty two bit ALU test bench
```

-ADD First Example (not overflow)

```
Library × sim ×
Transcript
# -- Compiling module thirty two bit ALU test bench
# Top level modules:
       thirty_two_bit_ALU_test_bench
VSIM 42> vsim work.thirty two bit ALU test bench
# vsim work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty_two_bit
 # Loading work.one_bit
# Loading work.for xor
 # Loading work.mux module
VSIM 43> step -current
 50 = 1
# S1 = 0
      result = 00000000000000000000000000001110
  VSIM 44>
Now: 20 ps Delta: 0
                        sim:/thirty_two_bit_ALU_test_bench
```

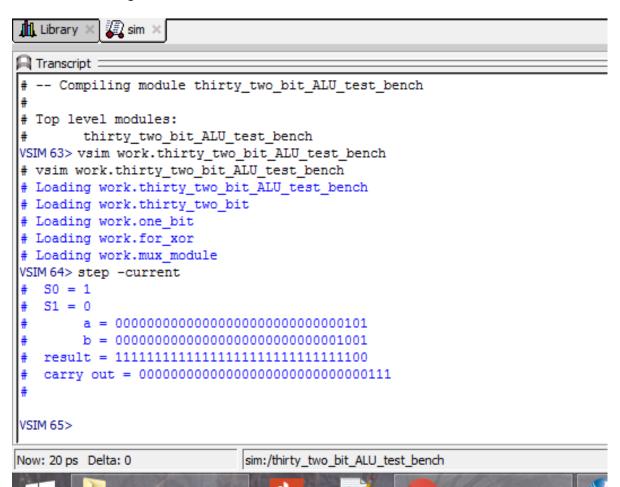
-ADD Second Example With OVERFLOW

```
Transcript =
# -- Compiling module thirty_two_bit_ALU_test_bench
# Top level modules:
      thirty two bit ALU test bench
VSIM 49> vsim work.thirty two bit ALU test bench
# vsim work.thirty_two_bit_ALU_test_bench
# Loading work.thirty_two_bit_ALU_test_bench
# Loading work.thirty two bit
# Loading work.one bit
# Loading work.for xor
# Loading work.mux module
VSIM 50> step -current
  50 = 1
  S1 = 0
       result = 10000000000000000000000000001110
  VSIM 51>
Now: 20 ps Delta: 0
                        sim:/thirty two bit ALU test bench
```

-SUBSTRACT For Pozitive Answer

```
Library × asim ×
# -- Compiling module thirty two bit ALU test bench
# Top level modules:
      thirty_two_bit_ALU_test_bench
VSIM 56> vsim work.thirty_two_bit_ALU_test_bench
# vsim work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty_two_bit_ALU_test_bench
# Loading work.thirty two bit
# Loading work.one_bit
# Loading work.for_xor
# Loading work.mux module
VSIM 57> step -current
 # S0 = 1
  S1 = 0
      VSIM 58>
Now: 20 ps Delta: 0
                     sim:/thirty_two_bit_ALU_test_bench
```

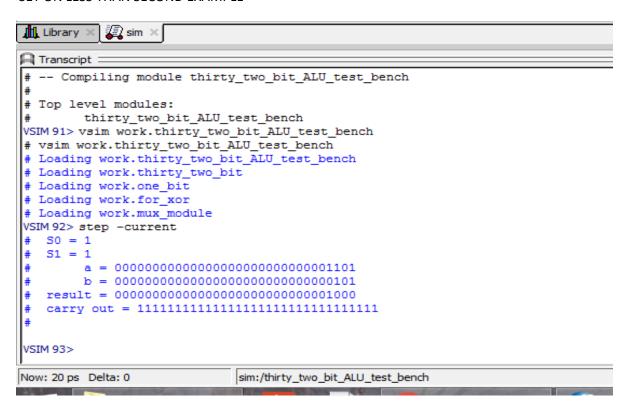
-SUBSTRACT For Negative Answer



-SET ON LESS THAN FIRST EXAMPLE

```
Library × sim ×
Transcript
# -- Compiling module thirty_two_bit_ALU_test_bench
# Top level modules:
        thirty_two_bit_ALU_test_bench
VSIM 98> vsim work.thirty_two_bit_ALU_test_bench
 # vsim work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty_two_bit_ALU_test_bench
 # Loading work.thirty_two_bit
 # Loading work.one_bit
 # Loading work.for_xor
 # Loading work.mux module
VSIM 99> step -current
   50 = 1
        b = 00000000000000000000000000001101
   result = 11111111111111111111111111111000
   carry out = 0000000000000000000000000000111
VSIM 100>
                            sim:/thirty_two_bit_ALU_test_bench
Now: 20 ps Delta: 0
```

-SET ON LESS THAN SECOND EXAMPLE



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