```
1   module dataMem
2      ( input wire clk, WE,
3        input wire [31:0] adress, writeData,
4        output wire [31:0] ReadData);
5
6       reg [7:0] RAM [255:0] //256 byte memory
7
8       assign ReadData = RAM[adress[31:0]];
9
10      initial begin
11        $readmemh("datamemory.txt", RAM);
12        #100;
13      end
14
15      always @(posedge clk)
16      begin
17        if(WE == 1'b1)
18           RAM[adress[31:0]] <= writeData;
19      end
20  endmodule
```