

18/12/2018

EE447 LABORATORY  
EXPERIMENT 5  
PRELIMINARY REPORT

Muttalip Caner TOL

2031466

Wednesday Afternoon

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1  ;*****
2  ; Program ADC.s
3  ; Takes analog signal between 000-FFF gives between 0-330
4  ;*****
5  ; EQU Directives
6
7  ;*****
8  ;LABEL          DIRECTIVE    VALUE          COMMENTS
9
10 ; ADC Registers
11 RCGCADC         EQU          0x400FE638      ; ADC clock register
12 ; ADC0 base address EQU 0x40038000
13 ADC0_ACTSS      EQU          0x40038000      ; Sample sequencer (ADC0 base address)
14 ADC0_RIS        EQU          0x40038004      ; Interrupt status
15 ADC0_IM         EQU          0x40038008      ; Interrupt select
16 ADC0_EMUX       EQU          0x40038014      ; Trigger select
17 ADC0_PSSI       EQU          0x40038028      ; Initiate sample
18 ADC0_SSMUX3     EQU          0x400380A0      ; Input channel select
19 ADC0_SSCTL3     EQU          0x400380A4      ; Sample sequence control
20 ADC0_SSFIFO3    EQU          0x400380A8      ; Channel 3 results
21 ADC0_PC         EQU          0x40038FC4      ; Sample rate
22 ADC0_ISC        EQU          0x4003800C      ; Interrupt Status and Clear
23 ; GPIO Registers
24 RCGCGPIO        EQU          0x400FE608      ; GPIO clock register
25 ;PORT E base address EQU 0x40024000
26 PORTE_DEN       EQU          0x4002451C      ; Digital Enable
27 PORTE_PCTL      EQU          0x4002452C      ; Alternate function select
28 PORTE_AFSEL     EQU          0x40024420      ; Enable Alt functions
29 PORTE_AMSEL     EQU          0x40024528      ; Enable analog
30
31
32 ;*****
33 ;LABEL          DIRECTIVE    VALUE          COMMENT
34              AREA          main, READONLY, CODE
35              THUMB
36              EXTERN        CONVRT          ; Reference external subroutines
37              EXPORT        __ADC          ; Make available
38
39 __ADC          PUSH        {R0-R6,R8-R12}  ; Start clocks for features to be used
40              LDR           R1, =RCGCADC    ; Turn on ADC clock
41              LDR           R0, [R1]
42              ORR           R0, R0, #0x01    ; set bit 0 to enable ADC0 clock
43              STR           R0, [R1]
44              NOP
45              NOP
46              NOP              ; Let clock stabilize
47              LDR           R1, =RCGCGPIO   ; Turn on GPIO clock
48              LDR           R0, [R1]
49              ORR           R0, R0, #0x10    ; set bit 4 to enable port E clock
50              STR           R0, [R1]
51              NOP
52              NOP
53              NOP              ; Let clock stabilize
54              ; Setup GPIO to make PE3 input for ADC0
55              ; Enable alternate functions
56              LDR           R1, =PORTE_AFSEL
57              LDR           R0, [R1]
58              ORR           R0, R0, #0x08    ; set bit 3 to enable alt functions on PE3
59              STR           R0, [R1]
60              ; PCTL does not have to be configured
61              ; since ADC0 is automatically selected when
62              ; port pin is set to analog.
63              ; Disable digital on PE3
64              LDR           R1, =PORTE_DEN
65              LDR           R0, [R1]
66              BIC           R0, R0, #0x08    ; clear bit 3 to disable digital on PE3
67              STR           R0, [R1]
68              ; Enable analog on PE3
69              LDR           R1, =PORTE_AMSEL
70              LDR           R0, [R1]
71              ORR           R0, R0, #0x08    ; set bit 3 to enable analog on PE3
72              STR           R0, [R1]
73              ; Disable sequencer while ADC setup
74              LDR           R1, =ADC0_ACTSS
75              LDR           R0, [R1]
76              BIC           R0, R0, #0x08    ; clear bit 3 to disable SS3
77              STR           R0, [R1]

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78      ; Select trigger source
79      LDR      R1, =ADC0_EMUX
80      LDR      R0, [R1]
81      BIC      R0, R0, #0xF000      ; clear bits 15:12 to select SOFTWARE
82      STR      R0, [R1]            ; trigger
83      ; Select input channel
84      LDR      R1, =ADC0_SSMUX3
85      LDR      R0, [R1]
86      BIC      R0, R0, #0x000F      ; clear bits 3:0 to select AIN0
87      STR      R0, [R1]
88      ; Config sample sequence
89      LDR      R1, =ADC0_SSCTL3
90      LDR      R0, [R1]
91      ORR      R0, R0, #0x06        ; set bits 2:1 (IE0, END0)
92      STR      R0, [R1]
93      ; Set sample rate
94      LDR      R1, =ADC0_PC
95      LDR      R0, [R1]
96      ORR      R0, R0, #0x01        ; set bits 3:0 to 0x1 for 125k sps
97      STR      R0, [R1]
98      ; Done with setup, enable sequencer
99      LDR      R1, =ADC0_ACTSS
100     LDR      R0, [R1]
101     ORR      R0, R0, #0x08        ; set bit 3 to enable seq 3
102     STR      R0, [R1]            ; sampling enabled but not initiated yet
103     ; start sampling routine
104     LDR      R3, =ADC0_RIS        ; interrupt address
105     LDR      R4, =ADC0_SSFI03     ; result address
106     LDR      R2, =ADC0_PSSI       ; sample sequence initiate address
107     LDR      R6, =ADC0_ISC
108     ; initiate sampling by enabling sequencer 3 in ADC0_PSSI
109     LDR      R0, [R2]
110     ORR      R0, R0, #0x08        ; set bit 3 for SS3
111     STR      R0, [R2]
112     ; check for sample complete (bit 3 of ADC0_RIS set)
113     Cont    LDR      R0, [R3]
114     ANDS     R0, R0, #8
115     BEQ      Cont
116     ;branch fails if the flag is set so data can be read and flag is cleared
117     LDR      R7, [R4]
118     ;map between 0-330
119     MOV      R0, #806
120     MOV      R1, #10000
121     MUL      R7, R0
122     UDIV     R7, R1
123
124     ;MOV      R0, R5                ;store the data
125     MOV      R0, #8
126     STR      R0, [R6]            ; clear flag
127     POP      {R0-R6, R8-R12}
128     BX      LR
129
130     END

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```

1  ;*****
2  ; Program BCD.s
3  ; This program converts the hex value to a BCD number with three
4  ; digits (X.YZ) between 3.30 and 0.00 .
5  ;*****
6  ; EQU Directives
7  ;*****
8  ;LABEL      DIRECTIVE  VALUE      COMMENT
9              AREA      main, READONLY, CODE
10             THUMB
11             EXTERN     __ADC
12             EXTERN     CONVRT      ; Reference external subroutines
13             EXTERN     OutChar
14             EXPORT     __main      ; Make available
15
16 __main       PUSH      {LR}
17             BL         __ADC
18             POP        {LR}
19             PUSH      {LR}
20             BL         CONVRT
21             POP        {LR}
22             MOV        R0, R7
23 loop        BL         __ADC
24             CMP        R7, R0
25             ITE HS     ; R1 <- |R7-R0|
26             SUBHS     R1, R7, R0 ;
27             SUBLO     R1, R0, R7 ;
28             CMP        R1, #20    ; Treshold = 0.20 Volt
29             BLO       loop
30             CMP        R7, #10    ; Single digit or not
31             BHS       high
32             MOV        R5, #0xA   ; New line
33             BL         OutChar
34             MOV        R5, #0x30   ; print "0"
35             BL         OutChar
36             MOV        R5, #0x2E   ; print "."
37             BL         OutChar
38             MOV        R5, #0x30   ; print "0"
39             BL         OutChar
40             PUSH      {LR}
41             BL         CONVRT      ; print single digit
42             POP        {LR}
43             MOV        R0, R7
44             B         loop
45
46 high        MOV        R2, #100
47             MOV        R8, R7
48             UDIV      R7, R2
49             MOV        R5, #0xA   ; add new line
50             BL         OutChar
51             PUSH      {LR}
52             BL         CONVRT      ; print the quotient
53             POP        {LR}
54             MOV        R5, #0x2E   ; print "."
55             BL         OutChar
56             CMP        R7, #0
57             BNE       THREE
58             MOV        R7, R8
59             PUSH      {LR}
60             BL         CONVRT      ; print the quotient
61             POP        {LR}
62             MOV        R0, R8
63             B         loop
64
65 THREE      MUL        R7, R2
66             SUBS     R7, R8, R7
67             CMP        R7, #10
68             BHS       high2
69             MOV        R5, #0x30   ; print "0"
70             BL         OutChar
71 high2      PUSH      {LR}
72             BL         CONVRT      ; print the remainder
73             POP        {LR}
74             MOV        R0, R8
75             B         loop
76             END

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