```verilog
1    module instructionMem
2      ( input wire [31:0] adr,
3        output wire [31:0] inst);
4
5        reg[31:0] RAM[63:0];
6
7        initial begin
8          $readmemh("instructions.txt",RAM);
9        end
10       assign inst = RAM[adr[31:2]];//pc should be multiples of 4
11   endmodule
```