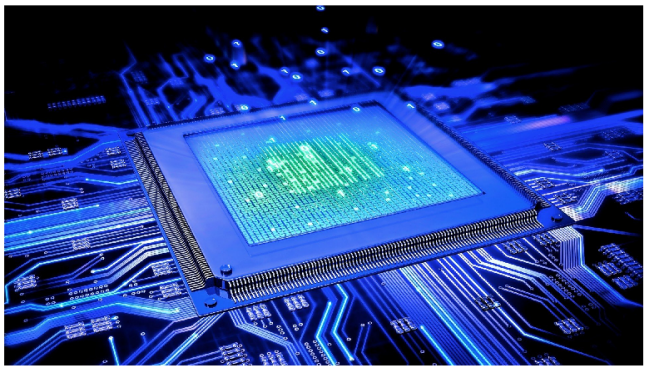
METU EE 446
Computer Architecture
Laboratory

Single Cycle
Processor Design



Laboratory Work 3 - Single Cycle Processor Design

Objectives

The purpose of this laboratory work is to practice the design of a 32-bit single cycle processor. You will construct a datapath and control unit of the single cycle processor like the one discussed in class. The designed processor will be able to execute all instructions given in the instruction set.

During this laboratory work, you will further improve your hard-wired controller design skills by designing the controller unit of the single-cycle processor. Finally, you will embed your design to the FPGA of DE0-Nano board and experiment it.

1 Preliminary Work

To fulfill the requirements of this laboratory work, the following tasks should be performed.

1.1 Reading Assignment

The laboratory manual where the regulations and some other useful information exist is available at the ODTUClass course page. Read that manual thoroughly. If you feel yourself unfamiliar with Verilog HDL programming and single cycle processor design, please refer to the corresponding lecture notes of EE445 course, which are available at the course page.

1.2 Single Cycle Processor Design with Verilog HDL (100% Credits)

For this laboratory work, you will design and implement a 32-bit single cycle processor which executes the instruction in only one clock cycle. First, you will design its datapath then you will implement corresponding controller.

Before starting this lab, you should be familiar with the single-cycle implementation of the processor described in lecture slides. The simplified single-cycle processor schematic, is shown in Figure 1. This version of a single-cycle processor can execute LDR instruction. Our model of the processor divides the machine into two major units: the control and the datapath. Each unit is constructed from various functional blocks. For example, the datapath contains the 32-bit ALU, the register file, the sign extension logic, two adders, and five multiplexers to choose appropriate operands.

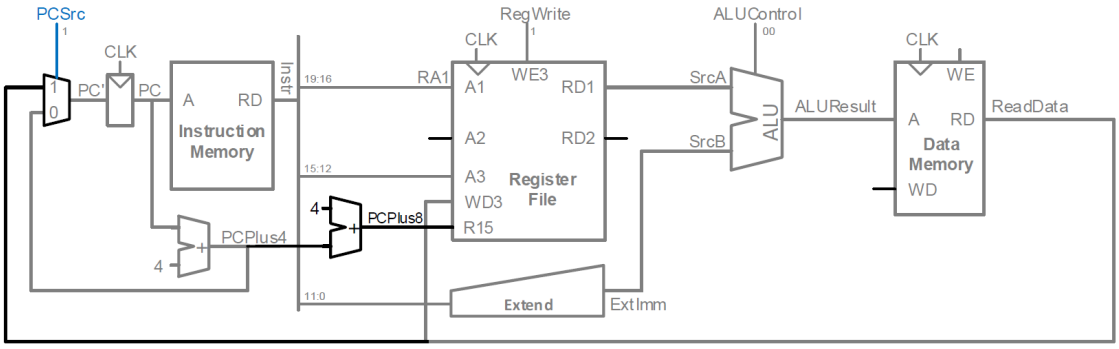


Figure 1: Datapath to execute LDR instruction

The processor you will design is not going to support all ARM instructions but only a restricted set that are listed in Figure 2. In order to design this processor you may extend the architecture given in Figure 1 as necessary.

You will need the following components to construct the CPU.

- Storage Elements
  - Instruction memory where instructions are stored
  - Data memory where data is stored
  - Register file
  - Program Counter
- Combinational Elements
  - ALU
  - Adders
  - Immediate Extender
  - Multiplexers

Mnemonic	Name		Operation
ADD	Addition	add rA, rB, rC	rA ← rB + rC
SUB	Subtraction	sub rA, rB, rC	rA ← rB - rC
AND	Logical And	and rA, rB, rC	rA ← rB & rC
ORR	Logical Or	orr rA, rB, rC	rA ← rB | rC
LSR	Logical shift right immediate	lsr rA, rB, rC	rA ← (rB >> imm)
LSL	Logical shift left immediate	lsl rA, rB, rC	rA ← (rB << imm)
CMP	Compare	cmp rA, rB, rC	set the flag if (rA - rB=0)
STR	Store	str rA, [rB, imm12]	Mem[rB + imm] ← rA
LDR	Load	ldr rA, [rB, imm12]	rA ← Mem[rB + imm]

Figure 2: Instruction Set

1.2.1 Datapath Design (40% Credits)

You are given an initial architecture in Figure 1. You will complete the datapath step by step so that the specifications given in Section 1.2 met. You can use your modules in your library which has been constructed in the scope of the first laboratory work. Additionally, you can add additional registers and multiplexers of any size if you need.

Considering the instruction set provided in Figure 2, perform the following design steps:

1. (30% Credits) For the instructions in the CPU that you are going to design, list all the steps that are needed for the execution of each instruction. While adding each instruction show all of the changes in the connections of the datapath.
2. (5% Credits) State the control signal inputs of your overall design. Draw a black box diagram of your architecture by indicating the inputs and outputs.
3. (5% Credits) Implement your datapath design in Schematic Editor of Quartus.

1.2.2 Controller Design (60% Credits)

In this step the controller for the single-cycle processor is to be designed. It will look like the controller which is in the lecture slides (Figure 3).

Perform the following steps:

1. (5% Credits) Draw the controller unit as a black box diagram and indicate its inputs and outputs.
2. (30% Credits) While adding each instruction show all of the changes in the control signals.
3. (5% Credits) Give the truth table for the main controller of the single-cycle processor.
4. (20% Credits) Implement your controller in Verilog HDL.

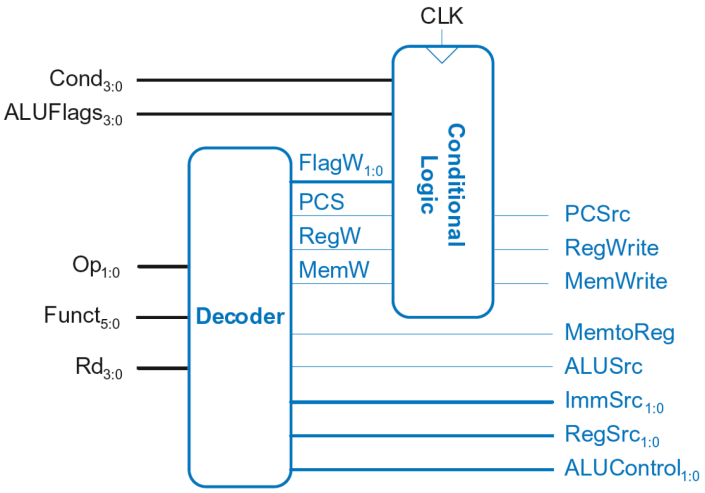


Figure 3: Controller

2 Experimental Work

2.1 Single Cycle Processor (100% Credits)

Load your processor designed in the Preliminary Work Part 1.2 to the DE0-Nano board. Test the correct functionality of your processor by storing all the implemented instructions in the instruction memory and verifying the correct execution of each instruction.

1. Prepare examples to be tested to verify the correct operation of your design. Ensure each instruction in the instruction set is covered.
2. Verify the operation of your design by performing the example operations and demonstrate it to your lab instructor.

!!! Important Notice !!! When using DEES in your experiments, **DO NOT CONNECT VCC pins of DE0-Nano Board** to DEES's VCC terminal. Also, to make a common voltage reference, CONNECT GND of DE0-Nano Board to DEES's GND terminal. Please make sure that you turn all supplies OFF while making any connection throughout laboratory work.

3 Parts List

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DE0-Nano Board
DEES
Oscilloscope
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