MIDDLE EAST TECHNICAL UNIVERSITY
ELECTRICAL AND ELECTRONICS ENGINEERING PROGRAM

EE445 (3-0)3 **COMPUTER ARCHITECTURE I** **2018-19 Fall**

Instructors:		**Office**	**Phone**	**e-mail**
Cüneyt F. BAZLAMAÇCI	(Sec.1)	A-408	210 2324	cuneytb@metu.edu.tr
Gözde B. AKAR	(Sec.2)	D-121/1	210 2341	bozdagi@metu.edu.tr

Course Schedule: Sec.1: Tuesday 11:40-12:30 and Thursday 10:40-12:30, D-131
Sec.2: Tuesday 14:40-15:30 and Thursday 13:40-15:30, D-131

Teaching Assistants:	**Office**	**Phone**	**e-mail**
Doğa Hakyemez	ARC-201	210 6096	dogahakyemez@gmail.com
Selin Böncü	A-404	210 4509	boncu@metu.edu.tr

Recommended Text Books:

Mano & Kime, "Logic and Computer Design Fundamentals", 4th Ed., Prentice Hall, 2008.
Mano "Logic Design", 4th Ed., Prentice Hall, 2008.
Mano, "Computer System Architecture", 2nd Ed., Prentice Hall, 1982
Harris & Harris, "Digital Design and Computer Architecture. ARM Edition", 1st Ed., Kaufmann, 2015.
Patterson & Hennessy, "Computer Organization and Design" (4th/5th Ed.), Kaufmann, 2014
Stallings, "Computer Organization & Architecture" (7th Ed. or later), Pearson, 2006.

Course Content: RTL. Algorithmic state machines. CPU organization. Arithmetic logic unit. Process control architectures. Instruction modalities. Microprogramming. Single cycle, multi cycle CPU architectures. Prerequisite: EE-348.

Course Objectives: Computers are integrated to our daily life and jobs. As a first step in becoming a computer designer or in writing better software, understanding the hardware layers together with software interface of a computer is critical. In this course, we will first review digital design fundamentals and introduce RTL, ASM, HDL concepts. Then we will study the basics of computer system organization, arithmetic processor design, performance and energy issues, and instruction set architectures. We will study macro-coding concepts, hardware and micro-programmed control for single- and multi-cycle datapath designs.

EE-446 Computer Architecture II will follow to study more advanced computer architecture concepts such as pipelining, memory and I/O organization, multiprocessors, etc.

Tentative Course Outline:

Week #	Topic		
1	Introduction. RTL		
2	ASM		
3	ASM (cont.)	Quiz1	
4	HDL		
5	Basic Comp Architecture	Quiz2	HW1 out
6	Basic Comp Architecture (cont.)		HW1 due
7	Arithmetic Processor Design	Quiz3	
8	Arithmetic Processor Design (cont.)		
9	ARM Instruction Set Architecture	MT	HW2 out
10	Microarchitecture		HW2 due
11	Microarchitecture	Quiz4	
12	Single cycle control and datapath		
13	Single cycle control and datapath (cont.)	Quiz5	HW3 out
14	Multicycle control and datapath(cont.)		HW3 due

Grading:			
	Midterm exam	: 30%	Date/time/place to be determined later
	Final exam	: 35%	Date/time/place to be determined later
	H.W. + Attendance	: 15%	Late submissions will be penalized 20% per week day
	Quiz	: 20%	Approx. every two weeks in class starting at week 3

EE445 course will be managed via odtuclass so pls. follow it.