Debugging and Profiling

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Introduction



- Parallel Nsight is a development environment for CUDA and graphics applications running on NVIDIA GPUs. It consists of:
 - CUDA Debugger
 - Graphics Debugger
 - Analysis and Profiling Tools



Introduction



- Supports Visual Studio.
- Eclipse version also available
- Also supports applications that use Direct3D 12 API
- Documentation available online:

http://docs.nvidia.com/gameworks/index.html#develope rtools/desktop/nvidia_nsight.htm



CUDA Debugger

- The CUDA Debugger helps you debug your CUDA applications.
 - You can set breakpoints in CUDA source code
 - inspect memory
 - view the values of local variables
 - perform memory checks
- You can use the CUDA Debugger with applications built with the CUDA Runtime (CUDART) API or with the CUDA Driver API.



Graphics Debugger

- The Graphics Debugger allows you to debug frame by each draw call. You can
 - debug vertex shaders
 - debug pixel shaders
 - view pipeline states



Analysis and Profiling Tools

- The Analysis tools help you to understand how workloads are distributed across your application.
- You can see -along a visual timeline-
 - API calls (CUDA C, OpenCL, DirectX, Microsoft DirectCompute, OpenGL, and Cg)
 - memory copies
 - kernel executions
 - CPU core and thread events
 - Custom user events
- You can gather and analyze kernel-level performance information



Target and Host Setup

Parallel Nsight allows you to debug your applications in two different ways:

- Local debugging, in which the host and target are on the same machine.
- Remote debugging, in which the host and target are on two different machines



Target and Host Setup

- Remote debugging:
 - The **host** machine will run Visual Studio to build your project, as well as to launch debugging sessions.
 - A separate computer is configured as the target machine. The target will
 - run the Parallel Nsight Monitor. The monitor detects incoming requests from the host to execute an application on the target machine.
 - run the application to be debugged or analyzed. Parallel Nsight software manages the synchronization of files between the host and target machines.



Local vs. Remote Debugging

- V2.2 onwards: Local CUDA debugging on a single GPU system.
 Note: Local debugging might adversely impact the performance of your application when debugging certain types of applications (such as most graphics applications).
- In remote debugging, Visual Studio environment will continue to run on the host machine, even if the target machine has to be rebooted because of an application crash.

 Some components of Parallel Nsight, such as shader debugging, will not work at all with a local debugging configuration.



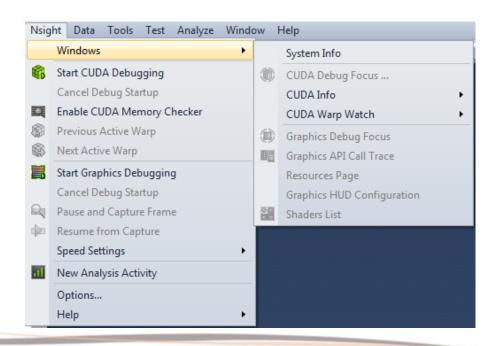
Target Setup

- The target computer does not need to be running Visual Studio.
- You need to install the Parallel Nsight Monitor on the target computer.
- See the guide for monitor setup.



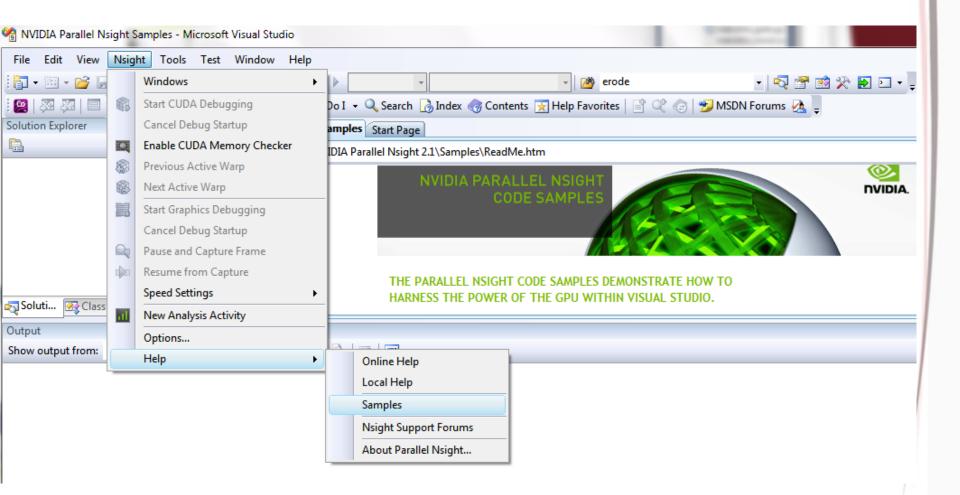
Host Setup

- Host is the computer that is running Visual Studio, where your application is being built and debugged.
- After you install Parallel Nsight on your computer, you will see a new menu called Nsight on your Visual Studio taskbar.
- See the documentation for installation.



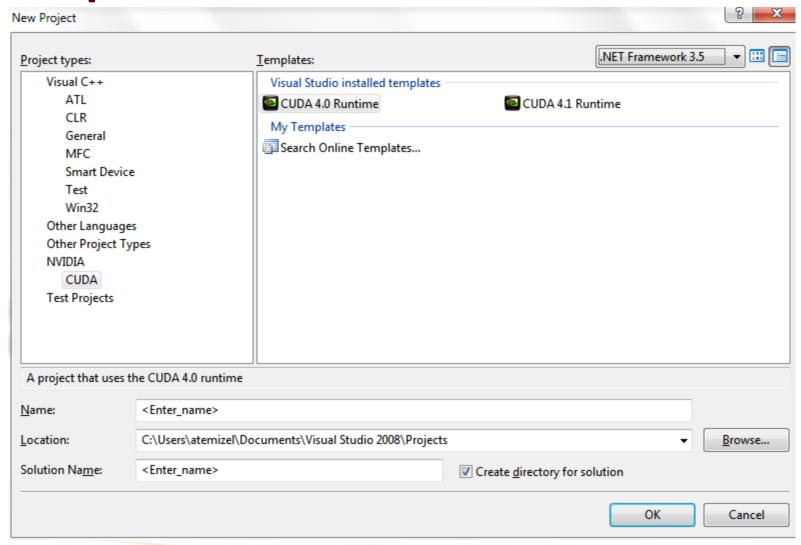


Samples





Templates

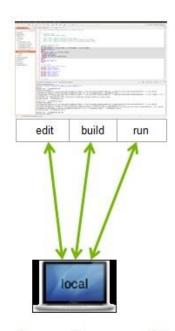




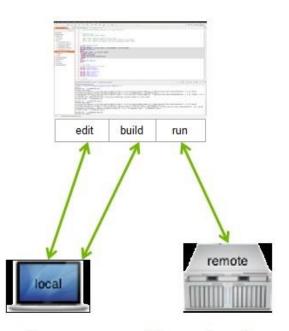
NVIDIA Nsight Eclipse Edition is a full-featured, integrated development environment that lets you develop CUDA applications for either your local (x86) system or a remote (x86 or ARM) target.

ARM target is typically a Jetson board

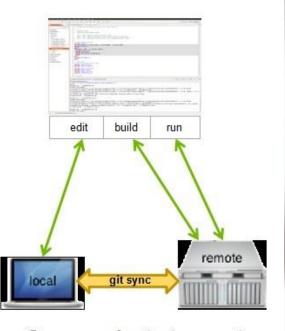




Create and run native builds on host

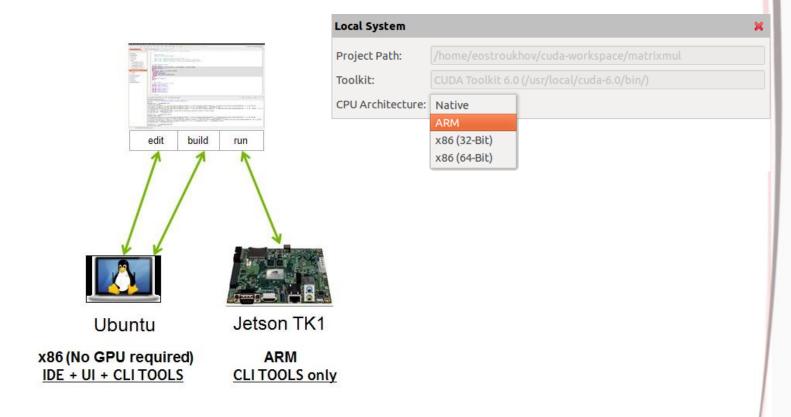


Cross compile on host and run on target



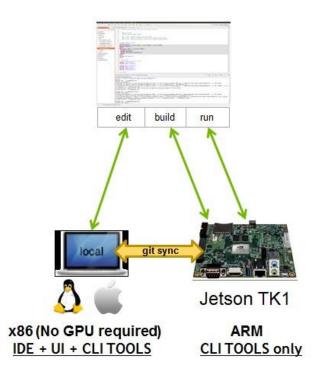
Sync projects to create remote builds on targets





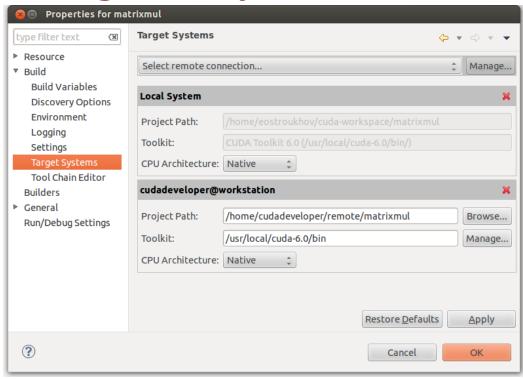
In the **cross compilation mode** the project resides on the host system and the cross compilation is also done on the host system. The cross compilation mode is only supported on an Ubuntu x86 host system.





In the **remote synchronized project mode** the project resides on the host system and gets synchronized with the remote target system. The compilation gets done natively on the target system. The remote synchronized project mode is supported on Mac OSX, Linux x86 and Linux POWER systems.





To create native remote build using remote synchronized project mode click on Manage... button to add a remote system, then select the project path, toolkit and the CPU architecture of the target system:

To synchronize projects between the host and target system, install and configure git on both the local and remote systems:

git config --global user.name <anyname> git config --global user.email <anyemail>



Nsight Eclipse Edition supports two remote development modes. Neither of these remote development modes requires an NVIDIA GPU to be present in your host system:

- Cross-compiling for ARM on your x86 host system requires that all of the ARM libraries with which you will link your application be present on your host system.
- Synchronize-projects mode: your source code is synchronized between host and target systems and compiled and linked directly on the remote target, which has the advantage that all your libraries get resolved on the target system and need not be present on the host.



<u>Jetpack L4T</u> installs the same version of the CUDA toolkit for both the host and target systems.

Get your host system set up for cross-platform CUDA development: https://devblogs.nvidia.com/cuda-jetson-nvidia-nsight-eclipse-edition/

The following target architectures are supported for cross compilation.

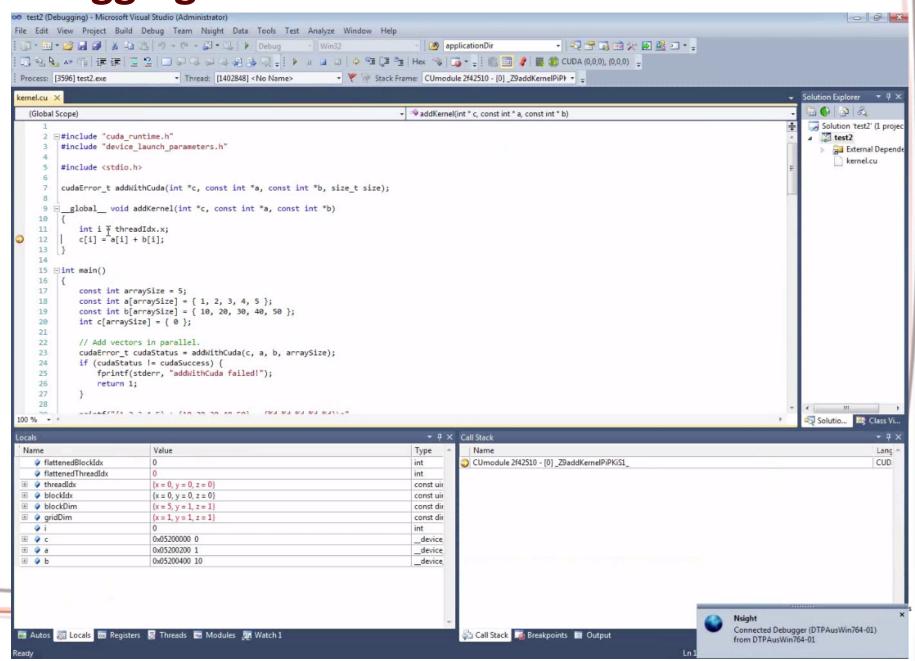
- x86_64: 64-bit x86 CPU architecture;
- armhf: 32-bit ARM CPU architecture, as found on Jetson TK1;
- aarch64: 64-bit ARM CPU architecture, found on Jetson TX1 and TX2 and certain Android systems;
- ppc64le: 64-bit little-endian IBM POWER8 architecture



For Jetson TK1 (NVIDIA Kepler GPU), choose 3.x GPU code and 3.x PTX code. For Jetson TX1 (NVIDIA Maxwell GPU), choose 5.x GPU code and 5.x PTX code. For Jetson TX2 (NVIDIA Pascal GPU), choose 6.x GPU code and 6.x PTX code



Debugging



Conditional Breakpoint

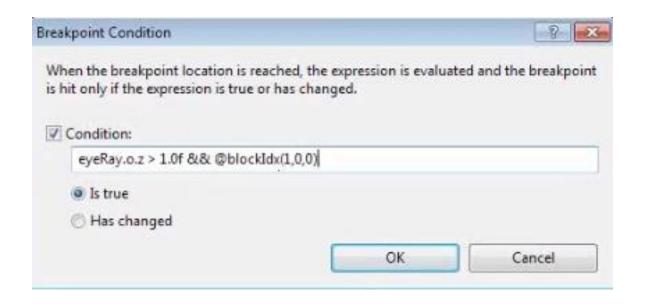
Right click on a breakpoint to set a condition.

```
1111
             uint x = blockIdx.x*blockDim.x + threadIdx.x;
   112
             uint v = blockIdx.v*blockDim.v + threadIdx.v;
             if ((x >= imageW) || (v >= imageH)) return;
   114
   115
            float u = (x / (float) imageW) *2.0f-1.0f;
   116
             float v = (v / (float) imageH) *2.0f-1.0f;
   117
             // calculate eye ray in world space
   118
   119
             Ray eyeRay;
   120
             eyeRay.o = make float3(mul(c invViewMatrix, make float4(0.0f, 0.0f, 0.0f, 1.0f)));
   121
             eyeRay.d = normalize(make float3(u, v, -2.0f));
             eyeRay.d = mul(c invViewMatrix, eyeRay.d);
   122
   123
   124
             // find intersection with box
   125
             float thear, tfar;
   126
             int hit = intersectBox(eyeRay, boxMin, boxMax, &tnear, &tfar);
   127
             if (!hit) return:
   128
             if (thear < 0.0f) thear - 0.0f.
                                      Breakpoint Condition
   129
   130
             // march along ray fro
                                       When the breakpoint location is reached, the expression is evaluated and the breakpoint
   131
             float4 sum = make flo
                                       is hit only if the expression is true or has changed.
             float t = tnear:
   133
             float3 pos = eyeRay.o
                                       Condition:
             float3 step = eyeRay.
   134
   135
                                           eyeRay.o.z > 1.0f
                                          Is true
                                          Has changed
RO = 0x00000001 R1 = 0x00fffa20 R2 =
                                                                               OK
                                                                                             Cancel
R5 = 0x03fffadc R6 = 0xbb45c9f8 R7 =
R10 = 0x000000000 R11 = 0x000000000 R12
```



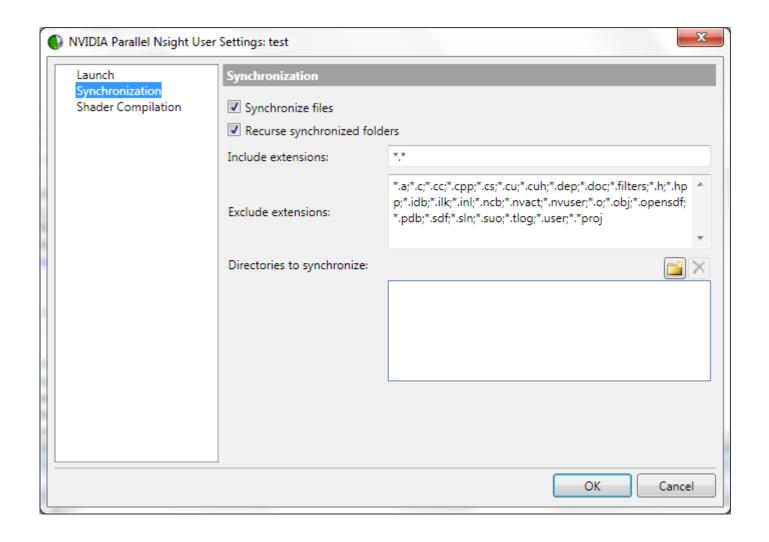
Conditional Breakpoint

 You can select the block as well. In this example, it will only hit the breakpoint if the block id is (1,0,0)



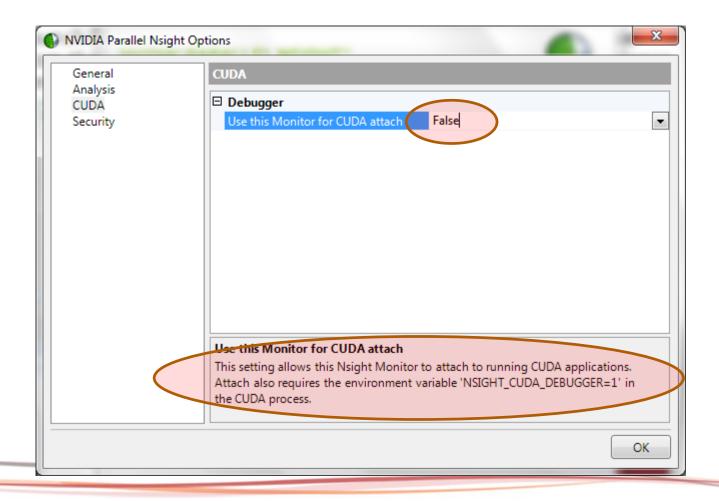


Remote Debugging-Synchronization





 Launch Parallel Nsight Monitor and set the following option to true from the options. This is set to false by default to prevent performance penalty when attaching to a process is not required.



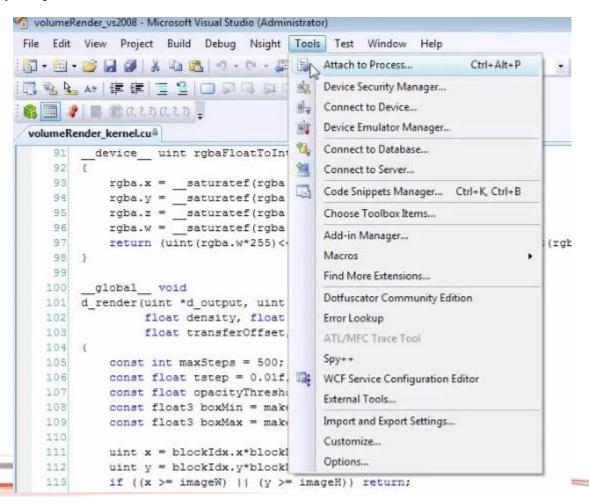


Set the environment variable and launch the process.
 Here we run an SDK sample called volumeRender

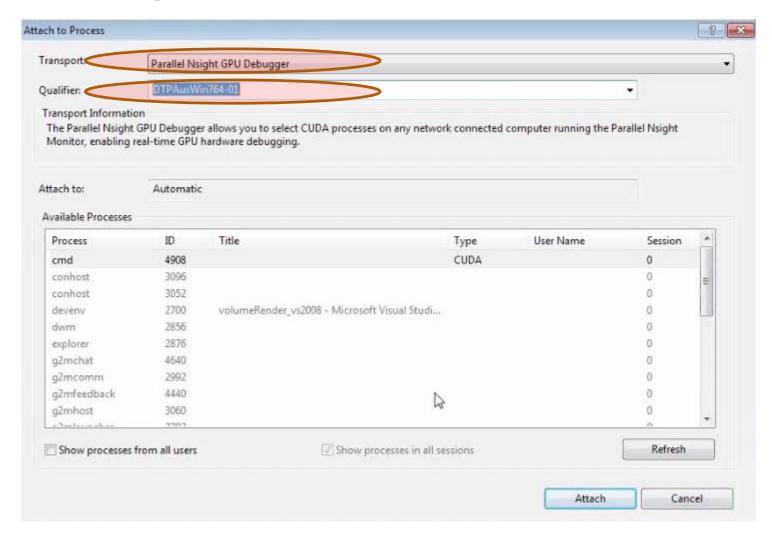
```
Administrator: Visual Studio Command Prompt (2010)
C:\SDKs\Compute\C\bin\win32\Debug)cmd.exe /c volumeRender.exe
[volumeRender.exel starting...
volumeRender.exe Starting...
Read '../../src/volumeRender/data/Bucky.raw', 32768 bytes
Press '+' and '-' to change density (0.01 increments)
       'l' and 'l' to change brightness
';' and ''' to modify transfer function offset
'.' and ',' to modify transfer function scale
C:\SDKs\Compute\C\bin\vin32\Debug>launch volumeRerNer.exe
C:\SDKs\Compute\C\bin\win32\Debag>SET NSIGHT_CUDA_DEBUGGER=1
C:\SDKs\Compute\C\bin\vin32\Deb@2cmd.exe /c volumeRender.exe
[volumeRender.exe] starting...
volumeRender.exe Starting...
Read '../../src/volumeRender/data/Bucky.raw', 32768 bytes
Press '+' and '-' to change density (0.01 increments)
       'l' and 'l' to change brightness
';' and ''' to modify transfer function offset
'.' and ',' to modify transfer function scale
 :\SDKs\Compute\C\bin\win32\Debug\
```



- Nsight Monitor will watch the processes that is running on the machine.
- Open the project source code in Visual Studio









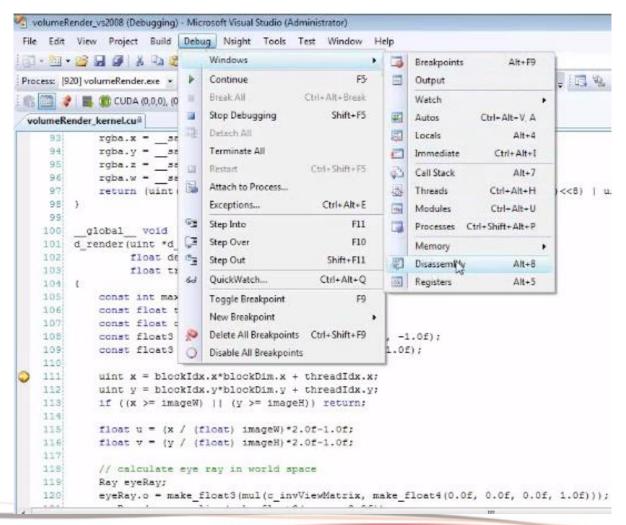
Assembly Debugging

- The assembly on a GPU is different from that of a CPU
- PTX is a machine-independent assembly language
- PTX is compiled down to SASS
- SASS is the code executed on a particular GPU family
- Most CUDA runtime applications use PTX, since this enables them to run on GPUs released after the original application



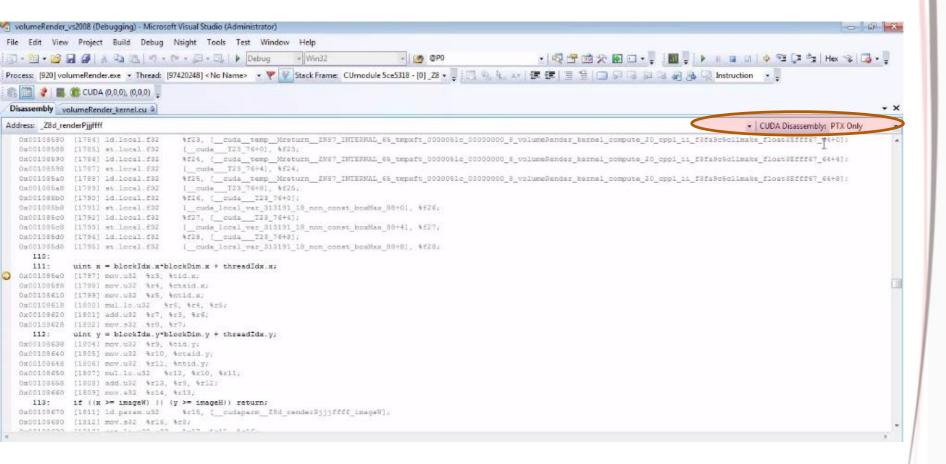
PTX/SASS Debugging

Set a breakpoint and start debugging



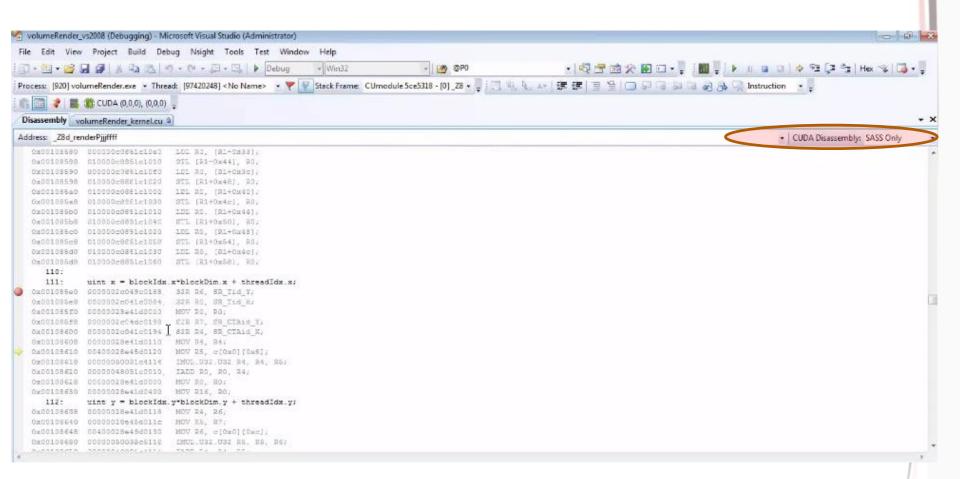


PTX Debugging





SASS Debugging





PTX and SASS

```
111: uint x = blockIdx.x*blockDim.x + threadIdx.x;
0x001085e0 [1797] mov.u32 %r3, %rid.u;
0x001085e0
                    0000002c049c0188 S2R R6, SR_Tid_Y;
0x001085e8
                    0000002q041c0084 S2R R0, SR_Tid_X;
0x001085f0
                     00000028e41d0000 MOV RO. RO.
0x001085f8 [1798] mov.u32 %r4, %ctaid.x;
                    0000002c04dc0198 S2R R7, SR CTAid Y:
0x001085f8
                    0x00108600
                    00000028e41d0110 MOV R4, R4;
0x00108608
0x00108610 [1799] mov.u32 %rf. %stid.x:
                    00400028e45d0120 MOV R5, c(0x0)[0x8];
0x00108610
0x00108618 [1800] mul.lo.u32 %r6, %r4, %r5;
0x00108618
                     00000050031c4114
                                     IMUL U32 U32 R4, R4, R5;
0x00108620 [1801] add.u32 %r7, %r3, %r6;
                     00000048031e0010
                                      IADD RO, RO, R4;
0x00108620
0x00108628 [1802] mov.s32 %r8, %r7;
                    000000028e41d00000 MOV RO, RO;
0x00108628
0x00108630
                   000000028e41d0400
                                    MOV R16, RO-
```



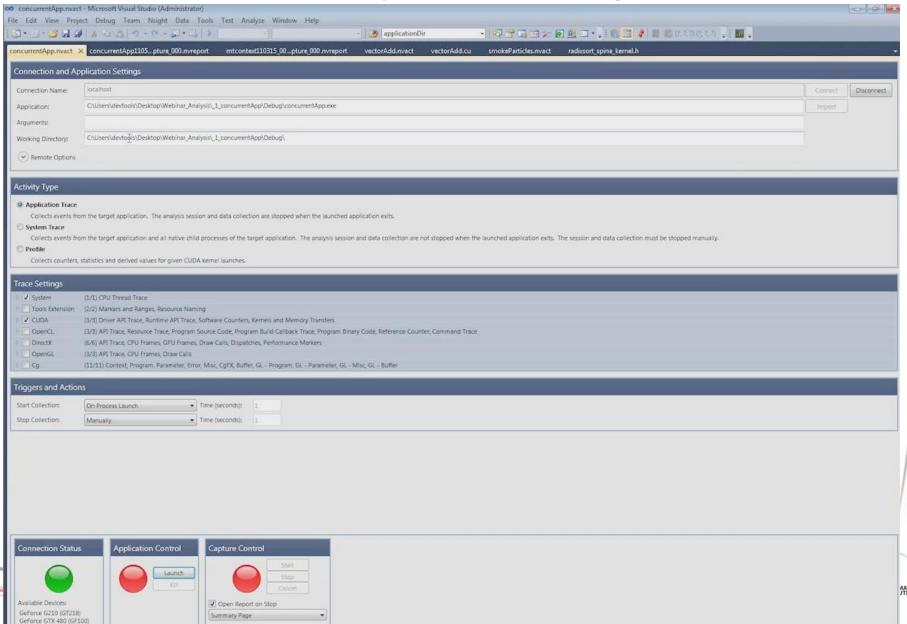
Performance Analysis-Profiling

We'll run concurrentApp.exe example.

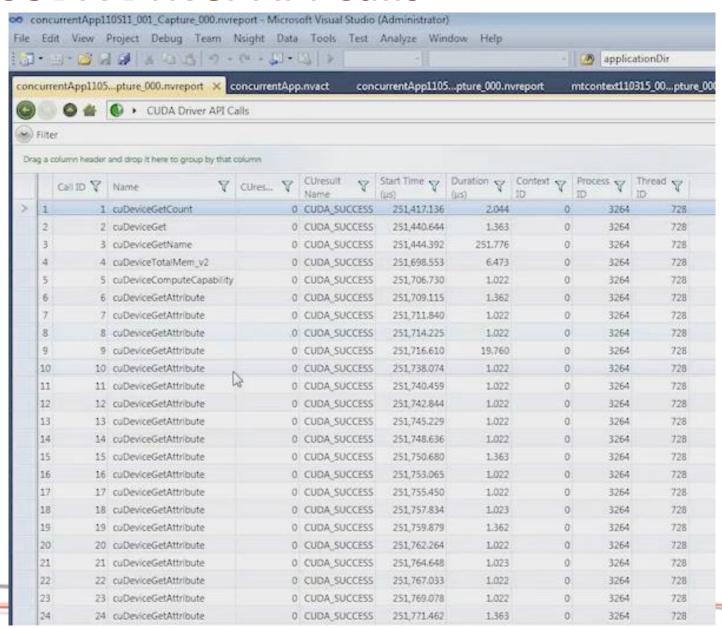
 The example has 4 kernels setup in 4 different streams so they can run concurrently.



Performance Analysis-Profiling

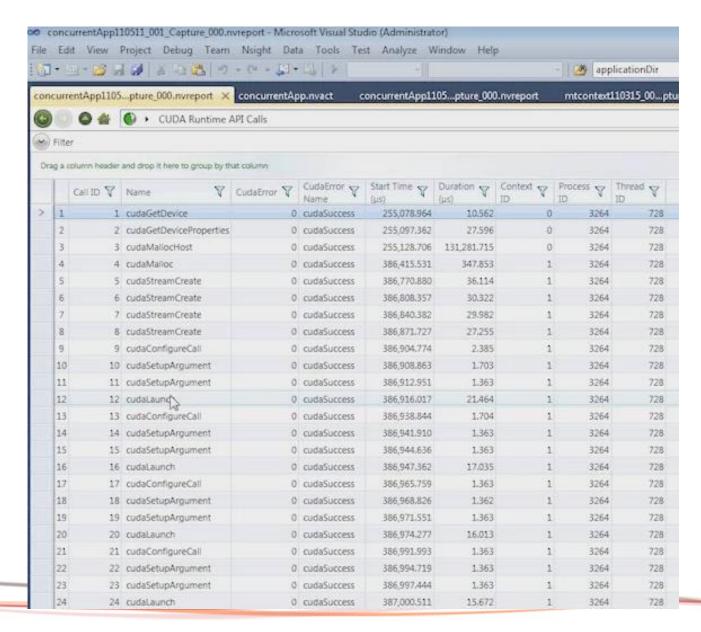


CUDA Driver API Calls



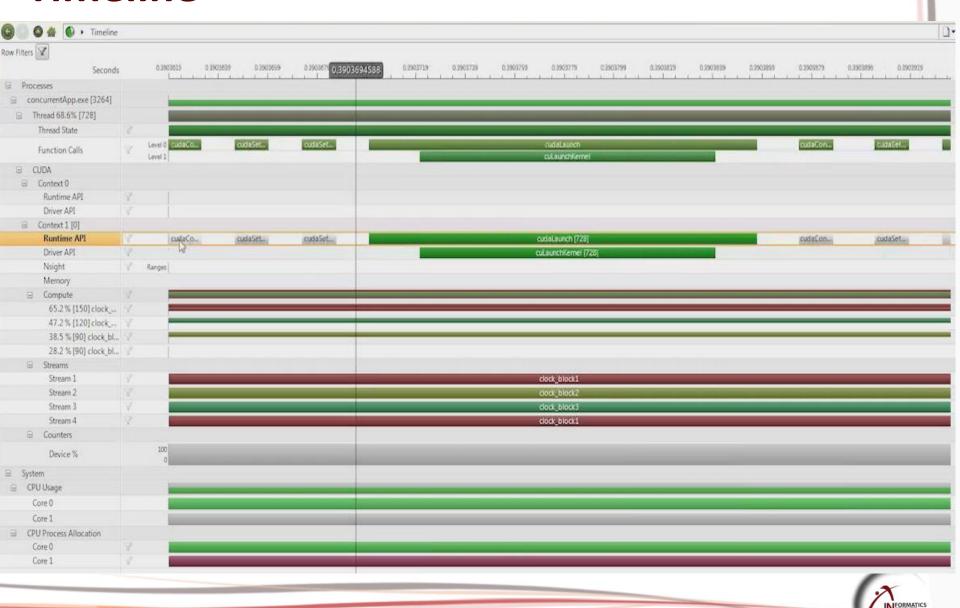


CUDA Runtime API Calls

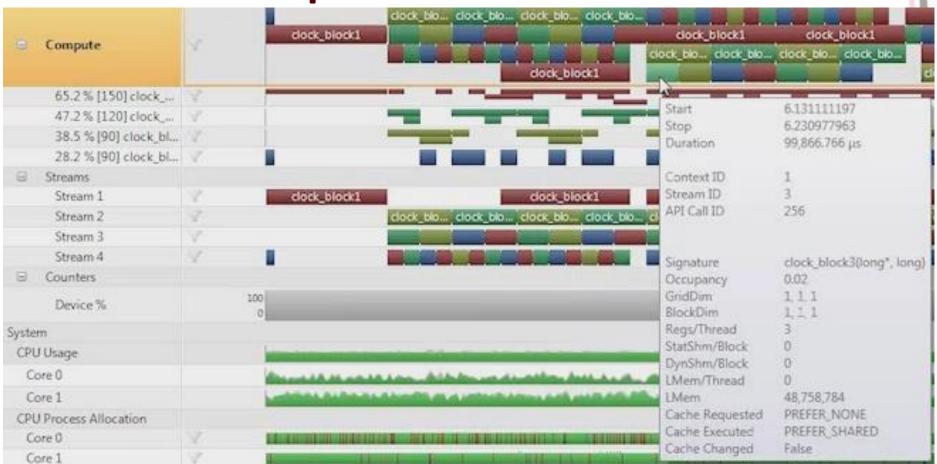




Timeline



Timeline- Compute Row



Older version (sequential execution)





Concurrent/Serialized Execution

Concurrent Trace Modes

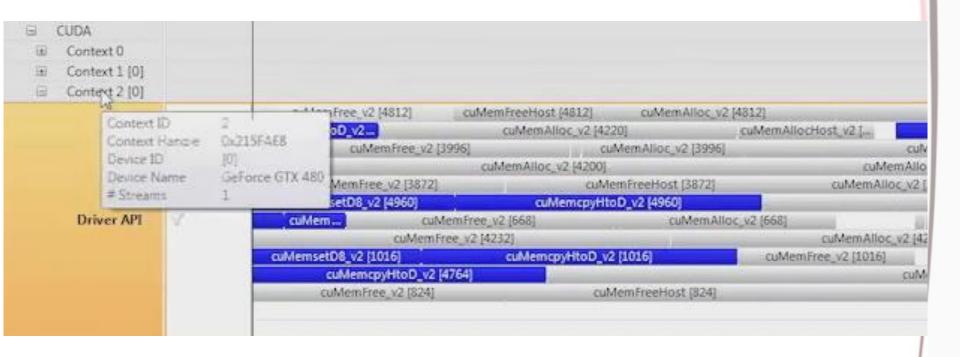
Trace Mode is configurable from the Nsight Options Menu

- Concurrent:
 - GPU overhead scales with number of warps launched
 - Additional GPU overhead introduced to cuCtxSynchronize()
 - Supported on Fermi cards only*
- Serialized:
 - Constant overhead per kernel launch
 - No additional GPU overhead





Parallel API calls





Profiling

December Capathatian

Activity Type Application Trace Collects events from the target application. The analysis session and data collection are stopped when the launched application exits. System Trace Collects events from the target application and all native child processes of the target application. The analysis session and data collection are not stopped when the launched application exits Profile Collects counters, statistics and derived values for given CUDA kernel launches. Experiment Settings Kernel Selection Kernels to Profile: Kernel Capture Limit Kernels: 1 Profile Options Print Progress Output to Console Non-Overlapping Input/Output Buffers **Experiment Configuration** Experiments to Run: Custom Presets ~ Experiment Tesla Fermi **CUDA Experiments** ^ Raw Counters - Fermi Architecture 1 Raw Counters - Tesla Architecture Achieved Occupancy Raw Counters - Fermi Architecture 3 Instruction Statistics Achieved Occupancy Achieved FLOPS Instruction Statistics Issue Efficiency

Parameters: Achieved Occupancy

 The multiprocessor occupancy is the ratio of active warps to the maximum number of warps supported on a multiprocessor of the GPU.

• The theoretical occupancy is the maximum occupancy given the execution configuration.

- Captures the achieved occupancy, which is the number of active warps per clock cycle divided by maximum warps per multiprocessor.
- Higher occupancy does not always equate to higher performance there
 is a point above which additional occupancy does not improve
 performance. However, low occupancy always interferes with the ability
 to hide memory latency, resulting in performance degradation.



Parameters: Achieved Occupancy

- The achieved occupancy may be lower than the theoretical occupancy for the following reasons:
 - The total number of blocks in the execution configuration is insufficient to saturate the device.
 - The thread blocks have high variance in execution times, often resulting in low number of active warps toward the end of the kernel execution.
 - The warps in thread blocks have high variance in execution times resulting in poor number of active warps throughout the kernel execution.



Parameters: Instruction Statistics

- Provides key metrics to evaluate the efficiency to execute the kernel's instruction on the target device, including instructions per clock cycle (IPC), instruction serialization, SM activity, as well as instructions per warp (IPW).
- If the executed IPC is low and the serialization high, the kernel likely has poor memory access patterns to shared/global memory.
- If the executed IPC is low and the serialization low, the kernel may execute a large number of high latency operations, such as double instructions, transcendentals, or memory operations.
- If the executed IPC is low and the achieved occupancy is low, the kernel launch fails to successfully hide latency.



```
62 [// Device Code

63 E_global__ void VecAdd_A(const float* A, const float* B, float* C)

64 {

65    int i = blockDim.x * blockIdx.x + threadIdx.x;

66    C[i] = A[i] + B[i];

67    }
```

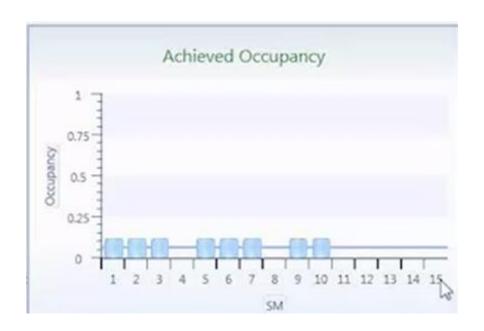


Occupancy Experiment- 8 blocks

Has 15 SMs

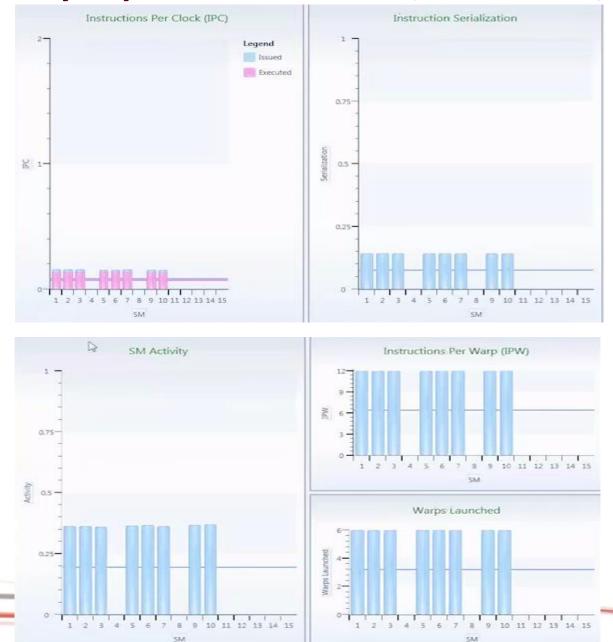
	nel: VecAdd_A I Dim: (8, 1, 1) 8		Block	Dim: {192, 1, 1}	Device: GeForce GTX 480 192 Compute Capability: 2.0	
	Variable	Achieved	Theoretical	Device Limit		
٨	Occupancy Per SM					
	Active Blocks		8	8	0 2 4 6	
	Active Warps	3.19	48	48	0 20 40	
	Active Threads		1536	1536	0 500 1000 1500	
	Occupancy	6.64 %	100.00 %	100.00 %	0 % 50 % 100 %	
^	Warps					
	Threads/Block		192	1024	n 500 1000	
	Warps/Block		6	32	ii 10 26 10	
	Block Limit		8	8	1 4 6 8	
^	Registers					
	Registers/Thread		4	63	20 40 60	
	Registers/Block		768	32768	0 10000 20000 30000	
	Block Limit		42	8		
A	Shared Memory					
	Shared Memory/Block		0	49152	II 20000 60000	
	Block Limit		8	8		

Occupancy Experiment- 8 blocks



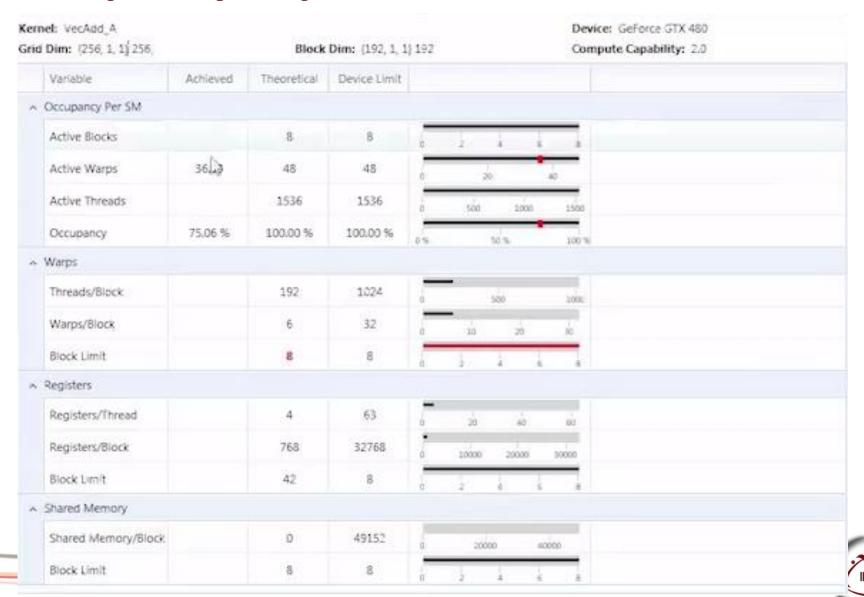


Occupancy Experiment- 8 blocks (Inst Stat. Tab)





Occupancy Experiment- 256 blocks



Occupancy Considerations

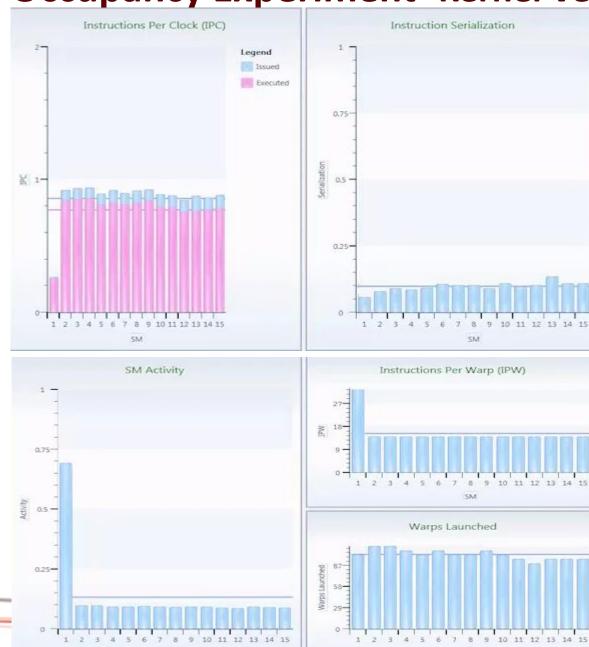
- Low occupancy is not always a bad thing.
 - If you are aiming for concurrent kernel operation then overall capacity could be distributed between different kernels.
 - Unused SMs would be used by other kernels.



```
// Device Code
   global_ void VecAdd_A(const float* A, const float* B, float* C)
64
        int i = blockDim.x * blockIdx.x + threadIdx.x;
65
        C[i] = A[i] + B[i];
66
67
68
69
   global void VecAdd B(const float* A, const float* B, float* C)
70
        int i = blockDim.x * blockIdx.x + threadIdx.x;
71
72
73
        if (blockIdx.x == 0)
74
            if (threadIdx.x == 0)
75
76
77
                for (int j = 0; j < blockDim.x; j++)
78
                    C[i+j] = A[i+j] + B[i+j];
79
80
81
82
        else
83
84
            C[i] = A[i] + B[i];
85
86
87 }
88
```



Occupancy Experiment- Kernel VecAdd_B

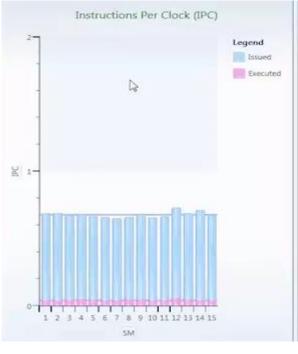


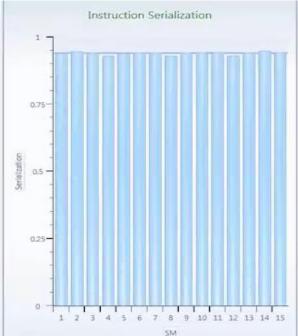


```
global__ void VecAdd_A(const float* A, const float* B, float* C)
{
   int i = blockDim.x * blockIdx.x + threadIdx.x;
   C[i] = A[i] + B[i];
}
```

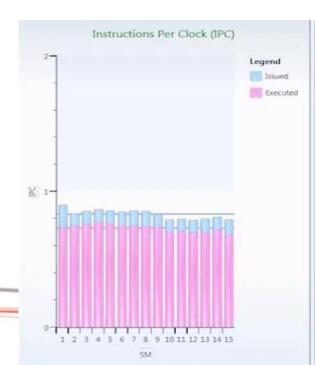
```
__global__ void VecAdd_C(const float* A, const float* B, float* C)
{
   int i = blockDim.x * threadIdx.x + blockIdx.x;
   C[i] = A[i] + B[i];
}
```

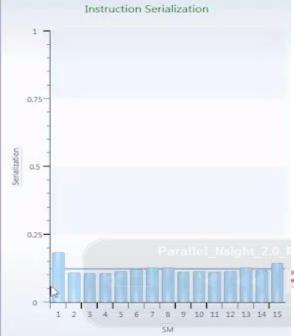






VecAdd_C





VecAdd_A



Instruction Serialization

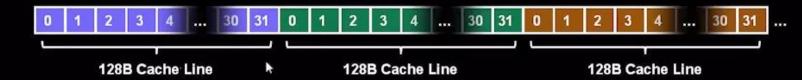
- "instruction replays" for warp's threads
- Occurs when threads in a warp execute/issue the same instruction after each other instead of in parallel
- Think of it as "replaying" the same instruction for different threads in a warp
- Some causes:
 - Shared memory bank conflicts
 - Constant memory access inefficiency



Serialization: Memory Access Pattern

VecAdd_A()

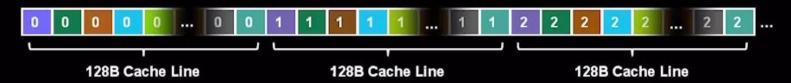
```
int i = blockDim.x * blockIdx.x + threadIdx.x;
C[i] = A[i] + B[i];
```



1 Instruction Executed 1 Instruction Issued **Each Memory Access:**

VecAdd_C()

```
int i = blockDim.x * threadIdx.x + blockIdx.x;
C[i] = A[i] + B[i];
```



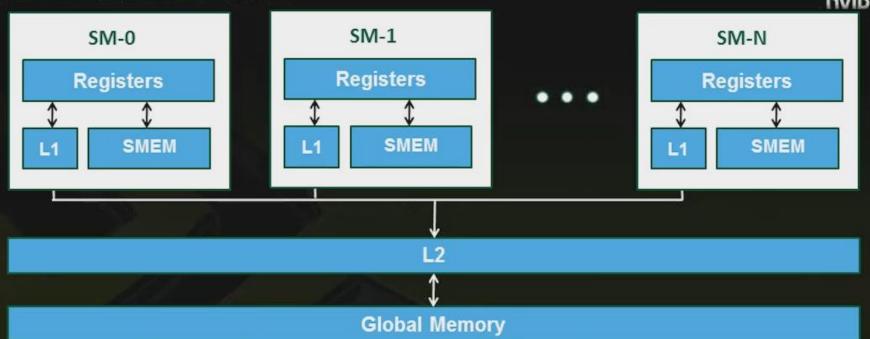
Each Memory Access:

1 Instruction Executed 32 Instructions Issued



Fermi Architecture





- SM Streaming multi-processors with multiple processing cores
 - Each SM contains 32 processing cores
 - Execute in a Single Instruction Multiple Thread (SIMT) fashion
 - Up to 16 SMs on a card for a maximum of 512 compute cores



Context Switch

- A grid is composed of blocks which are completely independent
- A block is composed of threads which can communicate within their own block
- 32 threads form a warp
 - Instructions are issued per warp
- If an operand is not ready the warp will stall
 - Context switch between warps when stalled
 - Context switch must be very fast



Context Switch

- Registers and shared memory are allocated for a block as long as that block is active
 - Once a block is active it will stay active until all threads in that block have completed
 - Context switching is very fast because registers and shared memory do not need to be saved and restored
- Goal: Have enough transactions in flight to saturate the memory bus
 - Latency can be hidden by having more transactions in flight
 - Increase active threads or Instruction Level Parallelism (ILP)
- Fermi can have up to 48 active warps per SM (1536 threads)

