Michael Canesche

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RESEARCH INTERESTS

Programming Languages, Compilers, Code Optimization, GPUs, Re-configurable Hardware, High Performance Computer, Artificial Intelligence, Machine Learning, Deep Learning.

SKILLS

Expertise: C, C++, Python, OpenMP, Cuda, Java, Verilog, (Intel/Vivado/LegUp) HLS.

EDUCATION

- **Universidade Federal de Minas Gerais (UFMG)** — **Minas Gerais, Brazil**
  PhD in Computer Science, Brazil — *April 2021 – February 2025 (Expected)*
  Advisor: Fernando Magno Quintão Pereira
  GPA: 8.98/10 (current)
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  MSc in Computer Science, Brazil — *March 2019 – February 2021*
  Advisor: Ricardo dos Santos Ferreira
  GPA: 9.04/10
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  BS in Computer Science, Brazil — *August 2016 – January 2019*
  GPA: 8.66/10, Graduated with Honors
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  BS in Chemistry, Brazil — *August 2010 – August 2014*
  GPA: 7.90/10

PROFESSIONAL EXPERIENCES

- **Universidade Federal de Minas Gerais (UFMG)** — **Minas Gerais, Brazil**
  Assistant teaching in Programming and Software Development II, DCC 204 — *March 2022 – July 2022*
  Total: 60 hours
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  Assistant teaching in Numerical Calculus, MAT 271 — *August 2015 – December 2017*
  Total: 1120 hours
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  Assistant teaching in Intermat, Math department — *March 2017 – July 2018*
  Total: 420 hours

RESEARCH PROJECTS

- **Automatic Benchmark Generation for Predictive Compilation**. Project Head: Fernando Pereira; Student: Michael Canesche, Cissa kind; 2022 - Present.
- **Obfuscation Code using Deep Learning**. Project Head: Fernando Pereira; Student: Michael Canesche, Thaís R. Damási, and Vinicíus s. Pacheco; 2022 - Present.
- **Side-Channel Elimination via Partial Control-Flow Linearization**. Project Head: Fernando Pereira; Student: Luigi Domenico, and Michael Canesche, ; 2021 - Present.
- **Code optimization in compiler design**. Project Head: Fernando Pereira; Student: Michael Canesche; 2021 - Present.
- **Bitwidth Minimization Problem in High-Level Synthesis**. Project Head: Fernando Pereira, Ricardo

Ferreira, and José A. Nacif; Students: Michael Canesche, and Maria Dalila Vieira; 2020 - 2021.
- **Placement and Routing on CGRAs and FPGAs**. Project Head: Ricardo Ferreira, and José A. Nacif; Students: Michael Canesche, Westerley Oliveira, Lucas Bragança, and Lucas Reis; 2019 - 2020.
- **Gene regulatory networks**. Project Head: Ricardo Ferreira; Students: Michael Canesche, Lucas Bragança, and Lucas Reis; 2020 - 2021.

Languages

- **English:** Fluent
- **Portuguese:** Native language

Evaluator

- CC Artifacts Evaluation 2022 - *link*

Prizes

- Top 10 best dissertations SBC at Brazil in 2022.
- Best Master's thesis at the Symposium on High Performance Computer Systems (WSCAD) in 2021.
- Best paper on XXI Symposium on High Performance Computing Systems (WSCAD) in 2020.
- Highest coefficient in the Computer Science course at UFV in 2019.

Main Published Papers

- Lucas Bragança, **Michael Canesche**, Jeronimo Penha, Josué Campos, José Augusto M Nacif, Ricardo S Ferreira. Fast flow cloud: A stream dataflow framework for cloud FPGA accelerator overlays at runtime, Concurrency and Computation: Practice and Experience (CCPE), 2022.
- Westerley C Oliveira, **Michael Canesche**, Lucas Reis, José Augusto M Nacif, Ricardo S Ferreira. Heterogeneous reconfigurable architectures for machine learning dataflows, Concurrency and Computation: Practice and Experience (CCPE), 2022.
- **Michael Canesche**, Ricardo Ferreira, José A. Nacif, Fernando M. Q. Pereira. A Polynomial Time Exact Solution to the Bit-Aware Register Binding Problem, ACM SIGPLAN 2022 International Conference on Compiler Construction (CC).
- **Michael Canesche**, Westerley Carvalho, Lucas Reis, Matheus Oliveira, Salles Magalhães, Peter Jamieson, Jaugusto M Nacif, Ricardo Ferreira. You Only Traverse Twice: A YOTT Placement, Routing, and Timing Approach for CGRAs, 2021 ACM Transactions on Embedded Computing Systems (TECS).
- **Michael Canesche**, Lucas Bragança, Omar P. V. Neto, José Augusto Nacif, Ricardo Ferreira. Google Colab CAD4U: Hands-on Cloud Laboratories for Digital Design, 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 1-5.
- Maria Vieira, **Michael Canesche**, Lucas Bragança, Josué Campos, Mateus Silva, Ricardo Ferreira, Jose A Nacif. RESHAPE: A Run-time Dataflow Hardware-based Mapping for CGRA Overlays, 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 1-5.
- **Michael Canesche**, Marcelo Menezes, Westerley Carvalho, Frank Torres, Peter Jamieson, José Augusto Nacif, Ricardo Ferreira. TRAVERSAL: A Fast and Adaptive Graph-based Placement and Routing for CGRAs, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). November, 2020.
- Fernando Passe, **Michael Canesche**, Omar Paranaiba Vilela Neto, Jose A Nacif, Ricardo Ferreira. Mind the Gap: Bridging Verilog and Computer Architecture, 2020 IEEE International Symposium on Circuits and Systems (ISCAS). December, 2020.
- Westerley Carvalho, **Michael Canesche**, Lucas Reis, Frank Torres, Lucas Silva, Peter Jamieson, José A. Nacif, Ricardo Ferreira. A Design Exploration of Scalable Mesh-based Fully Pipelined Accelerators, 2020

The International Conference on Field-Programmable Technology (FPT). November, 2020.

- Westerley Oliveira, **Michael Canesche**, Lucas Reis, José Nacif, Ricardo Ferreira Design Exploration of Machine Learning Data-Flows onto Heterogeneous Reconfigurable Hardware, XXI Symposium on High Performance Computing Systems (WSCAD). October, 2020.
- Lucas Bragança, **Michael Canesche**, Ricardo Ferreira, José Augusto M Nacif HPCGRA-An Orthogonal Designed CGRA Generator for High Performance Spatial Accelerators, XXI Symposium on High Performance Computing Systems (WSCAD). October, 2020.
- Lucas Bragança, Ricardo Ferreira, **Michael Canesche**, Marcelo M Menezes, Maria D Vieira, Jeronimo Penha, Peter Jamieson, José Augusto M Nacif READY: A fine-grained multithreading overlay framework for modern CPU-FPGA dataflow applications, ACM Transactions on Embedded Computing Systems (TECS). October, 2019.
- Jeronimo Costa Penha, Lucas Bragança, Kristtopher Coelho, **Michael Canesche**, Jansen Silva, Giovanni Comarela, José Augusto M Nacif, Ricardo Ferreira A gpu/fpga-based k-means clustering using a parameterized code generator, Symposium on High Performance Computing Systems (WSCAD). October, 2018.