Michael Canesche

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RESEARCH INTERESTS

Compilers, Code Optimization, Re-configurable Hardware, High Performance Computer, Artificial Intelligence, Machine Learning, Deep Learning.

SKILLS

Expertise: C, C++, Python, OpenMP, Cuda, Java, Verilog, Intel HLS, Vivado HLS, and LegUp HLS.

EDUCATION

- **Universidade Federal de Minas Gerais (UFMG)** — **Minas Gerais, Brazil**
  PhD in Computer Science, Brazil — *April 2021 – February 2025 (Expected)*
  Advisor: Fernando Magno Quintão Pereira
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  MSc in Computer Science, Brazil — *March 2019 – February 2021*
  Advisor: Ricardo dos Santos Ferreira
  GPA: 9.04/10
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  BS in Computer Science, Brazil — *August 2016 – January 2019*
  GPA: 8.66/10, Graduated with Honors
- **Universidade Federal de Viçosa (UFV)** — **Minas Gerais, Brazil**
  BS in Chemistry, Brazil — *August 2010 – August 2014*
  GPA: 7.90/10

RESEARCH PROJECTS

- **Bitwidth Minimization Problem in High-Level Synthesis**. Head Project: Fernando Quintão, Ricardo Ferreira, and José A. Nacif; Students: Michael Canesche, and Maria Dalila Vieira; 2020 - actual.
- **Placement and Routing on CGRAs and FPGAs**. Head Project: Ricardo Ferreira, and José A. Nacif; Students: Michael Canesche, Westerley Oliveira, Lucas Bragança, and Lucas Reis; 2019 - actual.
- **Gene regulatory networks**. Head Project: Ricardo Ferreira; Students: Michael Canesche, Lucas Bragança, and Lucas Reis; 2020 - actual.

Languages

- **English:** Intermediary
- **Portuguese:** Native language

Prizes

- Best Master's Dissertation at the Symposium on High Performance Computer Systems (WSCAD) in 2021
- Best paper on XXI Symposium on High Performance Computing Systems (WSCAD) in 2020.
- Highest coefficient in the Computer Science course at UFV in 2019.

Papers

- Michael Canesche, Westerley Carvalho, Lucas Reis, Matheus Oliveira, Salles Magalhães, Peter Jamieson, Jaugusto M Nacif, Ricardo Ferreira. You Only Traverse Twice: A YOTT Placement, Routing, and Timing Approach for CGRAs, 2021 ACM Transactions on Embedded Computing Systems (TECS).
- Michael Canesche, Lucas Bragança, Omar P. V. Neto, José Augusto Nacif, Ricardo Ferreira. Google Colab CAD4U: Hands-on Cloud Laboratories for Digital Design, 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 1-5.
- Maria Vieira, Michael Canesche, Lucas Bragança, Josué Campos, Mateus Silva, Ricardo Ferreira, Jose A Nacif. RESHAPE: A Run-time Dataflow Hardware-based Mapping for CGRA Overlays, 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 1-5.
- Michael Canesche, Marcelo Menezes, Westerley Carvalho, Frank Torres, Peter Jamieson, José Augusto Nacif, Ricardo Ferreira. TRAVERSAL: A Fast and Adaptive Graph-based Placement and Routing for CGRAs, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD). November, 2020.
- Fernando Passe, Michael Canesche, Omar Paranaiba Vilela Neto, Jose A Nacif, Ricardo Ferreira. Mind the Gap: Bridging Verilog and Computer Architecture, 2020 IEEE International Symposium on Circuits and Systems (ISCAS). December, 2020.
- Westerley Carvalho, Michael Canesche, Lucas Reis, Frank Torres, Lucas Silva, Peter Jamieson, José A. Nacif, Ricardo Ferreira. A Design Exploration of Scalable Mesh-based Fully Pipelined Accelerators, 2020 The International Conference on Field-Programmable Technology (FPT). November, 2020.
- Westerley Oliveira, Michael Canesche, Lucas Reis, José Nacif, Ricardo Ferreira Design Exploration of Machine Learning Data-Flows onto Heterogeneous Reconfigurable Hardware, XXI Symposium on High Performance Computing Systems (WSCAD). October, 2020.
- Lucas Bragança Silva, Michael Canesche, Ricardo Ferreira, José Augusto M Nacif HPCGRA-An Orthogonal Designed CGRA Generator for High Performance Spatial Accelerators, XXI Symposium on High Performance Computing Systems (WSCAD). October, 2020.
- Fernando Passe, Lucas Bragança, Michael Canesche, Felippe Cathoud, José A Nacif, Ricardo Ferreira Plain: Ferramenta para Desenvolvimento de Aceleradores para Overlays em FPGA na Nuvem em Tempo de Execução, XXI Symposium on High Performance Computing Systems (WSCAD). October, 2020.
- Wallace Rosa, Hector Baranda, Michael Canesche, Marcelo Menezes, Lucas Bragança, Salles Magalhaes, José Augusto Nacif, Ricardo Ferreira Simulação de Redes Reguladoras de Genes com Lógica Booleana e Limiar em Plataformas Alto Desempenho, XX Symposium on High Performance Computing Systems (WSCAD). November, 2019.
- Lucas Bragança Da Silva, Ricardo Ferreira, Michael Canesche, Marcelo M Menezes, Maria D Vieira, Jeronimo Penha, Peter Jamieson, José Augusto M Nacif READY: A fine-grained multithreading overlay framework for modern CPU-FPGA dataflow applications, ACM Transactions on Embedded Computing Systems (TECS). October, 2019.
- Ricardo Ferreira, Michael Canesche, Kristtopher Coelho, Jose Nacif Minimum Switching Networks, VIII Brazilian Symposium on Computing Systems Engineering (SBESC). November, 2018.
- Jeronimo Costa Penha, Lucas Bragança, Kristtopher Coelho, Michael Canesche, Jansen Silva, Giovanni Comarela, José Augusto M Nacif, Ricardo Ferreira A gpu/fpga-based k-means clustering using a parameterized code generator, Symposium on High Performance Computing Systems (WSCAD). October, 2018.
- Michael Canesche, Vanessa Vasconcelos, Fernando Passe, Jeronimo Penha, Ricardo Ferreira Exemplos e aplicações utilizando a ferramenta ADD, Symposium on High Performance Computing Systems (WSCAD). October, 2018.
- Fernando Passe, Vanessa Vasconcelos, Michael Canesche, Ricardo Ferreira Perspectivas para o uso do Node-Red no Ensino de IoT, International Journal of Computer Architecture Education. December, 2017.