ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	4 (MAKE-UP)
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GROUP NO	:	

GROUP MEMBERS:

150210108 : Mustafa Emre Taflan

150200097 : Mustafa Can Çalışkan

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1 INTRODUCTION

During the experiment we had a chance to experience real life implementations on breadboard of latches and flip flops we learned in the lectures.

2 EXPERIMENT

2.1 PART 1

In this part, SR type latch without an enable input was implemented. As shown in Figure 1, SR-latch consists of two NOR gates which have connections with outputs and inputs called feedback mechanism. Two inputs of the SR-latch are S which means set to HIGH and R which means reset to LOW. Two outputs of the SR-latch are Q and Q neg. R and Q neg are connected with the first NOR gate as inputs. In addition to that, S and Q are connected to the second NOR gate as inputs. The outputs of the first and the second NOR gates Q and Q neg, respectively. As observed in Table 1, because of latch's feedback mechanism, second output is always the complemented version of the output Q. So, both inputs can't be 1 at the same time. When both of the outputs are zero, latch conserves its current state.

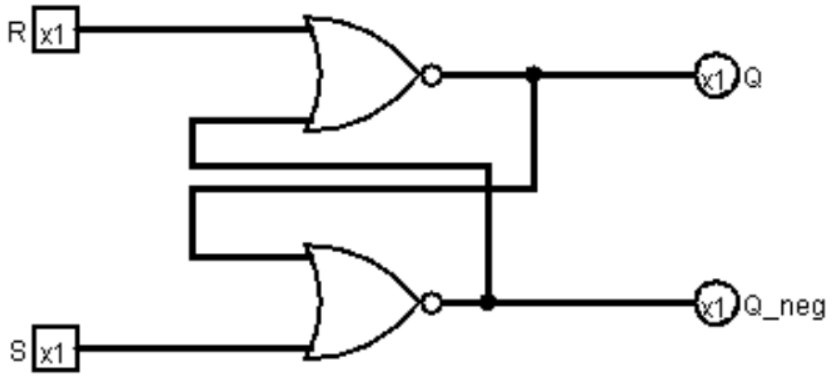

Figure 1: Circuit design of the SR-latch

Q(t)	S	R	Q(t+1)	Q(t+1)'
0	0	0	0	1
0	0	1	0	1
0	1	0	1	0
0	1	1	ϕ (Forbidden)	ϕ (Forbidden)
1	0	0	1	0
1	0	1	0	1
1	1	0	1	0
1	1	1	ϕ (Forbidden)	ϕ (Forbidden)

Table 1: SR Latch truth table without enable input

2.2 PART 2

In this part, SR latch module with an enable input was implemented. We were restricted to use only 2-input NAND gates. As shown in Figure 2, SR-latch with enable input has four NAND gates. The first NAND gate has inputs S and E which is enable input and the output of this gate is S neg. The second NAND gate has inputs R and E and the output of this gate is R neg. The third NAND gate has inputs S neg and Q neg and the output of this gate is Q. The last NAND gate has two inputs R neg, Q and the output of this gate is Q neg. As observed in Table 2, the enable input is used to activate and deactivate latches. When E is LOW, the other inputs are not cared and the SR latch conserves its previous state. When E is HIGH, SR latch works as expected.

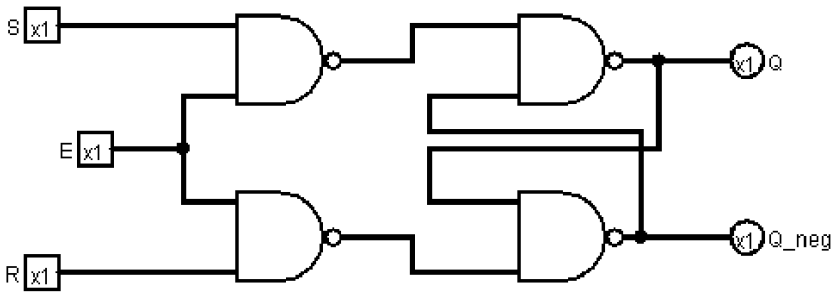

Figure 2: Circuit design of the SR Latch with an enable input

E	Q(t)	S	R	Q(t+1)	Q(t+1)'
0	0	ϕ	ϕ	0	1
0	1	ϕ	ϕ	1	0
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	1	0
1	0	1	1	ϕ (Forbidden)	ϕ (Forbidden)
1	1	0	0	1	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	ϕ (Forbidden)	ϕ (Forbidden)

Table 2: SR Latch truth table with enable input.

2.3 PART 3

Negative edge triggered D flip-flop was implemented using two type D latches and a hex inverter in part 3. As shown in Figure 3, the output of the first D-latch is connected as the input of the second D-latch. Clock signal is sent as inverted to the second D-latch to get falling edge triggered D flip-flop. Clock signal is sent using debounced pushbutton. When clock is HIGH, the first D-latch is enabled and output of the first one gets value from D input but the second D-latch is disabled so output preserves its previous value. When clock is equal to 0, which means negative edge, the first one is disabled so it cannot get new input, conserves the previous state but the second one is enabled. Output Q gets value from output of the first D-latch. Truth table of the negative edge D flip-flop can be shown in Table 3.

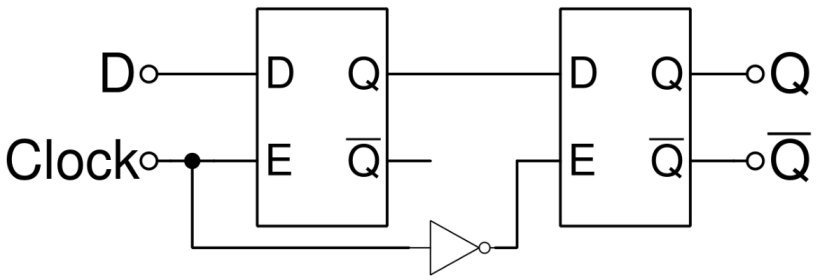

Figure 3: Circuit design of the D flip-flop

Clock	D	Q(t+1)	Q(t+1)'
↘	0	0	1
↘	1	1	0
↗	0	1	0
↗	1	1	0

Table 3: D flip flop truth table.

3 DISCUSSION

We used necessary gates and their inputs to implement the desired circuit memory elements.

4 CONCLUSION

We couldn't use the time efficiently because of the faults in gates and breadboards. We had to replace the gates with healthy ones. Also we did misconnections in some parts. As a result we were able to do only first 3 parts. But it was a beneficial experiment and we learned a lot.