Clocked Synchronous Sequential Circuits

In sequential circuits, output values depend on both the input values and the state of the circuit. Output = f(Input, State)

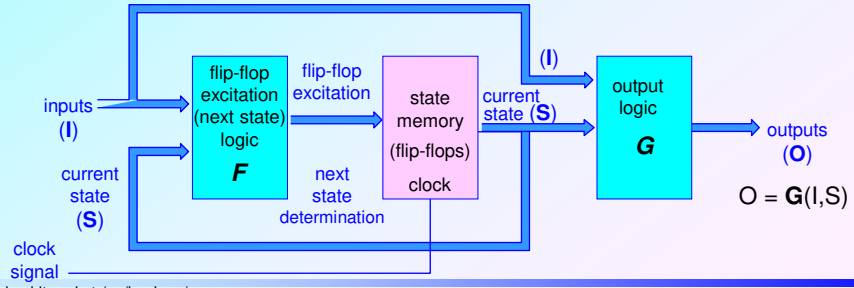
Clocked synchronous sequential circuits are designed based on the ***finite state machine*** model, where the current state is stored in memory elements (flip-flops).

All flip-flops are triggered with the same **clock signal** (synchronized). Therefore, the machine can change its state only during the active transition of the clock signal.

A sequential circuit can be designed as either a Mealy or Moore model.

a) Mealy Model *(George H. Mealy (1927-2010), computer scientist, USA)*

In this model, outputs (O) are determined by a function of current input values (I) and current state (S). O = **G**(I,S)



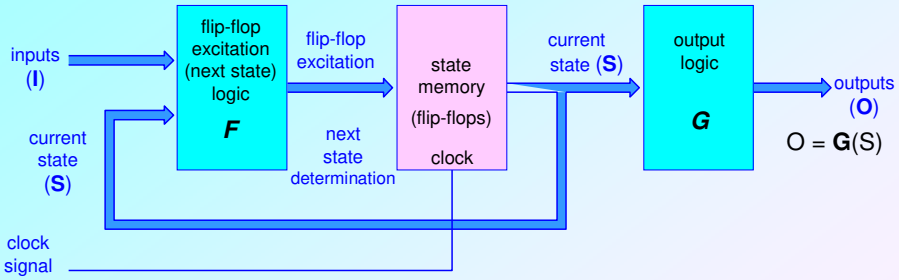
b) Moore Model

Edward Forrest Moore (1925-2003) Mathematician, computer scientist, USA

In this model, the output depends only on the current state.

Input values determine only the next state.

And the state determines the output. O = **G**(S)



Most sequential circuits can be designed using either one of these models (Mealy or Moore).

Next States in Mealy and Moore models: In both models, next state S^+ is determined by a function H, which is a combination of function F and characteristic equations of the flip-flops. S^+ = **H**(I,S)

Analysis of clocked synchronous sequential circuits

Before we start to design sequential circuits, we will see how to analyze a given sequential circuit.

Reminder: Implementation of a sequential circuit means implementation of the functions F (flip-flop excitation) and G (output). (See 8.1 and 8.2)

I: Input, S: Current State, S^+: Next state, O : Output

$S^+ = \mathbf{H}(I,S)$, Mealy: $O = \mathbf{G}(I,S)$ Moore: $O = \mathbf{G}(S)$

Analyzing a synchronous circuit means determining the behavior of the circuit (i.e., answering the question "What does the circuit do?"), which is given by the functions F and G .

The analysis of a synchronous circuit consists of five steps:

1. Determine the expressions of the function F (inputs of flip-flops).
2. Use F and characteristic functions of the flip-flops to find the expression of H.
3. Construct the state table that specifies the next state of the circuit for every possible combination of input and current state.
4. Determine the expressions of the output function G.
5. Determine the output values using G, and construct the state/output table.

(Optional) To see the behavior of the circuit better, draw the state diagram (also called a state graph), which shows all state transitions and outputs of the machine graphically.

Determination of next states (function H):

The **F** function of a clocked sequential circuit determines the input values of the flip-flops (flip-flop excitation).

These input values, along with the current state of the flip-flop, determine the next state of the flip-flop (i.e., the output of the flip-flop after the transition of the clock signal) (Slides 8.1 and 8.2).

$S^+ = \mathbf{H}(I,S)$

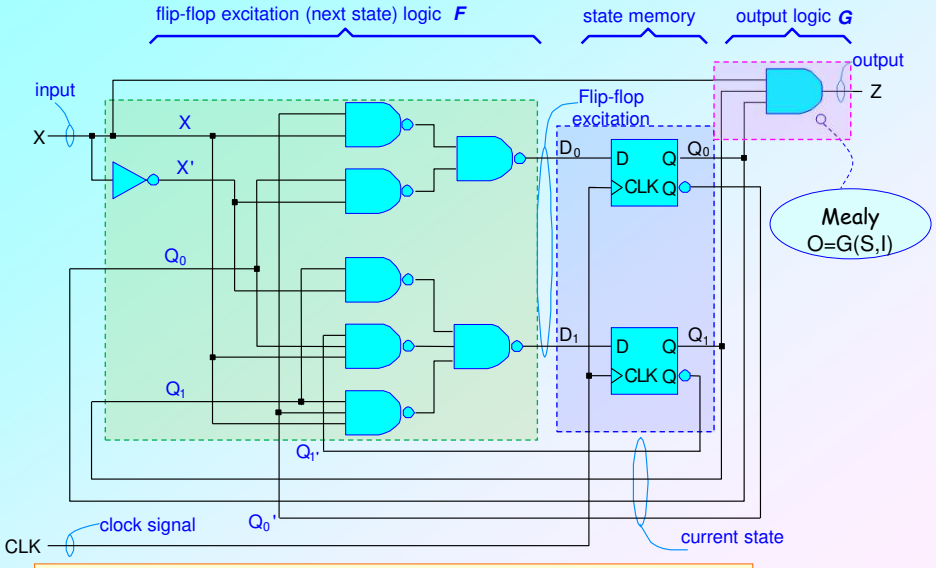
Function H is a combination of function F and characteristic equations of the flip-flops.

The functional behavior of a latch or flip-flop can be described by a **characteristic equation** that specifies the flip-flop's next state as a function of its inputs and current state.

Characteristic equations for the flip-flops:

S-R FF :	$Q(t+1) = S + \overline{R} \cdot Q(t)$	(SR = 0)
J-K FF :	$Q(t+1) = J \cdot \overline{Q(t)} + \overline{K} \cdot Q(t)$	
D FF :	$Q(t+1) = D$	
T FF :	$Q(t+1) = T \oplus Q(t)$	

Example: Analyze the given clocked synchronous circuit.



$S=\{Q_0(t),Q_1(t)\}$ $S^+=\{Q_0(t^+), Q_1(t^+)\} = ff(D_0,D_1)$ $I=\{X\}$ $O=\{Z\}$

1. Determine the expression for the F function that drives the flip-flops:

$$D_0 = Q_0 \bullet X' + Q_0' \bullet X$$
$$D_1 = Q_1 \bullet X' + Q_1' \bullet Q_0 \bullet X + Q_1 \bullet Q_0' \bullet X \qquad F(S,I)$$

2. Determine expressions for next states $S^+=\{Q_0(t^+), Q_1(t^+)\}$; $S^+= H(S,I)$

$Q_0^+ = D_0$ (D Flip-flop characteristic equation)

$Q_1^+ = D_1$

$$Q_0^+ = Q_0 \bullet X' + Q_0' \bullet X$$
$$Q_1^+ = Q_1 \bullet X' + Q_1' \bullet Q_0 \bullet X + Q_1 \bullet Q_0' \bullet X \qquad S^+ = H(S,I)$$

3. Construct the state transition table

Q_1Q_0	$Q_1^+ Q_0^+$ X=0	$Q_1^+ Q_0^+$ X=1
00	00	01
01	01	10
10	10	11
11	11	00

Inputs

Current States

Next States

To make the table easier to understand, we assign state names to state codes.

00: A
01: B
10: C
11: D

State Table

S	S^+ X=0	S^+ X=1
A	A	B
B	B	C
C	C	D
D	D	A

S: Current state S^+: Next state Q_1 and Q_0: State variables

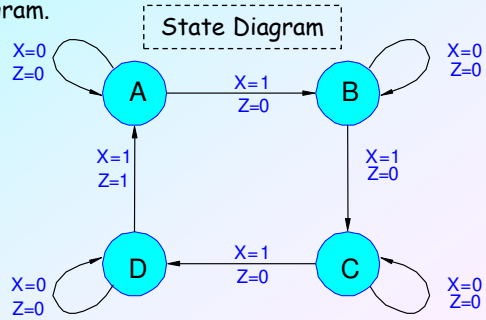
4. Determine the expression for the output function O = G(S,I) .

$Z = Q_1 \bullet Q_0 \bullet X$ (Mealy model because output depends both on input and state)

5. Construct the state/output table

S^+,Z / S \ X	0	1
A	A,0	B,0
B	B,0	C,0
C	C,0	D,0
D	D,0	A,1

This table presents the behavior of the finite state machine.
This behavior can also be presented graphically by a state diagram.



Reading the table:

When the machine is in state A:
if it receives a "1" at the input, the output becomes 0;
after the transition of the clock signal, the machine goes to state B.

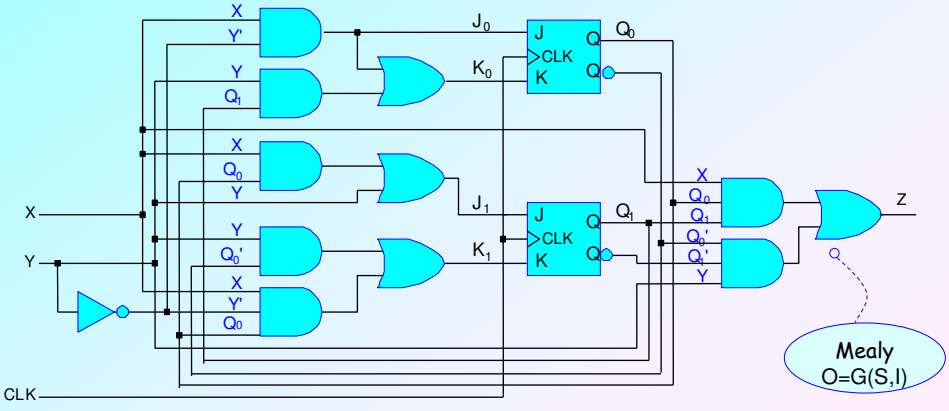
Verbal expression of the behavior of the circuit: We assume that A is the initial state. Only if the number of 1s received at the input is a multiple of 4, the output is 1. Otherwise, the output is 0.

Example: Analysis of a clocked synchronous circuit with J-K flip-flops

Unlike the previous example, when determining the expressions for the next states (Q_i^+) here, we will use the characteristic function for the JK flip-flop.

Reminder: $Q^+ = J \bullet Q' + K' \bullet Q$ (characteristic function for the JK flip-flop)

Circuit:



1. Determine the F function that drives the inputs of the flip-flops:

$J_0 = X \bullet Y'$
$K_0 = X \bullet Y' + Y \bullet Q_1$

$J_1 = X \bullet Q_0 + Y$
$K_1 = Y \bullet Q_0' + X \bullet Y' \bullet Q_0$

2. Determine the next state $S^+=\{Q_0(t^+), Q_1(t^+)\}$ expressions. $S^+= H(S,I)$

$Q_0^+ = J_0 \bullet Q_0' + K_0' \bullet Q_0$ (J-K FF characteristic function)
$Q_0^+ = X \bullet Y' \bullet Q_0' + (X \bullet Y' + Y \bullet Q_1)' \bullet Q_0$
$Q_0^+ = X \bullet Y' \bullet Q_0' + X' \bullet Y' \bullet Q_0 + X' \bullet Q_1' \bullet Q_0 + Y \bullet Q_1' \bullet Q_0$
$Q_0^+ = X \bullet Y' \bullet Q_0' + X' \bullet Y' \bullet Q_0 + Y \bullet Q_1' \bullet Q_0$ (minimization)

$Q_1^+ = J_1 \bullet Q_1' + K_1' \bullet Q_1$ (J-K FF characteristic function)
$Q_1^+ = (X \bullet Q_0 + Y) \bullet Q_1' + (Y \bullet Q_0' + X \bullet Y' \bullet Q_0)' \bullet Q_1$
$Q_1^+ = X \bullet Q1' \bullet Q_0 + Y \bullet Q_1' + X' \bullet Y' \bullet Q_1 + Y' \bullet Q_1 \bullet Q_0' + X' \bullet Q_1 \bullet Q_0 + Y \bullet Q_1 \bullet Q_0$
$Q_1^+ = X \bullet Q_1' \bullet Q_0 + Y \bullet Q_1' + Y \bullet Q_0 + X' \bullet Q_1 \bullet Q_0 + Y' \bullet Q_1 \bullet Q_0'$ (minimization)

3. Determine the expression of the output function G.

$Z = X \bullet Q_1 \bullet Q_0 + Y \bullet Q_1' \bullet Q_0'$

State/Output Table:

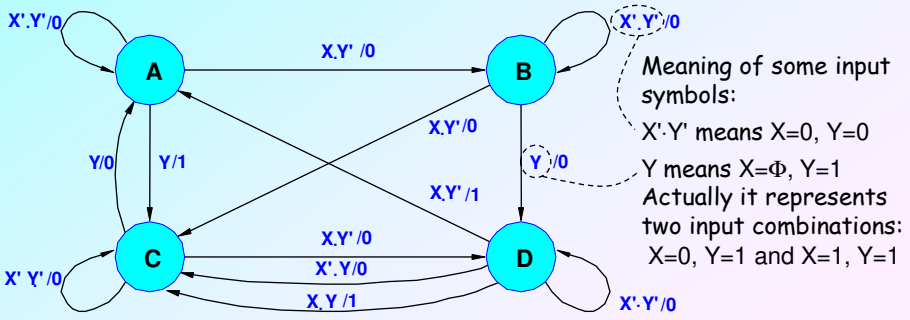
$Q_1^+ Q_0^+ , Z$

Q_1Q_0	XY = 00	01	10	11
00	00,0	10,1	01,0	10,1
01	01,0	11,0	10,0	11,0
10	10,0	00,0	11,0	00,0
11	11,0	10,0	00,1	10,1

S^+ , Z

S	XY = 00	01	10	11
A	A,0	C,1	B,0	C,1
B	B,0	D,0	C,0	D,0
C	C,0	A,0	D,0	A,0
D	D,0	C,0	A,1	C,1

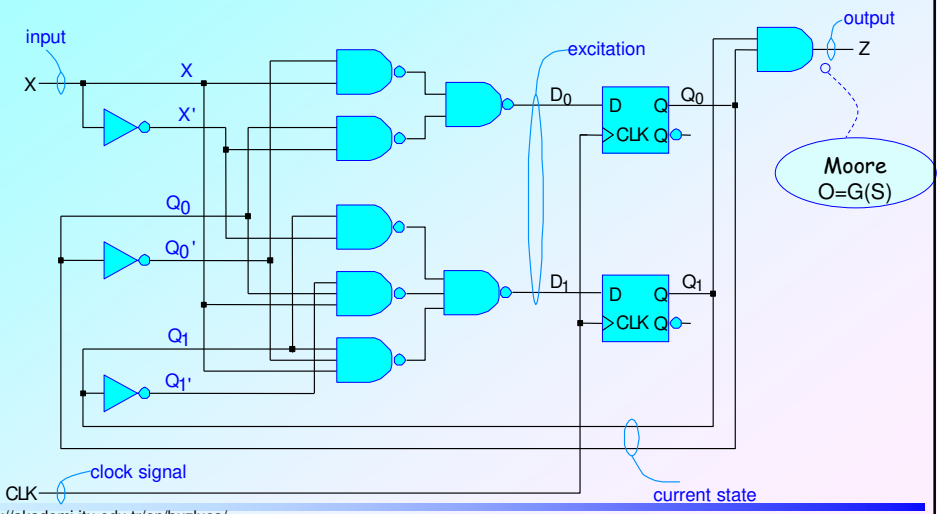
State Transition Diagram:



Analysis of a clocked synchronous sequential circuit designed according to the Moore model:

Remember that in Moore model, the output depends only on the current state.

In the circuit below, output Z depends only on state variables (Q_1,Q_0).



The analysis of circuits designed according to the Moore model is very similar to that of circuits designed according to the Mealy model.

They differ only in the construction and interpretation of the state/output table.

1. Determine the expression for the F function that drives the flip-flops:

$$D_0 = Q_0 \bullet X' + Q_0' \bullet X$$
$$D_1 = Q_1 \bullet X' + Q_1' \bullet Q_0 \bullet X + Q_1 \bullet Q_0' \bullet X$$

2. Determine the next state $S^+=\{Q_0(t^+), Q_1(t^+)\}$ expressions. $S^+= H(S,I)$

$$Q_0^+ = D_0$$
$$Q_1^+ = D_1$$
$$Q_0^+ = Q_0 \bullet X' + Q_0' \bullet X$$
$$Q_1^+ = Q_1 \bullet X' + Q_1' \bullet Q_0 \bullet X + Q_1 \bullet Q_0' \bullet X$$

3. Construct the transition table and the state table.

$Q_1^+ Q_0^+$ / Q_1Q_0 \ X	0	1
00	00	01
01	01	10
10	10	11
11	11	00

For simplicity, letters of the alphabet are assigned to state codes.

S^+ / S \ X	0	1
A	A	B
B	B	C
C	C	D
D	D	A

S: Current state S^+: Next state Q_1 and Q_0: State variables

4. Determine the expression of the output function G

$Z = Q_1 \cdot Q_0$ (**Moore** model; output depends only on state variables.)

5. Construct the state/output table.

S^+ / X / S	0	1	Z
A	A	B	0
B	B	C	0
C	C	D	0
D	D	A	1

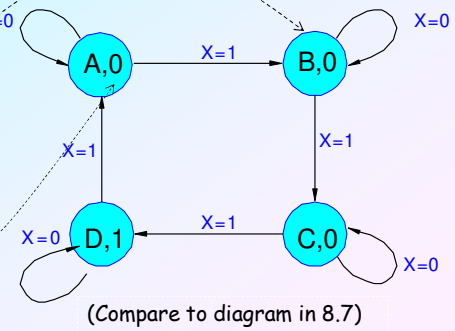
Since the output depends only on the present state in the Moore model, there is only a single output column (only one output value is written in each row), independent of the input.

Each row corresponds to a state.

Reading the table and diagram:

When the machine is in state A: if it receives a "1" at the input, after the transition of the clock signal,

- the machine goes to state B, and then
- the output becomes 0.



In the state diagram of a circuit in the Moore model, the output value for each state is written in the state circle because the output is a function of only the present state.

(Compare to diagram in 8.7)

Interpretation of Outputs in Mealy and Moore Models

If you check the output of a digital circuit at a certain moment, you will always read a logical 0 or 1 (except high impedance outputs).

However, this value may not be valid due to some reasons. For example, due to internal delays, the circuit might not have finished its job, yet.

Therefore, it is important when to read (sample) the output.

In clocked synchronous sequential circuits, outputs are sampled (read) at different times depending on the model (Mealy or Moore).

Mealy Model:

Since the output depends also on the input, if the input changes, the output changes at the same time (actually, after the propagation delay).

A circuit designed using the Mealy model operates as follows:

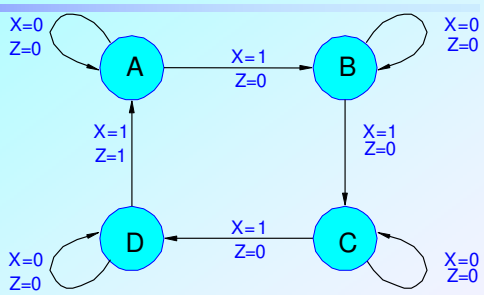
1. Input values (I) are applied.
2. **Output values are obtained** as a function of the input and current state.
   O=G(S,I)
3. The active edge of the clock signal (for example, rising edge (0 to 1 transition)) arrives at the flip-flops.
4. The machine goes to the next state. The next state is a function of the input and current state. $S^+=H(S,I)$

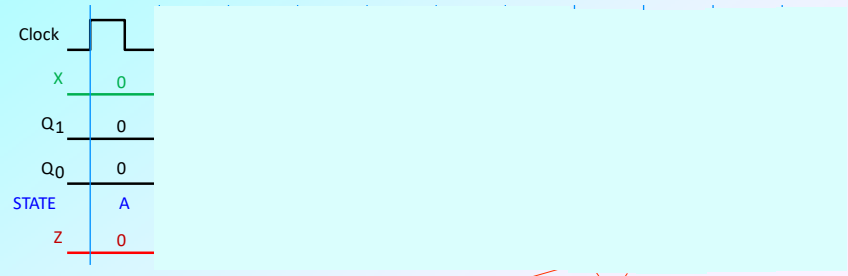
Example: The timing diagram of the sequential circuit designed according to the Mealy model with the given state diagram is shown below.

State Coding:

Q_1Q_0

0 0 : A
0 1 : B
1 0 : C
1 1 : D





The output which corresponds to a given input appears immediately following application of that input.

Moore Model:

In the Moore model, since the output is the function of the state only, change in the input cannot affect the output immediately.

The effect of changes in input can be seen on the output just after the change in the state.

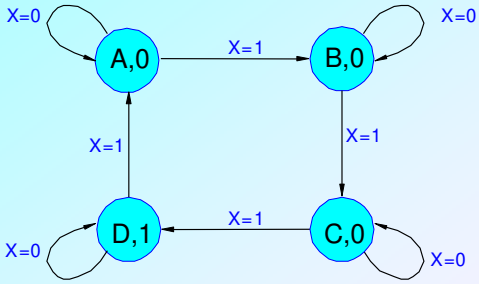
A circuit designed using the Moore model operates as follows:

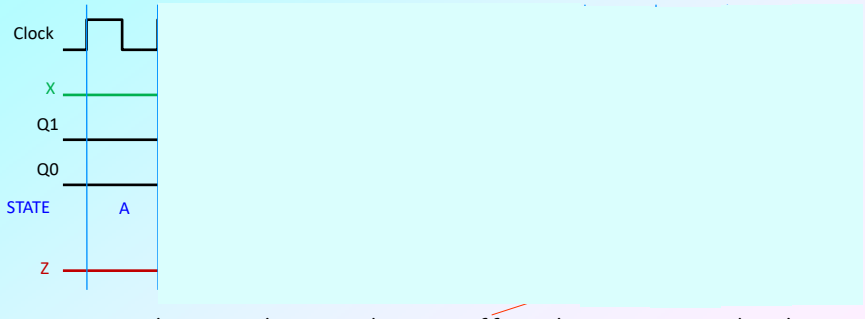
1. Input values (I) are applied.
2. The active edge of the clock signal (for example, rising edge (0 to 1 transition)) arrives at the flip-flops.
3. The machine goes to the next state. The next state is a function of the input and current state. $S^+=H(S,I)$
4. The **output value is determined** as a function of the **new state**.
   $O=G(S)$

In the Moore model, the output which results from application of a given input does not appear until after the clock pulse.

Therefore, the output sequence is displaced in time with respect to the input sequence.

Example: The timing diagram of the sequential circuit designed according to the Moore model with the given state diagram is shown below.

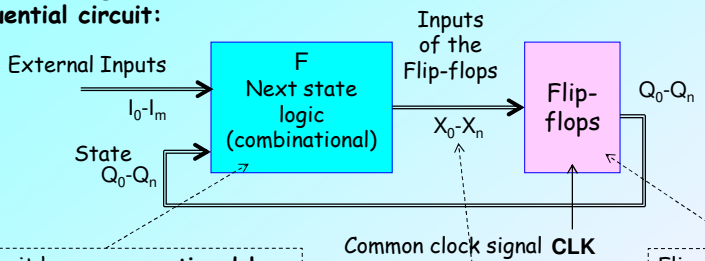




A change in the input does not affect the output immediately.

The Role of the Clock Signal

Next State Logic of a sequential circuit:



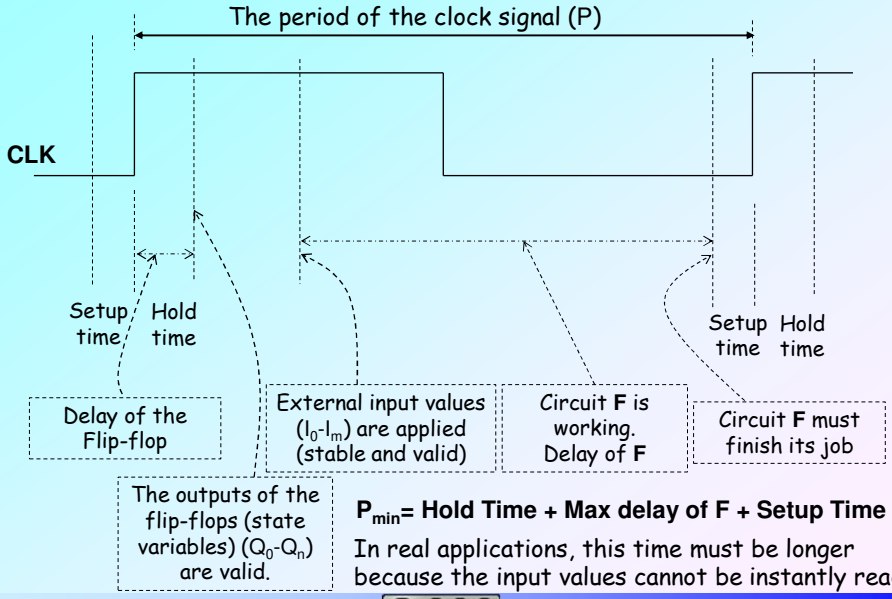
This circuit has a **propagation delay**. The output values (X_0-X_n) are not always valid. There may also be hazards.

These values (X_0-X_n) must be stable and valid on the active edge of the clock (for example, on the rising edge).

Flip-flops also have propagation delays (setup time, hold time).

- The speed (period) of the clock signal is determined based on the maximum delay (longest path) in the **F** circuit.
- Before the active edge of the clock (for example, a rising edge) arrives, the circuit **F** must finish its job, and the inputs of the flip-flops must be stable and valid.
- Possible hazards in **F** must also end before the clock signal becomes active.

Determining the speed (period) of the clock signal



P_{min}= Hold Time + Max delay of F + Setup Time

In real applications, this time must be longer because the input values cannot be instantly ready.