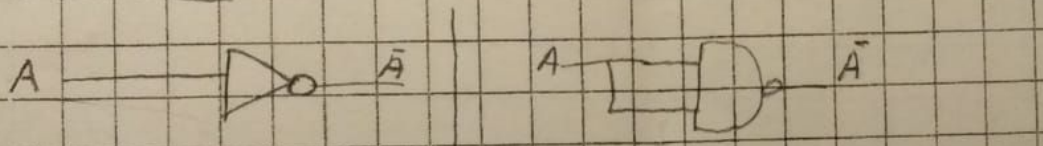
DENEY PROTOKOL KAĞIDI

Deney No	Deney Tarihi	Deney Adı
06	29.03.2024	Logic Gates and Basic Memory Circuits

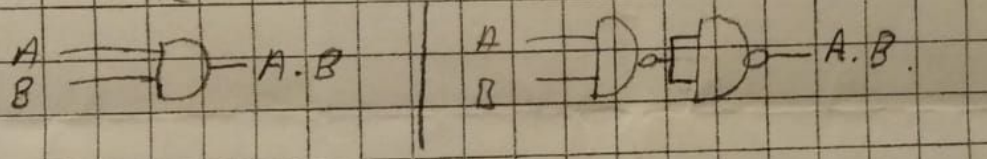
Grup No	Öğrenci No	Adı Soyadı
C10	150200097	Mustafa Can Gülaslan
C10	150200095	Teoman Türkoğlu
C10	150200907	Erol Kocoğlu
C10	150200712	Fitnat Çörüş

Araş Gör Ve imzası	Onur Aydınoğlu

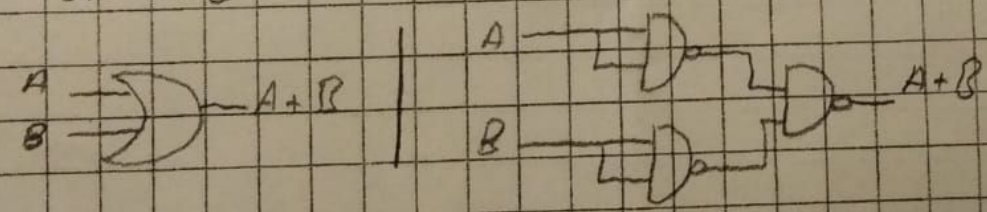
1) Not Gate



And Gate



Or Gate



2) S-R Latch truth table

S	R	Q
1	1	no change
0	1	1
1	0	0
0	0	invalid

3) D Latch truth table

E	D	Q
0	x	Q
1	0	0
1	1	1

4) Master-Slave D flip-flop truth table

D	clk	Q	Q'
0	↑	0	1
1	↑	1	0
x	D	Q	Q'
x	1	Q	Q'

4) The circuit consists of 2 D flip-flops connected together. When the clock is 1, input is stored in the second flip-flop, but the first flip-flop cannot change its state. When the clock is 0, the first one can change its state, while the second one cannot.

The output can only change state when the clock makes a transition from low to high (↑)