Arm Cortex-M0+ Instruction Set Summary

Operation	Description	Assembler
Move	8-bit immediate	MOVS Rd, #<imm>
	Lo to Lo	MOVS Rd, Rm
	Any to Any	MOV Rd, Rm
	Any to PC	MOV PC, Rm
Add	3-bit immediate	ADDS Rd, Rn, #<imm>
	All registers Lo	ADDS Rd, Rn, Rm
	Any to Any	ADD Rd, Rd, Rm
	Any to PC	ADD PC, PC, Rm
	8-bit immediate	ADDS Rd, Rd, #<imm>
	With carry	ADCS Rd, Rd, Rm
	Immediate to SP	ADD SP, SP, #<imm>
	Form address from SP	ADD Rd, SP, #<imm>
	Form address from PC	ADR Rd, <label>
Subtract	Lo and Lo	SUBS Rd, Rn, Rm
	3-bit immediate	SUBS Rd, Rn, #<imm>
	8-bit immediate	SUBS Rd, Rd, #<imm>
	With carry	SBCS Rd, Rd, Rm
	Negate	RSBS Rd, Rn, #0
Multiply	Multiply	MULS Rd, Rm, Rd
Compare	Compare	CMP Rn, Rm
	Negative	CMN Rn, Rm
	Immediate	CMP Rn, #<imm>
Logical	AND	ANDS Rd, Rd, Rm
	Exclusive OR	EORS Rd, Rd, Rm
	OR	ORRS Rd, Rd, Rm
	Bit clear	BICS Rd, Rd, Rm
	Move NOT	MVNS Rd, Rm
	AND test	TST Rn, Rm
Shift	Logical shift left by immediate	LSLS Rd, Rm, #<shift>
	Logical shift left by register	LSLS Rd, Rd, Rs
	Logical shift right by immediate	LSRS Rd, Rm, #<shift>
	Logical shift right by register	LSRS Rd, Rd, Rs
	Arithmetic shift right	ASRS Rd, Rm, #<shift>
	Arithmetic shift right by register	ASRS Rd, Rd, Rs
Rotate	Rotate right by register	RORS Rd, Rd, Rs
Load	Word, immediate offset	LDR Rd, [Rn, #<imm>]
	Halfword, immediate offset	LDRH Rd, [Rn, #<imm>]
	Byte, immediate offset	LDRB Rd, [Rn, #<imm>]
	Word, register offset	LDR Rd, [Rn, Rm]
	Halfword, register offset	LDRH Rd, [Rn, Rm]
	Signed halfword, register offset	LDRSH Rd, [Rn, Rm]
	Signed byte, register offset	LDRSB Rd, [Rn, Rm]
	PC-relative	LDR Rd, <label>
	SP-relative	LDR Rd, [SP, #<imm>]
	Multiple, excluding base	LDM Rn!, {<loreglist>}
	Multiple, including base	LDM Rn, {<loreglist>}

Store	Word, immediate offset	STR Rd, [Rn, #<imm>]
	Halfword, immediate offset	STRH Rd, [Rn, #<imm>]
	Byte, immediate offset	STRB Rd, [Rn, #<imm>]
	Word, register offset	STR Rd, [Rn, Rm]
	Halfword, register offset	STRH Rd, [Rn, Rm]
	Byte, register offset	STRB Rd, [Rn, Rm]
	SP-relative	STR Rd, [SP, #<imm>]
	Multiple	STM Rn!, {<loreglist>}
Push	Push	PUSH {<loreglist>}
	Push with link register	PUSH {<loreglist>, LR}
Pop	Pop	POP {<loreglist>}
	Pop and return	POP {<loreglist>, PC}
Branch	Conditional	B<cc> <label>
	Unconditional	B <label>
	With link	BL <label>
	With exchange	BX Rm
	With link and exchange	BLX Rm
Extend	Signed halfword to word	SXTH Rd, Rm
	Signed byte to word	SXTB Rd, Rm
	Unsigned halfword	UXTH Rd, Rm
	Unsigned byte	UXTB Rd, Rm
Reverse	Bytes in word	REV Rd, Rm
	Bytes in both halfwords	REV16 Rd, Rm
	Signed bottom half word	REVSH Rd, Rm

Condition code suffixes

Suffix	Flags	Meaning
EQ	Z = 1	Equal, last flag setting result was zero
NE	Z = 0	Not equal, last flag setting result was non-zero
CS or HS	C = 1	Higher or same, unsigned
CC or LO	C = 0	Lower, unsigned
MI	N = 1	Negative
PL	N = 0	Positive or zero
VS	V = 1	Overflow
VC	V = 0	No overflow
HI	C = 1 and Z = 0	Higher, unsigned
LS	C = 0 or Z = 1	Lower or same, unsigned
GE	N = V	Greater than or equal, signed
LT	N != V	Less than, signed
GT	Z = 0 and N = V	Greater than, signed
LE	Z = 1 and N != V	Less than or equal, signed
AL	Can have any value	Always. This is the default when no suffix is specified.