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BLG 212E Microprocessor Systems – Quiz 2

Question 1)

Examine the following ARM assembly code snippet, focusing on the sequence of function calls and the stack state during execution. Using the labeled instructions (I1–I19), complete the following tasks **(Note: The main function will be executed once)**:

1. Instruction Execution Order: List the precise sequence in which each instruction (I1 to I19) executes.
2. Stack State Analysis: Draw the state of the stack after each PUSH and POP operation. For each step, show the stack's contents and indicate any changes made by each PUSH or POP instruction.
3. Register Values: At the end what are the values of R0, R1, R2 registers?

```
__main  FUNCTION
        EXPORT  __main
        BL        foo       ; I1
        B       __main      ; I2
foo
        PUSH {LR}           ; I3
        MOVS R0, #5         ; I4
        MOVS R1, #10        ; I5
        MOVS R2, #15        ; I6
        BL bar              ; I7
        POP {PC}            ; I8
tar
        PUSH {LR}           ; I9
        ADD R0, R0, R3      ; I10
        ADD R1, R1, R4      ; I11
        POP {PC}            ; I12
bar
        PUSH {LR}           ; I13
        PUSH {R0, R1, R2}   ; I14
        MOVS R3, #25        ; I15
        MOVS R4, #30        ; I16
        BL tar              ; I17
        POP {R0, R1, R2}    ; I18
        POP {PC}            ; I19
```

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!!! WRITE THE SOLUTION TO QUESTION 2 ON THIS PAGE BY FOLLOWING THE TEMPLATE BELOW!!!

A 2.1) INSTRUCTION EXECUTION ORDER

1. I1	2. I3	3. I4	4. I5	5. I6	6. I7	7. I13	8. I14	9. I15	10. I16
11. I17	12. I9	13. I10	14. I11	15. I12	16. I18	17. I19	18. I8	19. I2	20.
21.	22.	23.	24.	25.	26	27.	28.	29.	30.

A 2.2) STACK STATE ANALYSIS

Template: LAST EXECUTED INSTRUCTION [e.g. I13]

STACK CONTENT
R20
R21
R22
R23

← Higher Address

NOTE: LR register stores the return address, which is the address of the instruction that comes after the branch instruction.

EXECUTED INS. : I3

STACK CONTENT
&I2 (Address of instruction I2)

EXECUTED INS. : I13

STACK CONTENT
&I2 (Address of instruction I2)
&I8 (Address of instruction I8)

EXECUTED INS. : I14

STACK CONTENT
&I2 (Address of instruction I2)
&I8 (Address of instruction I8)
15 (Value of R2)
10 (Value of R1)
5 (Value of R0)

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EXECUTED INS. : I19

STACK CONTENT
&I2 (Address of instruction I2)
&I8 (Address of instruction I8)
15 (Value of R2)
10 (Value of R1)
5 (Value of R0)
&I18 (Address of instruction I18)

EXECUTED INS. : I12

STACK CONTENT
&I2 (Address of instruction I2)
&I8 (Address of instruction I8)
15 (Value of R2)
10 (Value of R1)
5 (Value of R0)

EXECUTED INS. : I18

STACK CONTENT
&I2 (Address of instruction I2)
&I8 (Address of instruction I8)

EXECUTED INS. : I19

STACK CONTENT
&I2 (Address of instruction I2)

EXECUTED INS. : I8

STACK CONTENT

A 2.3) REGISTER VALUES

R0	R1	R2
5	10	15