Istanbul Technical University

BLG 231E - Digital Circuits
Assignment 2
Solution Key

1) a)i) First Canonical Form ; Sum of Products (SoP)

	H	M	L	F	Y
0	0	0	0	0	**0**
1	0	0	0	1	**0**
2	0	0	1	0	**0**
3	0	0	1	1	**1**
4	0	1	0	0	**0**
5	0	1	0	1	**0**
6	0	1	1	0	**1**
7	0	1	1	1	**1**
8	1	0	0	0	**0**
9	1	0	0	1	**0**
10	1	0	1	0	**1**
11	1	0	1	1	**1**
12	1	1	0	0	**1**
13	1	1	0	1	**1**
14	1	1	1	0	**1**
15	1	1	1	1	**1**

Y(H,M,L,F) = H'M'LF + H'MLF' + H'MLF+ HM'LF' + HM'LF + HML'F' + HML'F + HMLF' + HMLF

1) a)ii)

	H	M	L	F	Y
0	0	0	0	0	**0**
1	0	0	0	1	**0**
2	0	0	1	0	**0**
3	0	0	1	1	**1**
4	0	1	0	0	**0**
5	0	1	0	1	**0**
6	0	1	1	0	**1**
7	0	1	1	1	**1**
8	1	0	0	0	**0**
9	1	0	0	1	**0**
10	1	0	1	0	**1**
11	1	0	1	1	**1**
12	1	1	0	0	**1**
13	1	1	0	1	**1**
14	1	1	1	0	**1**
15	1	1	1	1	**1**

Second Canonical Form (Product of Sums)
Y(H,M,L,F) =
(H+M+L+F).(H+M+L+F').(H+M+L'+F).(H+M'+L+F).(H+M'+L+F').(H'+M+L+F).
(H'+M+L+F')

1) b)

Y= H'M'LF+ H'MLF'+ H'MLF+ HM'LF'+HM'LF+ HML'F'+ HML'F+ HMLF'+ HMLF

Distributive

=H'LF(M'+M)+ H'ML(F'+F)+HM'L(F'+F)+ HML'(F'+F)+ HML(F'+F)

Inverse

=H'LF(1) + H'ML(1) + HM'L(1) + HML'(1) + HML(1)

Identity

=H'LF + H'ML + HM'L + HML' + HML

Distributive

=H'LF + ML(H'+H) + HL(M'+M) + HM(L'+L)

Inverse

=H'LF + ML(1) + HL(1) + HM(1)

Identity

=H'LF + ML + HL + HM

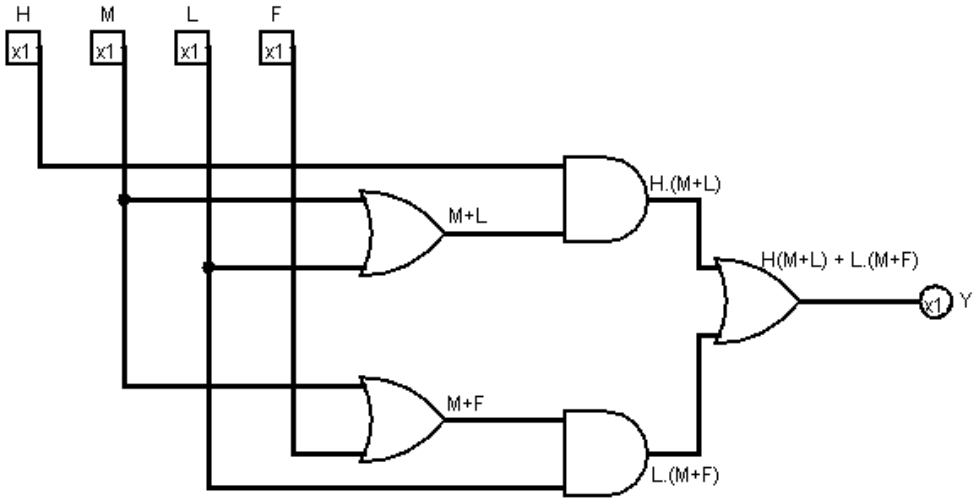
Consensus

=H'LF + ML + HL + HM + LF

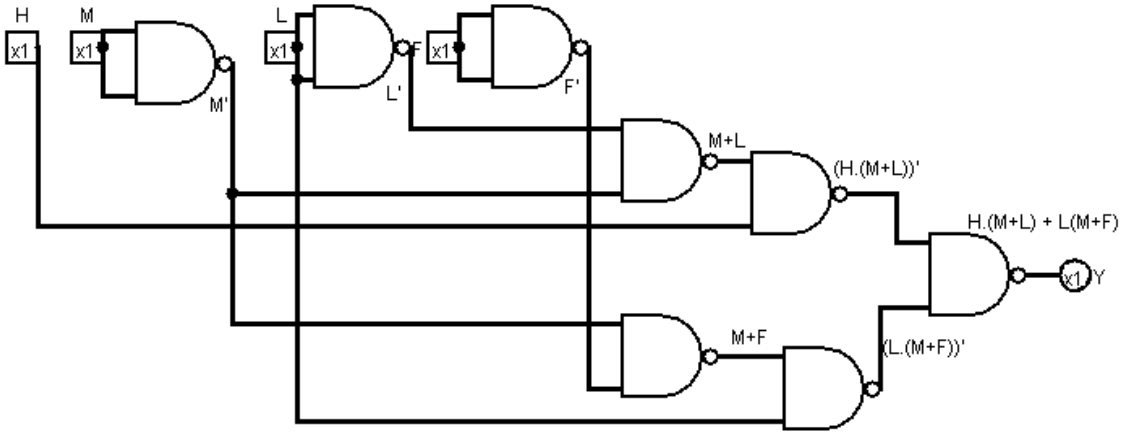
Absorption

=ML + HL + HM + LF ***Final***

2) a) If we take some common expressions into same paranthesis for convenience -> H.(M+L) + L(M+F)



2) b) If we take some common expressions into same paranthesis for convenience -> H.(M+L) + L(M+F)



3) Advantages of using only-NAND gates (1 NAND vs 1 "AND,OR")

*It is a universal gate. Easy to find, and cheaper

* In many cases, using only NAND may allow us to implement circuits with fever ICs. However, for both circuits in 2a and 2b we need two ICs. For example, for 2a we need one 7408 and one 7432. For 2b, wee need two 7400s.

Disadvantages of using only "NAND" gates instead of "AND, NOT, OR gates only"

- The number of gates increases for this particular circuit (8 versus 5)
- Since there are Four layers-like system it may cause propagation delay