ISTANBUL TECHNICAL UNIVERSITY
COMPUTER ENGINEERING DEPARTMENT

EXPERIMENT NO : 2
EXPERIMENT DATE : 31.03.2023
LAB SESSION : FRIDAY - 10.30
GROUP NO : G3

GROUP MEMBERS:

150200010 : Ahmet Emre Buz
150200097 : Mustafa Can Çalışkan

SPRING 2023

Contents

1 INTRODUCTION **1**

2 PRELIMINARY **1**

2.1 1

2.2 TRUTH TABLE 3

3 EXPERIMENT **4**

3.1 4

3.2 4

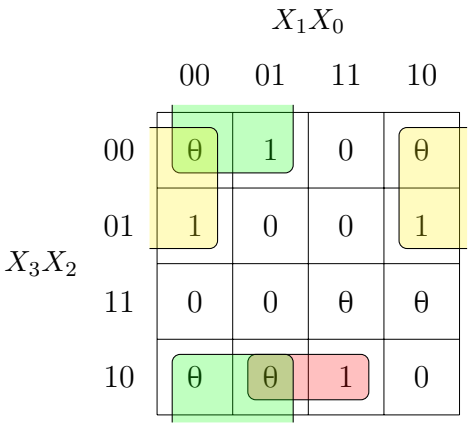
4 DISCUSSION **4**

1 INTRODUCTION

In this experiment, we implemented and simulated desired designs using Verilog.

2 PRELIMINARY

2.1



min terms and their binary representations

Minterm	*Binary representation*
0	0000
1	0001
4	0100
2	0010
8	1000
6	0110
9	1001
11	1011
14	1110
15	1111

merging of min term

Minterm	*Binary representation*
0,1	000-
0,4	0-00
0,2	00-0
0,8	-000
1,9	-001
4,6	01-0
2,6	0-10
8,9	100-
$\boxed{6, 14}$	$\boxed{-110}$
$\boxed{9, 11}$	$\boxed{10-1}$
$\boxed{11, 15}$	$\boxed{1-11}$
$\boxed{14, 15}$	$\boxed{111-}$

merging of min term pairs

Minterm	*Binary representation*
$\boxed{0, 2, 4, 6}$	$\boxed{0--0}$
$\boxed{0, 1, 8, 9}$	$\boxed{-00-}$

	minterms			
	1	4	6	11
-110			X	
10-1				X
1-11				X
111-				
0–0		X	X	
-00-	X			

All extracted essential prime implicants : -00-,0–0,1-11

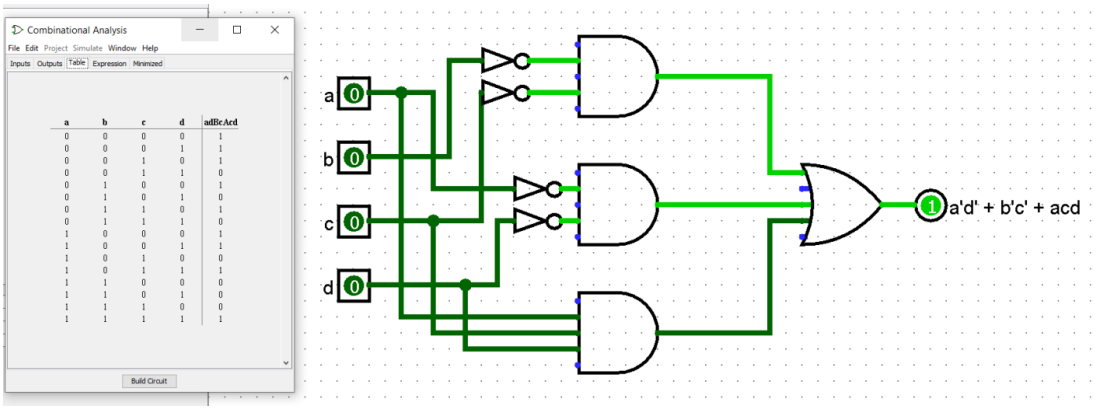
Minimal Quine-McCluskey Expression = b'c' + a'd' + acd

2.2 TRUTH TABLE

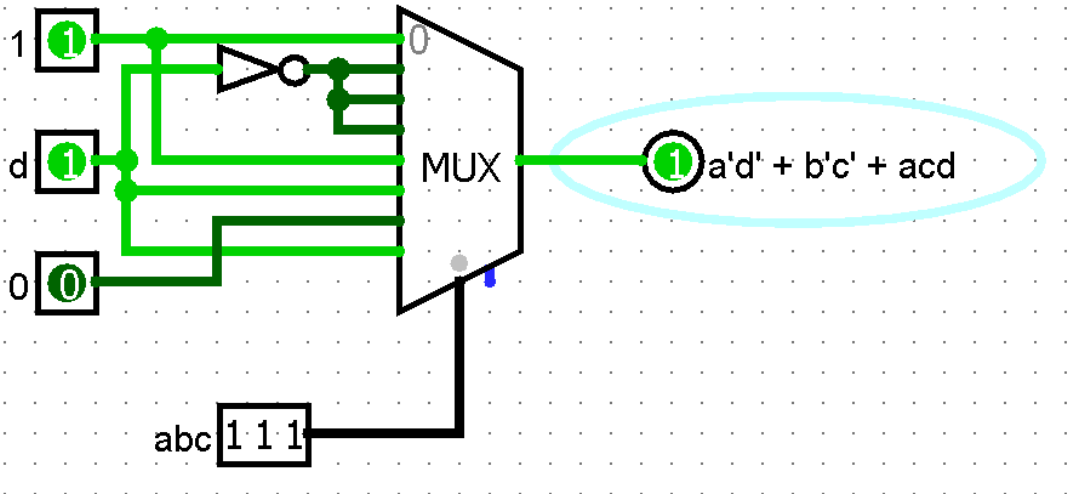
A	B	C	D	$Result$
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

3 EXPERIMENT

3.1



3.2



4 DISCUSSION

Don't cares are often used in logic design because they allow for simplification of the design by ignoring certain input or output states that are not relevant to the overall function. This can reduce the number of gates required and improve the efficiency of the circuit.