Faculty of Computer and Informatics Engineering

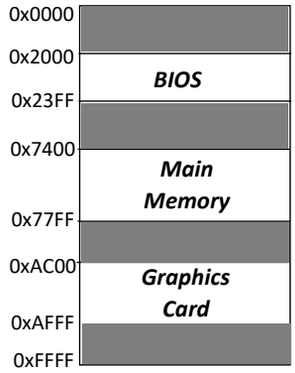
B

BLG 212E
Microprocessor Systems
10.10.2022

Quiz #1

1. The following questions are according to the memory map given on the side.
   a) Draw the chip select input of *BIOS*, *Main Memory*, and *Graphics Card* separately using the NAND circuit.

   b) Fill the following table according to the address input in which the chip selection area will be enabled or disabled.



Address Input	$\overline{CS_{BIOS}}$	$\overline{CS_{Memory}}$	$\overline{CS_{Graphics}}$
0x2103	0	1	1
0xE4C7	1	1	1
0xAD30	1	1	0
0x6B20	1	1	1

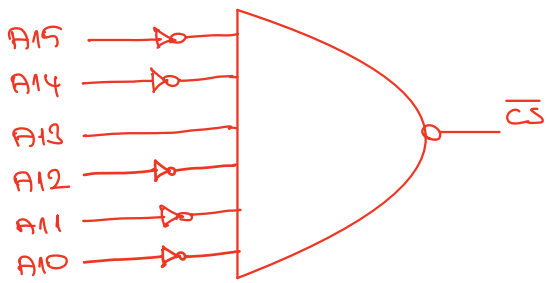
2. Build a memory that spans between $6000 and $9FFF with 4Kx8 memory chips for a CPU with 8-bit data bus and 16-bit address bus.
   a) Calculate the memory address range for all chips.
   b) How many 4K chips are needed?
   c) Draw the memory design by showing all necessary connections. (Address bus, Data bus, Chip select signals). Use an address decoder (determine its type) and logic gates (determine their types). Assume the decoder select signal and the memory chip select signals are active high.

Duration: 40 minutes

(1)

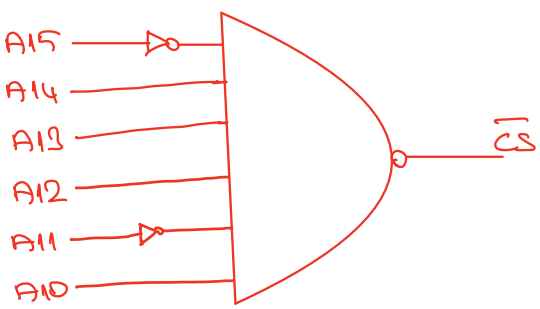
a) BIOS

0x 2000 ⇒ 0010 00|00 0000 0000
0x 23FF ⇒ 0010 00|11 1111 1111



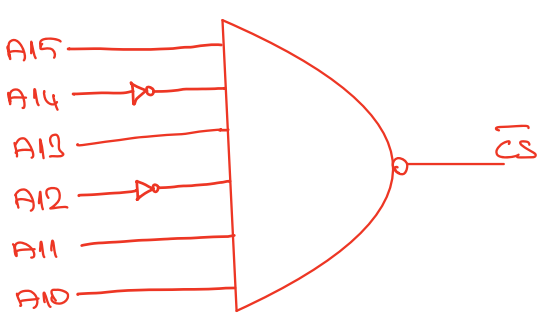
MAIN MEMORY

0x7400 ⇒ 0111 01|00 0000 0000
0x77FF ⇒ 0111 01|11 1111 1111



GRAPHICS CARD

0xAC00 ⇒ 1010 11|00 0000 0000
0x AFFF ⇒ 1010 11|11 1111 1111



② a)

$6000	⇒	0110	0000	0000	0000
$6FFF		0110	1111	1111	1111
$7000	⇒	0111	0000	0000	0000
$7FFF		0111	1111	1111	1111
$8000	⇒	1000	0000	0000	0000
$8FFF		1000	1111	1111	1111
$9000	⇒	1001	0000	0000	0000
$9FFF		1001	1111	1111	1111

b) 4

c)