ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY HOMEWORK REPORT

HOMEWORK NO	:	3
HOMEWORK DATE	:	28.04.2023
LAB SESSION	:	FRIDAY - 10.30
GROUP NO	:	G3

GROUP MEMBERS:

150200010 : Ahmet Emre Buz

150200097 : Mustafa Can Çalışkan

SPRING 2023

Contents

1 INTRODUCTION **1**

2 HOMEWORK **1**

2.1 PART 1 1

2.2 PART 2 3

2.3 PART 3 4

2.4 PART 4 5

2.5 PART 5 7

2.6 PART 6 9

3 CONCLUSION **10**

REFERENCES **11**

1 INTRODUCTION

In this homework, we implemented and simulated desired designs such as bus, three state buffers and memory modules using Verilog.

2 HOMEWORK

2.1 PART 1

8-bit bus by using 3-state buffers

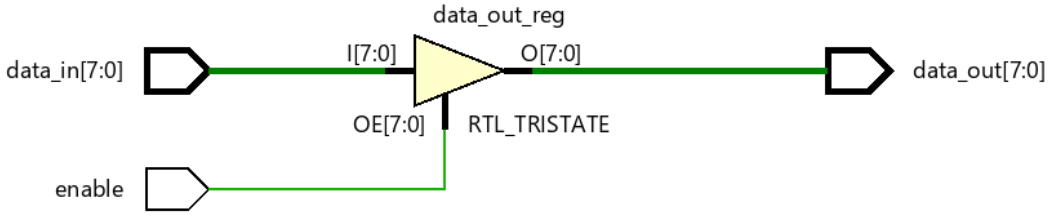

Figure 1: 3-state buffer

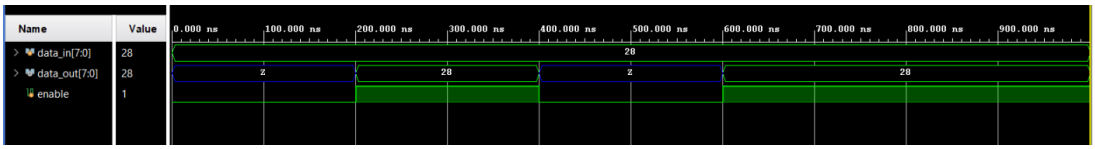

Figure 2: 3-state buffer simulation results

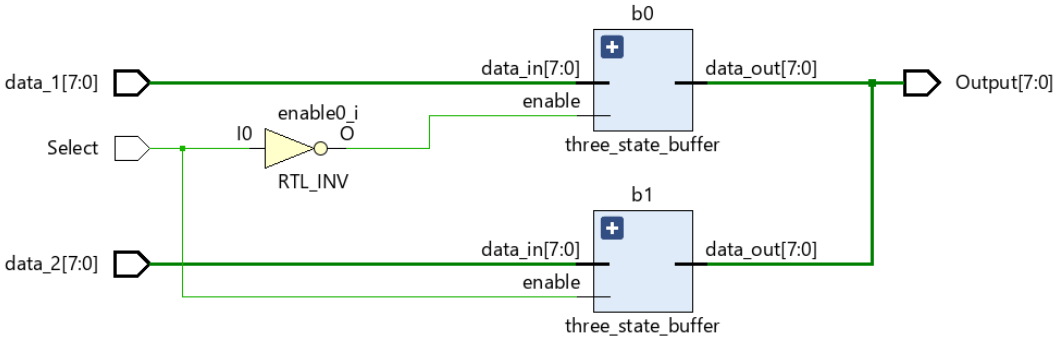

Figure 3: 8-bit bus

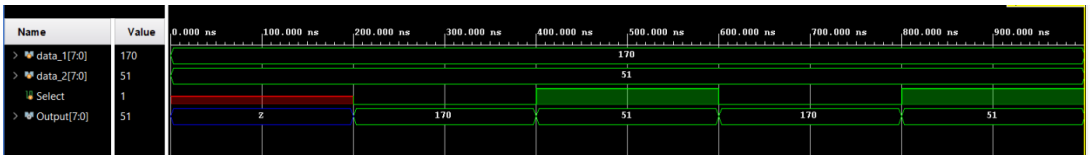

Figure 4: 8-bit bus simulation results

The eight_bit_bus module is a circuit that takes two 8-bit data inputs, and selects one of them to be the output based on the value of a select signal. When the select signal is low, the first input is passed through to the output, and when the select signal is high, the second input is passed through to the output. This is achieved using two three-state buffers, one for each input, which are enabled or disabled based on the select signal.

2.2 PART 2

8-bit bus by using 3-state buffers with 2 output

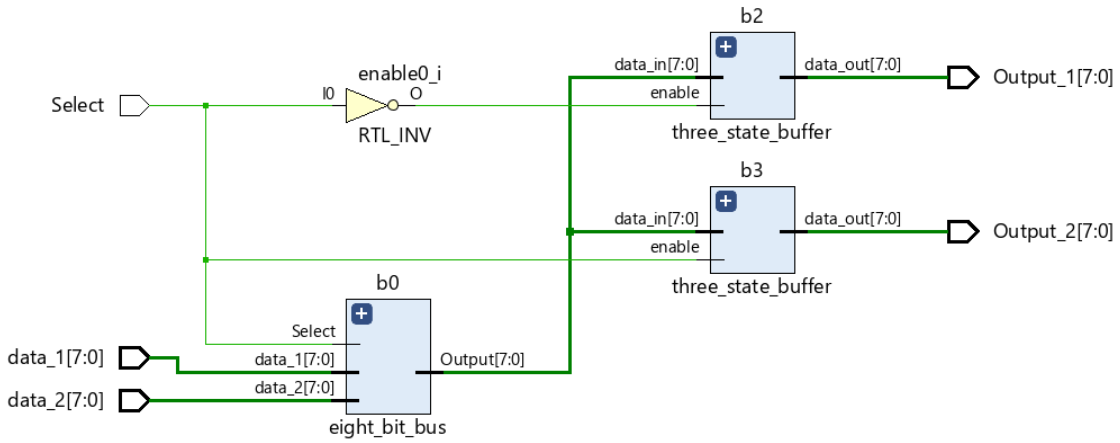

Figure 5: 8-bit bus with 2 output

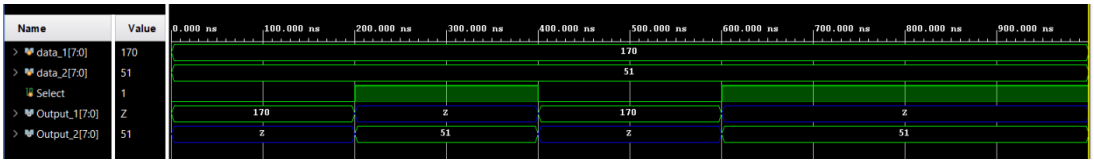

Figure 6: 8-bit bus with 2 output simulation results

The module takes two 8-bit data inputs and selects one of them to be the output for Output_1 or Output_2 based on the value of the Select signal. It does this using a combination of the 8-bit bus module to select which input data signal to use and two three-state buffers to select which output to drive. When Select is low, the left_out signal is passed through to Output_1, and when Select is high, left_out is passed through to Output_2.

2.3 PART 3

8-bit memory line module

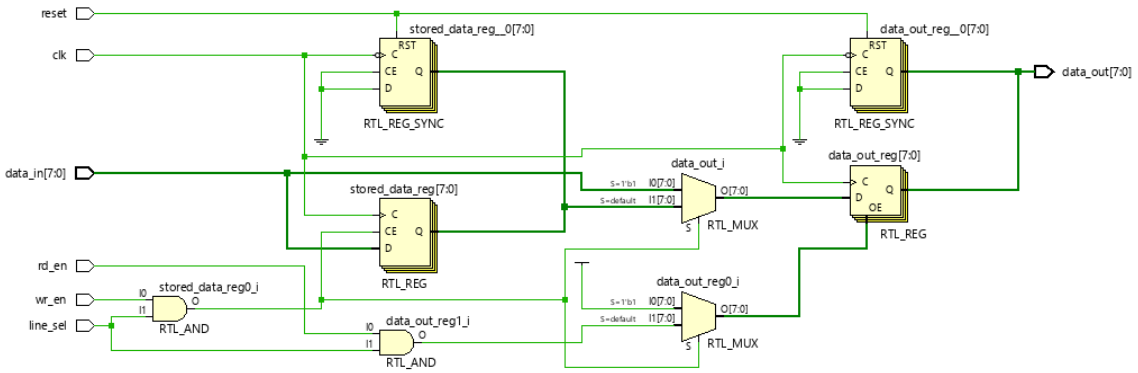

Figure 7: 8-bit memory line

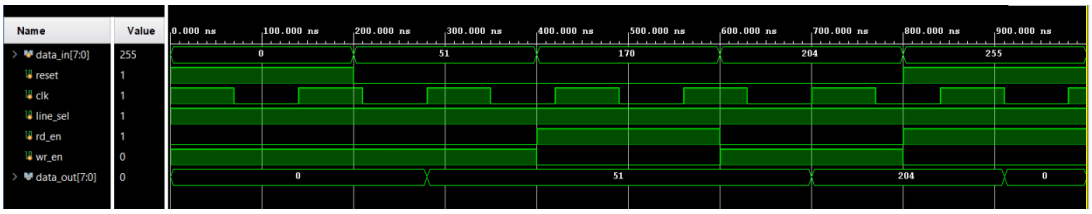

Figure 8: 8-bit memory line simulation results

The module is an 8-bit memory cell that can store and output a single value. It has a clock input and separate read/write enable inputs. When the write enable input is high, the module writes the input data to its internal memory. When the read enable input is high, the module outputs the stored value. It also has a 3-state output, which is used when neither read nor write operation is enabled.

2.4 PART 4

8 byte memory module

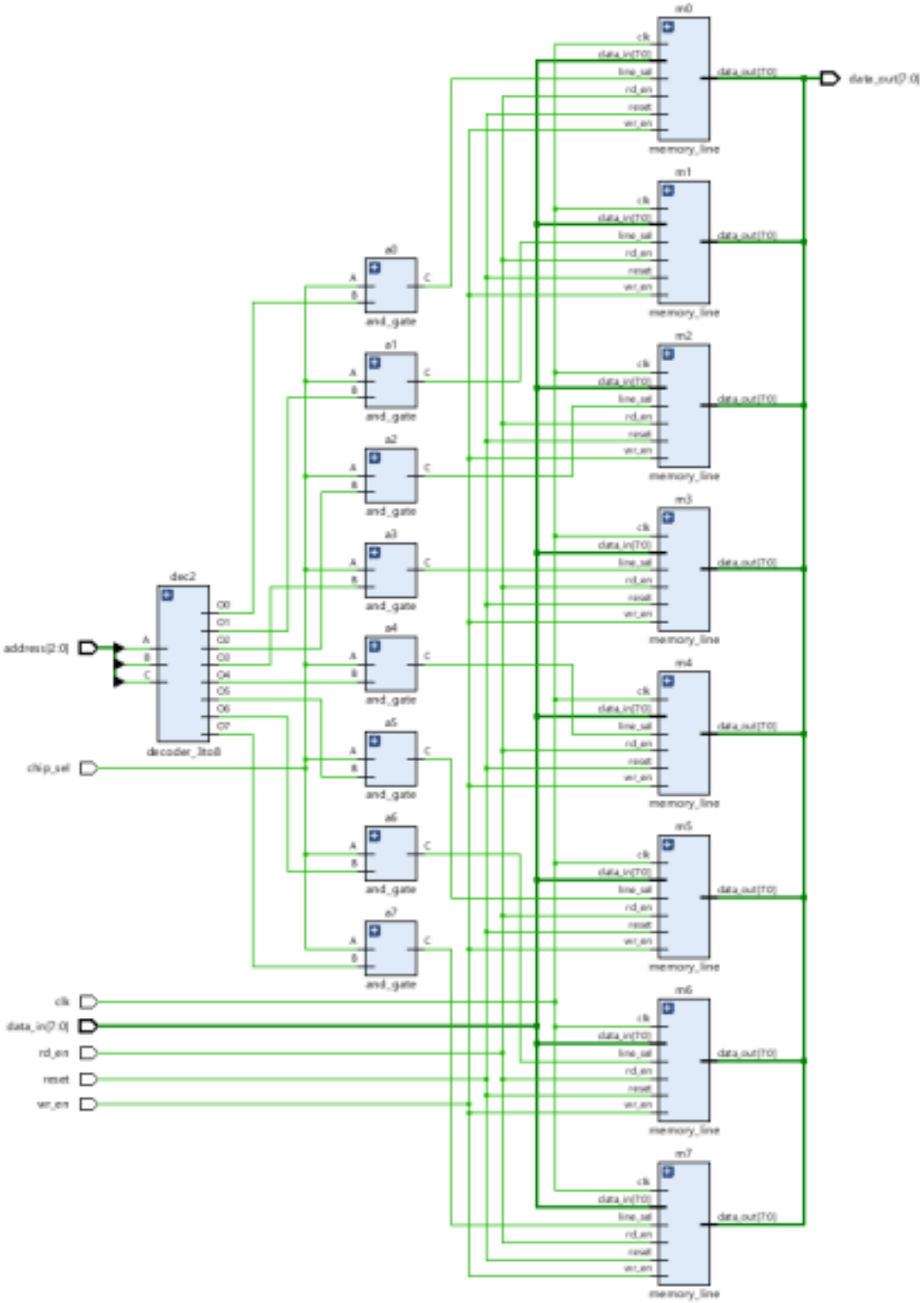

Figure 9: 8 byte memory

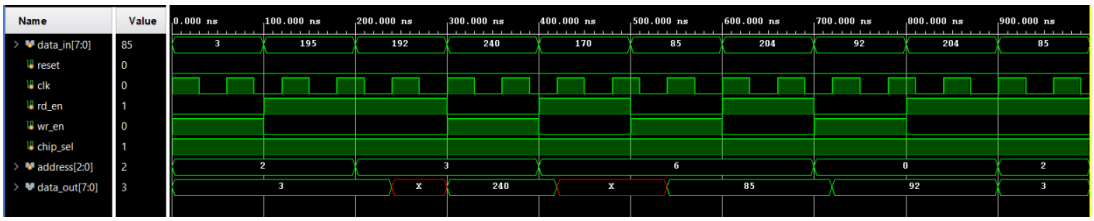

Figure 10: 8 byte memory simulation results

This module is a memory module that takes in data input, a reset signal, a clock signal, read and write enables, chip select signal, and an address. It also outputs data output. It uses a 3-to-8 decoder to decode the address, and 8 AND gates to select the appropriate memory line based on the chip select signal and the decoded address. There are 8 memory lines, each consisting of a memory element that stores the data and outputs it when the read enable signal is high. The module outputs the data output of the selected memory line based on the chip select and decoded address.

2.5 PART 5

32 byte memory module

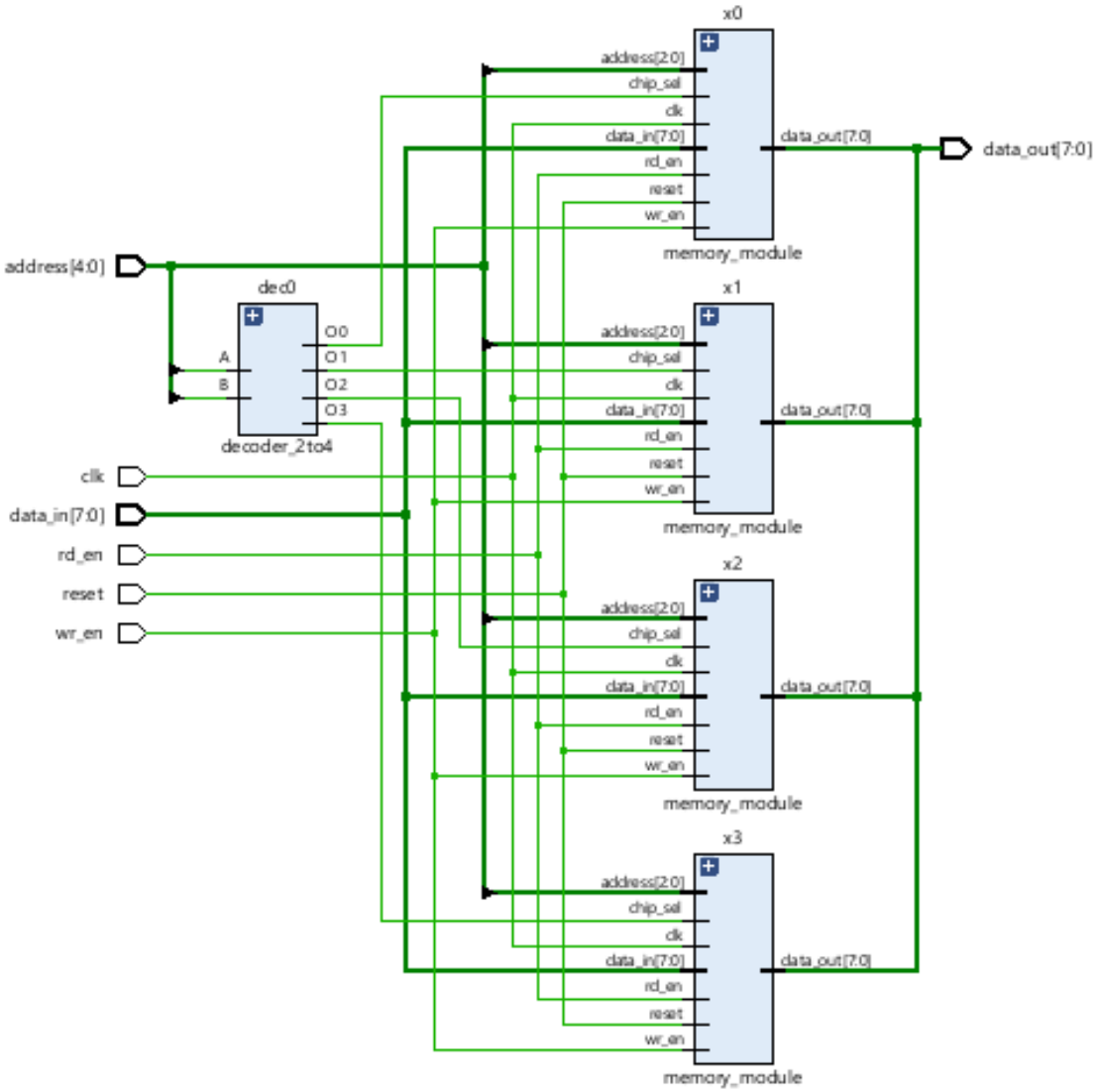

Figure 11: 32 byte memory

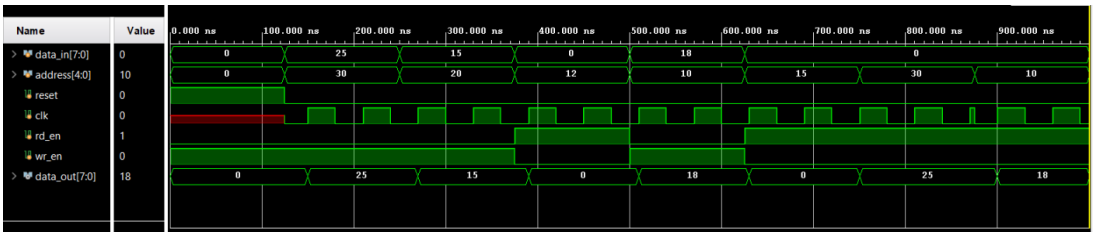

Figure 12: 32 byte memory simulation results

The module is a memory module that takes in 8-bit data and a 5-bit address and outputs 8-bit data. It has 4 instances of the 8 byte memory module, which is used to implement a 32x8 memory. The address is decoded by a 2-to-4 decoder, and the output from each decoder line is connected to one instance of the 8 byte memory module. The rd_en and wr_en signals are used to control the read and write operations, and reset is used to reset the memory. The clk signal is the clock input.

2.6 PART 6

128 byte memory module

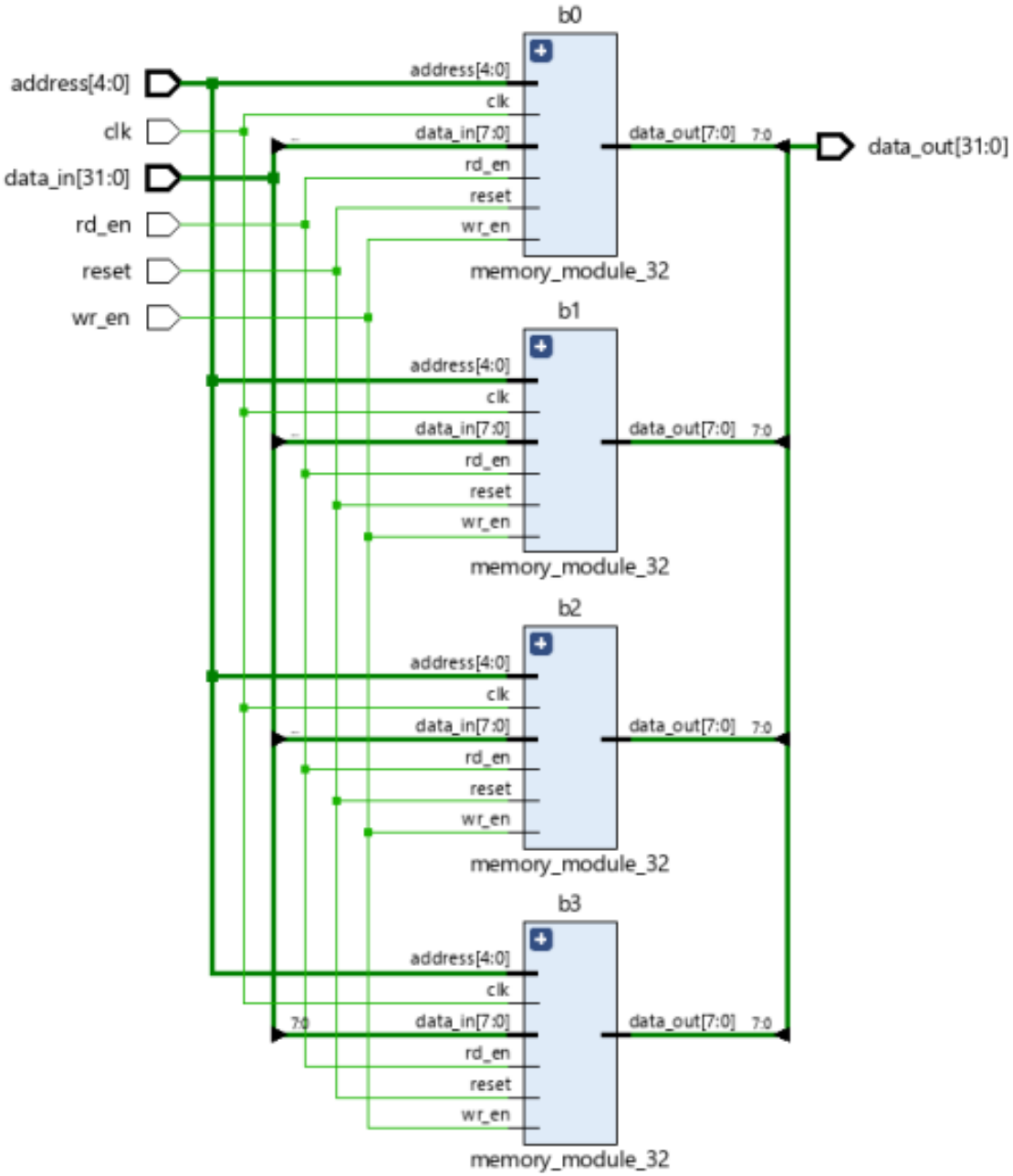

Figure 13: 128 byte memory

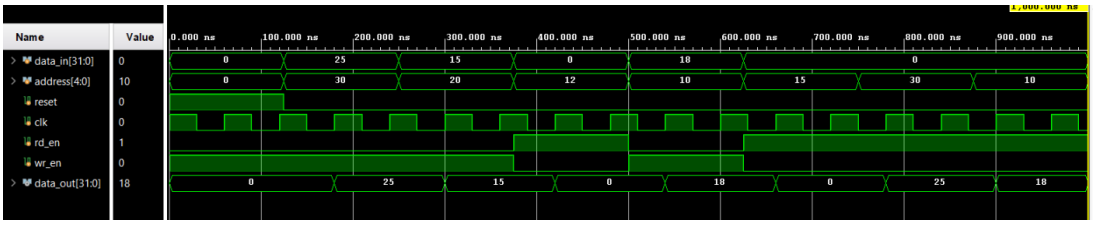

Figure 14: 128 byte memory simulation results

This module is a 128 byte memory module that consists of four 32 byte memory modules, each of which has its own data input, read and write enable signals, reset signal, clock signal, and output data. The memory modules are selected using the 5-bit address input. The output data of each memory module is combined to form the 128-bit final output. The module instantiates four instances of a 32 byte memory module and assigns the final output as the concatenation of the output of each 32 byte memory module.

3 CONCLUSION

In this experiment, we implemented and simulated desired designs such as bus, three state buffers and memory modules using Verilog.

REFERENCES