# BLG 231E HW4


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Label 1: When x is 0, the output (Z) does not contain C’. Thus, C’ will be produced when x = 1.

Label 2: Since the parallel adder is transformed into the subtractor when x is 1, the carry in bit is set to 1 if x = 1. ( A – C = A + (C’ + 1) )

Label 3: When y is 1, the output (Z) does not contain B. Therefore, B will be produced when y = 0.

Label 4: Since A will be produced when x = 0 or y = 1, A is connected to 1 input of MUX above, and 0 input of MUX below.