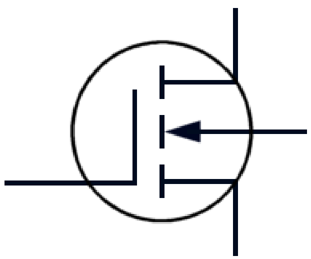
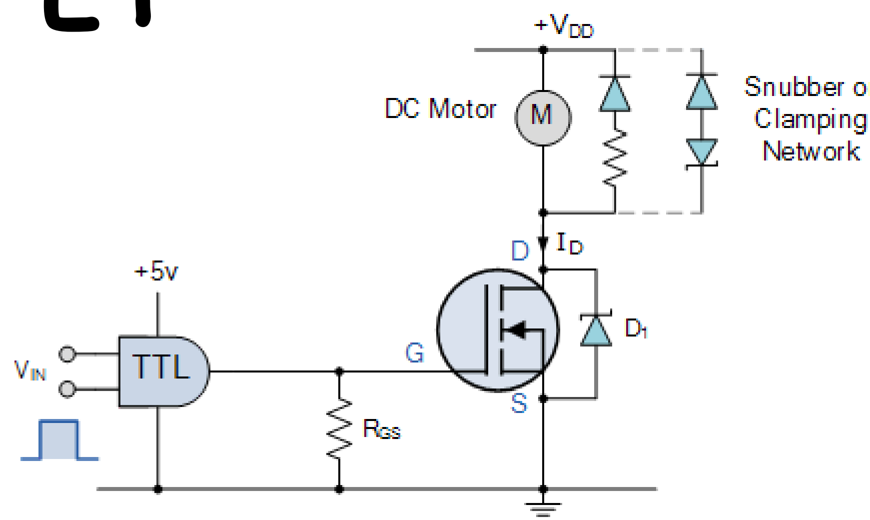
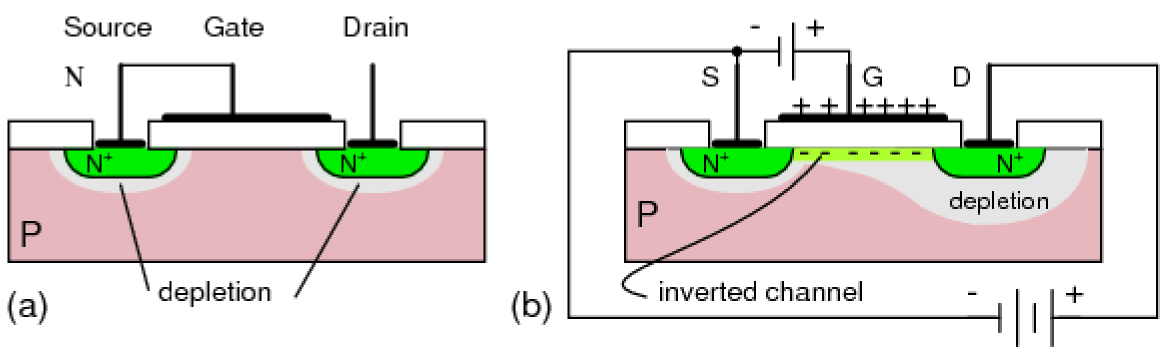
MOSFET




+VDD
DC Motor
M
Snubber or
Clamping
Network
ID
D
+5v
VIN
TTL
G
D1
S
RGS

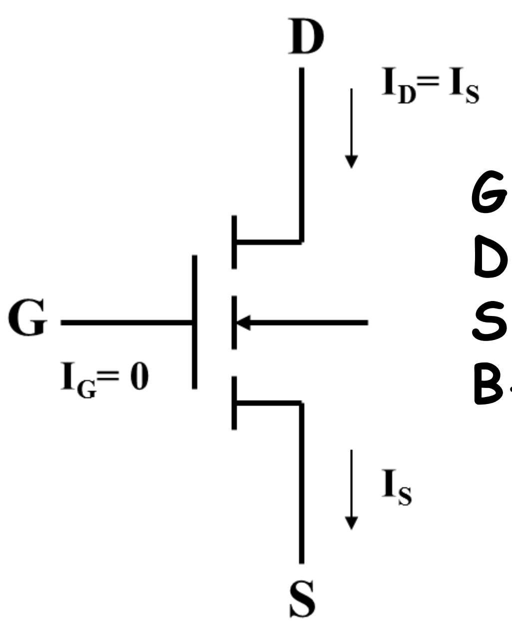

Source
Gate
Drain
N
N+
N+
P
(a)
depletion
-
+
S
G
D
N+
N+
depletion
P
inverted channel
(b)
-
+

MOSFET

MOSFET stands for **metal-oxide semiconductor field-effect transistor**.

Unlike BJT which is '**current controlled**', the MOSFET is a **voltage controlled** device.

The MOSFET has "**gate**", "**Drain**", "**Source**" and "**Body**" terminals.



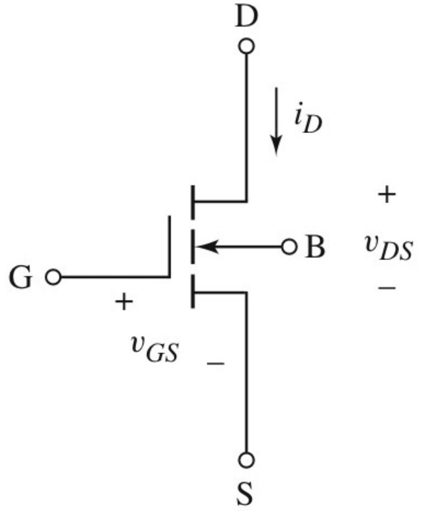
G-Gate
D-Drain
S-Source
B-Substrate or Body

MOSFET

MOSFET – Metal-Oxide-Semiconductor Field Effect Transistor:

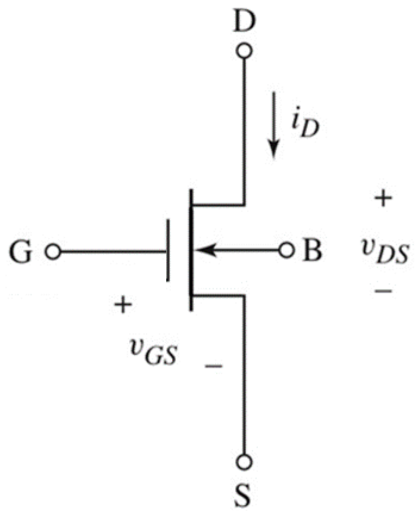
❖ **Enhancement-type:**

- n-channel (NMOS)
- p-channel (PMOS)



❖ **Depletion-type:**

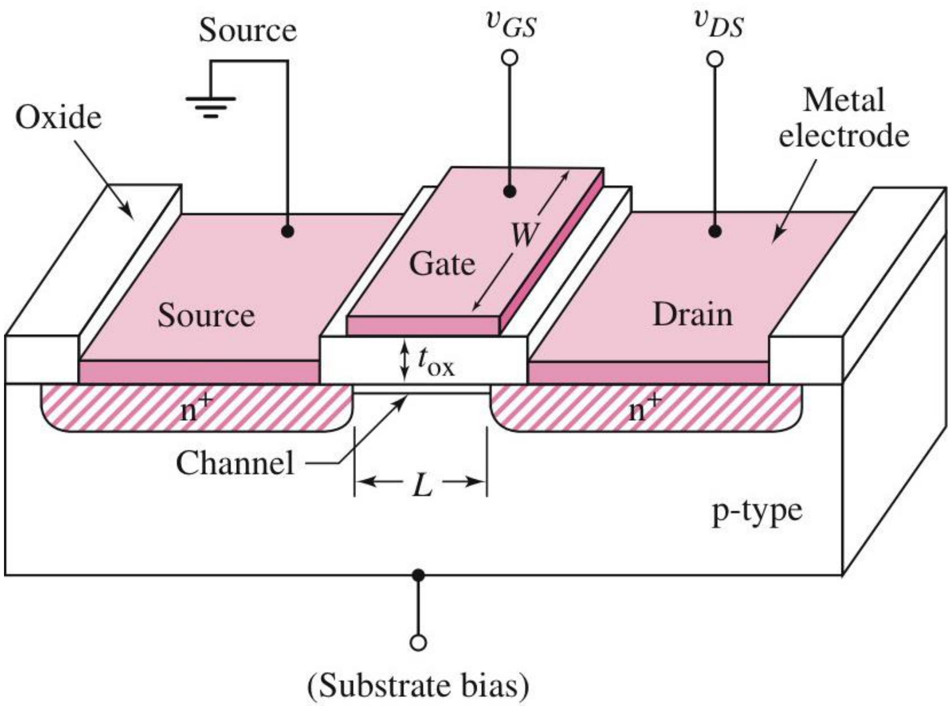
- n-channel
- p-channel



MOSFET n-channel Enhancement-Type

Structure

- p-type substrate
- Two heavily-doped (n^+) regions created in the substrate to form the drain and the source.

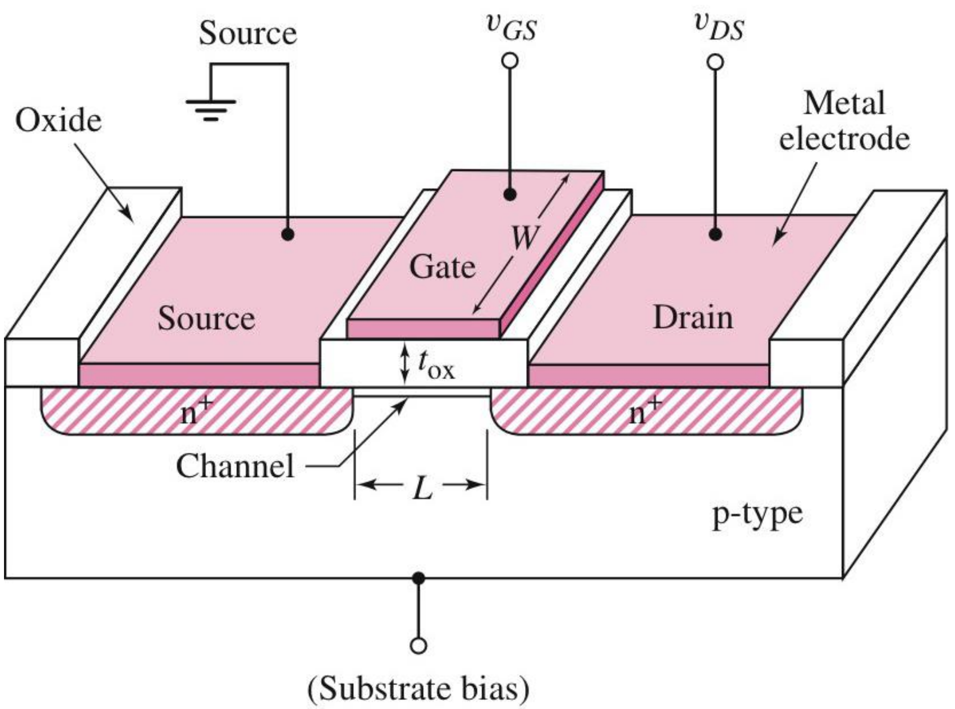


- A thin (0.02 to 0.1 μm) layer of silicon dioxide (SiO_2) is grown on the surface of the substrate covering the area between the source and the drain.

MOSFET — n-channel Enhancement-Type

Structure

- SiO_2 is an excellent insulator.
- Metal is deposited on the top of the SiO_2 layer to form the gate electrode.
- Metal contacts are also made to the source region, drain region and the substrate.

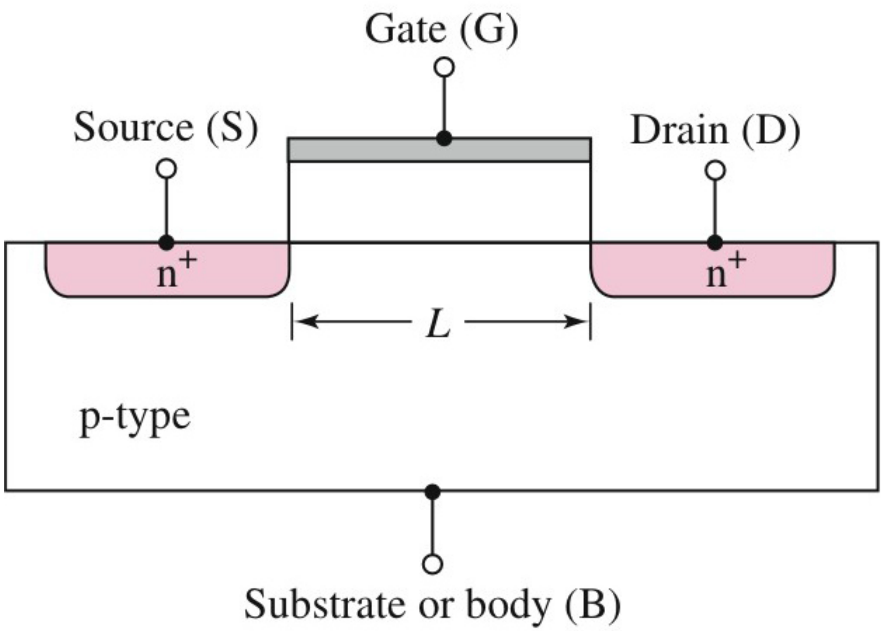


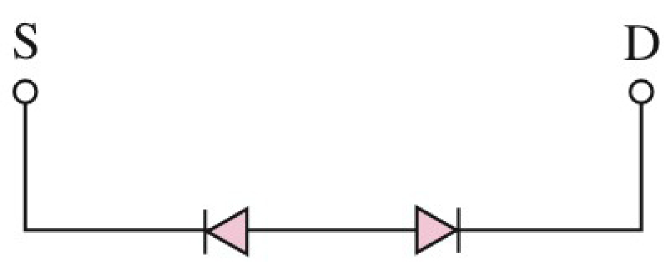
- Terminals are from these metal contacts which form the drain (D), source (S), gate (G) and substrate or body (B) terminals.

MOSFET — n-channel Enhancement-Type

Operation

- **With zero bias** at the gate, the source and the drain are separated by the p-region – equivalent to **two back-to-back diodes.**
- In this condition, the current is zero.

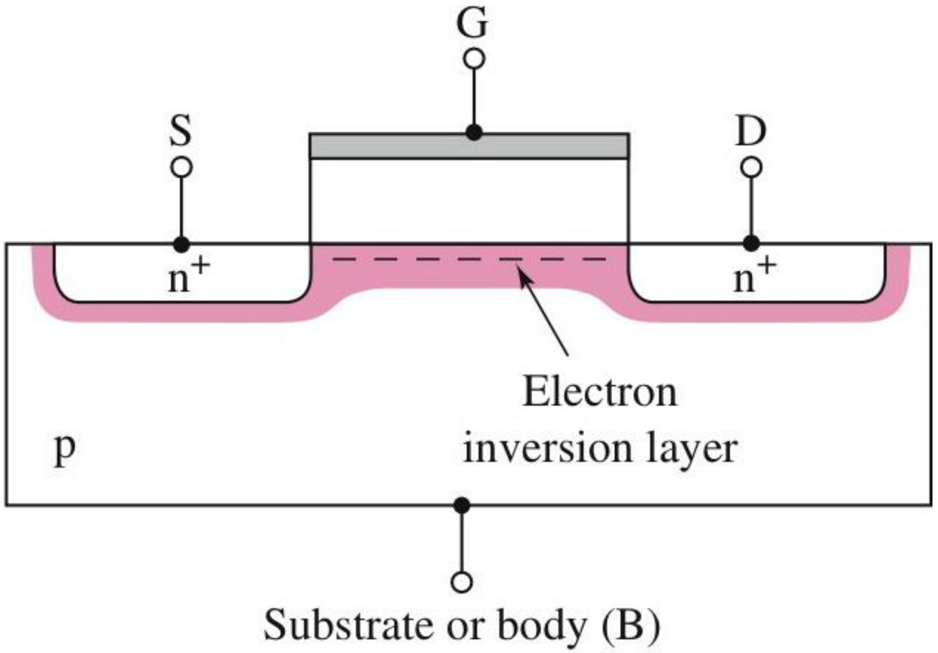




MOSFET n-channel Enhancement-Type

Operation

- *A gate voltage is required to create a conduction path.*

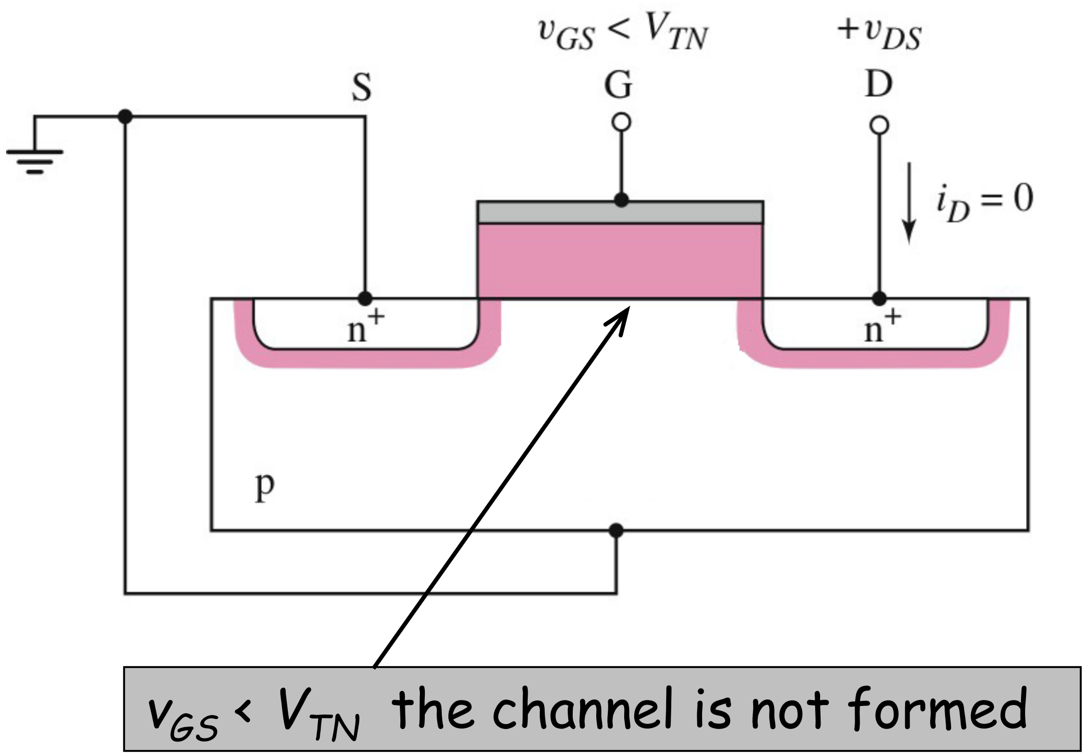


MOSFET n-channel Enhancement-Type

Current-voltage characteristics

- In order to create ***to create a conduction path between drain and source terminals***, the gate-to-source voltage (v_{GS}) must be applied to the gate of the transistor.

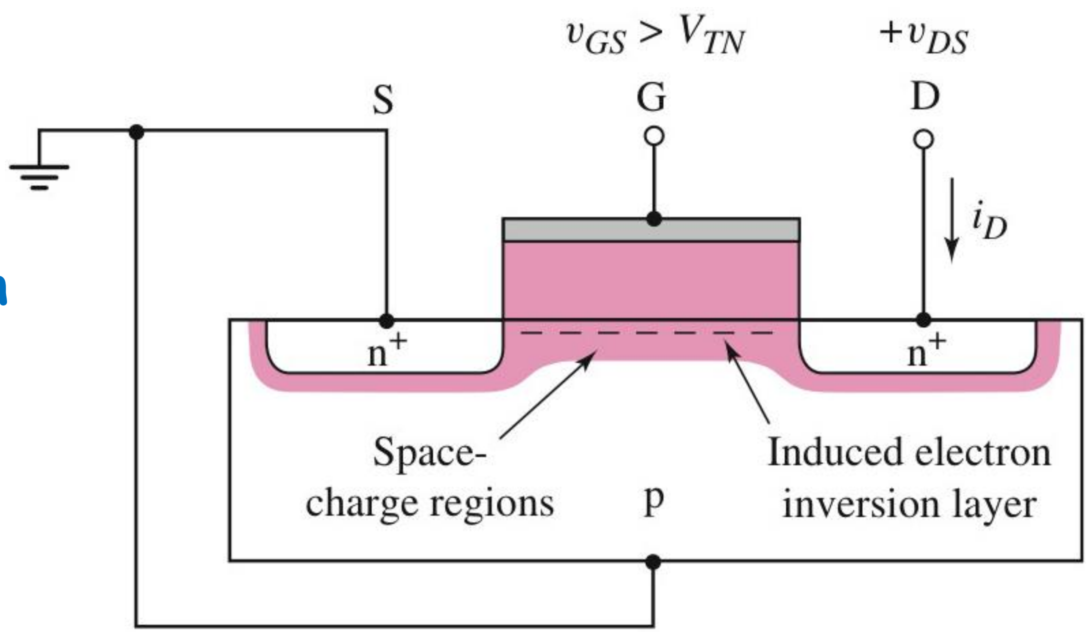
- This voltage must be above a minimum value known as the **threshold voltage (V_{TN})** which is positive for NMOS.



MOSFET n-channel Enhancement-Type

Current-voltage characteristics

- **When v_{GS} exceeds V_{TN},** the channel is formed.
- Current will flow **if a voltage is applied between the drain and the source (v_{DS}).** This current is known as the drain current (i_D)



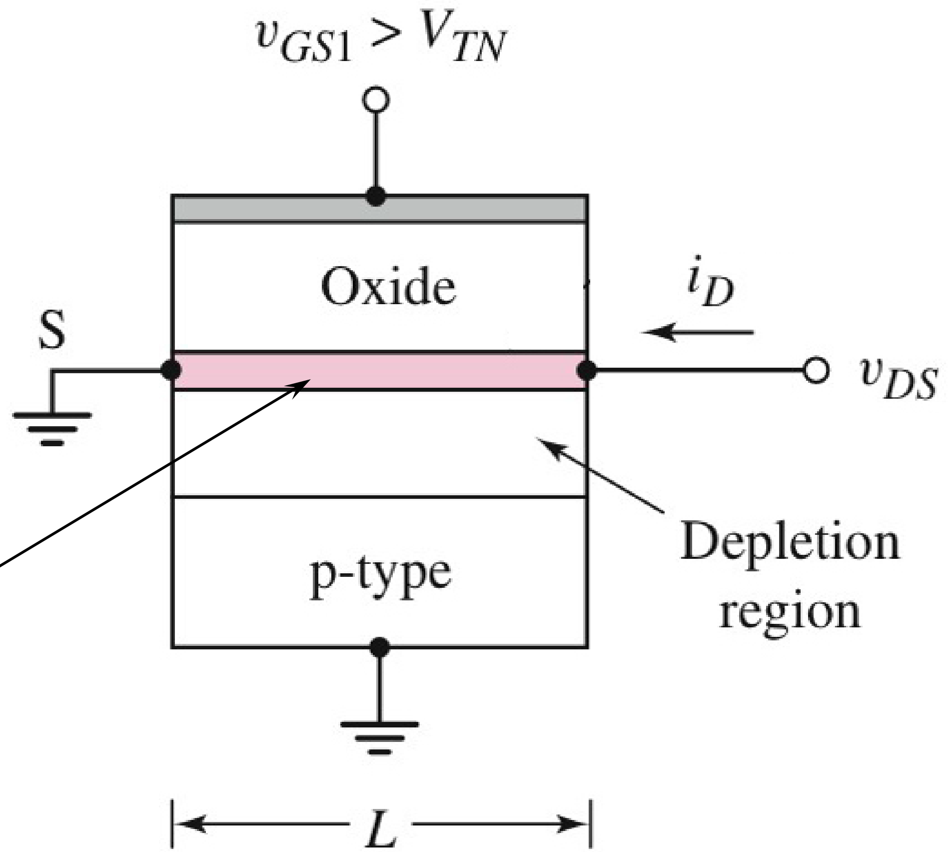
Positive gate bias attracts electrons into channel.

- The carriers in the conduction path are electrons – hence the term **n-channel MOSFET (NMOS).**

MOSFET n-channel Enhancement-Type

Current-voltage characteristics

For small values of v_{DS}, the channel depth is constant over the whole length from the source to the drain.



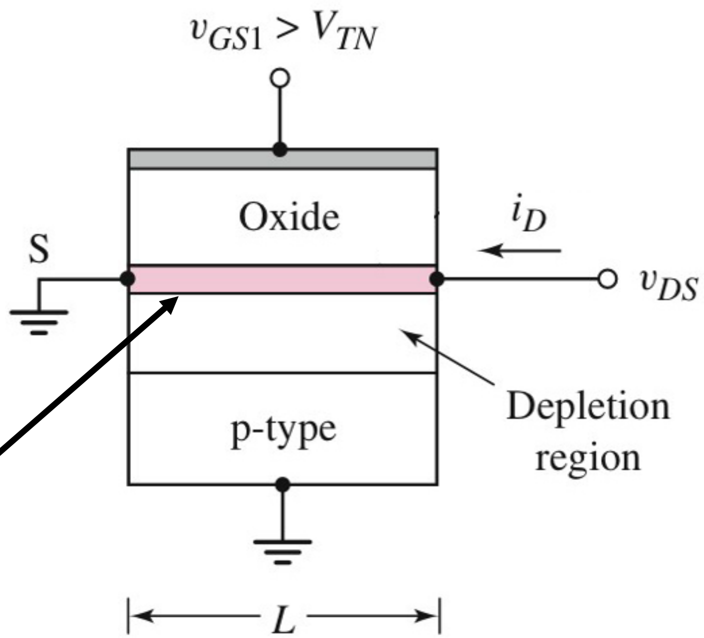
Constant channel depth

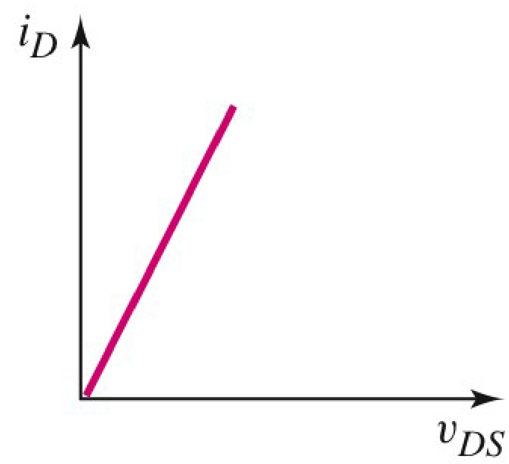
MOSFET n-channel Enhancement-Type

Current-voltage characteristics

The constant channel depth causes the MOSFET to operate as a **linear resistance** (indicated by the linear relationship between i_D and v_{DS}) whose value is controlled by v_{GS}.

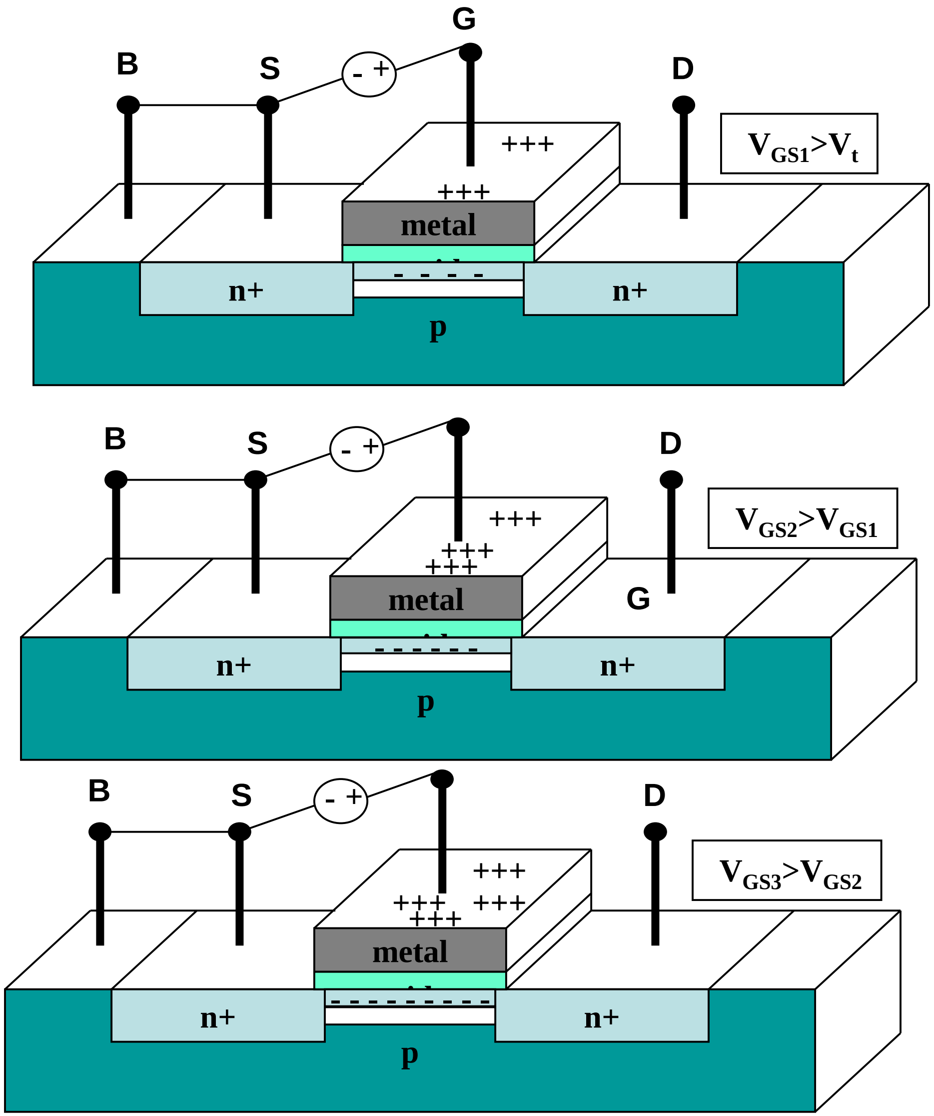
However, i_D is zero for $v_{GS} < V_{TN}$ for any value of v_{DS}.



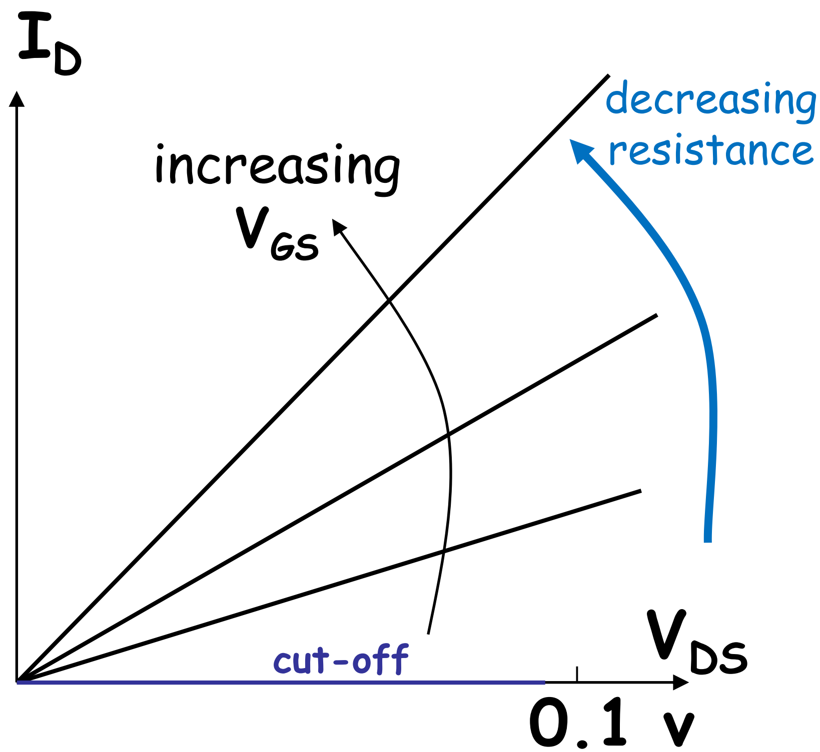


The constant channel depth

A voltage-controlled resistor @small V_{DS} (*Enhancement mode*)



Positive gate bias attracts electrons into channel.



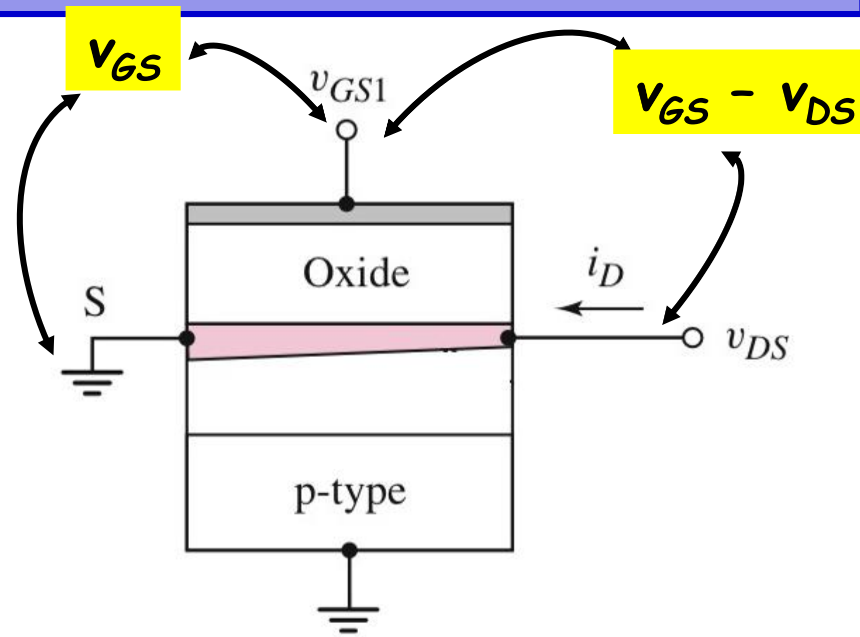
Increasing V_{GS} puts more charge in the channel, allowing more drain current to flow.

MOSFET n-channel Enhancement-Type

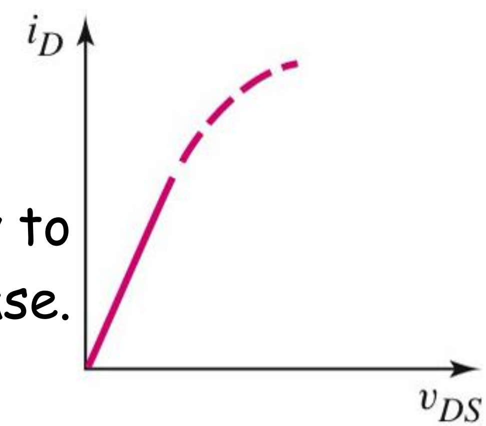
Current-voltage characteristics

As the drain voltage increases, the voltage drop along the channel increases from 0 to v_{DS}.

The voltage between the gate and *the points along the channel* decreases from v_{GS} at the source end to (v_{GS} - v_{DS}) at the channel end, **resulting in a decrease in channel depth** at the drain (Figure).



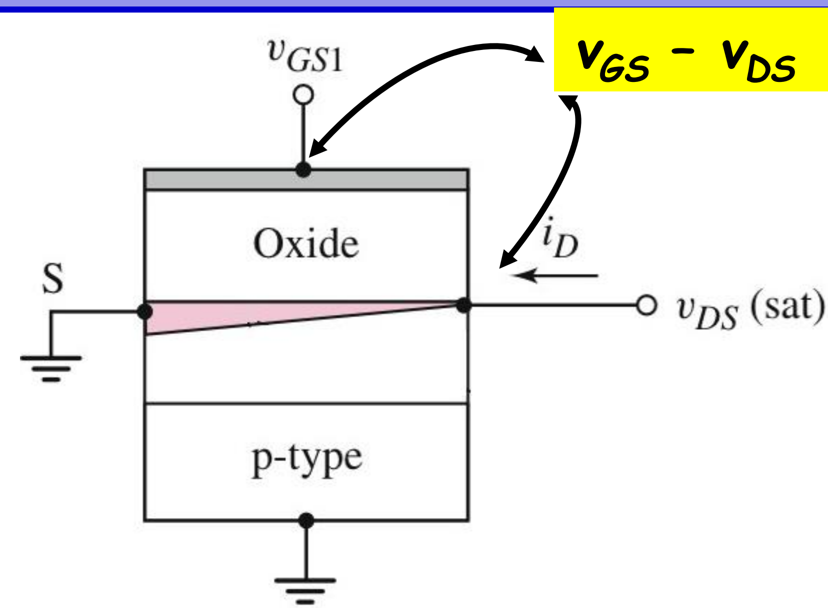
This causes the conductivity to decrease.



MOSFET n-channel Enhancement-Type

Current-voltage characteristics

As the drain voltage increases to the point where $v_{GS} - v_{DS} = V_{TN}$, the channel depth will be zero.

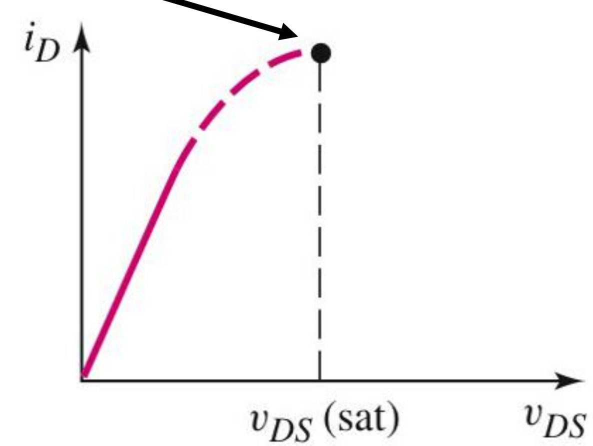


The incremental conductivity is zero and the slope of the i_D versus v_{DS} curve is also zero. At the saturation point;

$$v_{GS} - v_{DS}(\text{sat}) = V_{TN}$$

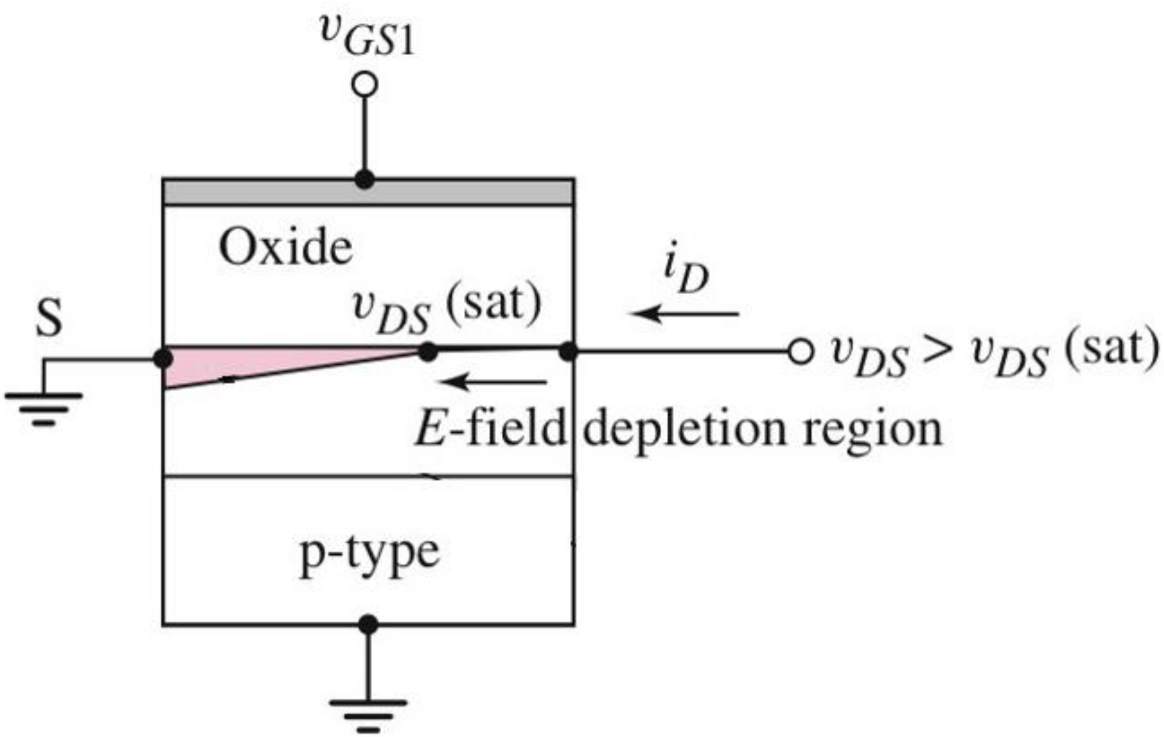
Or;

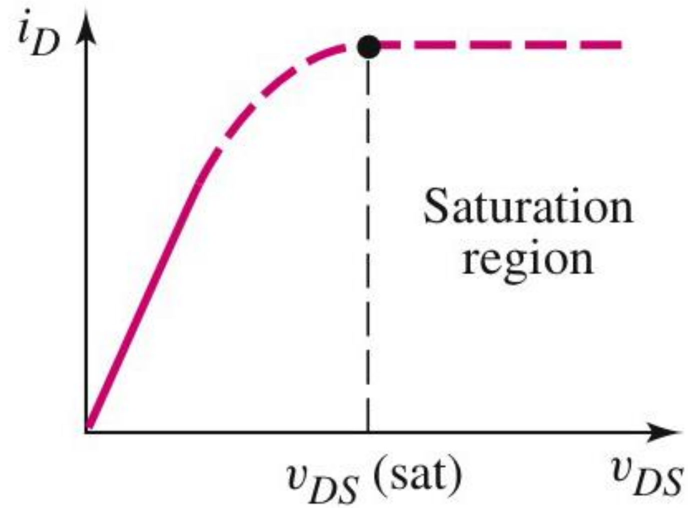
$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$



MOSFET n-channel Enhancement-Type

Current-voltage characteristics





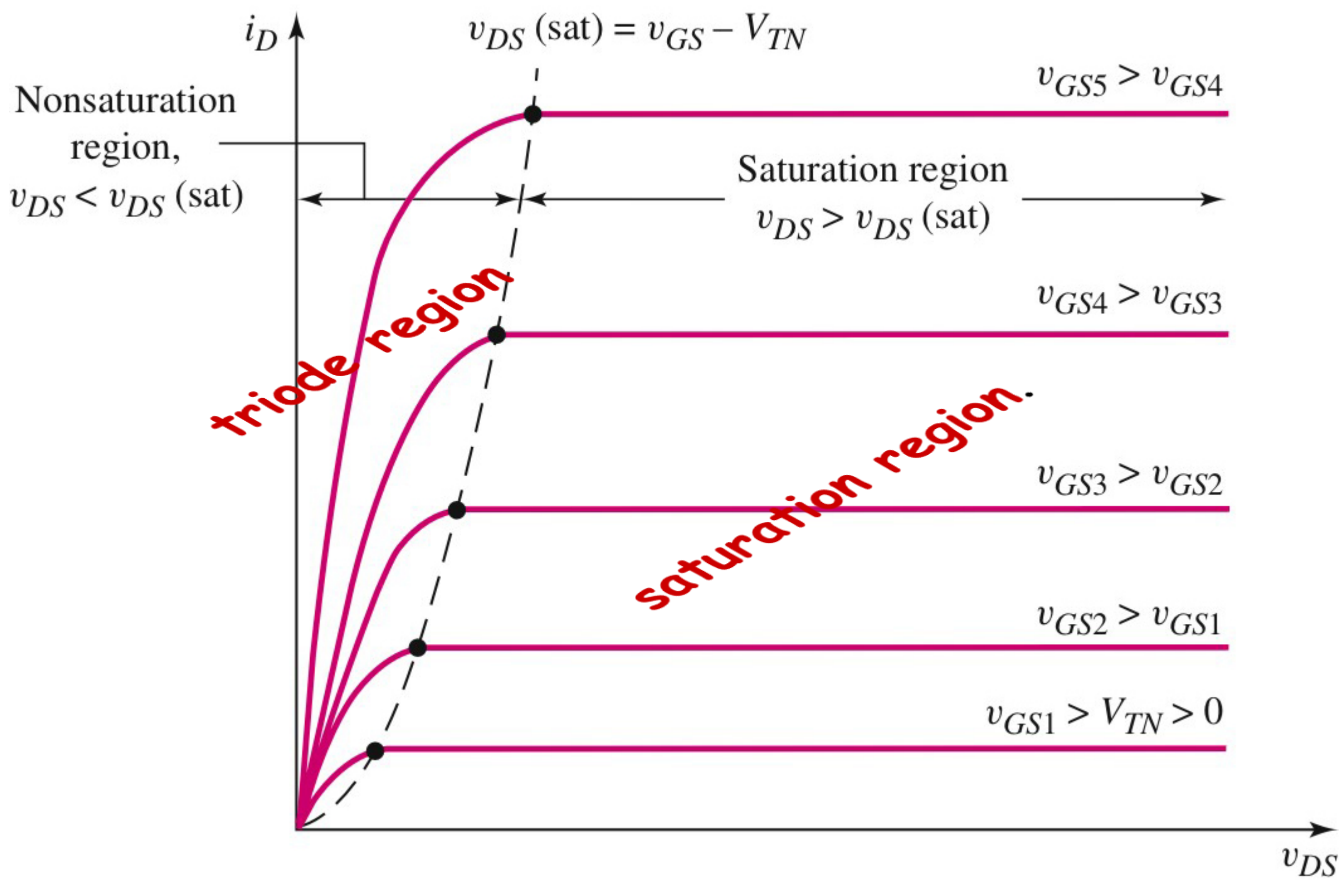
For $v_{DS} > v_{DS}(\text{sat})$, i_D is constant – **saturation region**

$$v_{DS}(\text{sat}) = v_{GS} - V_{TN}$$

MOSFET n-channel Enhancement-Type

Current-voltage characteristics

As the v_{GS} increases, the i_D increases.



MOSFET n-channel Enhancement-Type

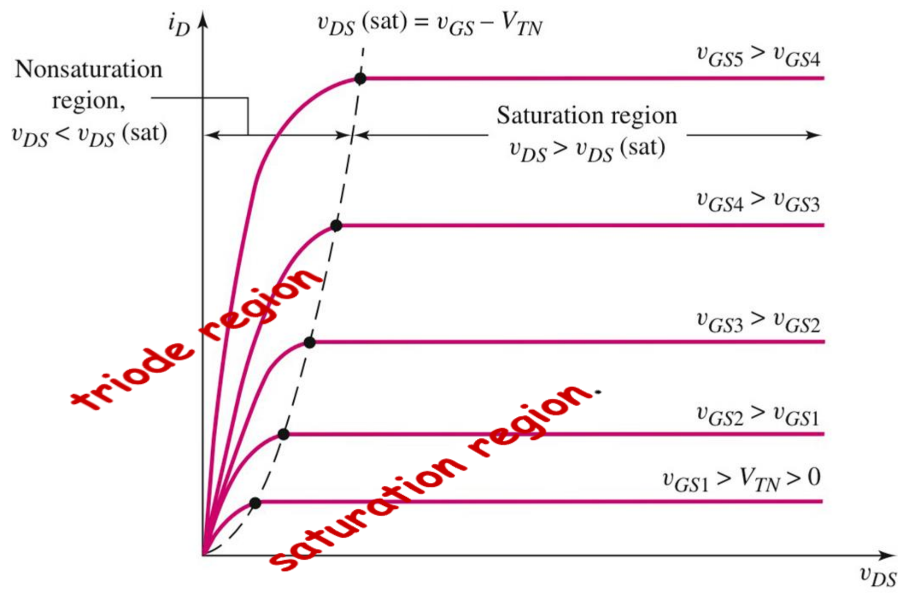
Current-voltage characteristics

The region where $v_{DS} < v_{DS}(sat)$ is known as the **triode region**. For ideal MOSFET, the drain current i_D in this region is given by the expression;

$$i_D = K_n\left[2(v_{GS} - V_{TN})v_{DS} - v_{DS}^2\right]$$

The region where $v_{DS} > v_{DS}(sat)$ is known as the **saturation region**. The drain current i_D in this region is given by the expression;

$$i_D = K_n(v_{GS} - V_{TN})^2$$



MOSFET n-channel Enhancement-Type

Current-voltage characteristics

The parameter K_n is called **conduction parameter** which for NMOS, is given by the expression;

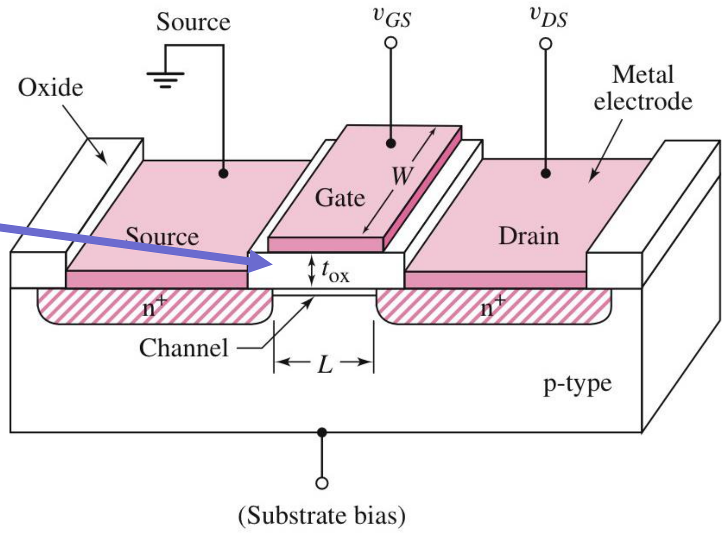
$$K_n = \frac{W\mu_n C_{ox}}{2L}$$

μ_n is the mobility of electrons in the SiO_2 layer and C_{ox} is the oxice capacitance per unit area given by the expression;

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

ε_{ox} = oxide permittivity

t_{ox} = oxide thickness



MOSFET — n-channel Enhancement-Type

Current-voltage characteristics

If we write;

$$k_n^{'} = \mu_n C_{ox}$$

the expression for K_n becomes;

$$K_n = \frac{k_n^{'}}{2} \cdot \frac{W}{L}$$

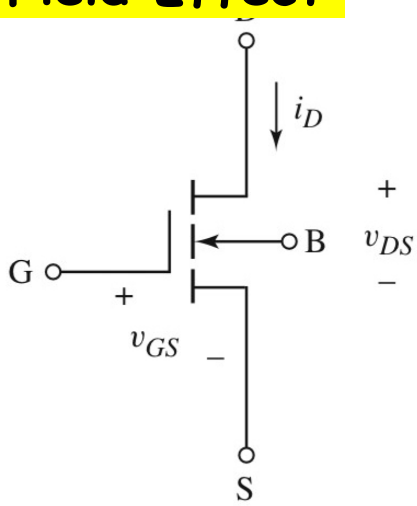
The expression for the drain current in the saturation region becomes;

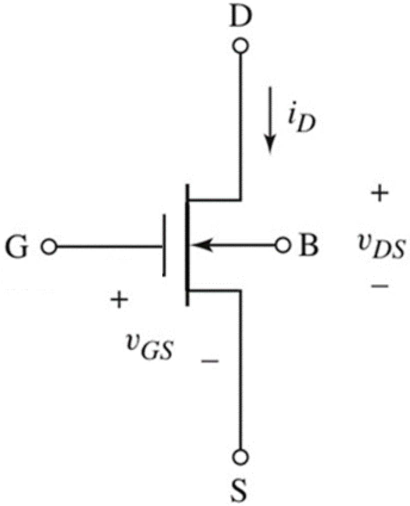
$$i_D = \frac{1}{2} k_n^{'} \frac{W}{L} \left(v_{GS} - V_{TN} \right)^2$$

MOSFET

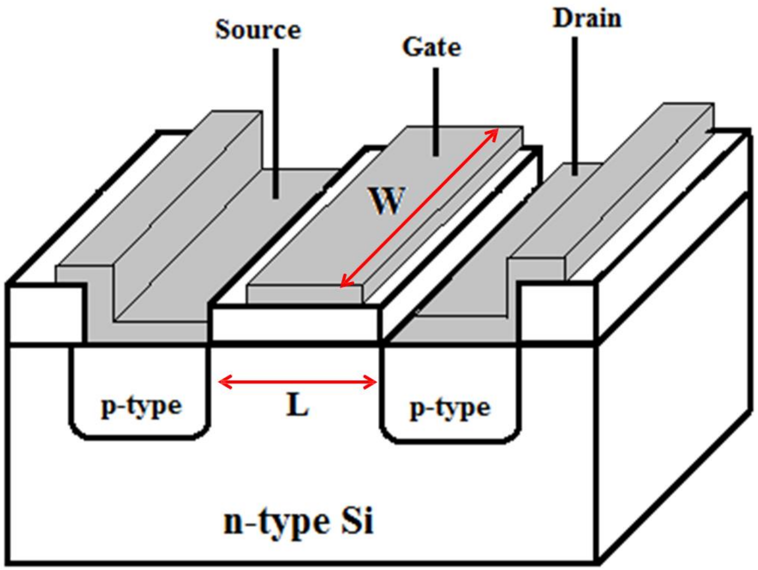
MOSFET – Metal-Oxide-Semiconductor Field Effect Transistor:

- **Enhancement-type:**
  - n-channel (NMOS)
  - p-channel (PMOS)
- **Depletion-type:**
  - n-channel
  - p-channel

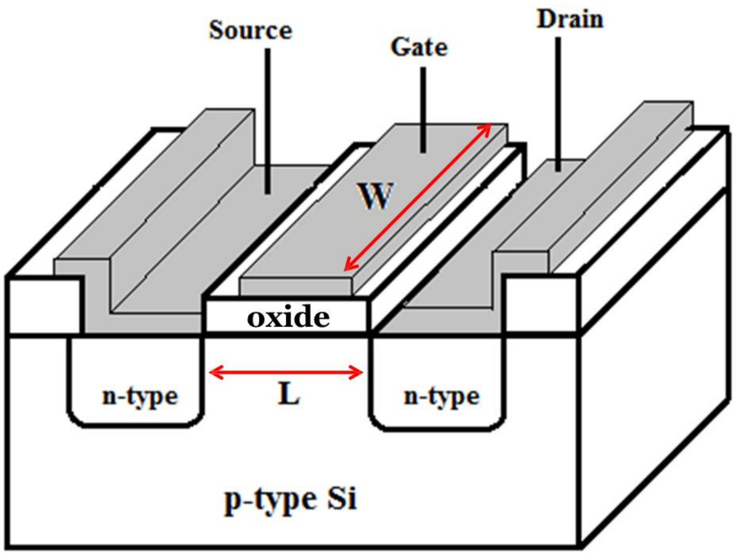




Cross-Sectional View of
<u>p channel Enhancement Mode</u>
Transistor



Cross-Sectional View of
<u>n channel Enhancement Mode</u>
Transistor

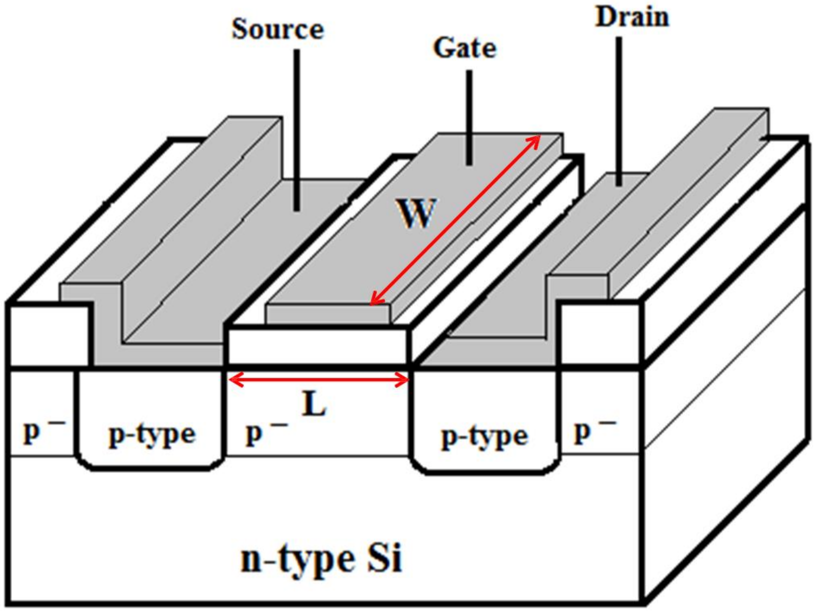


Enhancement mode

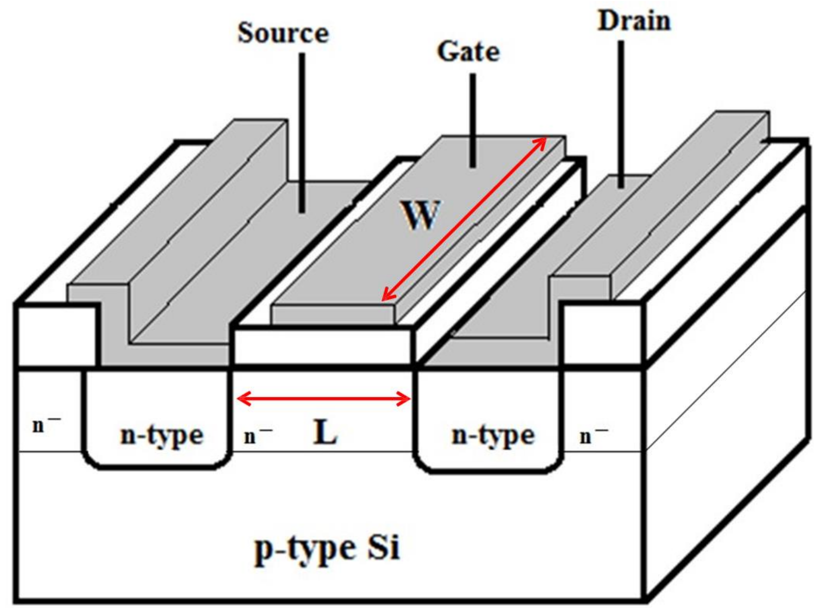
- **Also known as Normally Off transistors.**
  - A voltage (at least equal to the threshold voltage) must be applied to the <u>gate</u> of the transistor

to create a conduction path between the <u>source</u> and the <u>drain</u> of the transistor.

p channel **Depletion** Mode Transistor



n channel **Depletion** Mode Transistor



Depletion mode

- **Also known as Normally On transistors.**
  - In order to prevent current from flowing between the source and drain,
  - a voltage (at least equal to the threshold voltage) must be applied to the gate of the transistor to
  - ***destroy the conduction path between*** the source and the drain.

MOSFET n-channel Enhancement-Type

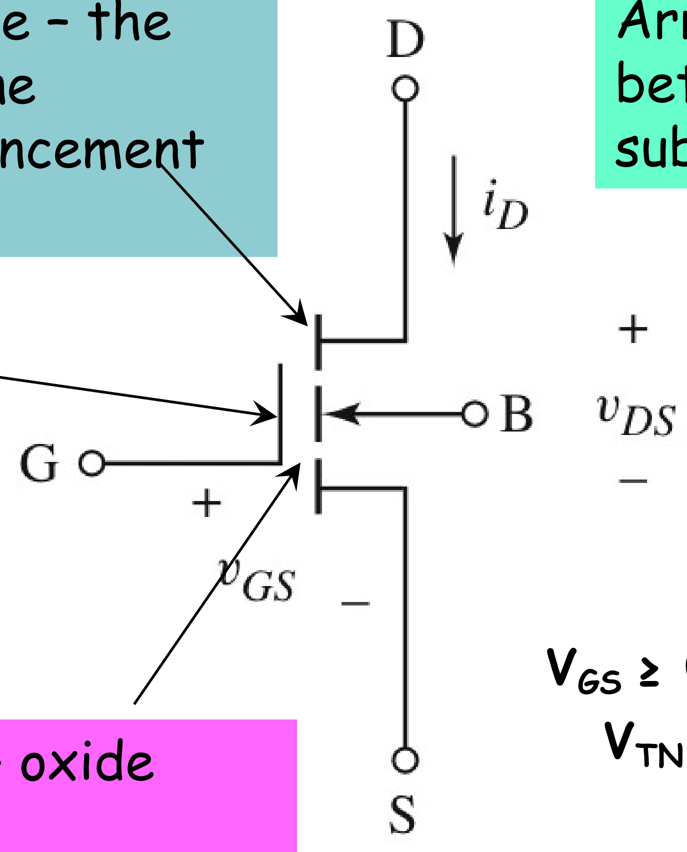
Circuit symbols and Conventions

Conventional symbol

Vertical broken line – the channel (broken line indicates the enhancement type

Arrowhead – polarity between the substrate and channel

Vertical solid line – gate electrode



Separation – oxide layer

$V_{GS} \geq 0V$, $V_{DS} \geq 0V$

V_{TN} is positive

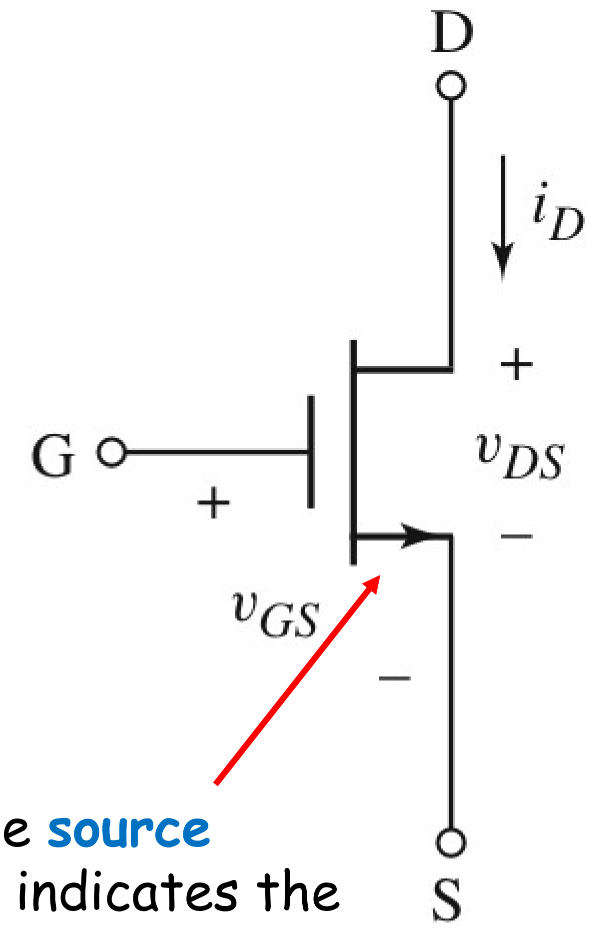
MOSFET n-channel Enhancement-Type

Circuit symbols and Conventions

In many cases, the substrate and source terminals are connected together. The circuit symbol can be simplified.

$V_{GS} \geq 0V$, $V_{DS} \geq 0V$

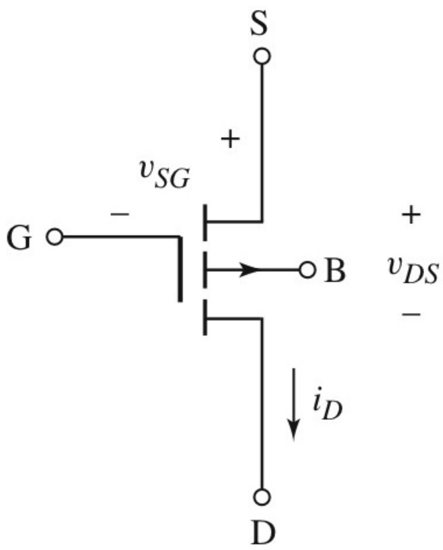
V_{TN} is positive



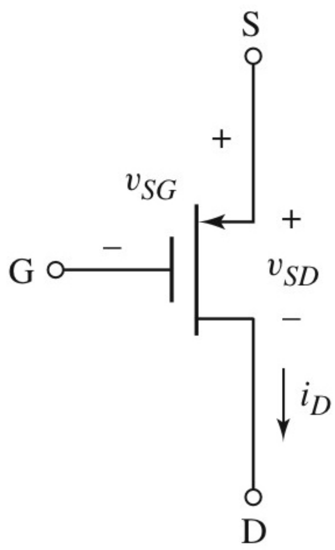
The arrowhead is in the **source terminal** and direction indicates the direction of current.

MOSFET p-channel Enhancement-Type

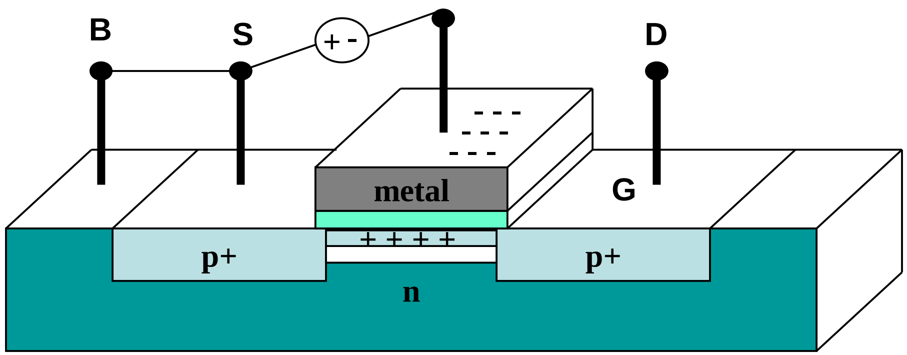
Circuit symbols and Conventions



(a)



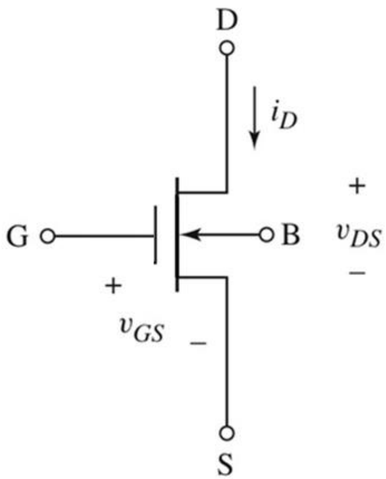
(b)

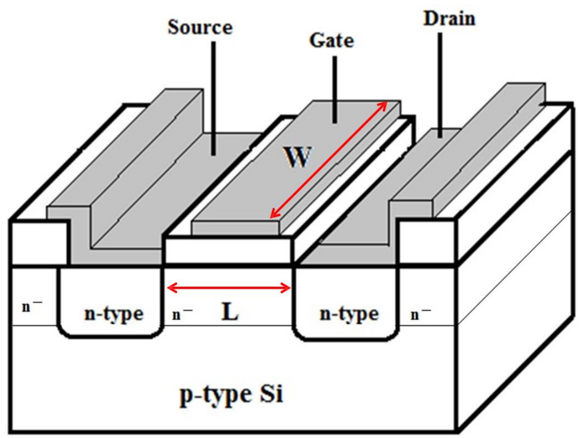


$V_{GS} \leq 0V$, $V_{DS} \leq 0V$

V_{TP} is negative

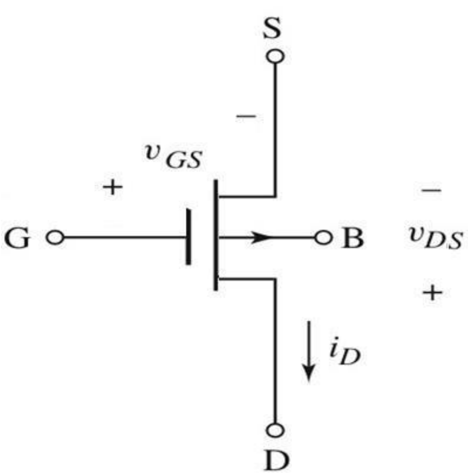
Symbols for n channel Depletion Mode MOSFET





in order to destroy the channel, gate voltage must be negative and less than the threshold voltage

Symbols for p channel Depletion Mode MOSFET



An enhancement MOSFET and a depletion MOSFET are **precisely** identical in **nearly** every way (e.g., same **modes**, same **equations**, same **terminal** names).

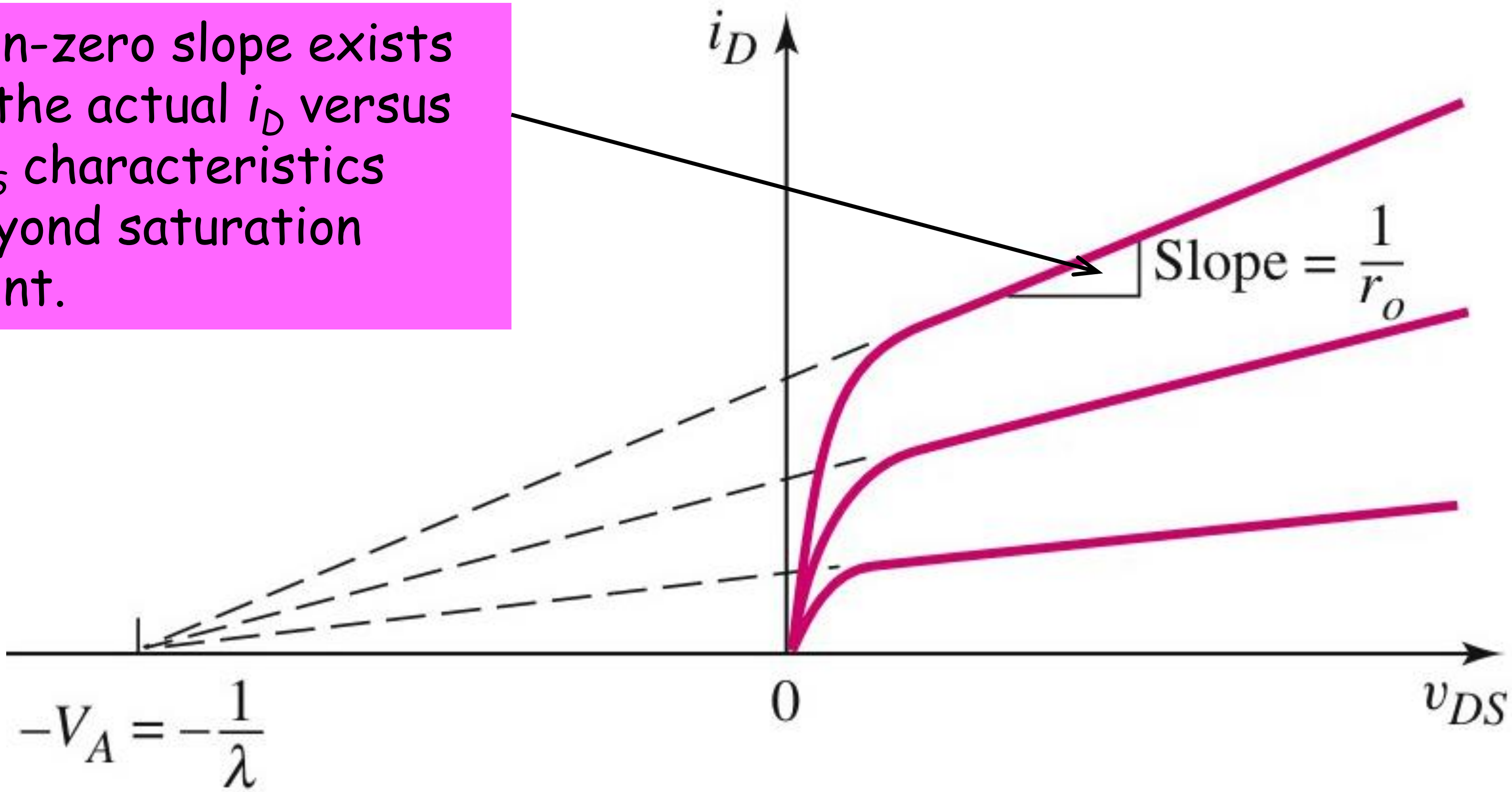
Except: The **threshold voltage** for a depletion **NMOS** device is **negative** (i.e., $V_t < 0$). While the threshold voltage for a depletion **PMOS** device is **positive** (i.e., $V_t > 0$).

MOSFET | n-channel Enhancement-Type

Non-ideal Current-voltage characteristics

The drain current i_D is dependent on the drain-to-source voltage v_{DS} due to **channel length modulation**.

Non-zero slope exists in the actual i_D versus v_{DS} characteristics beyond saturation point.

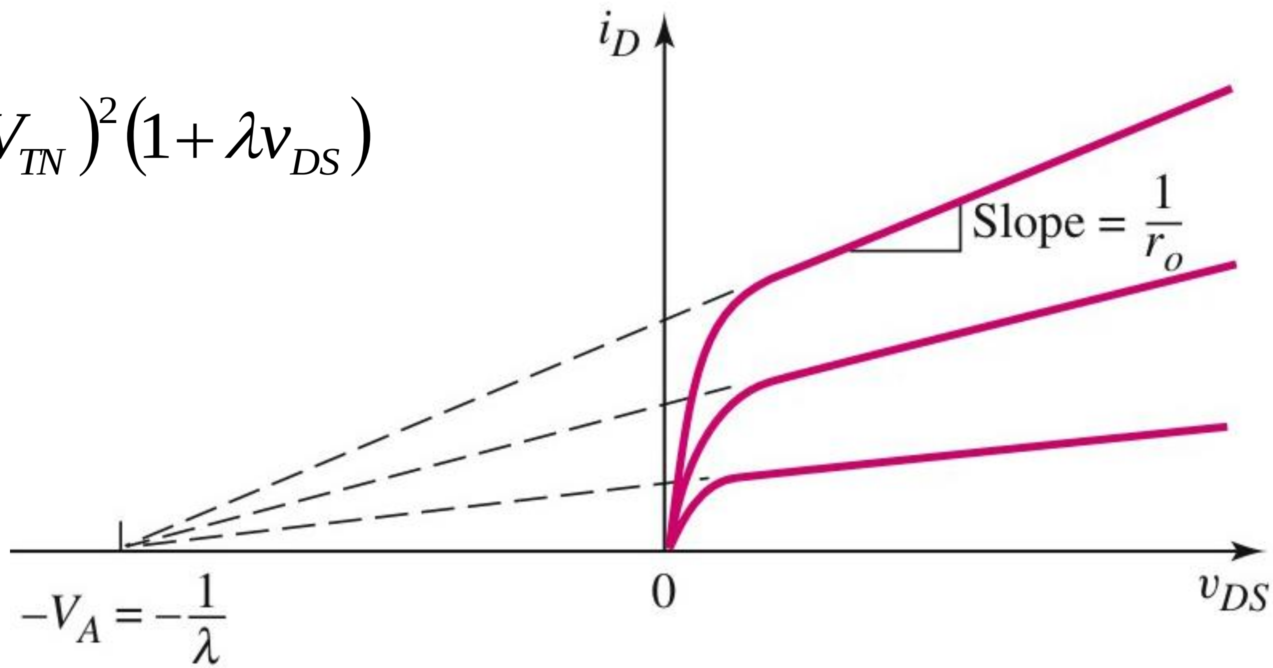


MOSFET n-channel Enhancement-Type

Non-ideal Current-voltage characteristics

In the saturation region, the drain current may expressed as;

$$i_D = K_n \left(v_{GS} - V_{TN}\right)^2 \left(1 + \lambda v_{DS}\right)$$

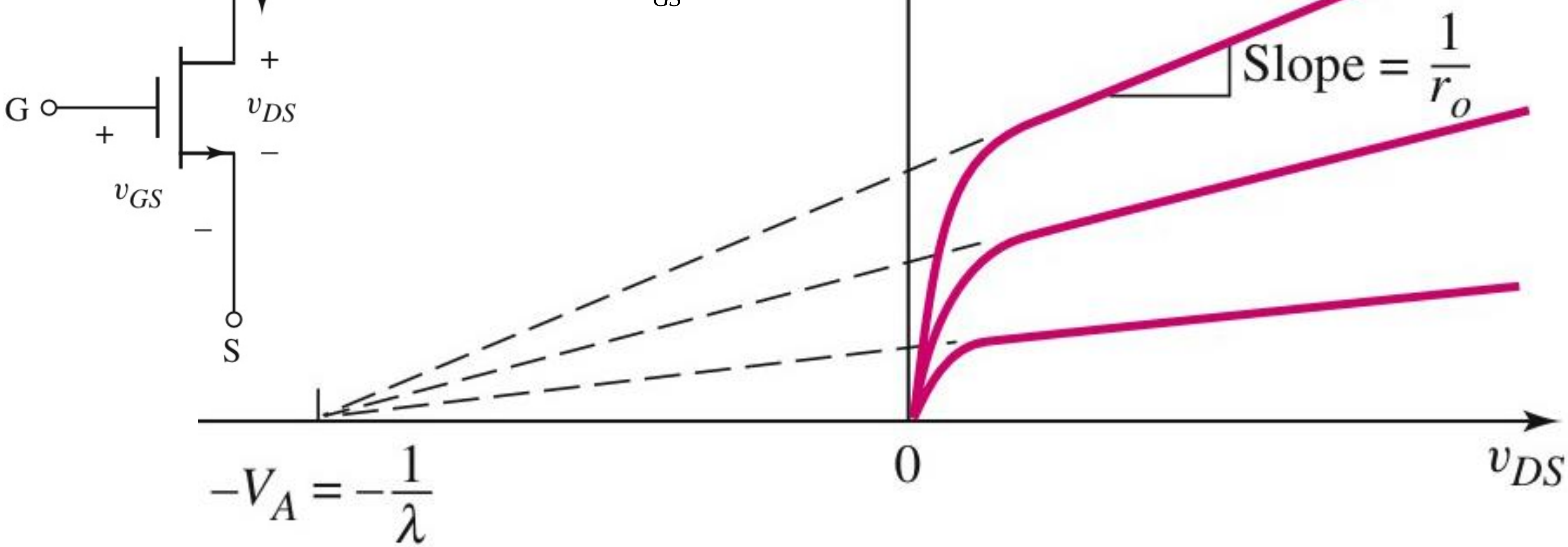


MOSFET n-channel Enhancement-Type

Non-ideal Current-voltage characteristics

The output resistance r_o is the inverse of the slope of the characteristics curves;

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Bigg|_{v_{GS} = \text{const}}$$



MOSFET n-channel Enhancement-Type

Non-ideal Current-voltage characteristics

Differentiating the expression for i_{DS} at the Q-point, gives us;

$$r_o = \left(\frac{\partial i_D}{\partial v_{DS}} \right)^{-1} \Bigg|_{v_{GS} = \text{const}} \qquad i_D = K_n (v_{GS} - V_{TN})^2 (1 + \lambda v_{DS})$$

$$r_o = \left[\lambda K_n (V_{GSQ} - V_{TN})^2 \right]^{-1}$$

or

$$r_o \cong \left[\lambda I_{DQ} \right]^{-1} = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$$