Faculty of Computer and Informatics Engineering

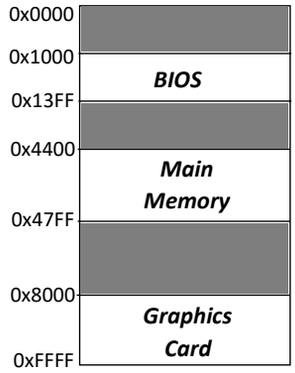
C

BLG 212E
Microprocessor Systems
10.10.2022

Quiz #1

1. The following questions are according to the memory map given on the side.
   a) Draw the chip select input of *BIOS*, *Main Memory*, and *Graphics Card* separately using the NAND circuit.

   b) Fill the following table according to the address input in which the chip selection area will be enabled or disabled.



Address Input	$\overline{CS_{BIOS}}$	$\overline{CS_{Memory}}$	$\overline{CS_{Graphics}}$
0x1023	0	1	1
0xC4B7	1	1	0
0x453F	1	0	1
0x6B20	1	1	1

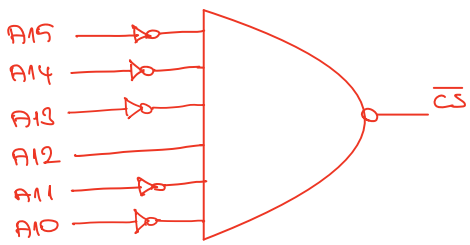
2. Build a memory that spans between $B000 and $EFFF with 4Kx8 memory chips for a CPU with 8-bit data bus and 16-bit address bus.
   a) Calculate the memory address range for all chips.
   b) How many 4K chips are needed?
   c) Draw the memory design by showing all necessary connections. (Address bus, Data bus, Chip select signals). Use an address decoder (determine its type) and logic gates (determine their types). Assume the decoder select signal and the memory chip select signals are active high.

Duration: 40 minutes

(1)

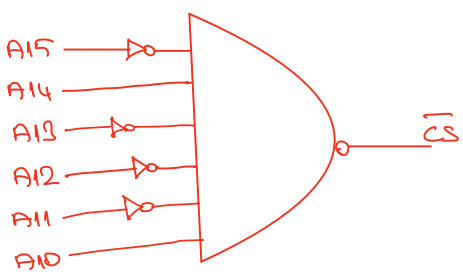
a) BIOS

0x1000 ⇒ 0001 0000 0000 0000
0x13FF ⇒ 0001 0011 1111 1111



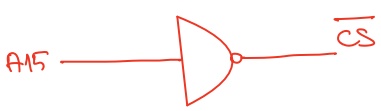
MAIN MEMORY

0x4400 ⇒ 0100 0100 0000 0000
0x47FF ⇒ 0100 0111 1111 1111



GRAPHICS CARD

0x8000 ⇒ 1000 0000 0000 0000
0xFFFF ⇒ 1111 1111 1111 1111



② a)

$B000	⇒	1011	0000	0000 0000
$BFFF		1011	1111	1111 1111
$C000	⇒	1100	0000	0000 0000
$CFFF		1100	1111	1111 1111
$D000	⇒	1101	0000	0000 0000
$DFFF		1101	1111	1111 1111
$E000	⇒	1110	0000	0000 0000
$EFFF		1110	1111	1111 1111

b) 4

c)