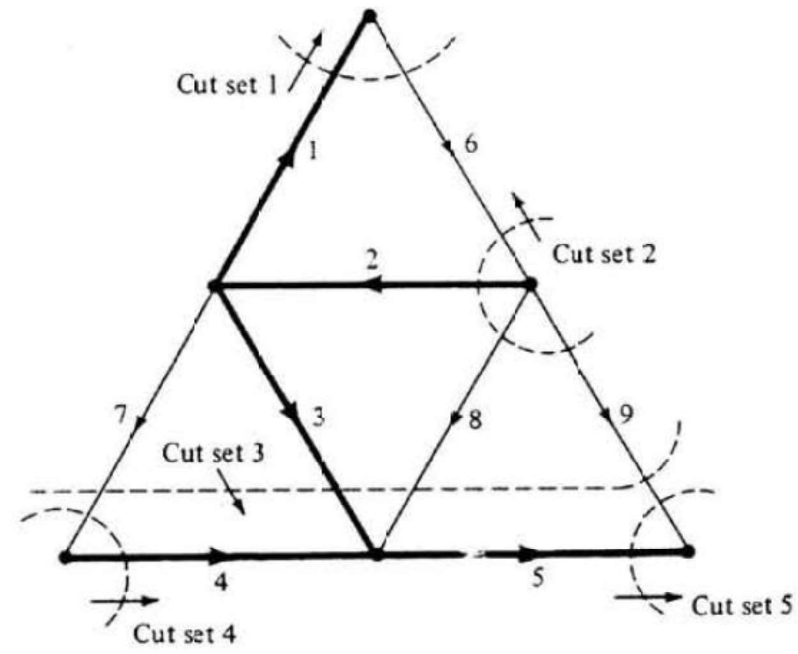
# KCL Equations Using Link Currents

- Let the link currents be: $i_{\ell 1}, i_{\ell 2}, i_{\ell 3}, i_{\ell 4}$ (4 links)
- Four link branches identify as:

$i_6 = i_{\ell 1}, i_7 = i_{\ell 2}, i_8 = i_{\ell 3}, i_9 = i_{\ell 4}$

- Determine the fundamental cut sets




Cut set 1: $\{1,6\}$ Cut set 2: $\{2,6,8,9\}$ Cut set 3: $\{3,7,8,9\}$

Cut set 4: $\{4,7\}$ Cut set 5: $\{5,9\}$

Cut set 1: $i_1 - i_6 = 0 \Rightarrow i_1 = i_6 = i_{\ell 1}$

Cut set 2: $i_2 - i_6 + i_8 + i_9 = 0 \Rightarrow i_2 = i_6 - i_8 - i_9$

$\Rightarrow i_2 = i_{\ell 1} - i_{\ell 3} - i_{\ell 4}$

Cut set 3: $i_3 + i_7 + i_8 + i_9 = 0 \Rightarrow i_3 = -i_7 - i_8 - i_9$

$\Rightarrow i_3 = -i_{\ell 2} - i_{\ell 3} - i_{\ell 4}$

Cut set 4: $i_4 - i_7 = 0 \Rightarrow i_4 = i_7 = i_{\ell 2}$

Cut set 5: $i_5 + i_9 = 0 \Rightarrow i_5 = -i_9 = -i_{\ell 4}$

**Recall:**
Cut set is a way to isolate node or nodes from the circuit. For fundamental cut set, consider one branch and some links one at a time

Direction of current is chosen w.r.t the reference direction of cut set

# KCL Equations Using Link Currents

$$\left.\begin{array}{ll} i_1 = i_{\ell 1} & i_6 = i_{\ell 1} \\ i_2 = i_{\ell 1} - i_{\ell 3} - i_{\ell 4} & i_7 = i_{\ell 2} \\ i_3 = -i_{\ell 2} - i_{\ell 3} - i_{\ell 4} & i_8 = i_{\ell 3} \\ i_4 = i_{\ell 2} & i_9 = i_{\ell 4} \\ i_5 = -i_{\ell 4} & \end{array}\right\}$$

- Equations can be written in matrix form as:

$$\begin{bmatrix} i_1 \\ i_2 \\ \vdots \\ i_9 \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & 0 & 0 & 0 \\ 1 & 0 & -1 & -1 \\ 0 & -1 & -1 & -1 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}}_{\ell} \begin{bmatrix} i_{\ell 1} \\ i_{\ell 2} \\ i_{\ell 3} \\ i_{\ell 4} \end{bmatrix} \Rightarrow \quad i = B^T i_\ell$$

$i_\ell$: link current vector
$B^T$:transpose of the fundamental loop matrix

# Graph Theory—Chord Current Method

- Linear circuits containing two-terminal resistors and independent sources, use the following steps:
  1. Pick a proper tree of the graph of the circuit which includes all voltage sources. Current sources are placed in co-trees
  2. Write the fundamental loop equations which do not correspond to the current sources in co-trees
  3. Write the $v - i$ relations of the resistors in the form of $v_k = R_k i_k$
  4. Substitute voltages in step 3 into step 2
  5. Write the fundamental cut-set equations which do not correspond to the voltage sources
  6. Substitute the fundamental loop equations in step 4 into the equations in step 5
  7. Present the equation in the following form:

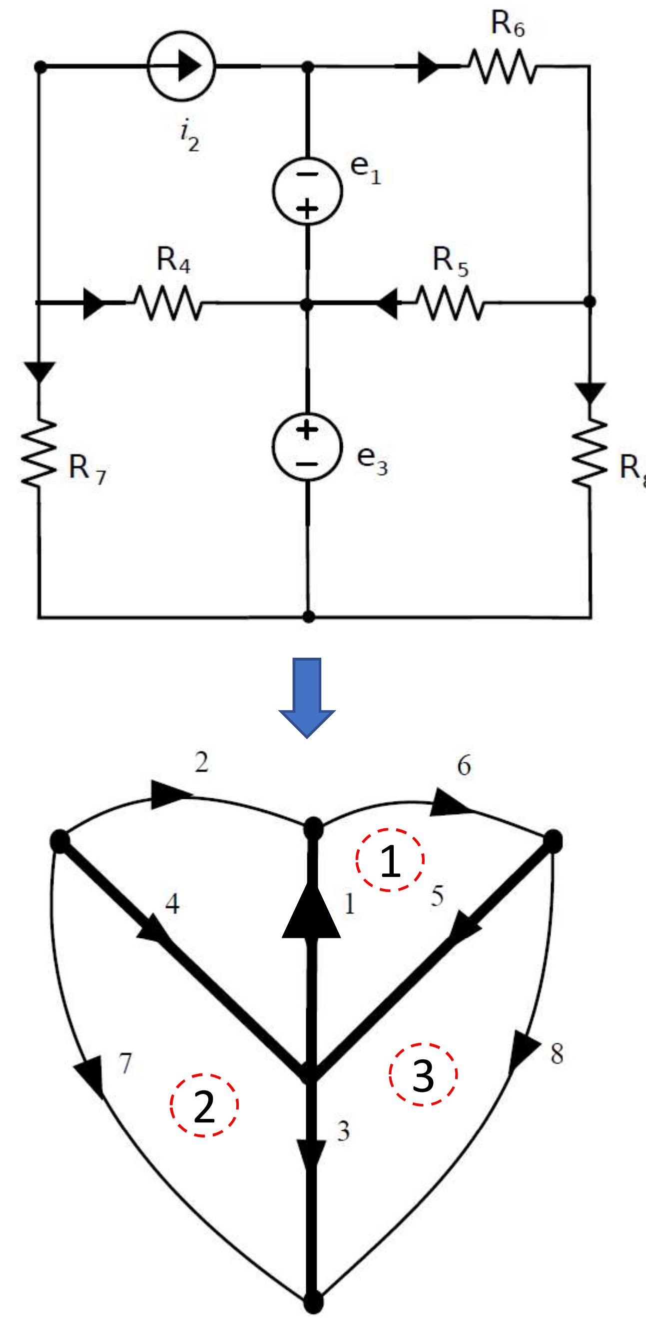
$$B i_{\ell'} + Q i_S + M v_S$$

$B$: Fundamental loop matrix
$i_{\ell'}$: link current vector
$Q$: Fundamental cut-set matrix
$i_S$: current source vector
$M$: Transpose of reduced incidence matrix
$v_S$: Voltage source vector

The rest of the slides are based on Müstak E. Yalçın's notes

# Example 1

1. Pick (draw) a proper tree of the circuit. All voltage sources will be on the tree and current source will be on the co-tree (link). Note: $i_6, i_7, i_8$ are unknows




Solid thick line: twig
Solid thin line: link

Direction of voltage source is chosen from + to -

Tree can be written as:

$$T = \{1,3,4,5\}$$

2. Write the fundamental loop equations which do not correspond to the current source in the co-tree.
   - In order to write the fundamental loop equation, the fundamental loops must be determined
   - 3 fundamental loops indicated by dashed red circles. Direction of loop is chosen based on the reference direction of the link

Fundamental loop equations:

Loop 1: $v_6 + v_5 + v_1 = 0$

Loop 2: $v_7 - v_3 - v_4 = 0$

Loop 3: $v_8 - v_3 - v_5 = 0$

**Recall:**
Fundamental loop contains only one link and some twigs. By definition, do not include the loop that contains current source

# Solution

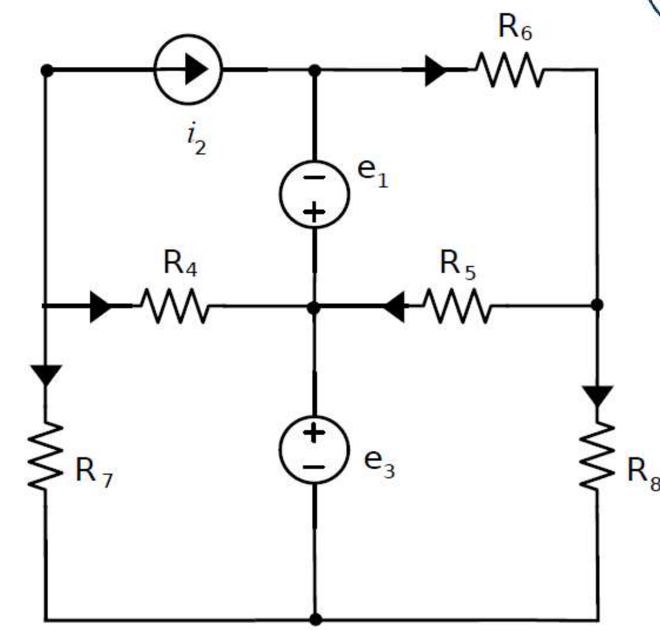
3. Write $v - i$ relations of the resistors: $v = iR$ (Ohm's law)

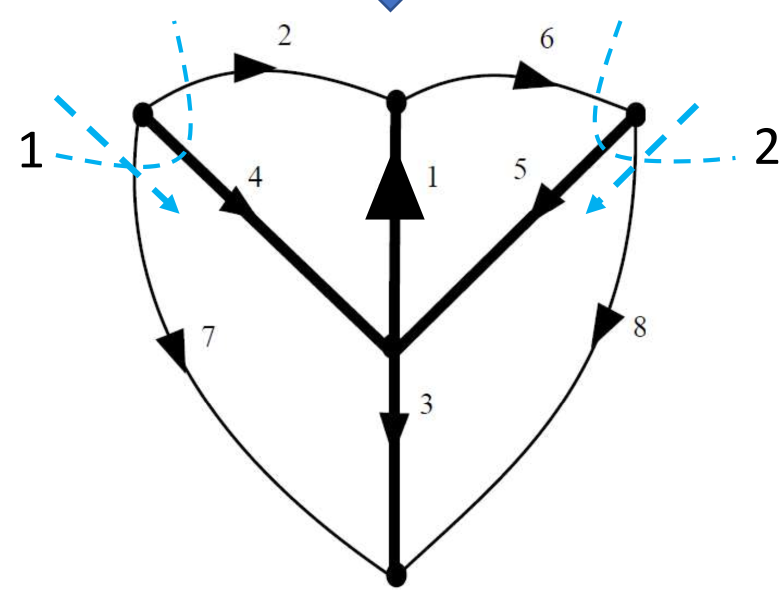
$$v_8 = R_8 i_8, \quad v_7 = R_7 i_7, \quad v_6 = R_6 i_6, \quad v_5 = R_5 i_5, \quad v_4 = R_4 i_4$$

4. Substitute voltages into the equations in step 2

$$\begin{aligned} v_6 + v_5 + v_1 &= 0 \\ v_7 - v_3 - v_4 &= 0 \\ v_8 - v_3 - v_5 &= 0 \end{aligned} \Rightarrow \begin{aligned} R_6 i_6 + R_5 i_5 + v_1 &= 0 \\ R_7 i_7 - v_3 - R_4 i_4 &= 0 \\ R_8 i_8 - v_3 - R_5 i_5 &= 0 \end{aligned}$$

5. Write the fundamental cut-set equations which do not correspond to the voltage sources
   - In order to write the fundamental cut-set equation, the fundamental cut-set of a tree must be determined
   - 2 fundamental cut-sets indicated by dashed blue lines. Direction of cut-sets is defined by the direction of the twig.




**Recall:**
Cut-set is partition of node (or vertex) of graph into two disjoint subset.
For fundamental cut-set, consider one tree branch with some links one at a time (do not intersect two or more branches at the same time).
Cut-set orientation (direction) is defined by the direction of twig.

# Solution

- Fundamental cut-set equations:

$$i_2 + i_4 + i_7 = 0 \Rightarrow i_4 = -i_2 - i_7$$
$$i_5 + i_8 - i_6 = 0 \Rightarrow i_5 = i_6 - i_8$$

6. Substitute currents into the equations in step 4

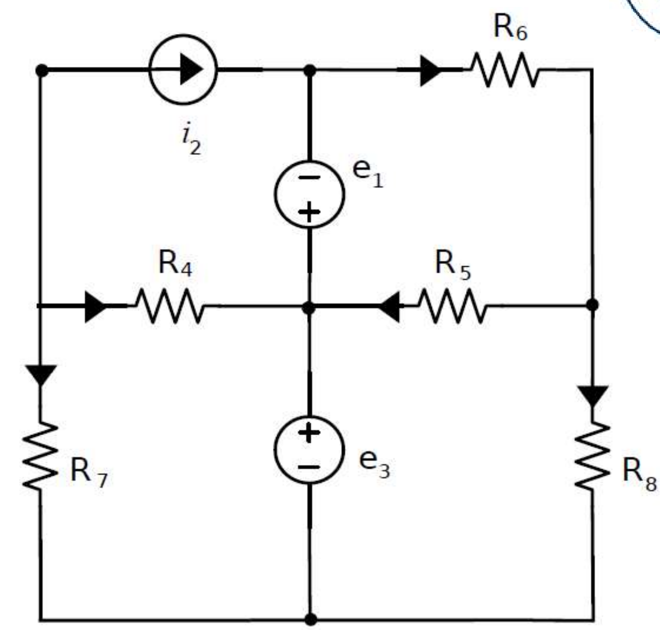
$$\left.\begin{aligned} R_6 i_6 + R_5(i_6 - i_8) + v_1 &= 0 \\ R_7 i_7 - R_4(-i_2 - i_7) - v_3 &= 0 \\ R_8 i_8 - R_5(i_6 - i_8) - v_3 &= 0 \end{aligned}\right\} \begin{aligned} (R_5 + R_6)i_6 - R_5 i_8 + v_1 &= 0 \\ (R_4 + R_7)i_7 + R_4 i_2 - v_3 &= 0 \\ (R_5 + R_8)i_8 - R_5 i_6 - v_3 &= 0 \end{aligned}$$

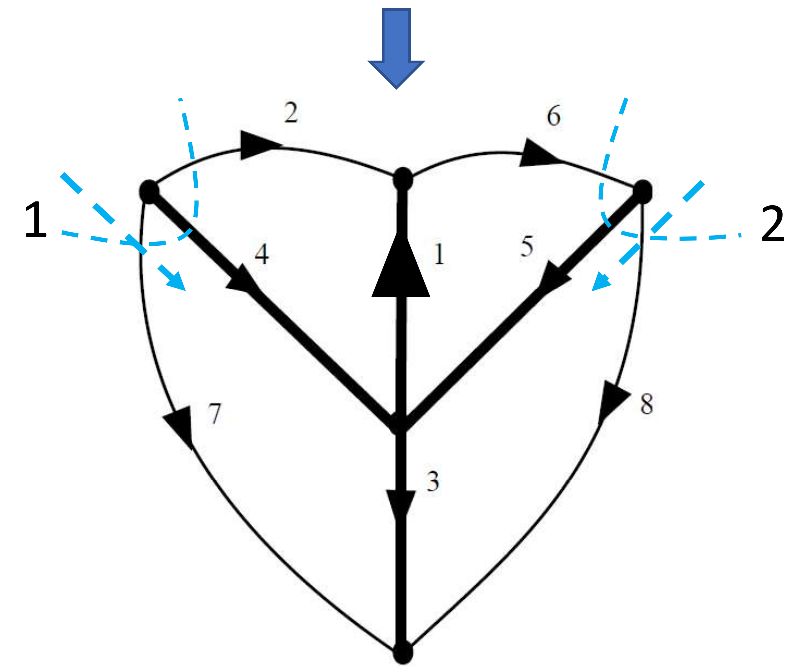
7. Finally, write these equations in matrix form as:

$$B i_{\ell'} + Q i_S + M v_S$$

$$\begin{bmatrix} R_5 + R_6 & 0 & -R_5 \\ 0 & R_4 + R_7 & 0 \\ -R_5 & 0 & R_5 + R_8 \end{bmatrix} \begin{bmatrix} i_6 \\ i_7 \\ i_8 \end{bmatrix} + \begin{bmatrix} 0 \\ R_4 \\ 0 \end{bmatrix} i_2 + \begin{bmatrix} 1 & 0 \\ 0 & -1 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \end{bmatrix} = 0$$

Unknown variables: $i_{\ell'} = i_6, i_7, i_8$ (link currents in co trees).



# Solution

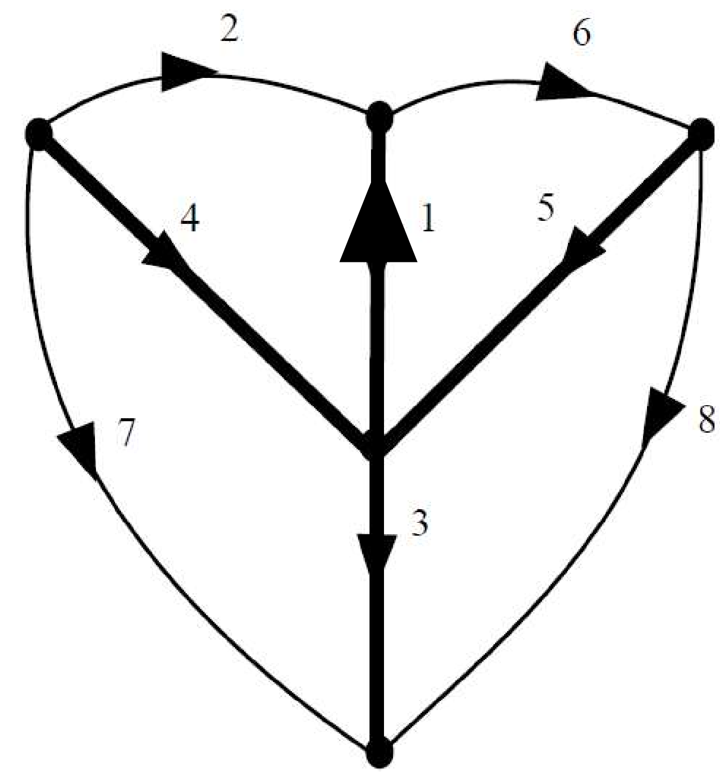
- After obtaining link currents ($i_6, i_7, i_8$), determine branch currents ($i_1$, $i_3$, $i_4$, $i_5$)
- Write branch currents in terms of link currents using KCL equations
- Apply KCL:

$$i_1 + i_2 = i_6 \Rightarrow i_1 = -i_2 + i_6$$

$$i_3 + i_7 + i_8 = 0 \Rightarrow i_3 = -i_7 - i_8$$

$$i_4 + i_2 + i_7 = 0 \Rightarrow i_4 = -i_2 - i_7$$

$$i_5 + i_8 = i_6 \Rightarrow i_5 = i_6 - i_8$$




- In matrix form:

$$\begin{bmatrix} i_1 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = \begin{bmatrix} -1 & 1 & 0 & 0 \\ 0 & 0 & -1 & -1 \\ -1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix} \begin{bmatrix} i_2 \\ i_6 \\ i_7 \\ i_8 \end{bmatrix}$$

# Graph Theory—Generalized Chord Current Method

- If linear circuits containing two-terminal resistors along with independent and dependent sources, use the following steps:

  - ❑ Follow the same steps mentioned earlier and treat dependent source as independent sources.

  - ❑ Place dependent voltage sources in a tree and place dependent current sources in a co-tree.

  - ❑ Using $v - i$ relations of the dependent sources, new unknown variables are written in terms of the link current, voltage sources, and current sources.

- If there is a multi-terminal component in the circuit, it can be considered as an independent source.

# Example 2

1. Pick (draw) a proper tree of the circuit. All voltage sources will be on the tree and current source will be on the co-tree (link).
   - Treat dependent sources as independent sources

Proper tree can be written as: $T = \{2,3,4,5,7\}$

2. Write the fundamental loop equations which do not correspond to the current source in the co-tree.
   - In this case, ignore link 6 & 8 as current sources located in link 6 & 8
   - Only one loop (direction of loop is same as direction of link)

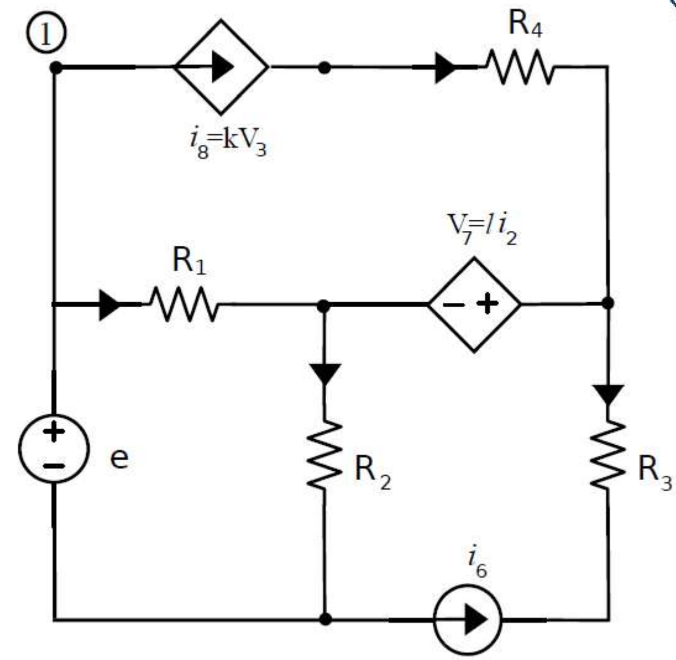
Fundamental loop equations: $v_1 + v_2 - v_5 = 0$

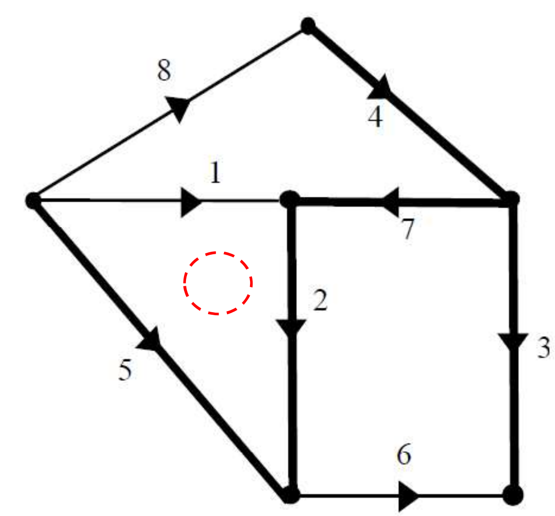
3. Write $v - i$ relations of the resistors: $v = iR$ (Ohm's law)

   $v_1 = R_1 i_1 \qquad v_2 = R_2 i_2 \qquad v_5$: voltage source

4. Substitute the equations in step 3 into the equations in step 2

$R_1 i_1 + R_2 i_2 - v_5 = 0$ where $v_5 = e$ $\Rightarrow$ $R_1 i_1 + R_2 i_2 - e = 0$



# Solution

5. Write the fundamental cut-set equations which do not correspond to the voltage sources
   - 3 fundamental loops indicated by dashed blue lines.

Cut-set 1: $i_3 + i_6 = 0$
Cut-set 2: $i_4 - i_8 = 0$
Cut-set 3: $i_2 - i_6 - i_1 - i_8 = 0$

Although three equations are found, only one of them will be used as there is only one equation in step 4. Since $i_1$ is new unknown in this example, only cut-set 3 equation will be used.

$$i_2 - i_6 - i_1 - i_8 = 0 \Rightarrow i_2 = i_1 + i_6 + i_8$$

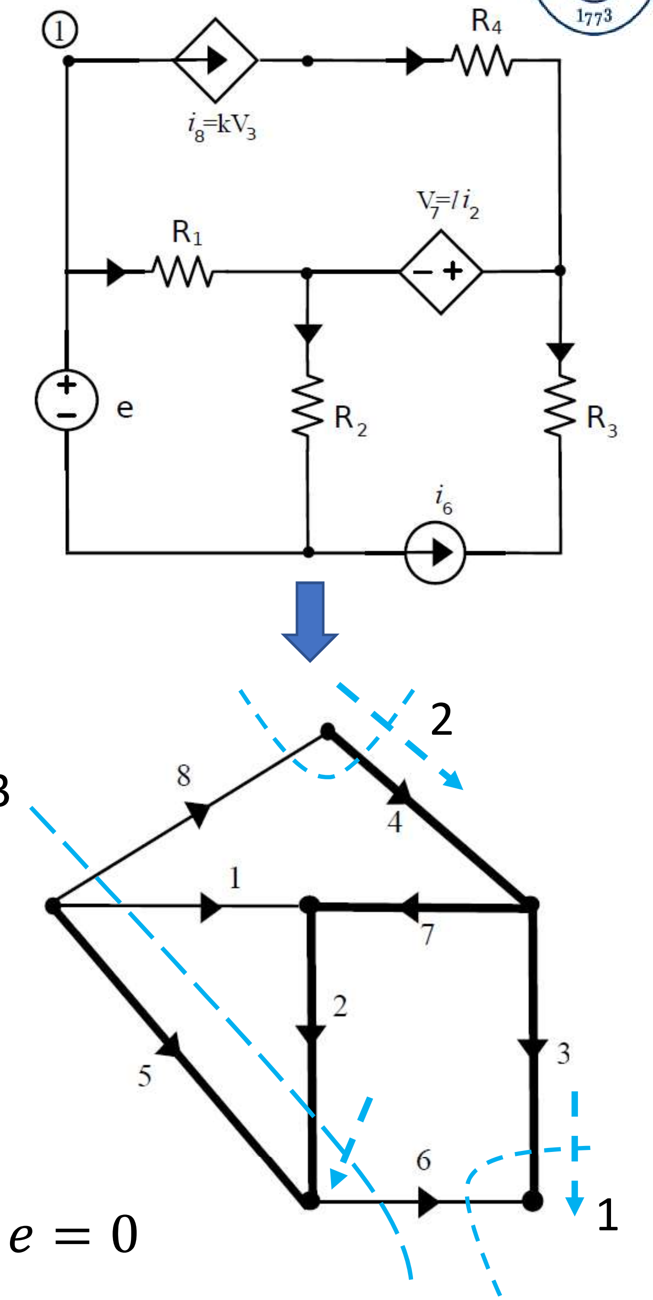
6. Substitute equation in step 5 into the equation in step 4

$$R_1 i_1 + R_2(i_1 + i_6 + i_8) - e = 0 \Rightarrow (R_1+R_2)i_1 + R_2 i_6 + R_2 i_8 - e = 0$$

$$v_3 = R_3 i_3 \text{ where } i_3 + i_6 = 0 \Rightarrow i_3 = -i_6 \Rightarrow v_3 = -R_3 i_6$$

$$i_8 = k v_3 \Rightarrow i_8 = -kR_3 i_6$$

$$(R_1+R_2)i_1 + R_2 i_6 - kR_2R_3 i_6 - e = 0 \Rightarrow (R_1+R_2)i_1 + (R_2 - kR_2R_3)i_6 - e = 0$$



# Graph Theory—Branch Voltage Method

- For a given circuit, use the following steps:
  1. Pick a proper tree which includes all voltage sources. Current sources are placed in a co-trees. Complete the tree with resistors.
  2. Write the fundamental cut-set equations for branches. Do not include branches that contain voltage sources.
  3. Write $v - i$ relations of resistors in the form of $i_k = G_k v_k$
  4. Substitute currents found in step 3 into the fundamental cut set equations in step 2
  5. Write fundamental loop equations. Do not include links that contain current sources.
  6. Substitute the fundamental loop equations in step 5 into the equations in step 4
  7. Present the equation in the following form:

$$MV_{b'} + Qi_S + Mv_S$$

$V_{b'}$: branch voltage vector
$Q$: Fundamental cut-set matrix
$i_S$: current source vector
$v_S$: Voltage source vector

# Example 3

1. Pick (draw) a proper tree of the circuit. All voltage sources will be on the tree and current source will be on the co-tree (link).
   - Start from the voltage sources. Direction of voltage sources from + to –
   - Tree should be connected, i.e., contains all nodes and has no loop

   Proper tree can be written as: $T = \{1,3,4,5\}$

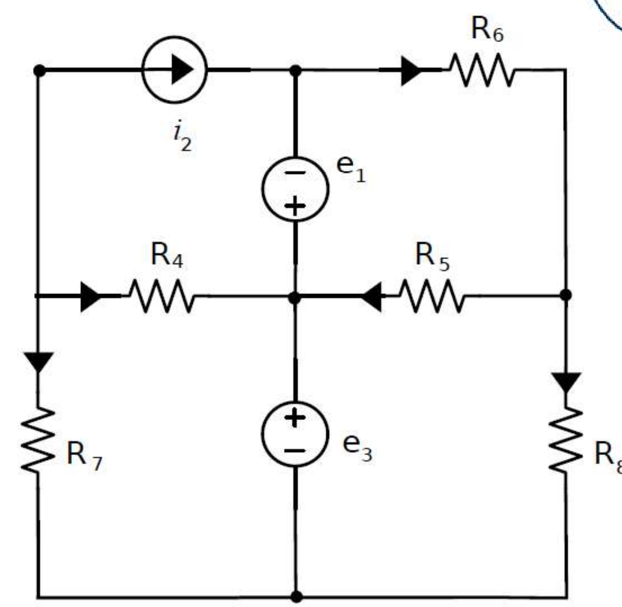
2. Write the fundamental cut set equations for branches.
   - Do not include branches that contain voltage sources
   - Write fundamental cut set equations for branches 4 & 5

   Cut-set 1: $i_2 + i_4 + i_7 = 0$
   Cut-set 2: $i_5 - i_6 + i_8 = 0$

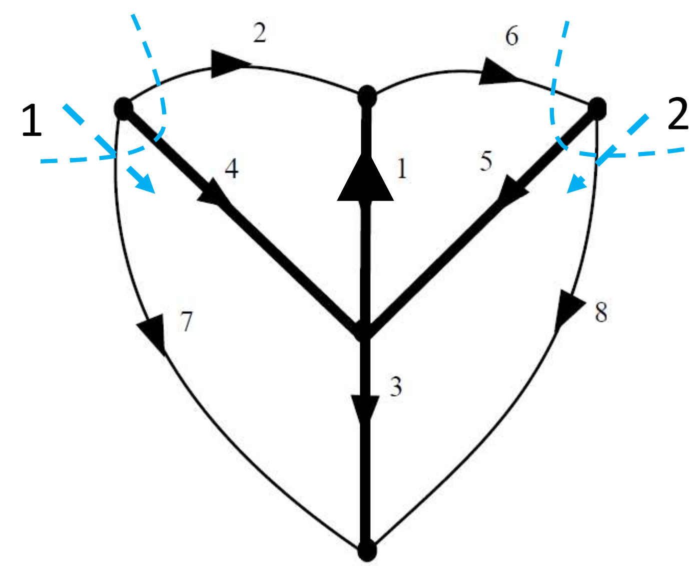
3. Write $v - i$ relations of resistors: $i_k = G_k v_k$

   $i_4 = G_4 v_4$ $\quad i_5 = G_5 v_5$ $\quad i_6 = G_6 v_6$

   $i_7 = G_7 v_7$ $\quad i_8 = G_8 v_8$




Unknows: $v_4, v_5$



# Solution

4. Substitute current found in step 3 into the fundamental cut set equations in step 2

$$i_2 + i_4 + i_7 = 0 \quad \Rightarrow \quad i_2 + G_4 v_4 + G_7 v_7 = 0$$

$$i_5 - i_6 + i_8 = 0 \quad \Rightarrow \quad G_5 v_5 - G_6 v_6 + G_8 v_8 = 0$$

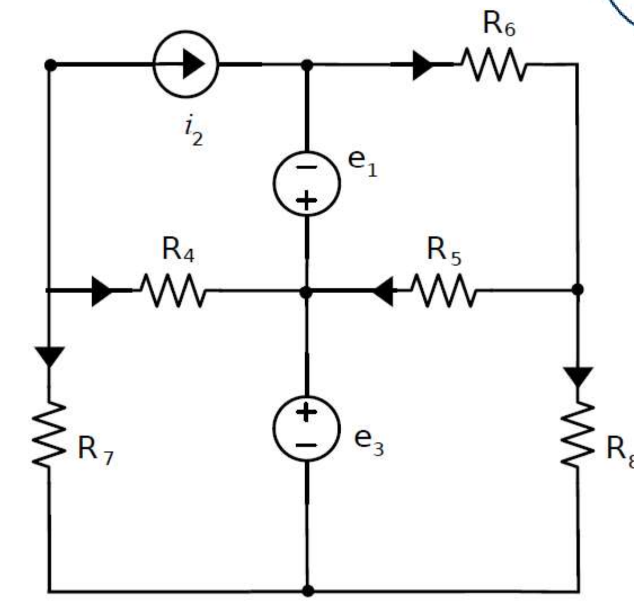
5. Write the fundamental loop equations which do not include link that contains current source.
   - 3 fundamental loops indicated by dashed red circles.

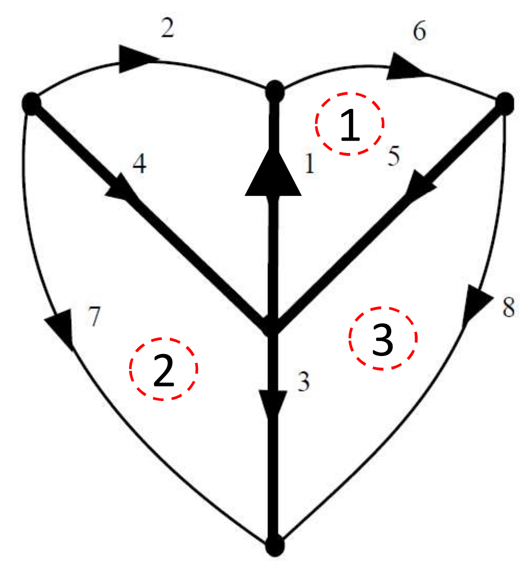
Fundamental loop equations:

Loop 1: $v_6 + v_5 + v_1 = 0$ | $v_6 = -v_1 - v_5$

Loop 2: $v_7 - v_3 - v_4 = 0$ | $v_7 = v_3 + v_4$

Loop 3: $v_8 - v_3 - v_5 = 0$ | $v_8 = v_3 + v_5$



# Solution

6. Substitute fundamental loop equations in step 5 into the equations in step 4

$$\left.\begin{aligned} v_6 &= -v_1 - v_5 \\ v_7 &= v_3 + v_4 \\ v_8 &= v_3 + v_5 \end{aligned}\right\} \Rightarrow \begin{aligned} &i_2 + G_4 v_4 + G_7 v_7 = 0 \\ &G_5 v_5 - G_6 v_6 + G_8 v_8 = 0 \end{aligned}$$

$$i_2 + G_4 v_4 + G_7 v_7 = 0 \Rightarrow i_2 + G_4 v_4 + G_7 (v_3 + v_4) = 0$$

$$G_5 v_5 - G_6 v_6 + G_8 v_8 = 0 \Rightarrow G_5 v_5 - G_6 (-v_1 - v_5) + G_8 (v_3 + v_5) = 0$$

$$i_2 + G_4 v_4 + G_7 v_3 + G_7 v_4 = 0 \Rightarrow i_2 + G_7 v_3 + (G_4 + G_7) v_4 = 0$$

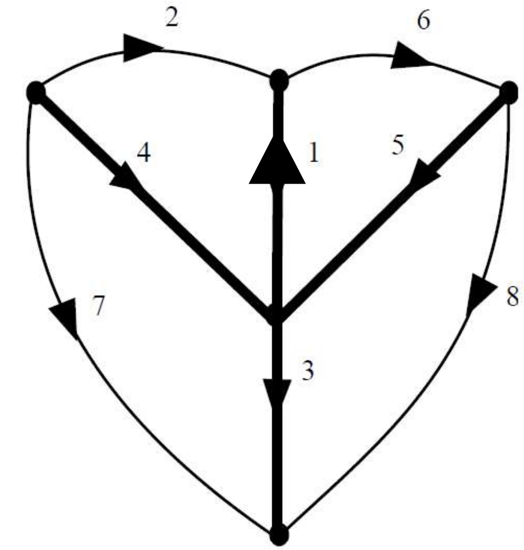
$$G_5 v_5 + G_6 v_1 + G_6 v_5) + G_8 v_3 + G_8 v_5 = 0 \Rightarrow G_6 v_1 + G_8 v_3 + (G_5 + G_6 + G_8) v_5 = 0$$

# Solution

7. Finally, present equations in the matrix form as: $MV_{b'} + Qi_S + Mv_S$

$$i_2 + G_7 v_3 + (G_4 + G_7)v_4 = 0$$

$$G_6 v_1 + G_8 v_3 + (G_5 + G_6 + G_8)v_5 = 0$$



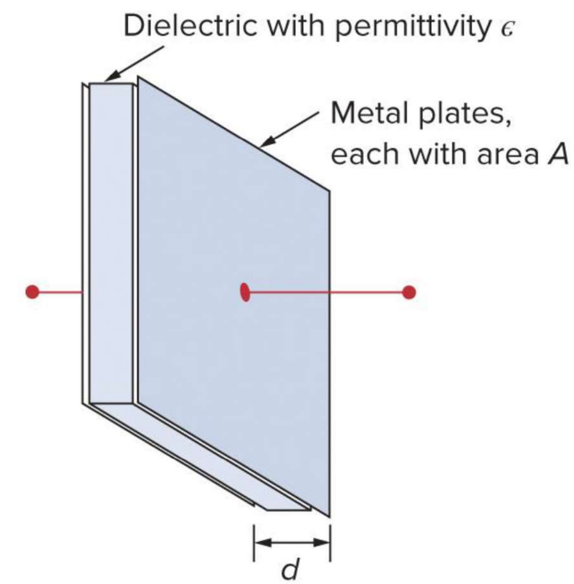

$$\underbrace{\begin{bmatrix} G_4 + G_7 & 0 \\ 0 & G_5 + G_6 + G_8 \end{bmatrix}}_{M} \underbrace{\begin{bmatrix} v_4 \\ v_5 \end{bmatrix}}_{V_b'} + \underbrace{\begin{bmatrix} 1 \\ 0 \end{bmatrix}}_{Q} \underbrace{i_2}_{i_S} + \underbrace{\begin{bmatrix} 0 & G_7 \\ G_6 & G_8 \end{bmatrix}}_{M} \underbrace{\begin{bmatrix} v_1 \\ v_3 \end{bmatrix}}_{v_S} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$$

- If values of resistors, current source and independent voltage sources ($v_1$ & $v_3$) are given, branch voltages $v_4$ & $v_5$ can be found from the above matrix.
- After finding $v_4$ & $v_5$, link voltages $(v_2, v_6, v_7, v_8)$ can be as follows:
- Apply KVL for each link on the digraph:

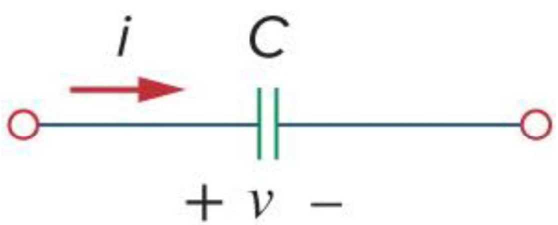
$$\left.\begin{aligned} v_2 - v_1 - v_4 &= 0 \\ v_6 + v_5 + v_1 &= 0 \\ v_7 - v_3 - v_4 &= 0 \\ v_8 - v_3 - v_5 &= 0 \end{aligned}\right\} \quad \begin{aligned} v_2 &= v_1 + v_4 \\ v_6 &= -v_1 - v_5 \\ v_7 &= v_3 + v_4 \\ v_8 &= v_3 + v_5 \end{aligned} \quad \Rightarrow \quad \begin{bmatrix} v_2 \\ v_6 \\ v_7 \\ v_8 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 1 & 0 \\ -1 & 0 & 0 & -1 \\ 0 & 1 & 1 & 0 \\ 0 & 1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_3 \\ v_4 \\ v_5 \end{bmatrix}$$

# Capacitors

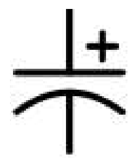
- What is a capacitor?
  - Passive element designed to store energy (electrical energy) in an E-field
  - Store and release electrical energy
  - One of the most common electrical components
- A typical capacitor: two conducting plates separated by an insulator (or dielectric)
- Plates: aluminum & Dielectric: air, ceramic, paper, or mica.



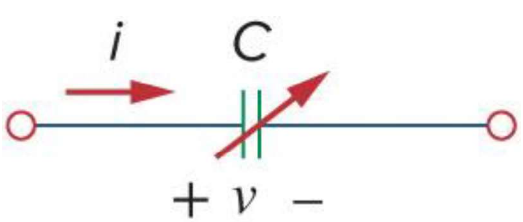

Fixed capacitor



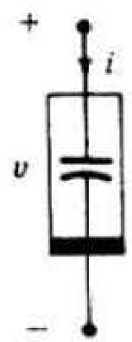

Fixed capacitor




Variable capacitor




Nonlinear capacitor




- If $v > 0$ and $i > 0$
- If $v < 0$ and $i < 0$

Capacitor is being charged

- If $vi < 0$ ($v$ and $i$ have opposite sign): capacitor is discharging

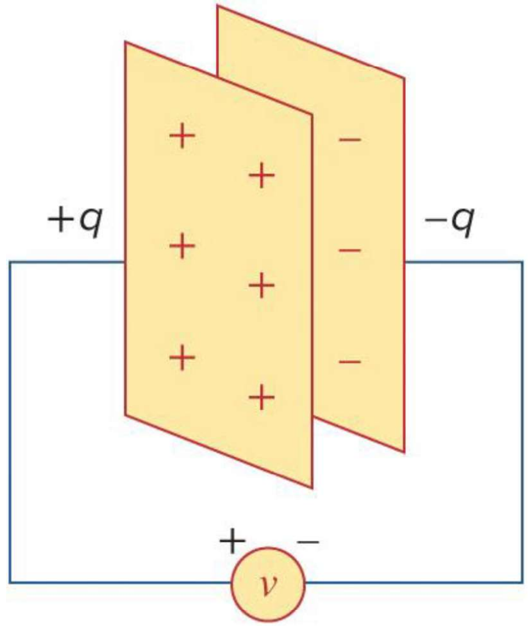
# Capacitors

- Connect a voltage source $v$ to the capacitor: a positive charge $q$ on one plate and a negative charge $-q$ on the other plate.
- During this process, electric charge stored in the capacitor
- Amount of charge stored is directly proportional to the applied voltage $v$:

$$\boxed{q = Cv}$$

q: the amount of charged stored in capacitor
C: the capacitance of the capacitor, unit is Farad (F)

$$1\ F = 1\frac{C}{V}$$




- Charge $q$ stored in a capacitor represented by

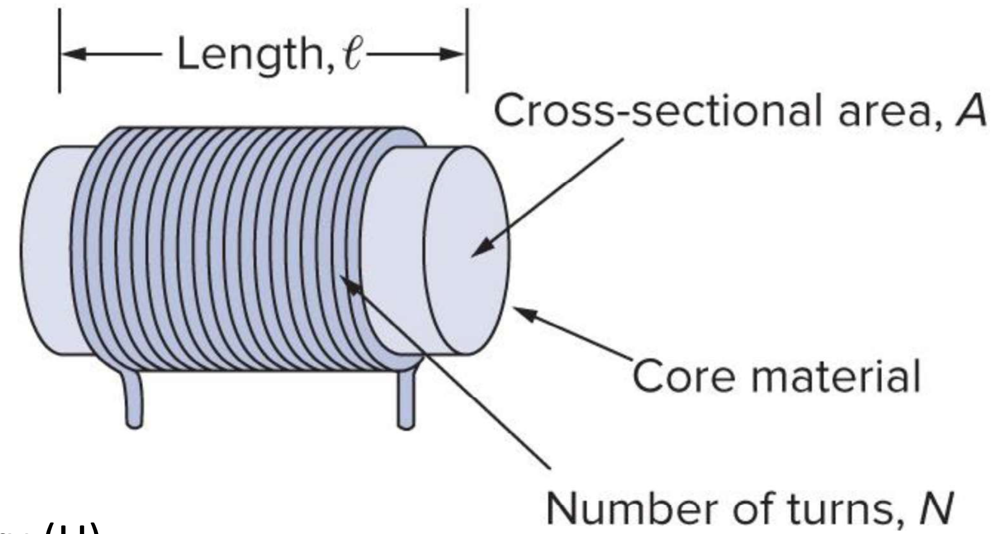
$q = Cv$ ⟹ Derivation of both sides ⟹ $\dfrac{dq}{dt} = C\dfrac{dv}{dt}$

By definition: $i = \dfrac{dq}{dt}$ ⟹ $\boxed{i = C\dfrac{dv}{dt}}$ Current-voltage relationship for a capacitor

Linear capacitor (Ideal capacitors are linear)

# Inductors

- What is an inductor?
  - Passive element designed to store energy in its magnetic field.
- Numerous applications in electronics and power systems: power supplies, transformers, TVs, electric motors, etc.
- Inductor: formed into a cylindrical coil with many turns of conducting wire
- Inductor: simply a coil of conducting wire
- If current is allowed to pass through an inductor, it is found that the voltage across the inductor is directly proportional to the time rate of change of the current:




$$\boxed{v = L\frac{di}{dt}}$$

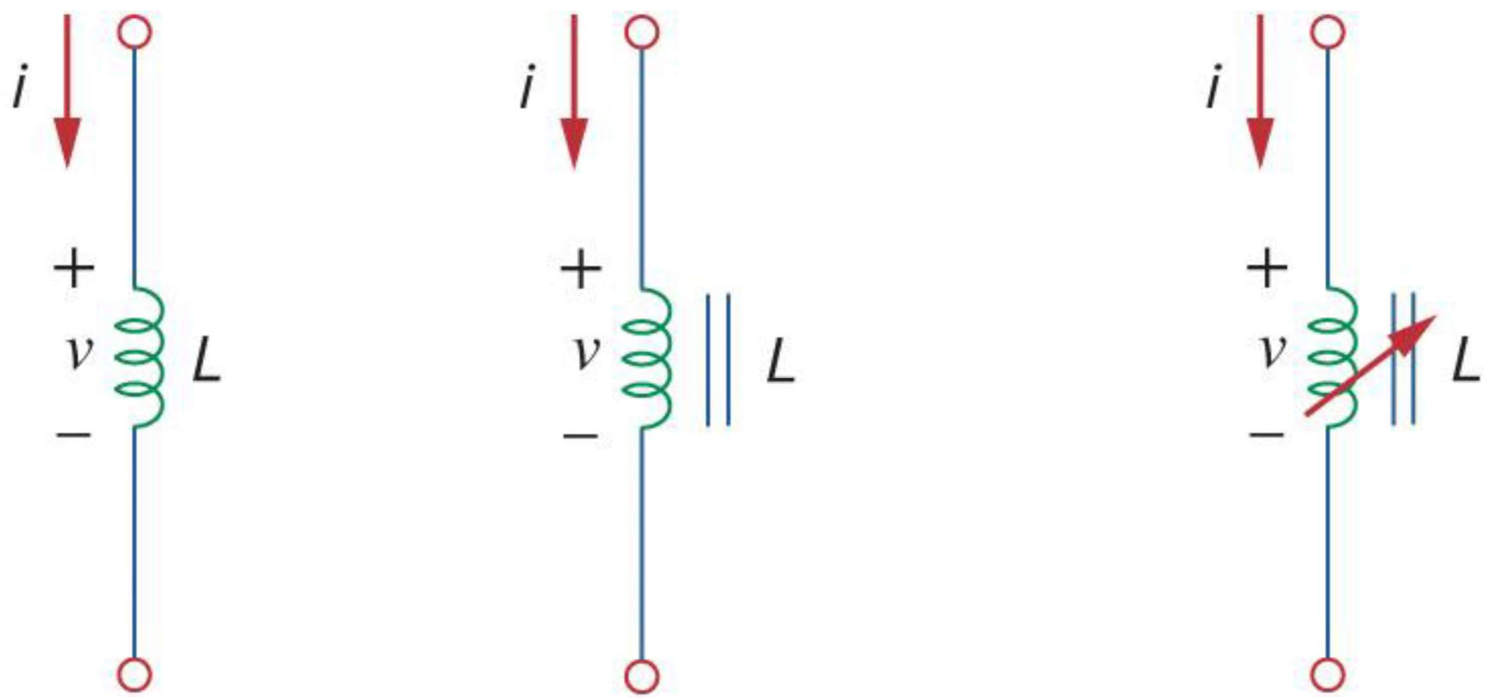
where L: inductance of the inductor, unit is henry (H)

1 henry (H)=1 volt-second per ampere $\left(H = \frac{Vs}{A}\right)$

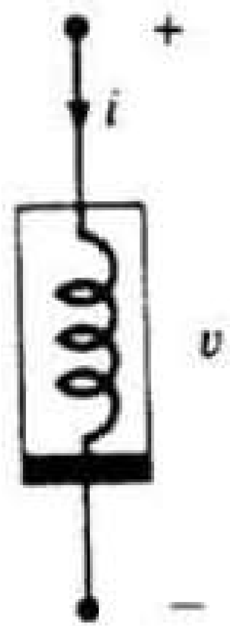
Voltage-current relationship for an inductor

# Inductors

- Inductors: fixed or variable
- Circuit symbol of inductor:



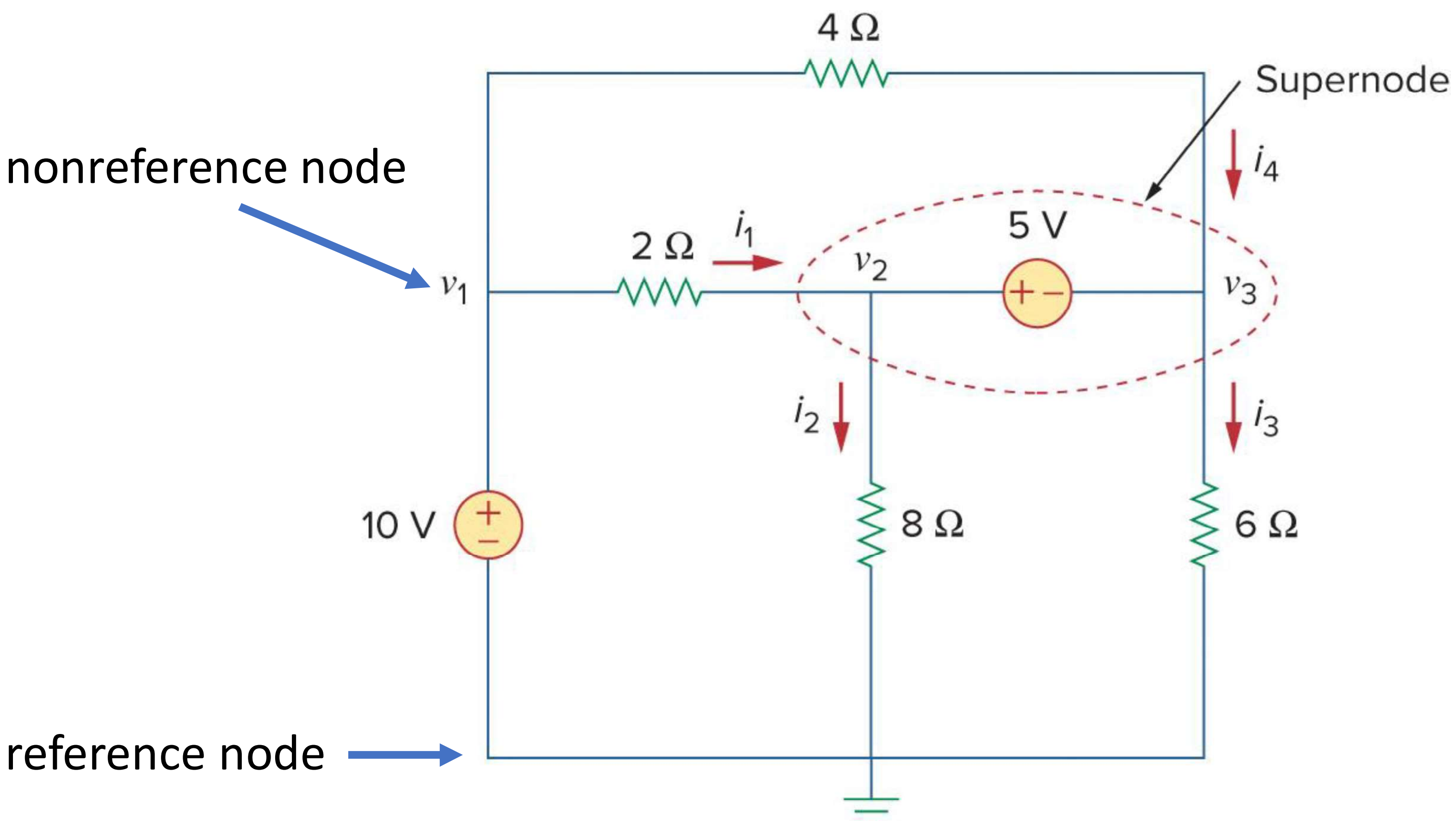

Nonlinear inductor



# Supernode

- If the voltage source (dependent or independent) is connected between two nonreference nodes, the two nonreference nodes form a **supernode**.
- Nodes 2 and 3 form a supernode
- KCL: $\sum i_{in} = \sum i_{out}$
- At supernode node: $i_1 + i_4 = i_2 + i_3$

KCL must be satisfied at the supernode. KCL not only applies to node but also closed surface



# Obtaining State Equations

- For solving the state equations, use the following steps:

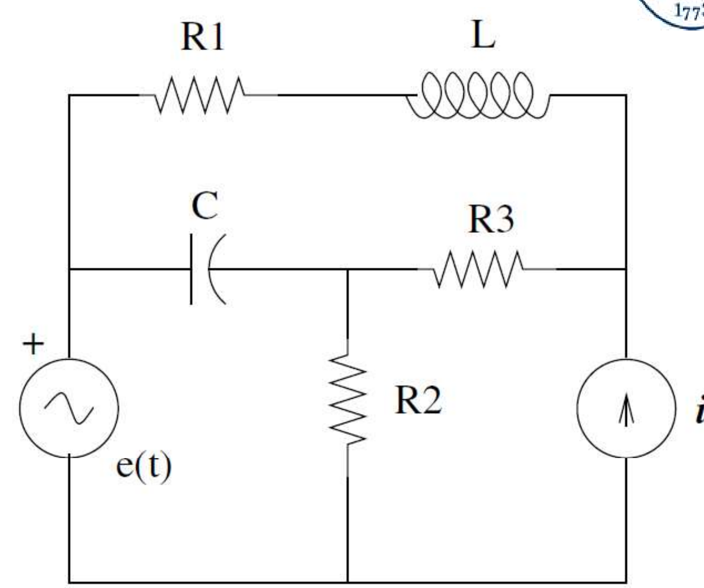
1. Pick (draw) a proper tree
   - The voltage sources must be placed in the tree
   - If the tree is not complete, the edges corresponding to as many capacitors as possible must be placed in the tree. If a capacitor in a loop which consisting entirely of capacitors and voltage sources, the capacitor must not placed in the tree.
   - If the tree is not complete, the edges corresponding to the resistors must be chosen and as many resistors as possible must be included.
   - If the tree is still not complete, then the edges corresponding to the inductors will be chosen until the tree is completed. If an inductor on a cut set which consisting entirely of inductors and current sources, the inductor must be placed in the tree.
   - All the edges corresponding to the current sources must be placed in the co-tree.
2. After selection of proper tree, the state variables are branch capacitor voltages and chord inductor currents.

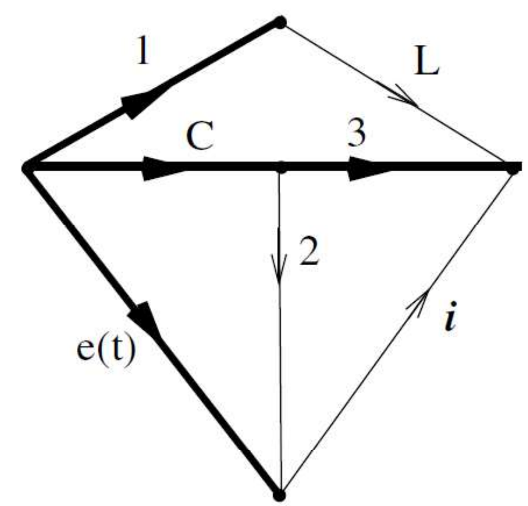
# Obtaining State Equations

3. Obtaining state equations from the circuit: Express the voltage across each element corresponding to a branch and the current through each element corresponding to non-branch edge in terms of voltage sources, current sources, and state variables. If not possible, assign a new voltage variable to a resistor corresponding to a branch and a new current variable to a resistor corresponding to a non-branch edge.
   a) Apply KVL to the fundamental loop determined by each non-branch inductor
   b) Apply KCL to the fundamental cut-set determined by each branch capacitor
   c) Apply KVL to the fundamental loop determined by each resistor with a new current variable assigned in
   d) Apply KCL to the node or super-node corresponding to the fundamental cut-set determined by each resistor with a new voltage variable assigned in
   e) Solve the simultaneous equations obtained from step c and d for the new variables in terms of the voltage sources, current sources, and the state variables.
   f) Substitute the expression obtained in step e into equations determined in step a and b

# Example 4

1. Pick (draw) a proper tree of the circuit. All voltage sources will be on the tree and current source will be on the co-tree (link).
   - Identify nodes. There are 5 nodes in the circuit.
   - Since direction of branches is not given, choose a direction.
   - Direction of resistor and inductor is arbitrary but direction for capacitor and voltage source is chosen from + to –
   - Place voltage source in a tree
   - If the tree is not complete, place capacitor in the tree.
   - If the tree is still not complete, use as many resistors as possible to complete the tree
   - If the tree is still not complete, select inductor to complete the tree
   - Place current source in the co-tree.




2. After selection of proper tree, the state variables are branch capacitor voltages and chord (link) inductor currents.
   - 1 capacitor on the tree branch and 1 inductor on the co-tree (chord or link). Thus, $v_c$ and $i_L$ are state variables.
   - RC circuit: 1st order differential equation

$$\dot{V}_c = f(V_c, i_L, e(t), i(t)) \quad \text{and} \quad \dot{i}_L = f(V_c, i_L, e(t), i(t))$$

# Solution

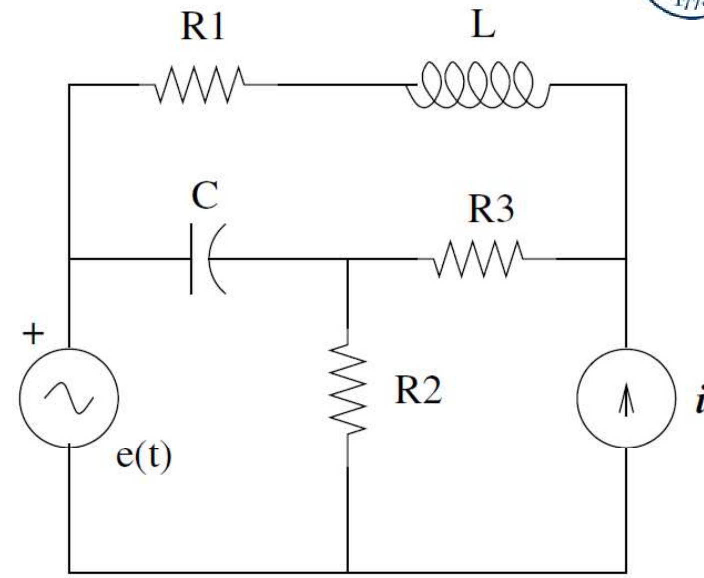
3. Obtaining state equations:
   a) Apply KVL to the fundamental loop determined by each link inductor
      - Since only one link inductor, circuit has one fundamental loop
      - Fundamental loop indicated by dashed red circle

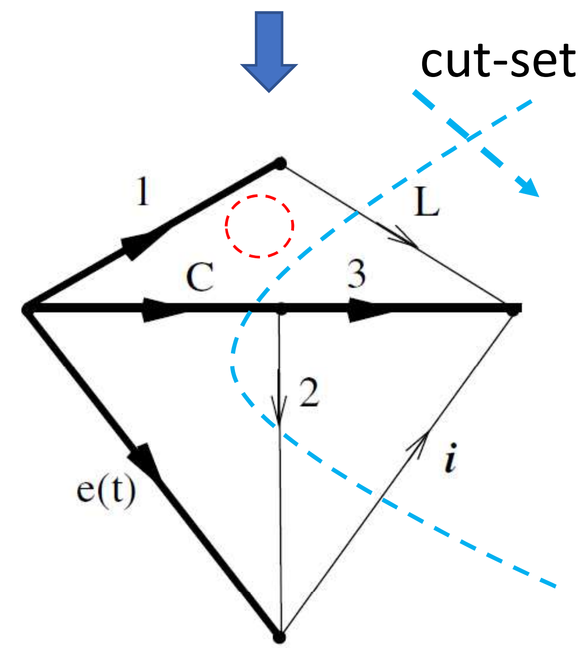
$$V_L - V_3 - V_c + V_1 = 0$$

   b) Apply KCL to the fundamental cut-set determined by each tree branch capacitor
      - Since one branch capacitor, circuit has one fundamental cut-set
      - Fundamental cut-set indicated by dashed blue line

$$i_L + i_C - i_2 + i = 0$$

$$\left.\begin{aligned} i_L + i_C - i_2 + i &= 0 \\ V_L - V_3 - V_c + V_1 &= 0 \end{aligned}\right\} \text{State equations}$$

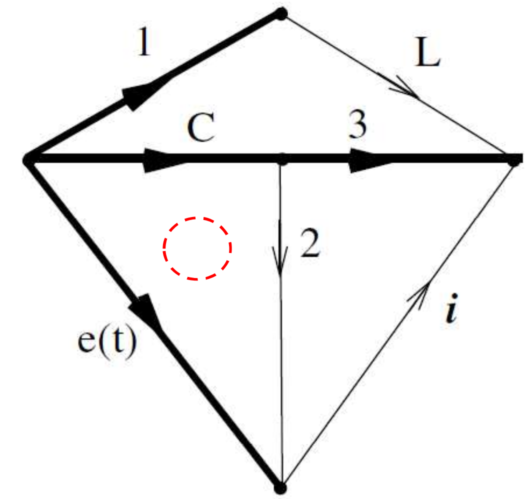


# Solution

$$i_L + i_C - i_2 + i = 0 \Rightarrow i_C = -i_L + i_2 - i$$

$$V_L - V_3 - V_c + V_1 = 0 \Rightarrow V_L = V_3 + V_c - V_1$$




- By definition: $i_C = C\dfrac{dV_C}{dt}$ and $V_L = L\dfrac{di_L}{dt}$

$$C\frac{dV_C}{dt} = -i_L + i_2 - i \qquad L\frac{di_L}{dt} = V_3 + V_c - V_1$$

c) Apply KVL to the fundamental loop determined by each resistor with a new current variable assigned in

- ❑ Fundamental loop determined by each resistor that contains a new loop
- ❑ Fundamental loop indicated by dashed red circle

$$V_2 - e + V_c = 0 \text{ where } V_2 = R_2 i_2 \Rightarrow \underbrace{R_2 i_2}_{\text{New variable}} = e - V_c$$

# Solution

d) Apply KCL to the node or super-node corresponding to the fundamental cut-set determined by each resistor with a new voltage variable assigned in

- Two fundamental cut-set as there are two resistors on tree branch
- Fundamental cut-sets indicated by dashed blue lines

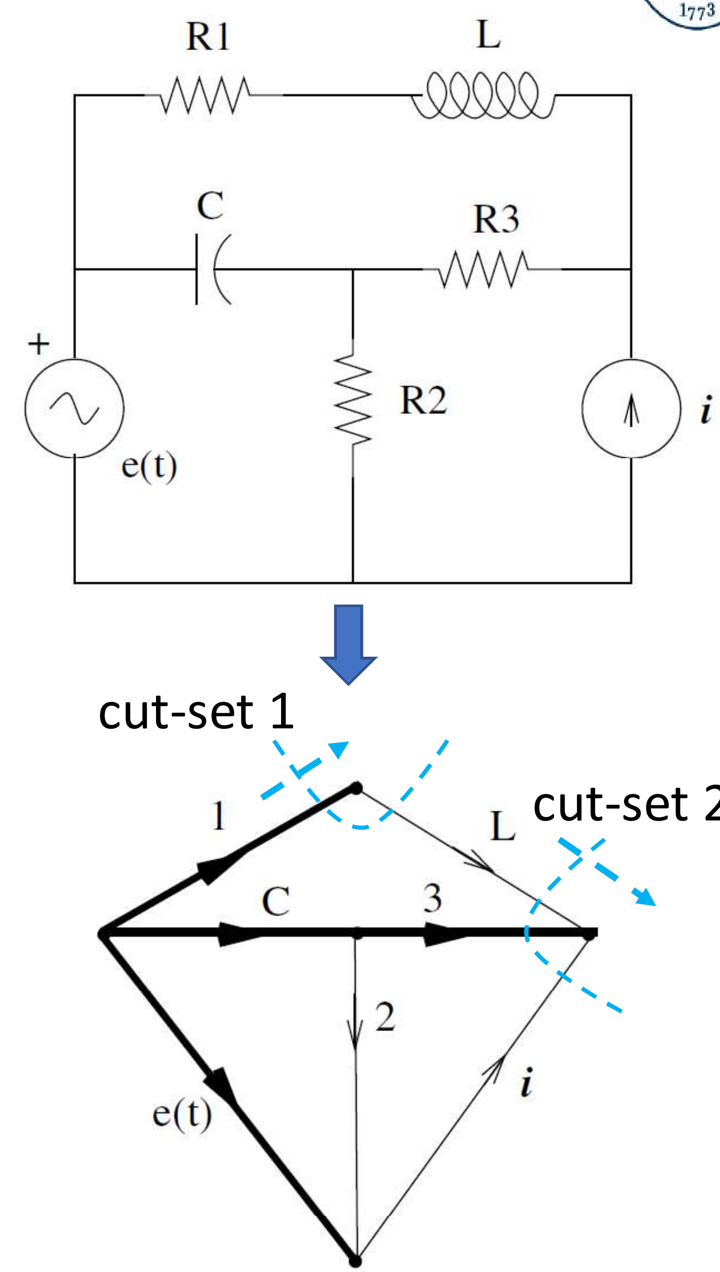
Cut set 1: $i_1 - i_L = 0$

Cut set 2: $i_3 + i_L + i = 0$

$$i_1 = i_L$$

$$i_3 = -i_L - i$$

New variables




- $i_1$ & $i_3$ can be written in terms of voltage variables:

$$i = GV \Rightarrow i_1 = G_1 V_1 \qquad i_3 = G_3 V_3$$

$$G_1 V_1 = i_L$$

$$G_3 V_3 = -i_L - i$$

New variables

# Solution

$$R_2 i_2 = e - V_c$$
$$G_1 V_1 = i_L$$
$$G_3 V_3 = -i_L - i$$

Solve these equations in terms of new variables ($i_2, V_1, V_3$)

$$\boxed{G = \frac{1}{R}}$$

$$i_2 = \frac{e}{R_2} - \frac{V_c}{R_2}$$
$$V_1 = R_1 i_L$$
$$V_3 = -R_3 i_L - R_3 i$$

Substitute new variables into state equations

$$i_L + i_C - i_2 + i = 0 \quad \Rightarrow \quad i_L + C\frac{dV_C}{dt} - \left(\frac{e}{R_2} - \frac{V_c}{R_2}\right) + i = 0$$

$$V_L - V_3 - V_c + V_1 = 0 \quad \Rightarrow \quad L\frac{di_L}{dt} - (-R_3 i_L - R_3 i) - V_c + R_1 i_L = 0$$

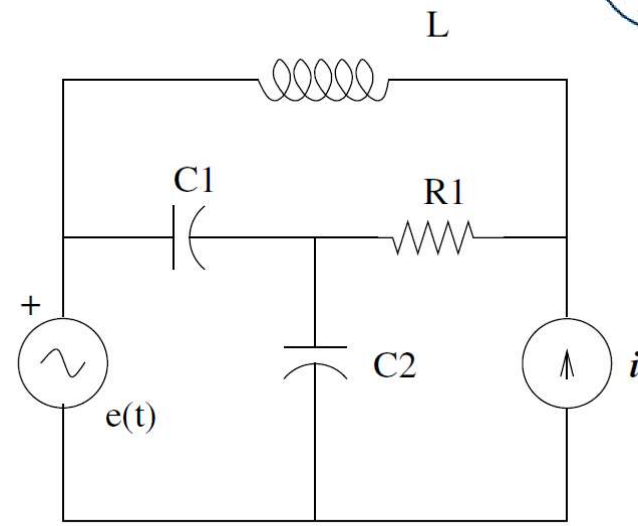
$$\frac{dV_C}{dt} = -\frac{1}{R_2 C}V_c - \frac{1}{C}i_L + \frac{1}{R_2 C}e - \frac{1}{C}i$$

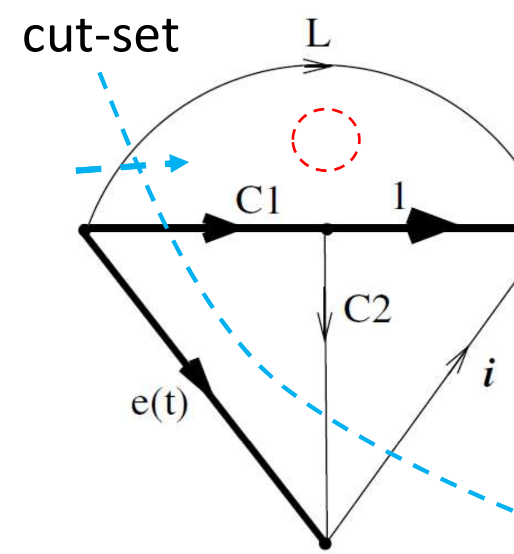
$$\frac{di_L}{dt} = \frac{1}{L}V_c - \frac{(R_1 + R_3)}{L}i_L - \frac{R_3}{L}i$$

$$\frac{d}{dt}\begin{bmatrix} V_C \\ i_L \end{bmatrix} = \begin{bmatrix} -\frac{1}{R_2 C} & -\frac{1}{C} \\ \frac{1}{L} & -\frac{(R_1 + R_3)}{L} \end{bmatrix}\begin{bmatrix} V_C \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{1}{R_2 C} \\ 0 \end{bmatrix} e(t) + \begin{bmatrix} -\frac{1}{C} \\ -\frac{R_3}{L} \end{bmatrix} i$$

# Example 5

1. Pick (draw) a proper tree of the circuit. All voltage sources will be on the tree and current source will be on the co-tree (link).
   - Identify nodes. There are 4 nodes in the circuit.
   - Since direction of branches is not given, choose a direction.
   - Place $C_1$ in the tree but $C_2$ in the co-tree (link) as two capacitors and voltage source make a loop in the circuit.
   - If the tree is still not complete, use as many resistors as possible to complete the tree
   - If cut-set consists of entirely inductors and current sources, place inductor in the tree. Otherwise, place inductor in the co-tree.




2. After selection of proper tree, the state variables are branch capacitor voltages and chord (link) inductor currents.
   - 1 capacitor on the tree ($C_1$) and 1 inductor ($L$) on the co-tree (chord or link). Thus, $v_{c1}$ and $i_L$ are state variables.

3. Obtaining state equations: Apply KVL and KCL

KVL to fundamental loop determined by inductor: $V_L - V_1 - V_{C1} = 0$

KCL to fundamental cut set determined by capacitor: $i_L + i_{C1} - i_{C2} + i = 0$

# Solution

$$i_{C1} = -i_L - i + i_{C2}$$

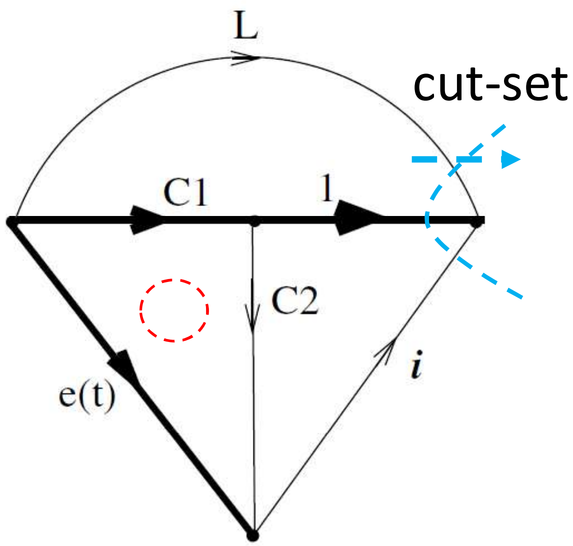
$$V_L = V_1 + V_{C1}$$

- By definition: $i_C = C\dfrac{dV_C}{dt}$ and $V_L = L\dfrac{di_L}{dt}$

$$C_1\frac{dV_{C1}}{dt} = -i_L - i + i_{C2}$$

$$L\frac{di_L}{dt} = V_1 + V_{C1}$$

State equations




- Apply KVL to the fundamental loop determined by capacitor $C_2$

$$V_{C1} + V_{C2} - e = 0 \Rightarrow V_{C2} = e - V_{C1}$$

- Apply KCL to the fundamental cut-set determined by resistor $R_1$

$$i_1 + i_L + i = 0 \Rightarrow i_1 = -i_L - i$$

$$i_1 = G_1V_1 \Rightarrow G_1V_1 = -i_L - i \Rightarrow G = \frac{1}{R} \Rightarrow V_1 = -R_1i_L - R_1i$$

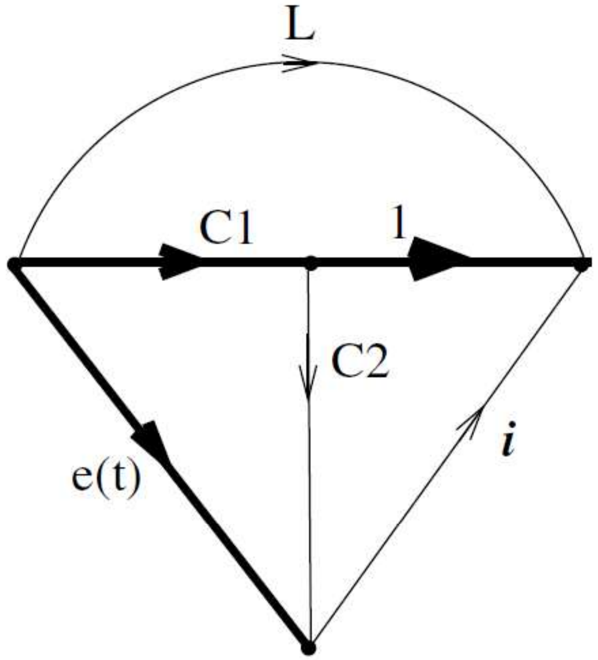
# Solution

- Determine $i_{C2}$ in state equations as:

$V_{C2} = e - V_{C1}$ ⟶ Take the derivative of both sides

$\frac{dV_{C2}}{dt} = \frac{de}{dt} - \frac{dV_{C1}}{dt}$ ⟶ Multiply both sides by $C_2$

$$\underbrace{\boxed{C_2 \frac{dV_{C2}}{dt}}}_{i_{C2}} = C_2 \frac{de}{dt} - C_2 \frac{dV_{C1}}{dt}$$




- State equations in standard form:

$$C_1 \frac{dV_{C1}}{dt} = -i_L - i + C_2 \frac{de}{dt} - C_2 \frac{dV_{C1}}{dt}$$

$$L \frac{di_L}{dt} = \underbrace{-R_1 i_L - R_1 i}_{V_1} + V_{C1}$$

# Solution

$$C_1 \frac{dV_{C1}}{dt} = -i_L - i + C_2 \frac{de}{dt} - C_2 \frac{dV_{C1}}{dt}$$

$$L \frac{di_L}{dt} = -R_1 i_L - R_1 i + V_{C1}$$

Rearrange the state equations

$$\frac{dV_{C1}}{dt} = -\frac{1}{C_1 + C_2} i_L + \frac{C_2}{C_1 + C_2} \frac{de}{dt} - \frac{1}{C_1 + C_2} i$$

$$\frac{di_L}{dt} = \frac{1}{L} V_{C1} - \frac{R_1}{L} i_L - \frac{R_1}{L} i$$

State equations in standard form

- In matrix form:

$$\frac{d}{dt}\begin{bmatrix} V_{C1} \\ i_L \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C_1 + C_2} \\ \frac{1}{L} & -\frac{R_1}{L} \end{bmatrix} \begin{bmatrix} V_{C1} \\ i_L \end{bmatrix} + \begin{bmatrix} \frac{C_2}{C_1 + C_2} \\ 0 \end{bmatrix} \frac{de}{dt} + \begin{bmatrix} -\frac{1}{C_1 + C_2} \\ -\frac{R_1}{L} \end{bmatrix} i$$