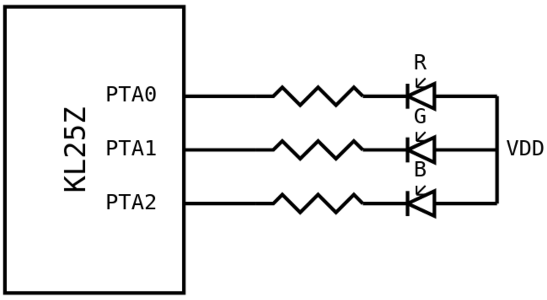
ID: BLG212E – Quiz 4 06.01.2025
Full Name:

Question 1) [50p]



Complete the provided **main()** function to sequentially turn on the **Red (PTA0)**, **Green (PTA1)**, and **Blue (PTA2)** LEDs of the KL25Z microcontroller, one at a time, for **1 second** each (for each second just one LED should be on state and others LEDs should remain off). Use the existing configuration, and assume the ***Delay(milliseconds)*** function already implemented for the delay.

SOLUTION:

```
int main() {
   // Enable Clock for Port A
   SIM->SCGC5 |= SIM_SCGC5_PORTA_MASK;  // M1 (Set Clock Error)

   // Configure PTA0 (Red), PTA1 (Green), PTA2 (Blue) as GPIO
   PORTA->PCR[0] &= ~PORT_PCR_MUX_MASK;  // M2 (Clear Mux Error)
   PORTA->PCR[0] |= PORT_PCR_MUX(1);     // M3 (Set Mux Error)

   PORTA->PCR[1] &= ~PORT_PCR_MUX_MASK;  // M2 (Clear Mux Error)
   PORTA->PCR[1] |= PORT_PCR_MUX(1);     // M3 (Set Mux Error)

   PORTA->PCR[2] &= ~PORT_PCR_MUX_MASK;  // M2 (Clear Mux Error)
   PORTA->PCR[2] |= PORT_PCR_MUX(1);     // M3 (Set Mux Error)

   // Set PTA0, PTA1, PTA2 as output
   PTA->PDDR |= MASK(0) | MASK(1) | MASK(2);  // M4 (Set PDDR)

   // Clear all pins (set high for common anode LEDs)
   PTA->PSOR = MASK(0) | MASK(1) | MASK(2);  // M5 (Clear State Error)

   while (1) {
      // Turn on Red (PTA0), delay, turn off
      PTA->PCOR = MASK(0);  // M6 (PCOR Misusage)
      Delay(1000);          // M8 (Delay)
      PTA->PSOR = MASK(0);  // M7 (PSOR Misusage)

      // Turn on Green (PTA1), delay, turn off
      PTA->PCOR = MASK(1);  // M6 (PCOR Misusage)
      Delay(1000);          // M8 (Delay)
      PTA->PSOR = MASK(1);  // M7 (PSOR Misusage)

      // Turn on Blue (PTA2), delay, turn off
      PTA->PCOR = MASK(2);  // M6 (PCOR Misusage)
      Delay(1000);          // M8 (Delay)
      PTA->PSOR = MASK(2);  // M7 (PSOR Misusage)
   }

   return 0;
}
```

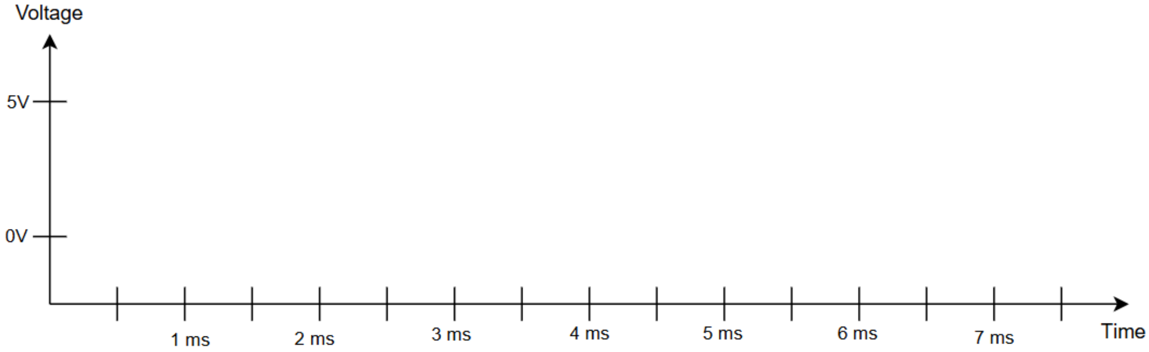
ID: BLG212E – Quiz 4 06.01.2025
Full Name:

Question 1 Common Mistakes and Explanation:

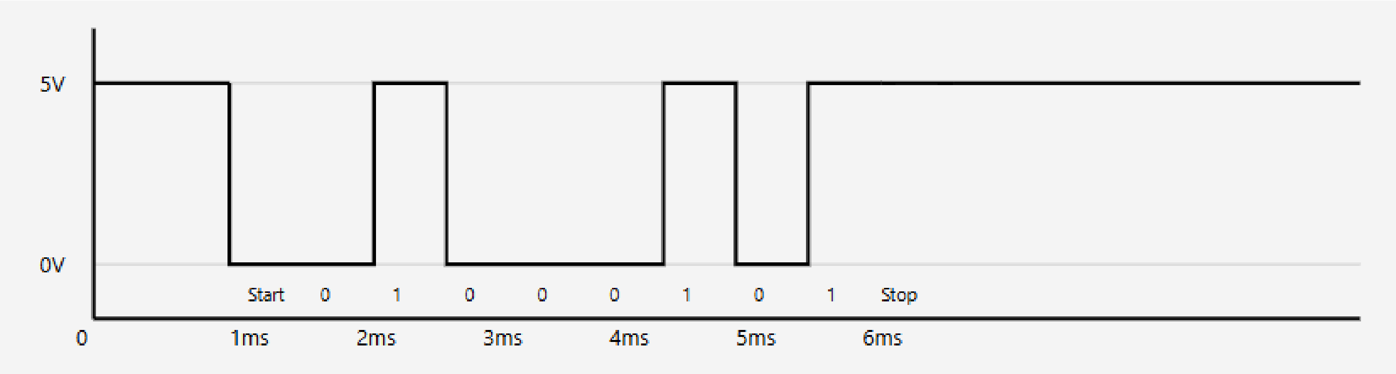
1. **M0 [-50p] (Completely Wrong):** Code does not meet the requirements or functionality is incorrect.
2. **M1 [-3p] (Set Clock Error):** Incorrect or missing clock enable configuration for the required port.
3. **M2 [-3p] (Clear Mux Error):** Failure to clear the MUX field in the PCR before setting it.
4. **M3 [-3p] (Set Mux Error):** Incorrect MUX value set for GPIO mode.
5. **M4 [-3p] (Set PDDR):** Failure to configure the pin direction as output using PDDR.
6. **M5 [-3p] (Clear State Error):** Initial state of the pin not cleared properly.
7. **M6 [-5p] (PCOR Misusage):** Incorrect use of PCOR, clearing unintended bits.
8. **M7 [-5p] (PSOR Misusage):** Incorrect use of PSOR, setting unintended bits.
9. **M8 [-3p] (Delay):** Improper or missing delay causing incorrect timing.
10. **M9 [-10p] (Loop Logic Error):** Incorrect loop implementation leading to invalid LED sequence.
11. **M10 [-5p] (Indexing Error):** Errors in accessing pin registers (e.g., wrong array indices).
12. **M11 [-10p] (PCOR/PSOR Confusion):** Misusing PCOR and PSOR for pin control operations.
13. **M12 [-10p] (Anode/Cathode Confusion):** Incorrect assumption about the LED configuration
14. **M13 [-15p] (Other):** Unique and critical errors not covered by the above categories.

Question 2) [50p]

Assume a serial port operating with a baud rate of 2000 bits per second. The protocol is 1 start, 8 data and 1 stop bit. Draw the waveform when the value 0xA2 is transmitted. The transmission of the value **starts from 1 ms timepoint**. You assume the channel is idle before and after the frame. Time flows from left to right.

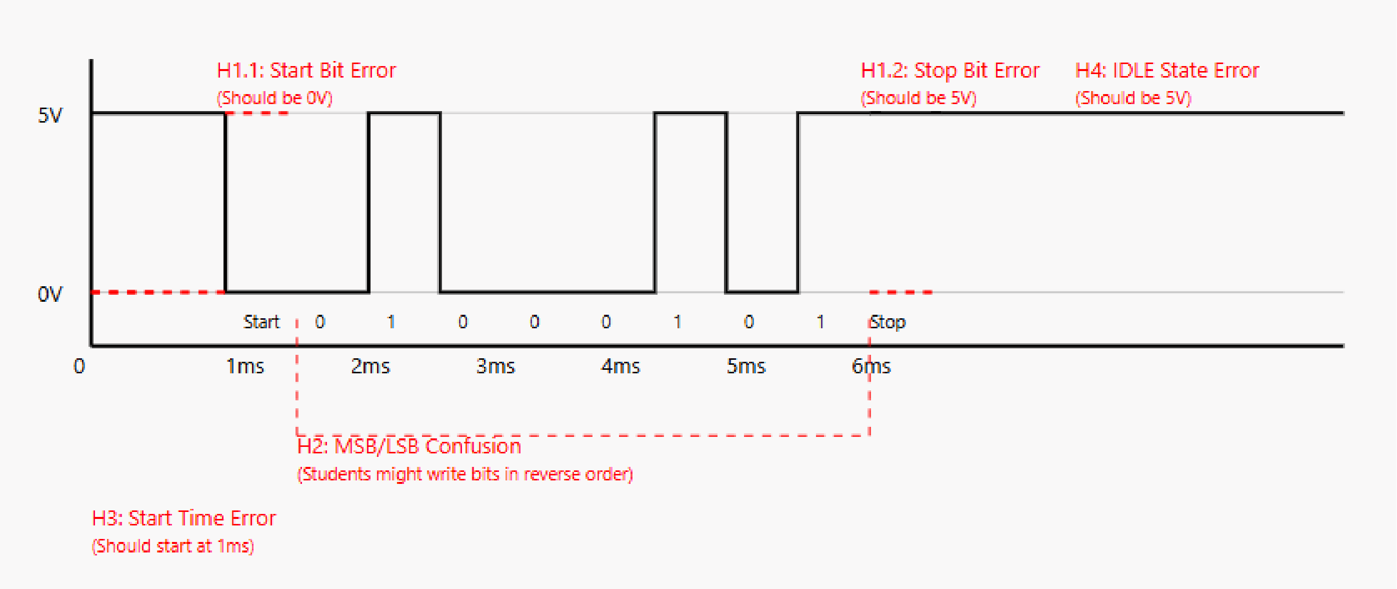


SOLUTION



ID: BLG212E – Quiz 4 06.01.2025

Full Name:



Question 2 Common Mistakes and Explanation:

- **H1.1 [-5p] (Start Bit Error):** The start bit should be 0V, indicating the start of transmission.
- **H1.2 [-5p] (Stop Bit Error):** The stop bit should be 5V, signaling the end of the frame.
- **H2 [-5p] (MSB/LSB Confusion):** The bits were written in reverse order; LSB should transmit first.
- **H3 [-5p] (Start Time Error):** Transmission should begin precisely at the 1 ms timepoint.
- **H4 [-5p] (IDLE State Error):** The idle state should remain at 5V before and after the frame.
- **H5 [-50p](Completely Wrong):** The waveform does not match the given protocol or data at all.
- **H6 [+5p] (Bonus +5p)**
- **H7 [-5p] (Bitrate Calc. Error):** Incorrect calculation of bit duration based on the baud rate.
- **H8 [-10p] (Other):** Additional critical issues like alignment, labeling, or incomplete waveforms.

ID: BLG212E – Quiz 4 06.01.2025

Full Name:

ASSUME THAT YOU ARE PROVIDED WITH THE FOLLOWING DEFINITIONS:

```
/** PORT - Register Layout Typedef */
typedef struct {
  __IO uint32_t PCR[32];  /** Pin Control Register n, array offset: 0x0,
     array step: 0x4 */
  __O  uint32_t GPCLR;    /** Global Pin Control Low Register, offset: 0x80 */
  __O  uint32_t GPCHR;    /** Global Pin Control High Register, offset: 0x84 */
  uint8_t RESERVED_0[24];
  __IO uint32_t ISFR;     /** Interrupt Status Flag Register, offset: 0xA0 */
} PORT_Type;

//MUX field of PCR must be configured with a value of (1) to be used for GPIO.

/* PORT – Peripheral instance base addresses */
/** Peripheral PORTA base address */
#define PORTA_BASE     (0x40049000u)
/** Peripheral PORTA base pointer */
#define PORTA          ((PORT_Type *) PORTA_BASE)

#define PORT_PCR_MUX_MASK   0x700u
#define PORT_PCR_MUX_SHIFT  8
#define PORT_PCR_MUX(x) (((uint32_t)(((uint32_t)(x))<<PORT_PCR_MUX_SHIFT))
                                   &PORT_PCR_MUX_MASK)
/*------------------------------------------------------------------------------------------------------------------------*/
/** GPIO - Register Layout Typedef */
typedef struct {
  __IO uint32_t PDOR;   /**< Port Data Output Register, offset: 0x0 */
  __O  uint32_t PSOR;   /**< Port Set Output Register, offset: 0x4 */
  __O  uint32_t PCOR;   /**< Port Clear Output Register, offset: 0x8 */
  __O  uint32_t PTOR;   /**< Port Toggle Output Register, offset: 0xC */
  __I  uint32_t PDIR;   /**< Port Data Input Register, offset: 0x10 */
  __IO uint32_t PDDR;   /**< Port Data Direction Register, offset: 0x14 */
} GPIO_Type;

/** Peripheral PTA base address */
#define PTA_BASE (0x400FF000u)
/** Peripheral PTA base pointer */
#define PTA ((GPIO_Type *)PTA_BASE)
/*System Integration Module Control Register */
//SIM->SCGC5  // Clock Control Register for GPIO Ports
#define SIM_SCGC5_PORTA_MASK              0x200u
```