ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY HOMEWORK REPORT

HOMEWORK NO	:	1
HOMEWORK DATE	:	10.03.2023
LAB SESSION	:	FRIDAY - 10.30
GROUP NO	:	G3

GROUP MEMBERS:

150200000 : Ahmet Emre Buz

150200001 : Mustafa Can Çalışkan

SPRING 2023

Contents

1 INTRODUCTION

In this experiment, we implemented and simulated desired designs using Verilog.

2 PRELIMINARY

For the given function

$$F(a, b, c, d) = \cup_1(1, 2, 5, 6, 9, 10, 13, 14) + \cup_d(4)$$

- Prime implicants using Karnaugh diagram:

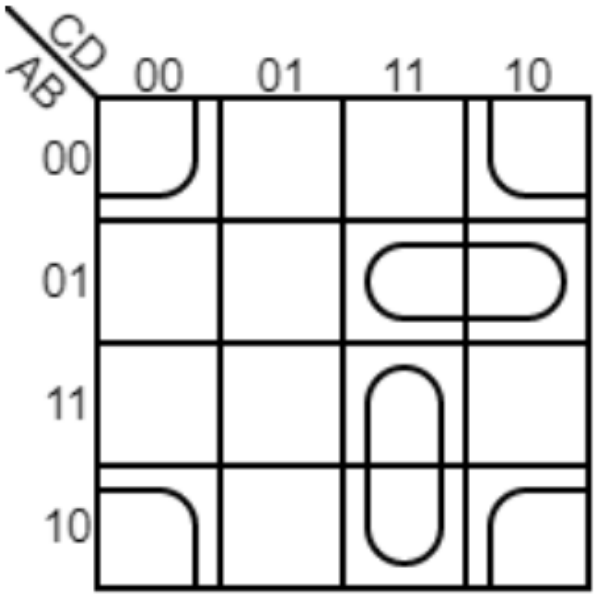

Figure 1: Karnaugh Map (created using the tool provided by boolean-algebra.com)

- Prime implicants using Quine-McCluskey method:

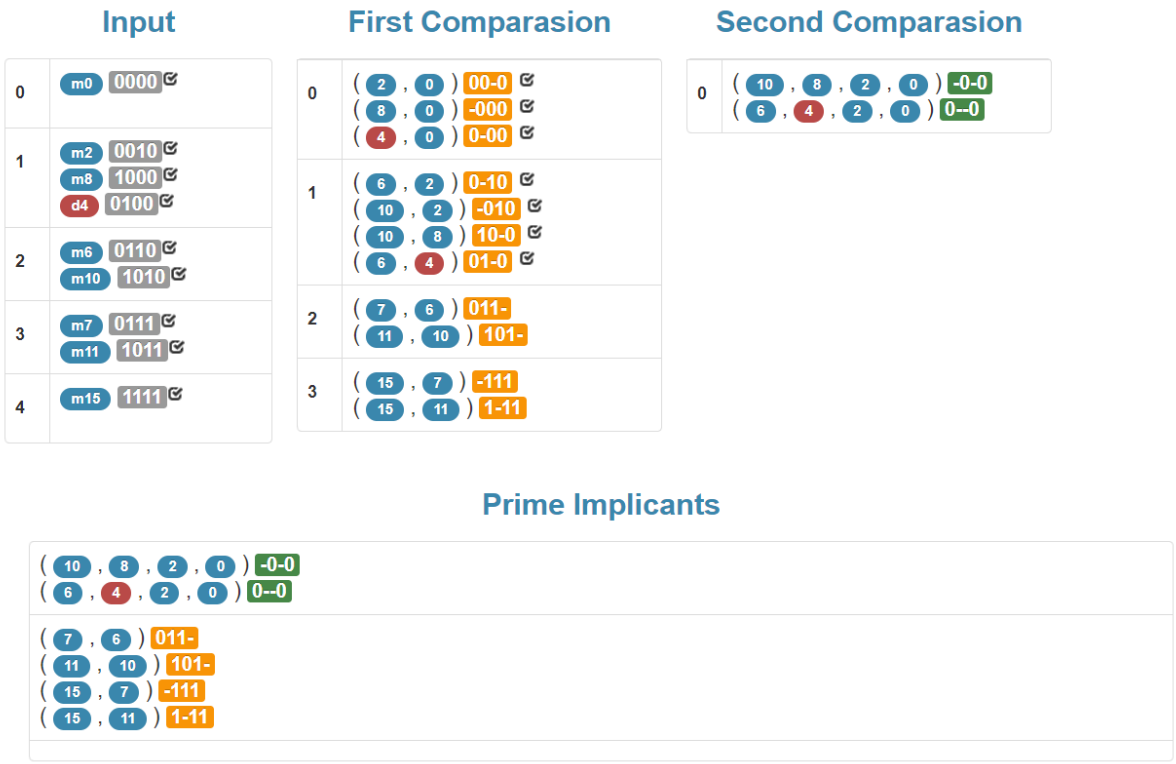

Figure 2: Quine-McCluskey Tables (created using the tool provided by quinemccluskey.com)

- Prime implicant chart and expression with the minimum cost:

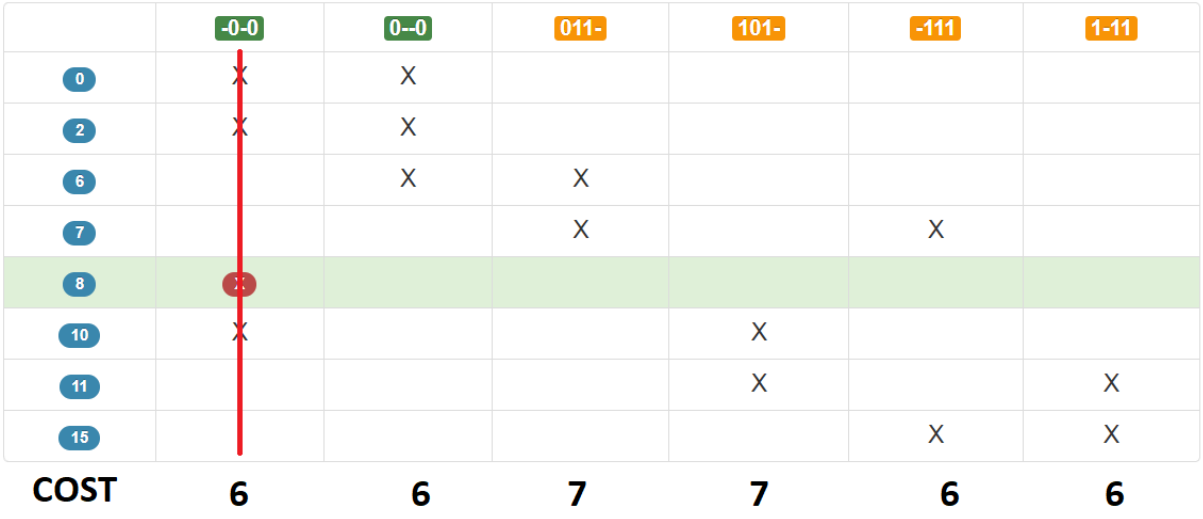

Figure 3: Prime implicant chart (created using the tool provided by quinemccluskey.com)

	0--0	011-	101-	-111	1-11
6	X	X			
7		X		X	
11			X		X
15				X	X
COST	6	7	7	6	6

Figure 4: Prime implicant chart (created using the tool provided by quinemccluskey.com)

Expression with the minimum cost:

$$F(a, b, c, d) = acd + a'bc + b'd'$$

- Lowest cost expression using NOT, AND, and OR gates:

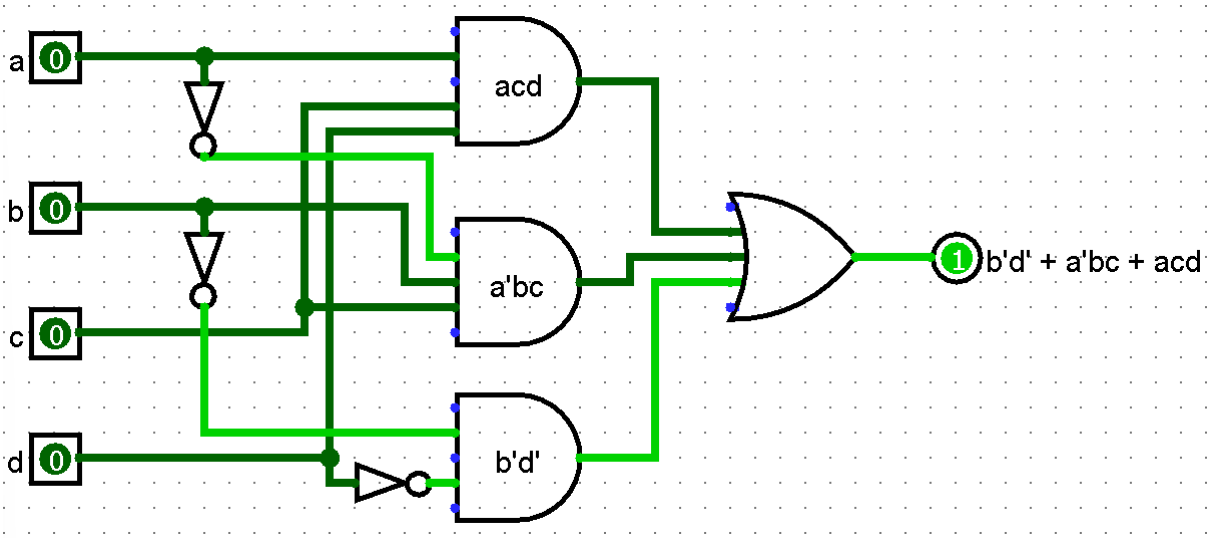

Figure 5: Design

a	b	c	d	bdAbcAcd
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Figure 6: Truth Table of Design

- Lowest cost expression using only NAND gates:

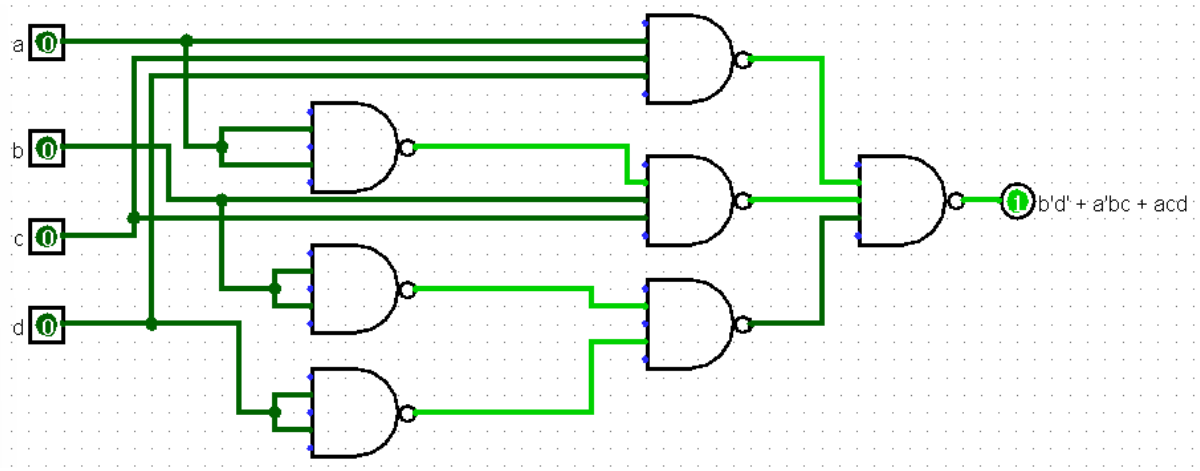

Figure 7: Design

a	b	c	d	bdAbcAcd
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Figure 8: Truth Table

- Lowest cost expression using a single 8:1 Multiplexer, AND, OR and NOT gates:

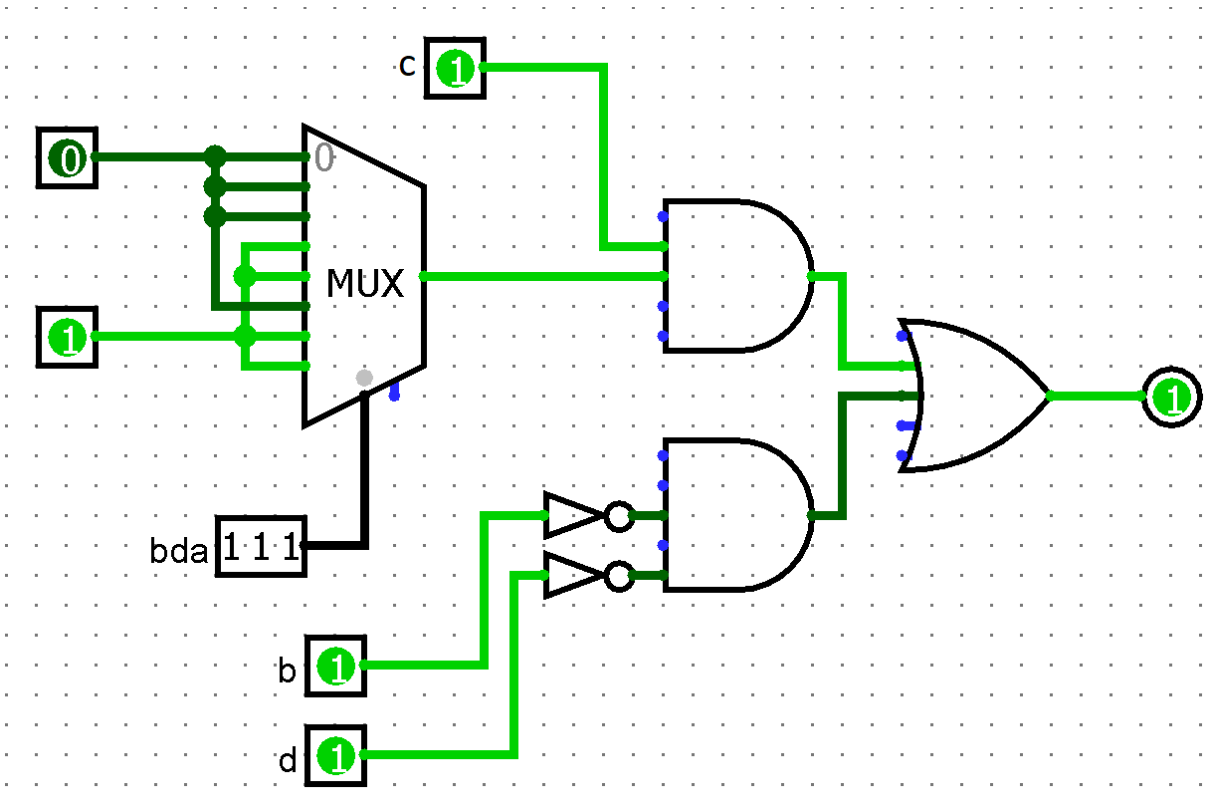

Figure 9: Design

b	d	a	c	$((\neg b \wedge \neg d) \vee ((\neg a \wedge b) \wedge c)) \vee ((a \wedge c) \wedge d)$	
1	1	1	1	1	C
1	1	1	0	0	
1	1	0	1	1	C
1	1	0	0	0	
1	0	1	1	0	0
1	0	1	0	0	
1	0	0	1	1	C
1	0	0	0	0	
0	1	1	1	1	C
0	1	1	0	0	
0	1	0	1	0	0
0	1	0	0	0	
0	0	1	1	1	1
0	0	1	0	1	
0	0	0	1	1	1
0	0	0	0	1	

Figure 10: Truth Table (created using the tool provided by emathhelp.net)

For the given function

$$F(a, b, c) = a'bc + ab'c$$

- Expression using ONE single 3:8 decoder, 2-input OR gates:

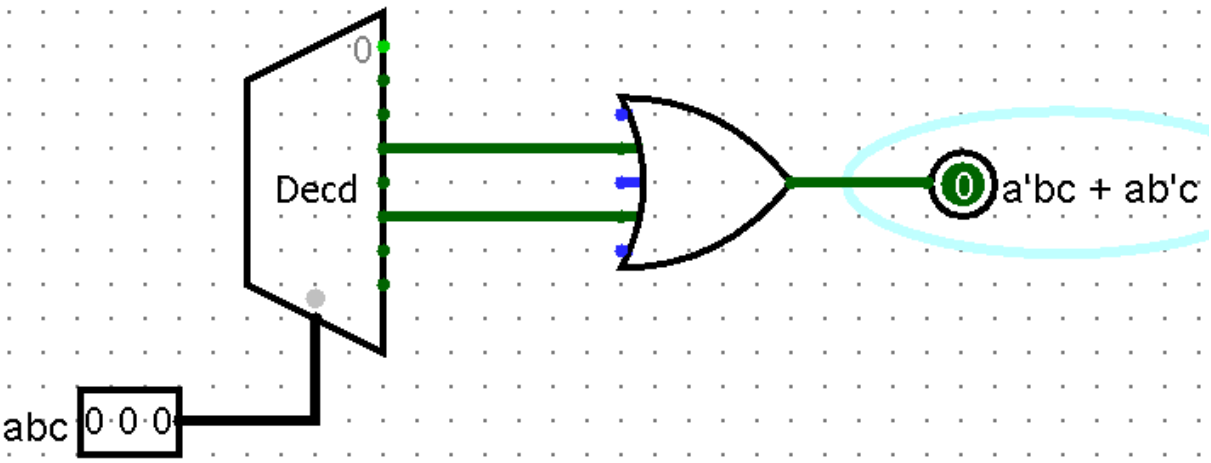

Figure 11: Design

a	b	c	$((\neg a \wedge b) \wedge c) \vee ((a \wedge \neg b) \wedge c)$
1	1	1	0
1	1	0	0
1	0	1	1
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	0
0	0	0	0

Figure 12: Truth Table (created using the tool provided by emathhelp.net)

For the given function

$$F(a, b, c) = abc' + ab$$

- Expression using ONE single 3:8 decoder, 2-input OR gates:

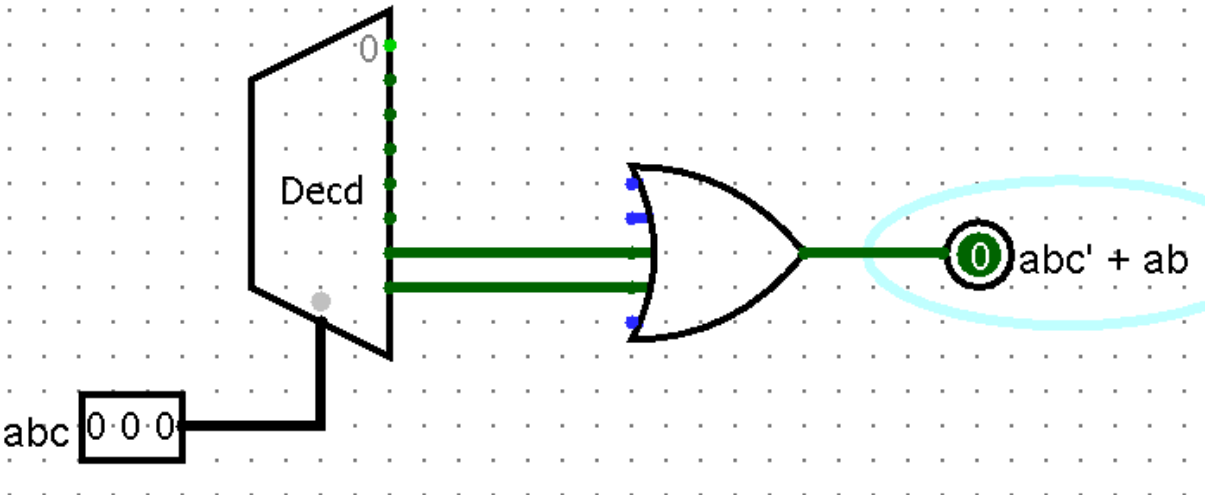

Figure 13: Design

a	b	c	$((a \wedge b) \wedge \neg c) \vee (a \wedge b)$
1	1	1	1
1	1	0	1
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

Figure 14: Truth Table (created using the tool provided by emathhelp.net)

3 EXPERIMENT

3.1 PART 1

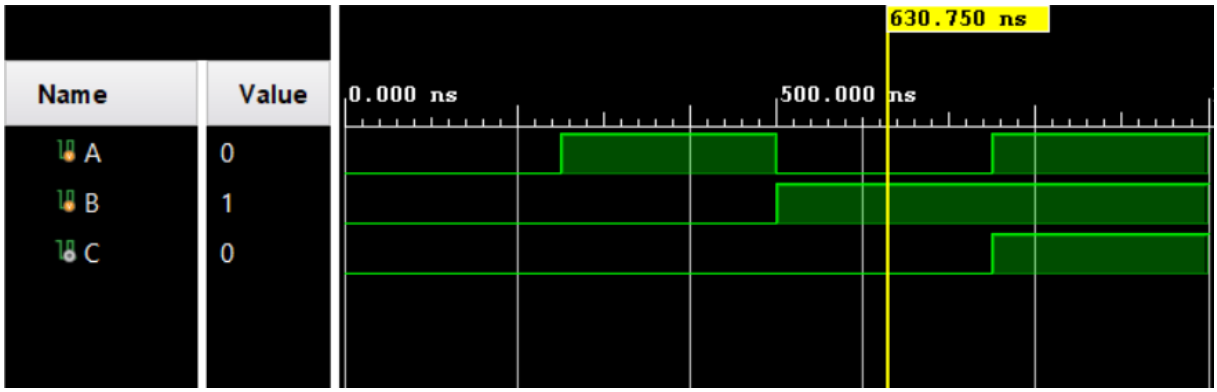

Figure 15: AND Gate Simulation Output

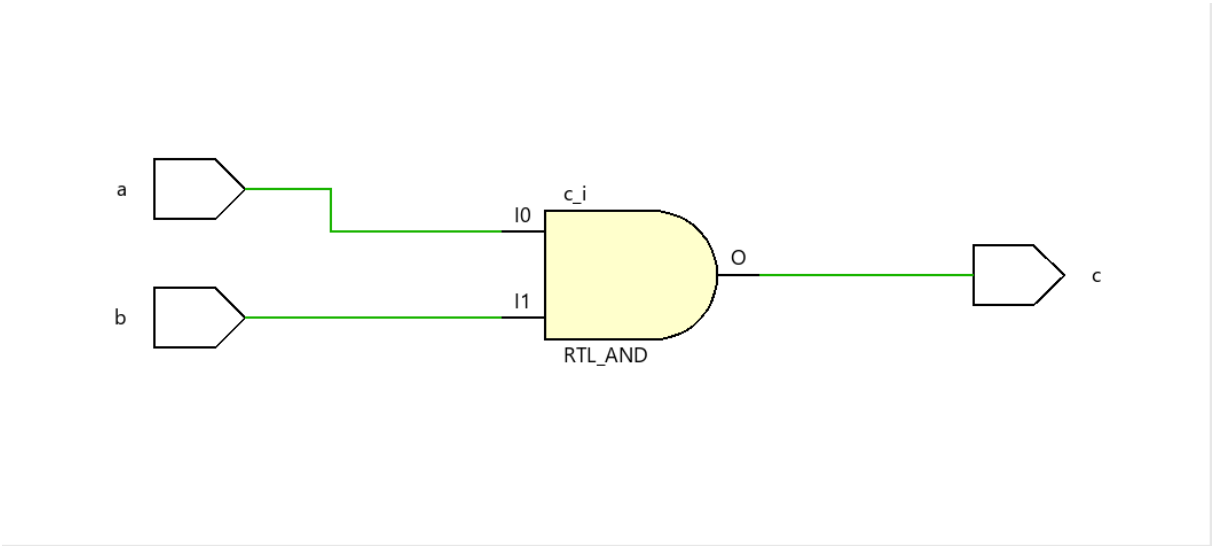

Figure 16: AND Gate Circuit

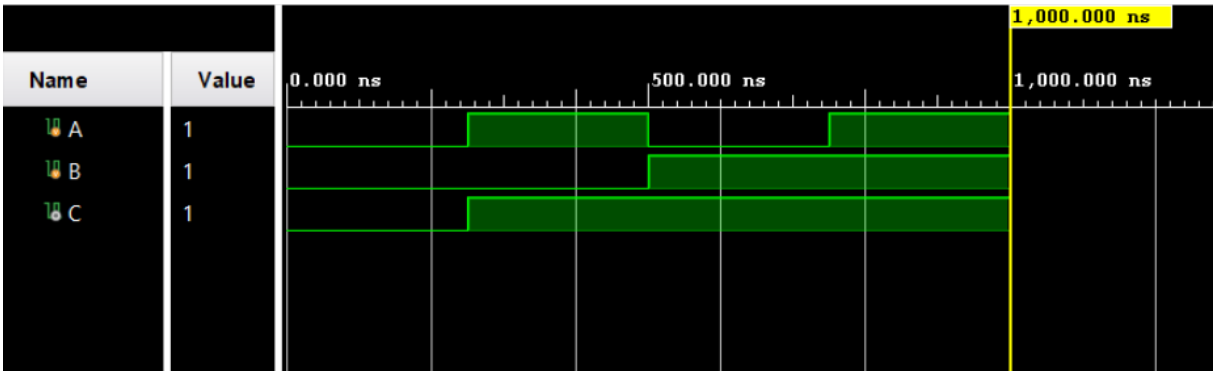

Figure 17: OR Gate Simulation Output

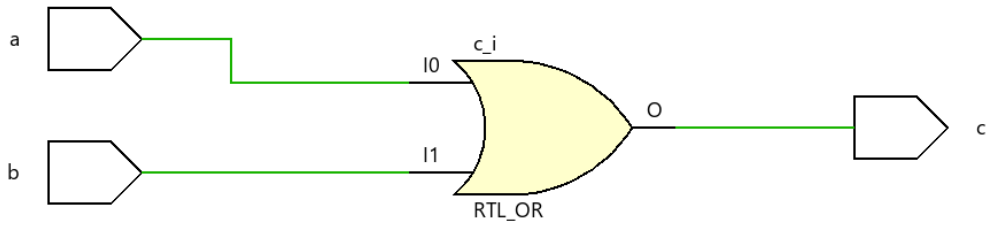

Figure 18: OR Gate Circuit

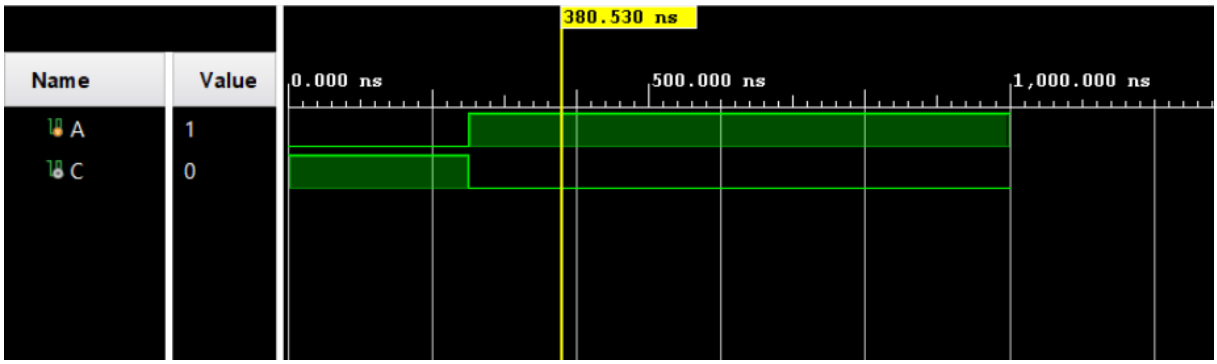

Figure 19: NOT Gate Simulation Output

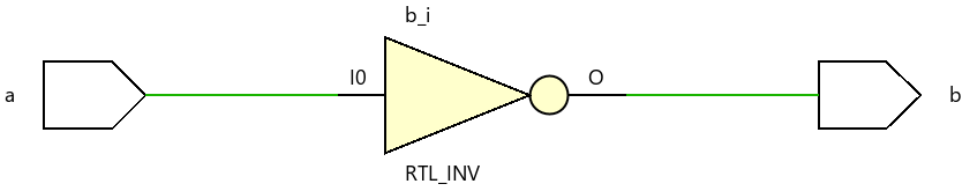

Figure 20: NOT Gate Circuit

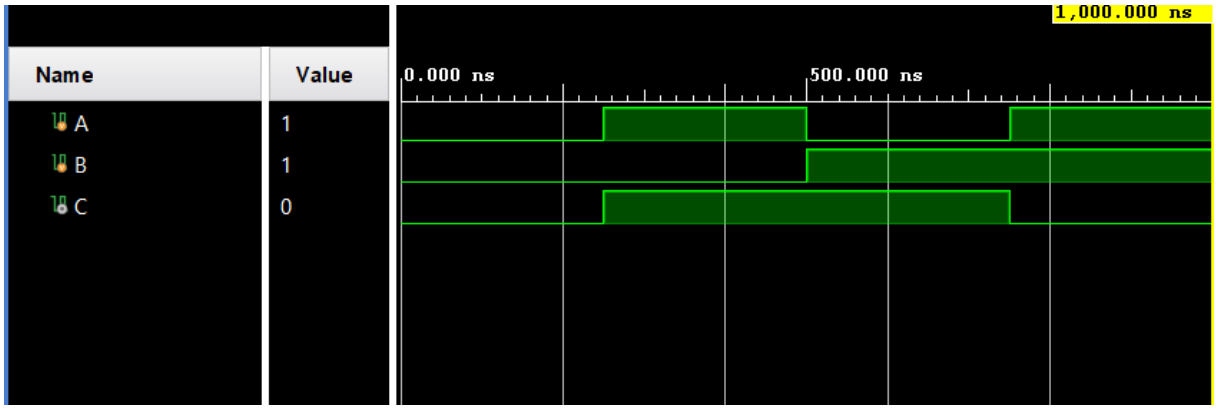

Figure 21: XOR Gate Simulation Output

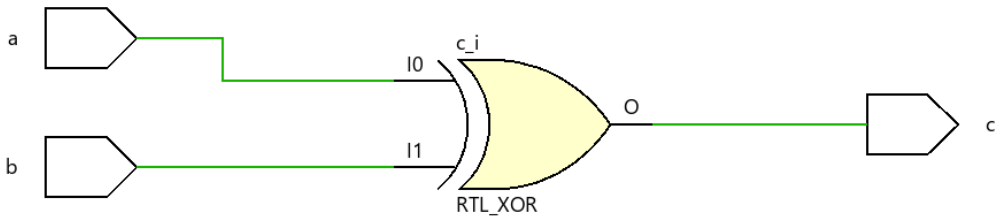

Figure 22: XOR Gate Circuit

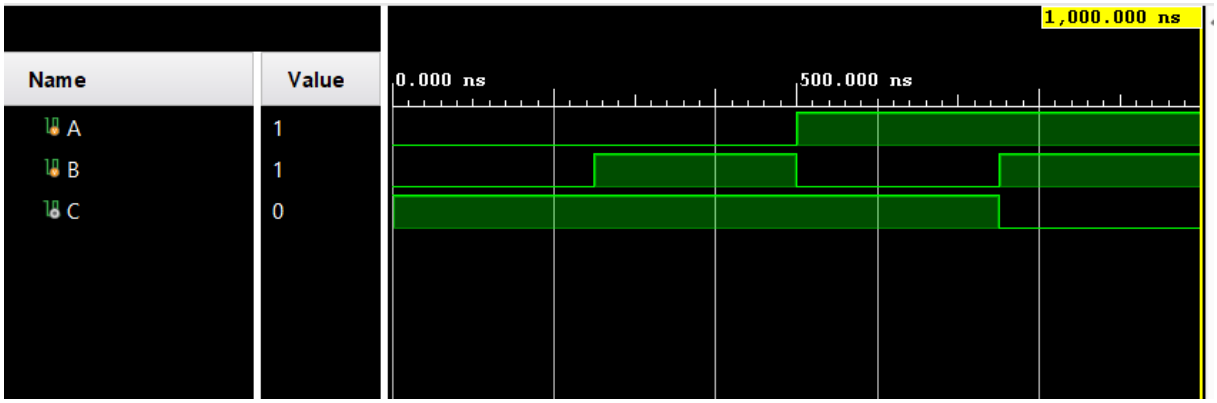

Figure 23: NAND Gate Simulation Output

Figure 24: NAND Gate Circuit

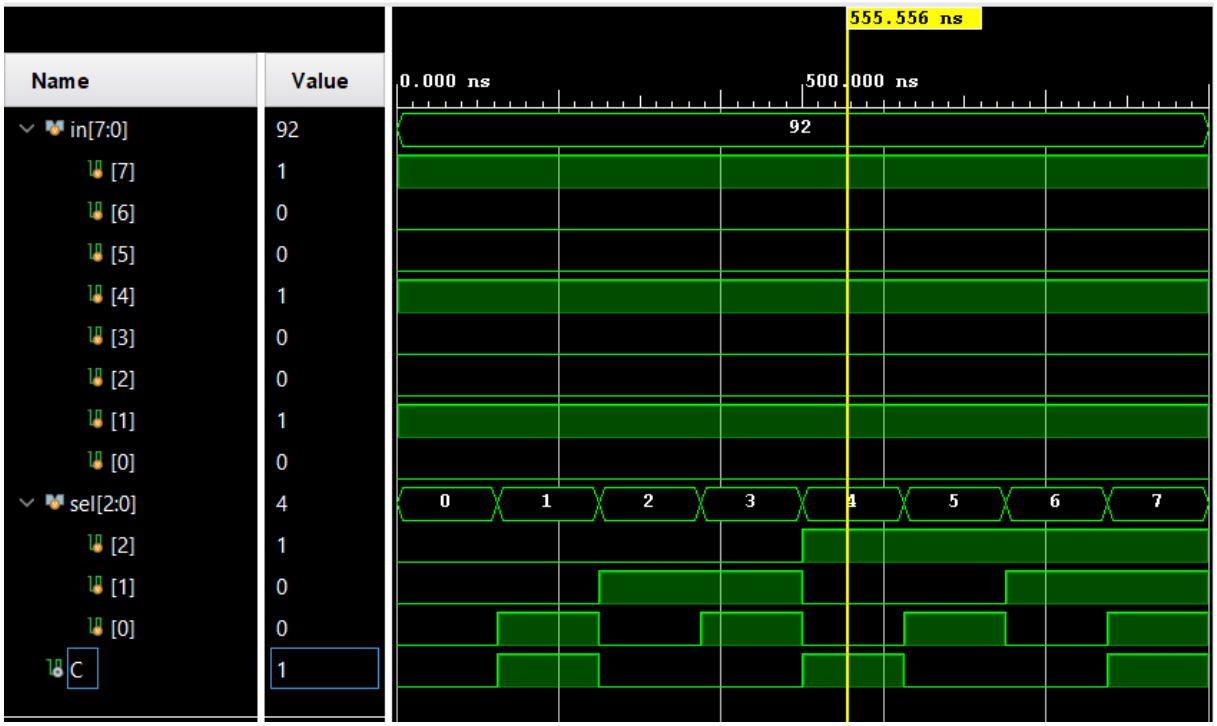

Figure 25: 8:1 Multiplexer Simulation Output

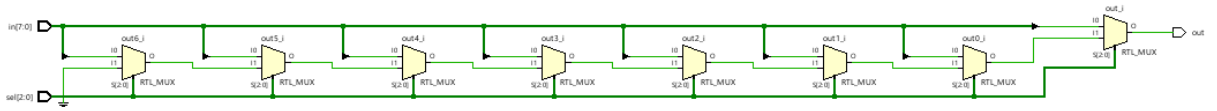

Figure 26: 8:1 Multiplexer Circuit

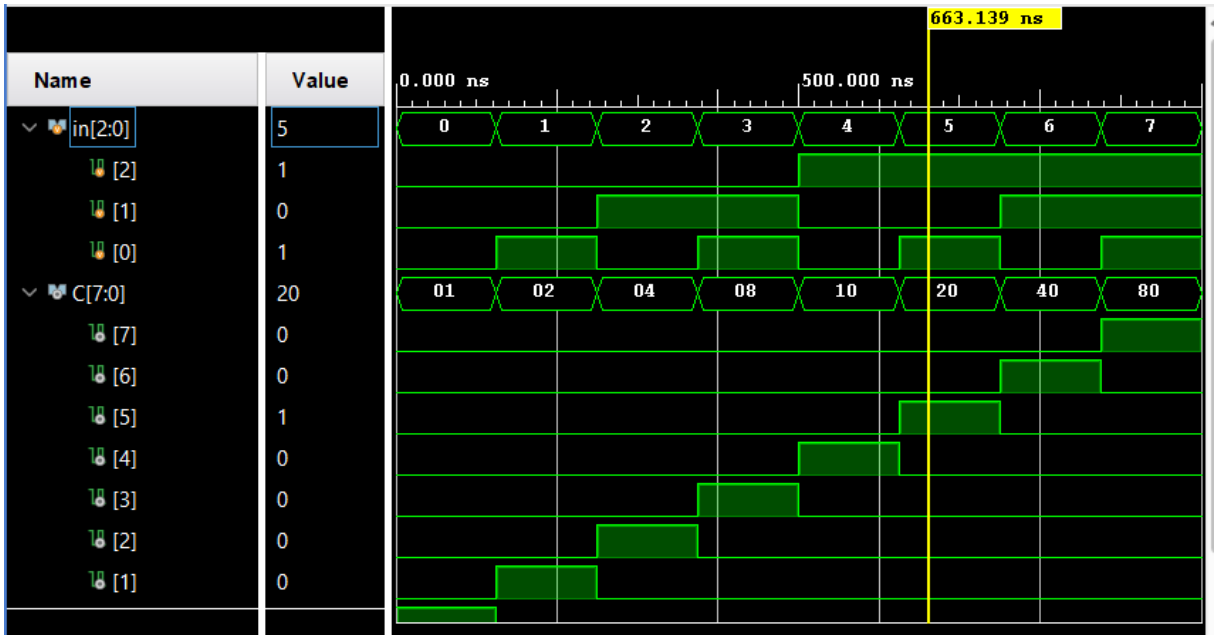

Figure 27: 3:8 Decoder Simulation Output

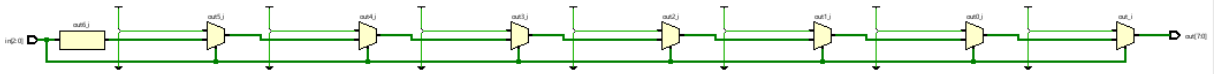

Figure 28: 3:8 Decoder Circuit

3.2 PART 2

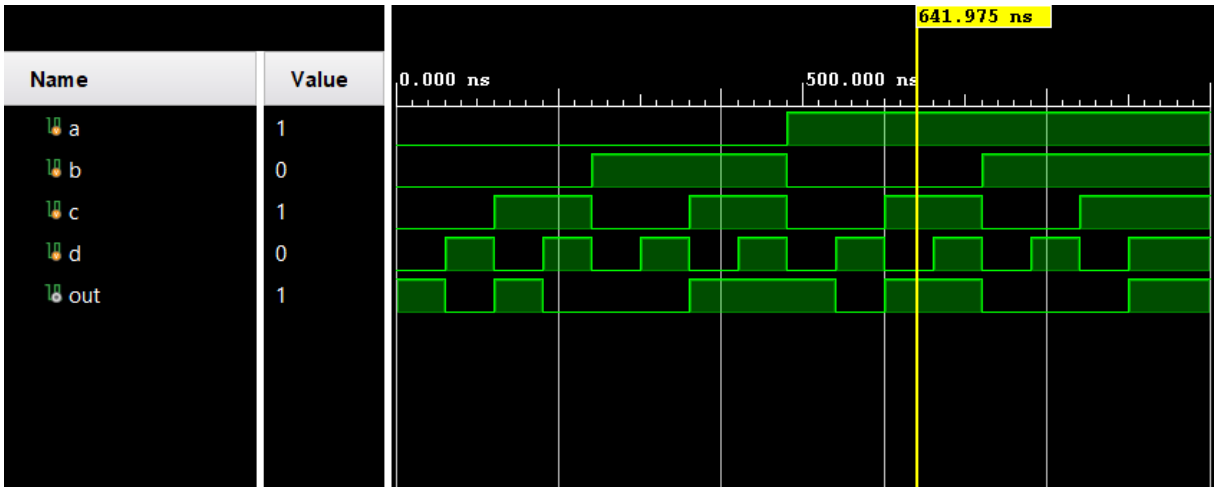

Figure 29: Part 2 Simulation Output

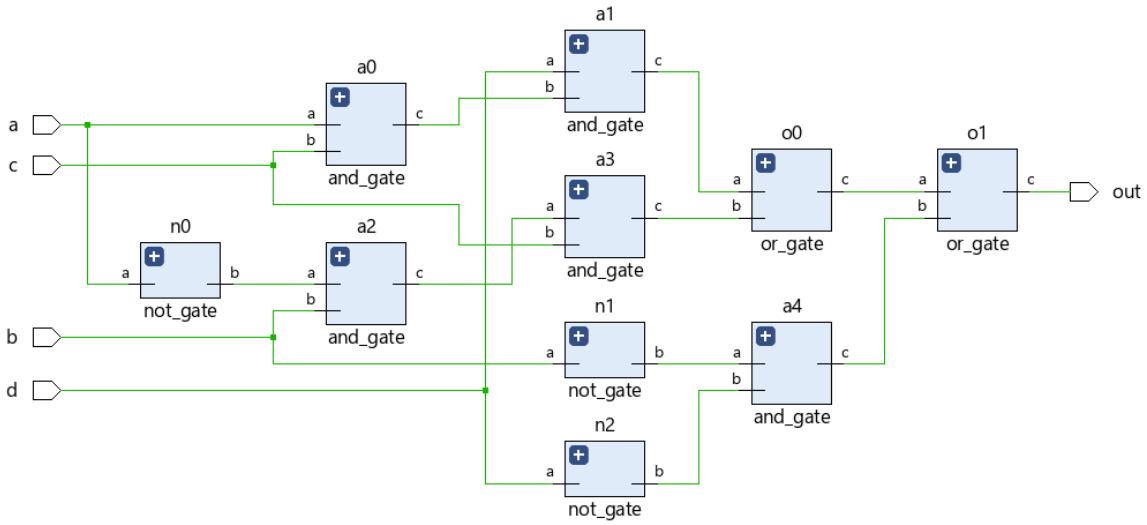

Figure 30: Circuit of Part 2

3.3 PART 3

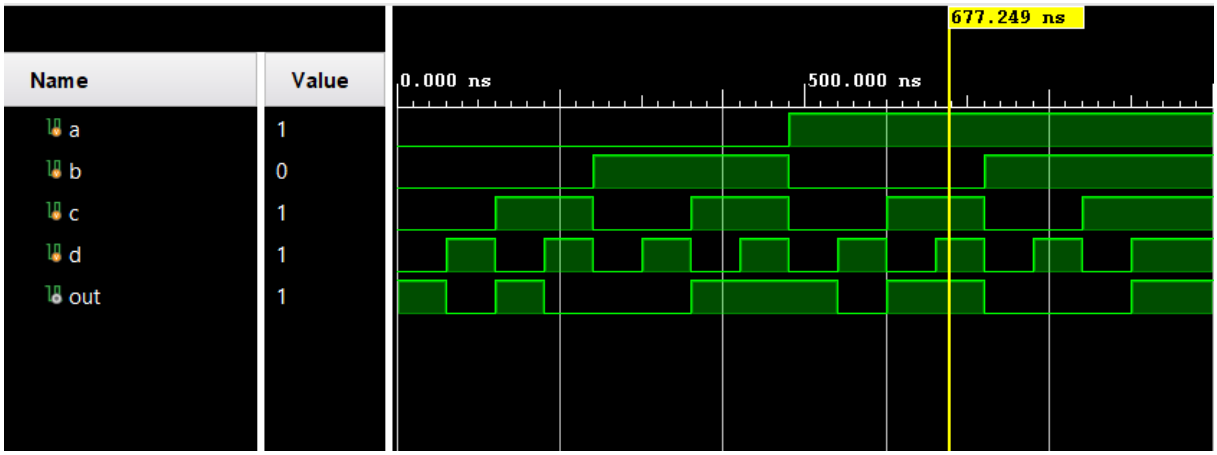

Figure 31: Part 3 Simulation Output

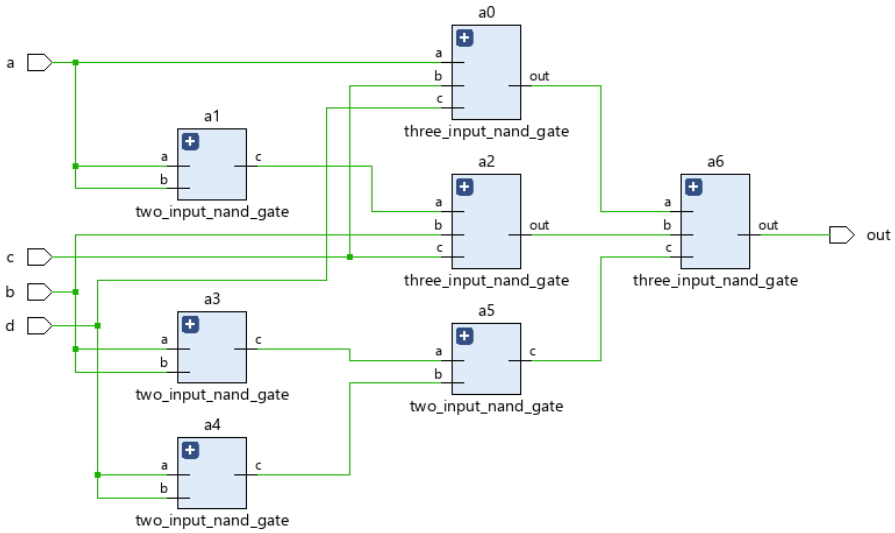

Figure 32: Circuit of Part 3

3.4 PART 4

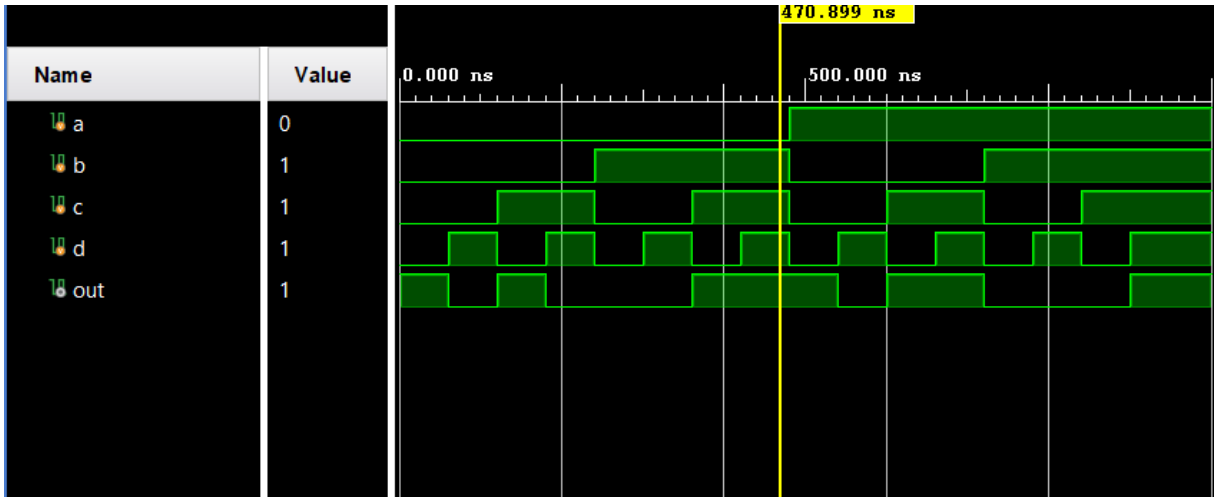

Figure 33: Part 4 Simulation Output

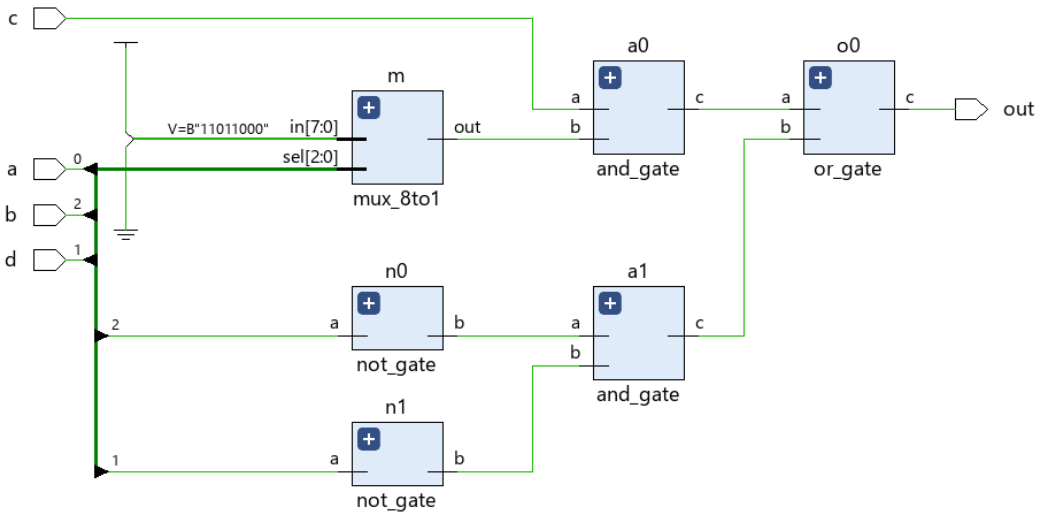

Figure 34: Circuit of Part 4

3.5 PART 5

- Equation 2

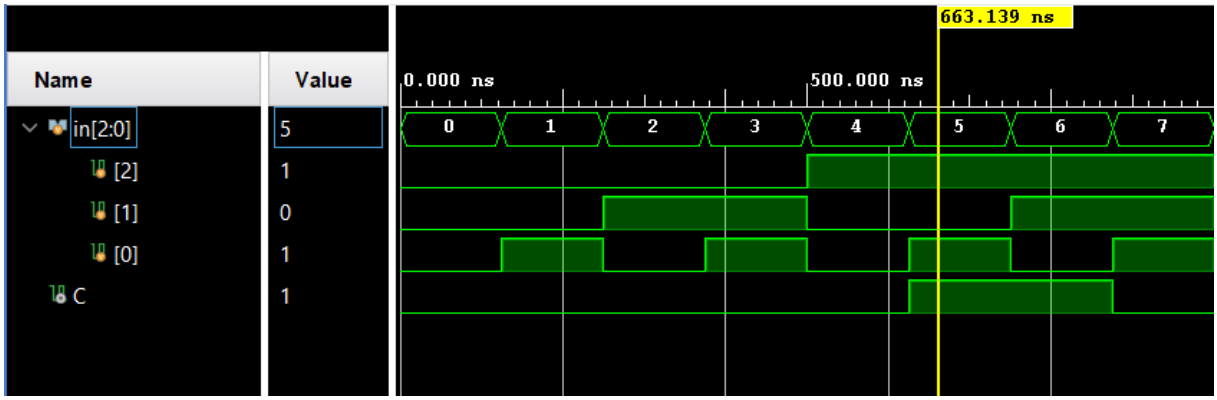

Figure 35: Simulation Output

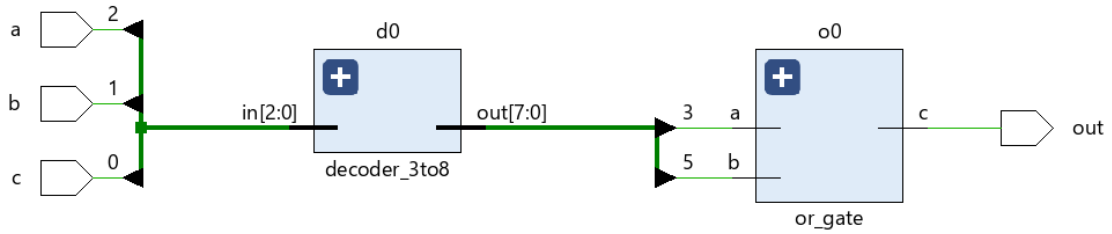

Figure 36: Circuit

- Equation 3

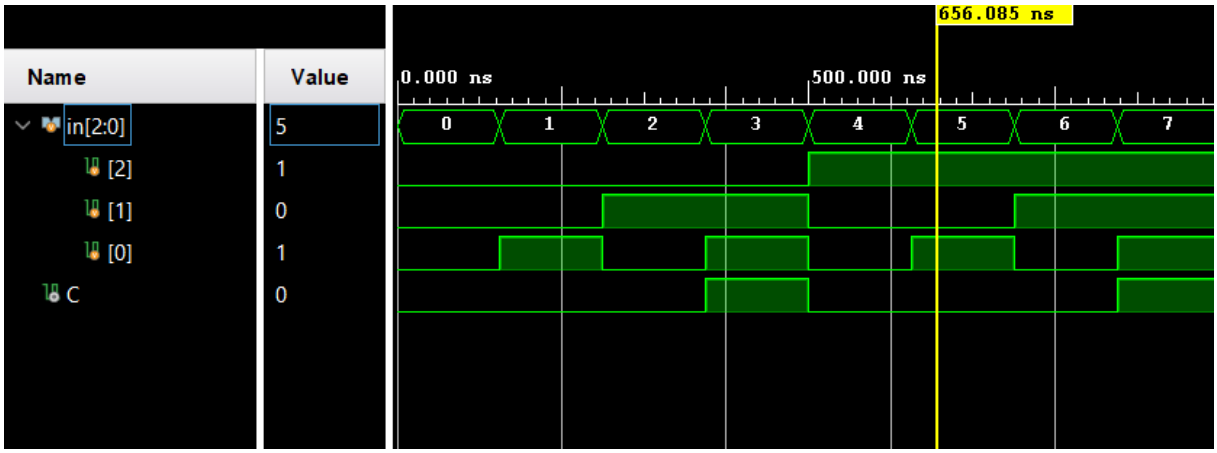

Figure 37: Simulation Output

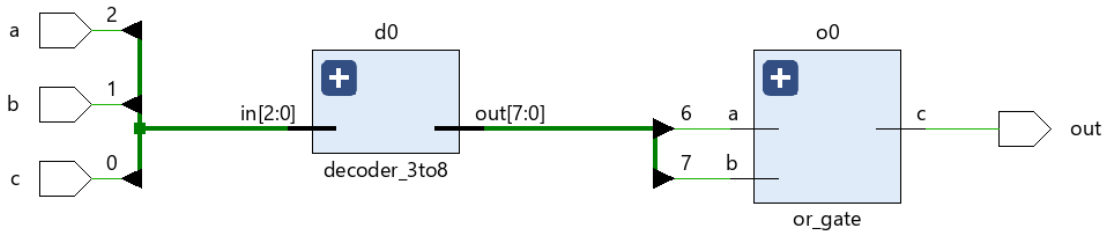

Figure 38: Circuit

3.6 PART 6

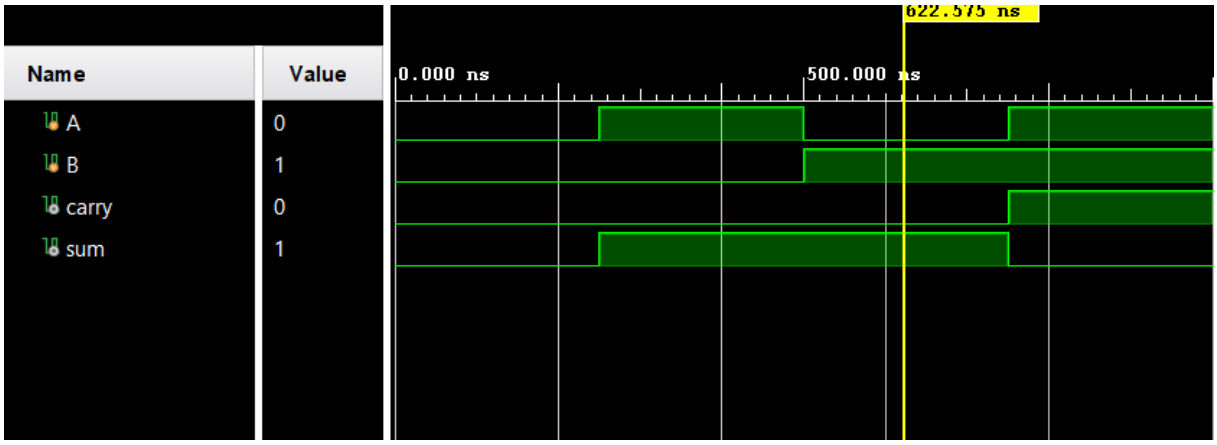

Figure 39: Simulation Output of Half Adder

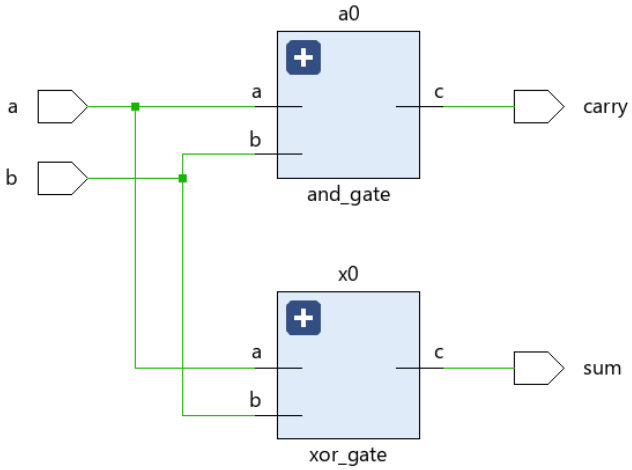

Figure 40: Circuit of Half Adder

3.7 PART 7

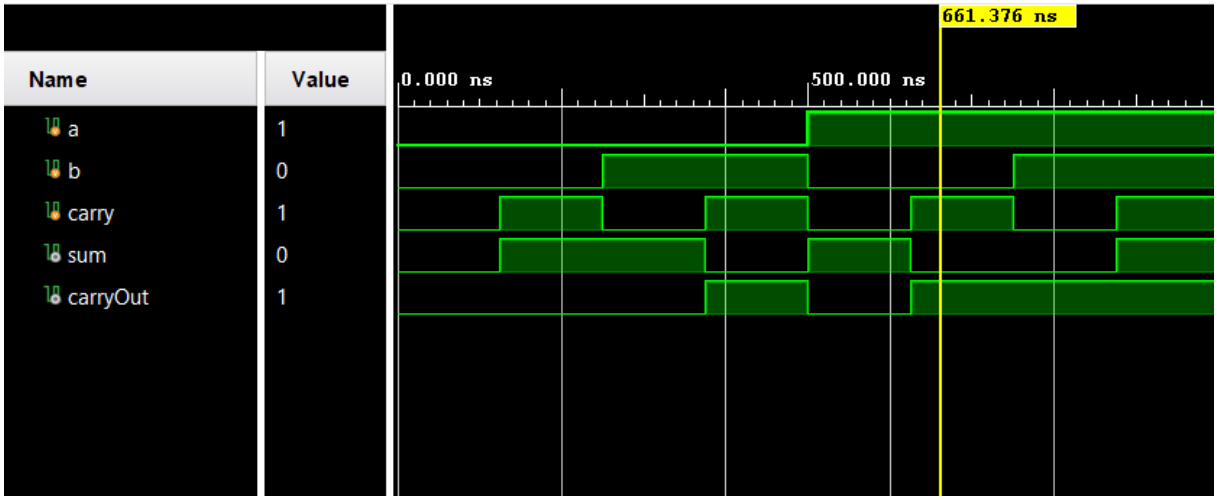

Figure 41: Simulation Output of 1-bit Full Adder

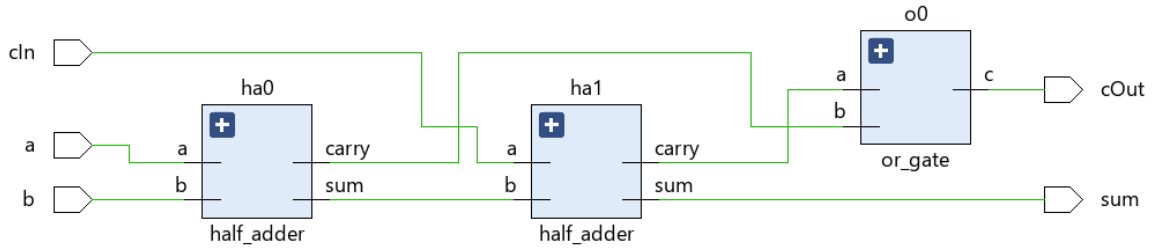

Figure 42: Circuit of 1-bit Full Adder

3.8 PART 8 [7 points]

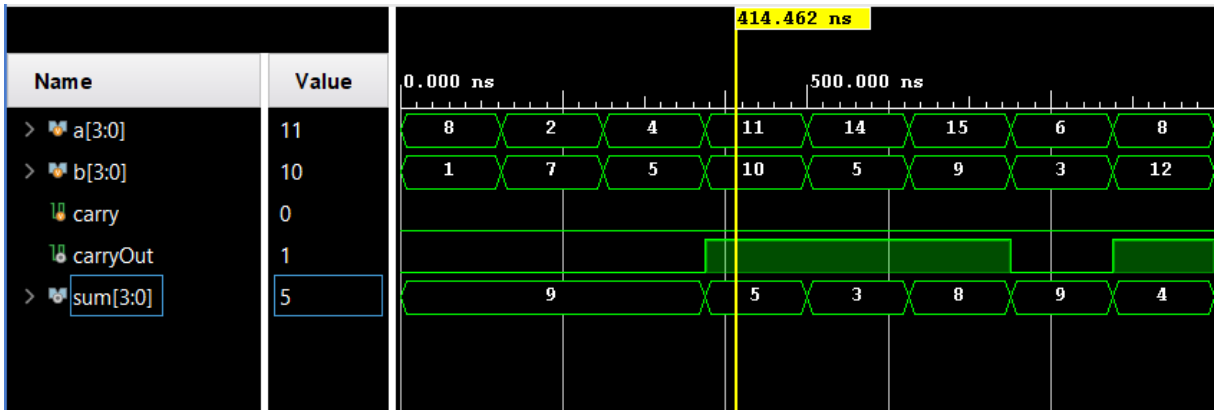

Figure 43: Simulation Output of 4-bit Full Adder

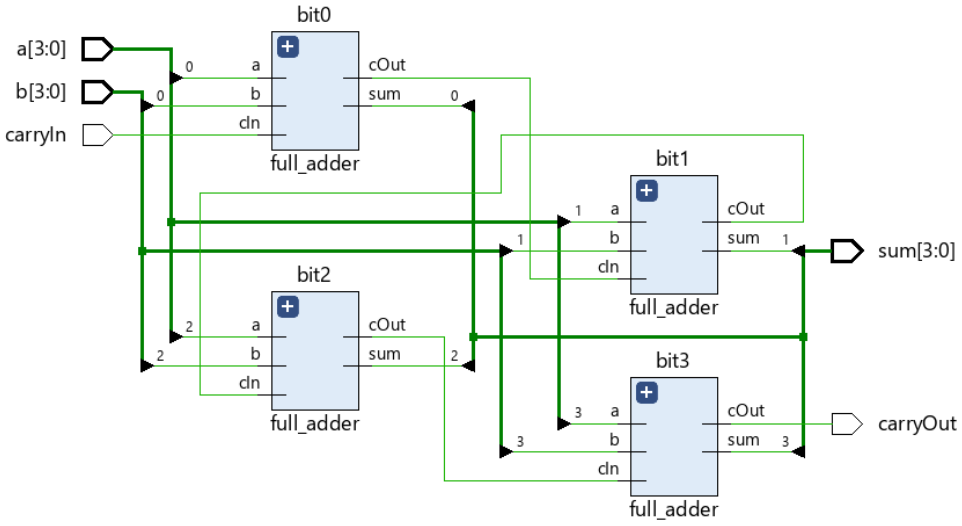

Figure 44: Circuit of 4-bit Full Adder

3.9 PART 9

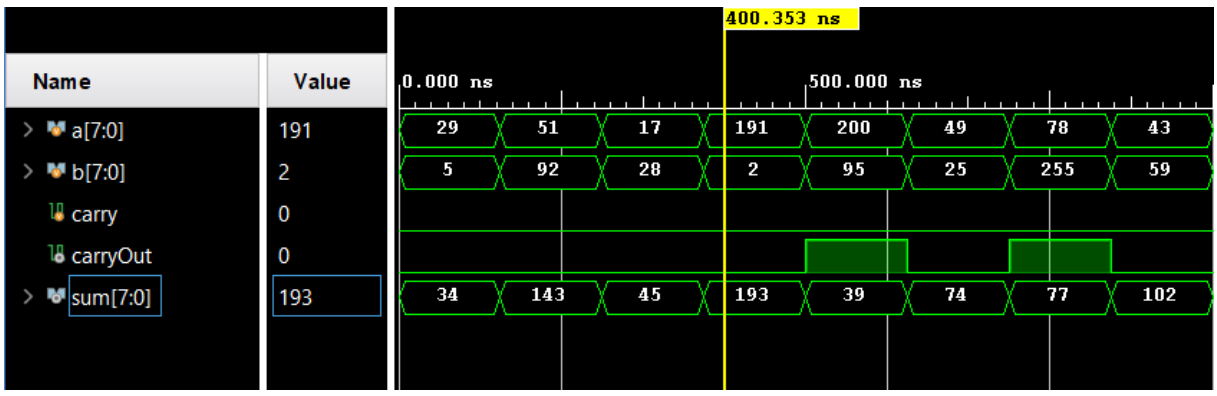

Figure 45: Simulation Output of 8-bit Full Adder

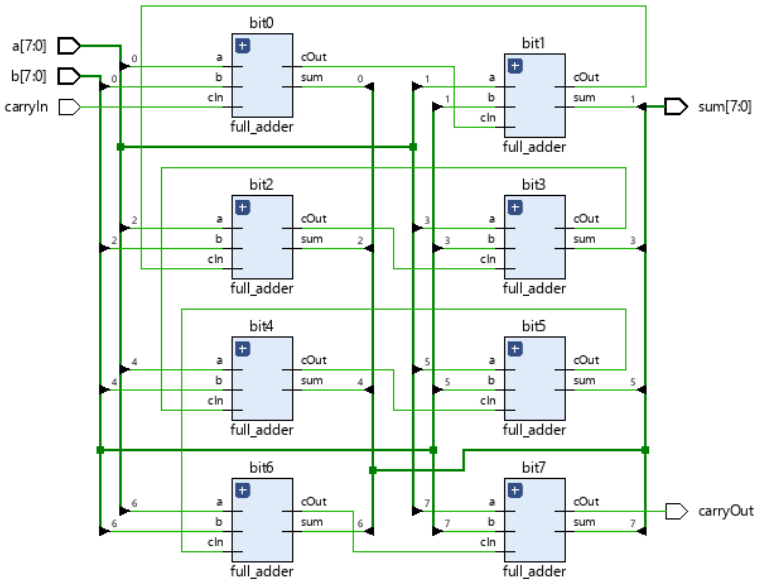

Figure 46: Circuit of 8-bit Full Adder

3.10 PART 10

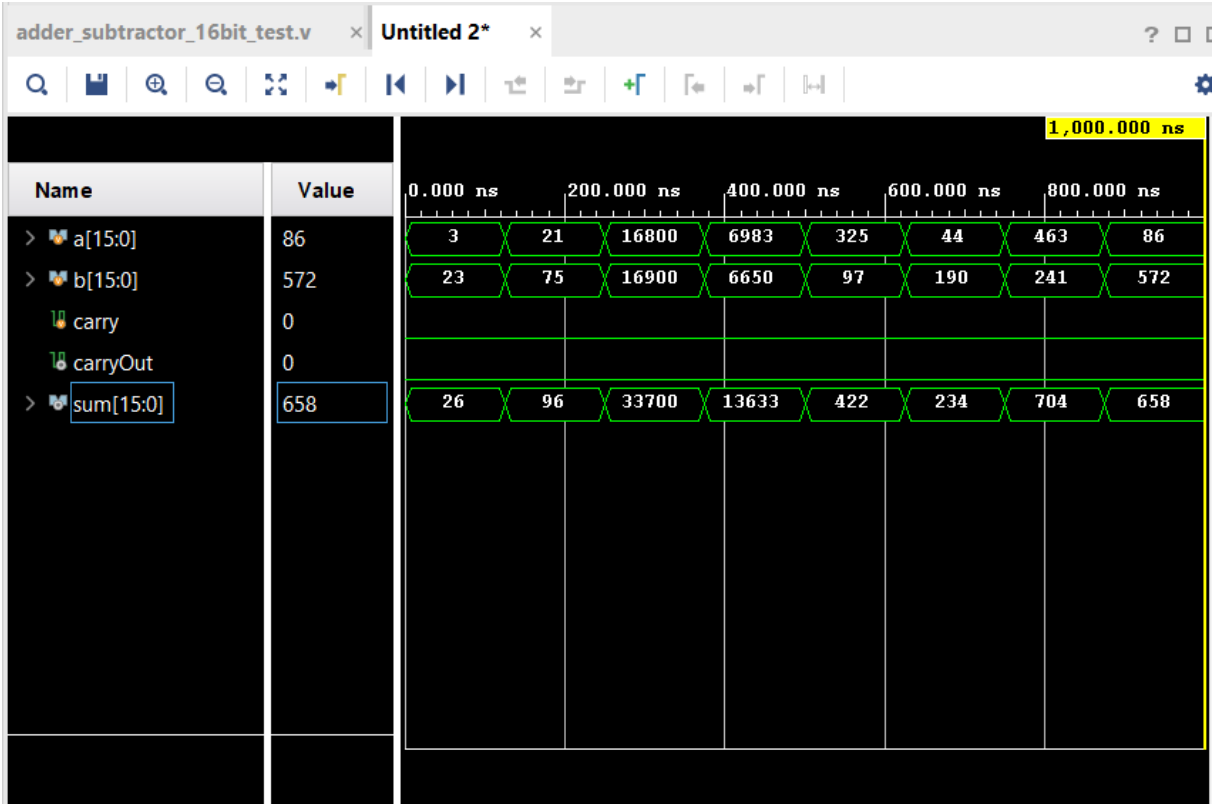

Figure 47: Simulation Output of 16-bit Adder-Subtractor

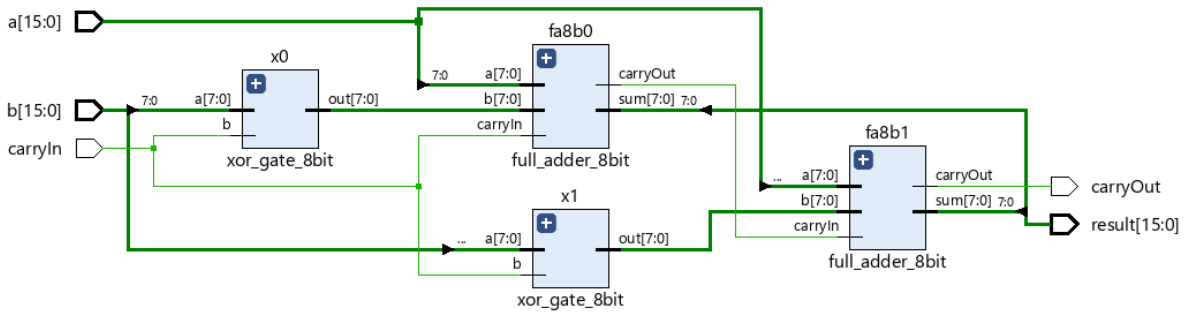

Figure 48: Circuit of 16-bit Adder-Subtractor

3.11 PART 11

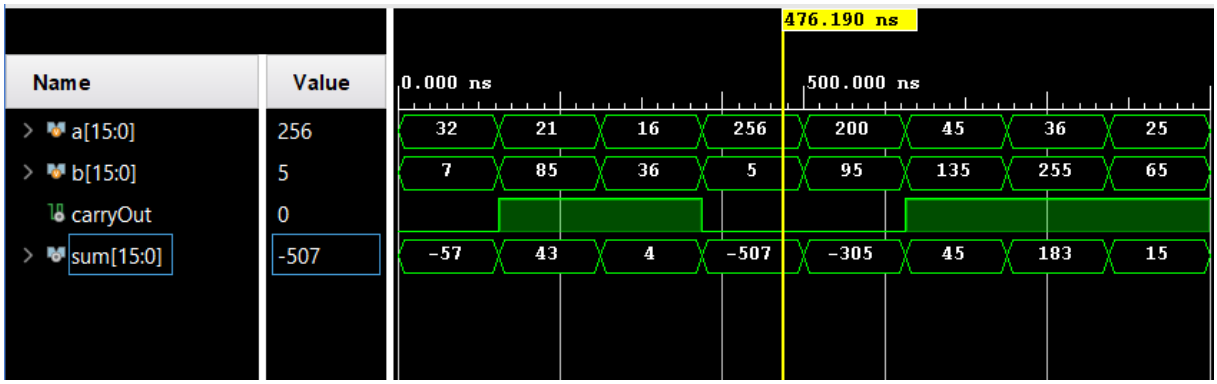

Figure 49: Simulation Output of B - 2A Expression

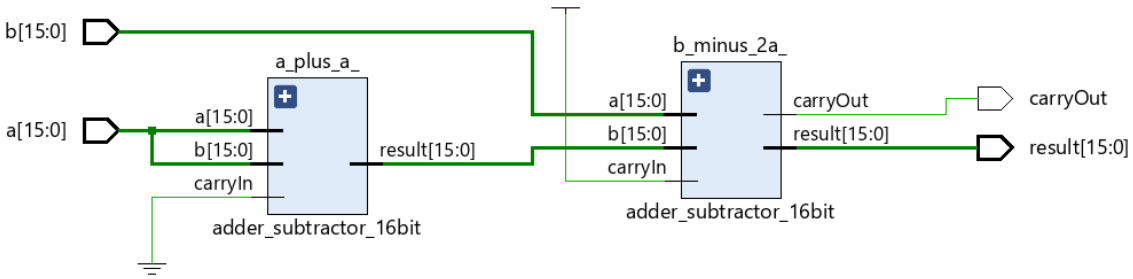

Figure 50: Circuit of B - 2A Expression

4 CONCLUSION

In this experiment, we implemented and simulated desired designs using Verilog.

REFERENCES