ISTANBUL TECHNICAL UNIVERSITY

COMPUTER ENGINEERING DEPARTMENT

BLG 242E

DIGITAL CIRCUITS LABORATORY EXPERIMENT REPORT

EXPERIMENT NO	:	1
EXPERIMENT DATE	:	10.03.2028
LAB SESSION	:	FRIDAY - 10.30
GROUP NO	:	G3

GROUP MEMBERS:

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Contents

1 INTRODUCTION

In this experiment, we observed given axioms and theorems, and implemented them in the experimental environments.

2 PRELIMINARY

$$a + a.b = a \qquad (1)$$

$$(a + b)(a + b') = a \qquad (2)$$

- Proving the given equality (1) by using the axioms of Boolean algebra:

$$a + a.b$$

$$a.(1 + b) \rightarrow \text{Distributivity}$$

$$a \rightarrow \text{Identity}$$

- Proving the given equality (2) by using the axioms of Boolean algebra:

$$(a + b)(a + b')$$

$$a + (b.b') \rightarrow \text{Distributivity}$$

$$a + 0 \rightarrow \text{Inverse}$$

$$a \rightarrow \text{Identity}$$

- Determine and prove the dual of the equality (1):

$$a + a.b \xrightarrow{dual} a.(a + b)$$

$$a.(a + b)$$

$$a.a + a.b \rightarrow \text{Distributivity}$$

$$a + a.b \rightarrow \text{Idempotency}$$

- Determine and prove the dual of the equality (2):

$$(a + b)(a + b') \xrightarrow{dual} (a.b) + (a.b')$$

$$(a.b) + (a.b')$$

$$a.(b + b') \rightarrow \text{Distributivity}$$

$$a + 1 \rightarrow \text{Inverse}$$

$$a = (a.b) + (a.b') = (a + b)(a + b')$$

- Complement of

$$F = ab + a'c$$

is:

$$F' = (a' + b').(a + c') \rightarrow \text{De Morgan's Rule}$$

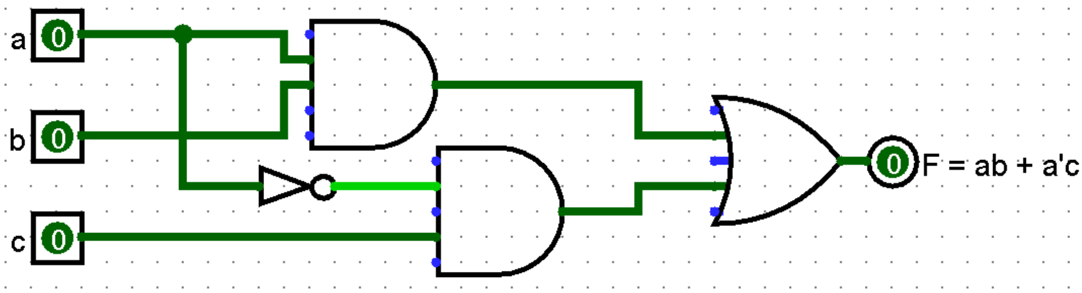

Figure 1: Design of F

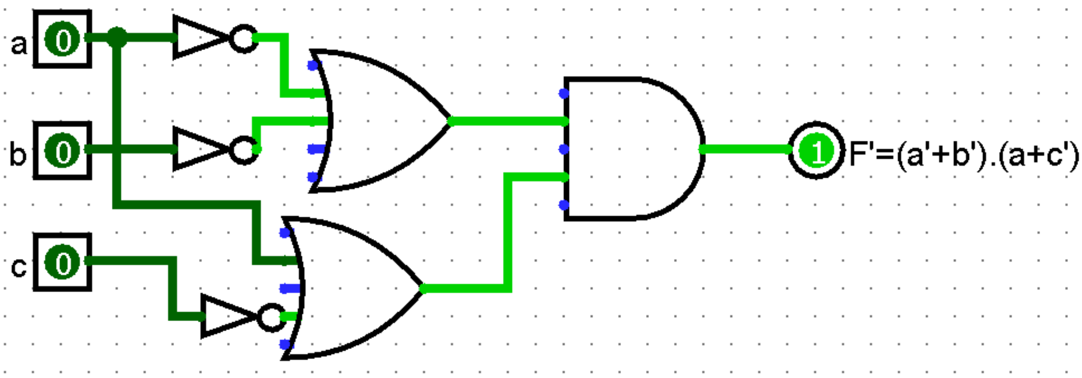

Figure 2: Design of F'

- Simplification of given function:

$$F(a,b,c,d) = \cup_1(1,2,5,6,9,10,13,14)$$

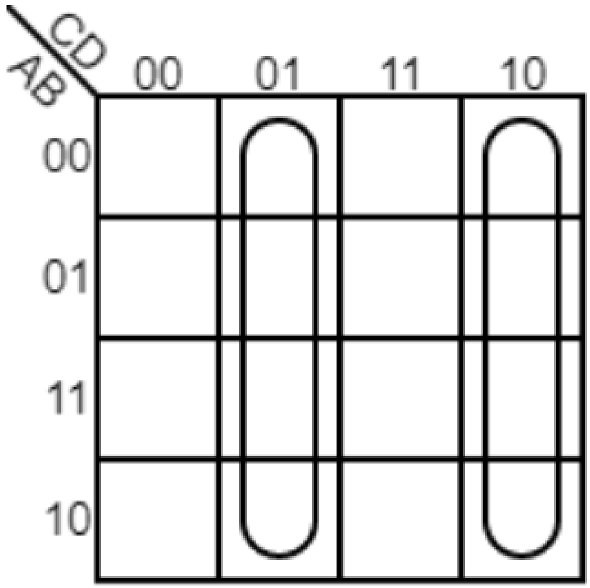

Figure 3: Karnaugh Map (created using the tool provided by boolean-algebra.com)

Expression obtained from Karnaugh map is:

$$F(a,b,c,d) = c'd + cd'$$

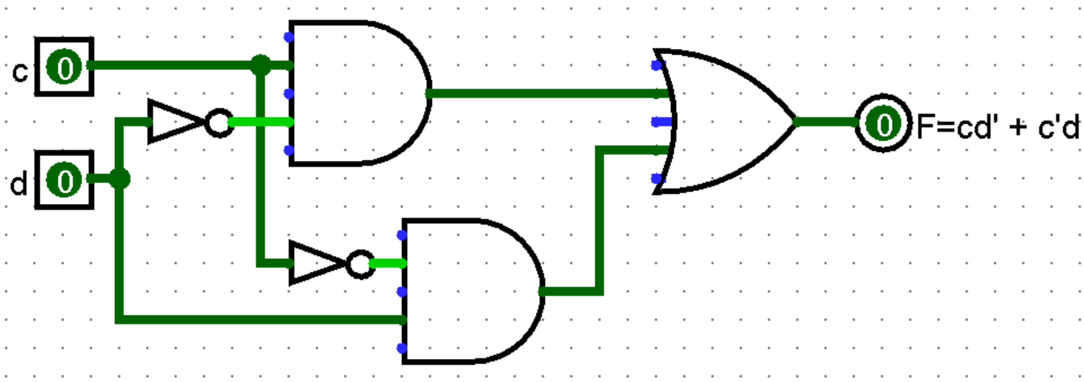

Figure 4: Design of F

3 EXPERIMENT

3.1 Part 1

In the first part of the experiment, 1 AND, 1 OR and 1 NOT gates are used to implement given expressions. The circuits below are designed.

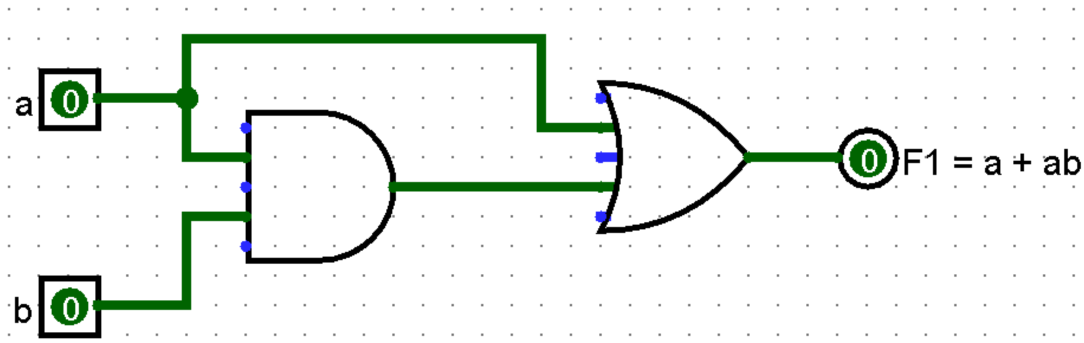

Figure 5: Design of F1

a	b	F1AAb
0	0	0
0	1	0
1	0	1
1	1	1

Figure 6: Truth Table of F1

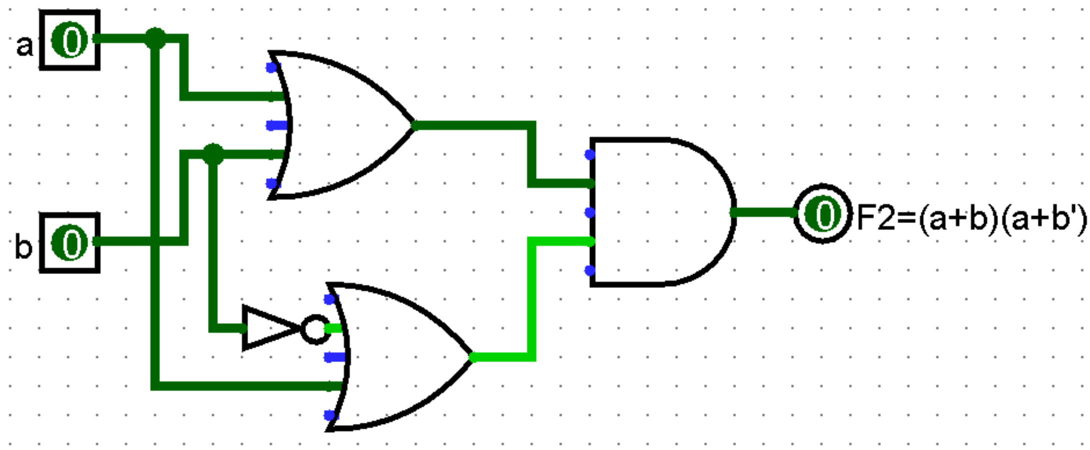

Figure 7: Design of F2

a	b	F2abab
0	0	0
0	1	0
1	0	1
1	1	1

Figure 8: Truth Table of F2

Moreover, these circuits are tested on C.A.D.E.T using a 7404 Hex Inverter, a 7408 Quadruple 2-input Positive-AND Gate and a 7432 Quadruple 2-input Positive-OR Gate.

3.2 Part 2

In the second part of the experiment, we determined the dual of the given theorem:

$$a + a.b \xrightarrow{dual} a.(a + b)$$

and implemented using AND and OR gates. The circuits below are designed.

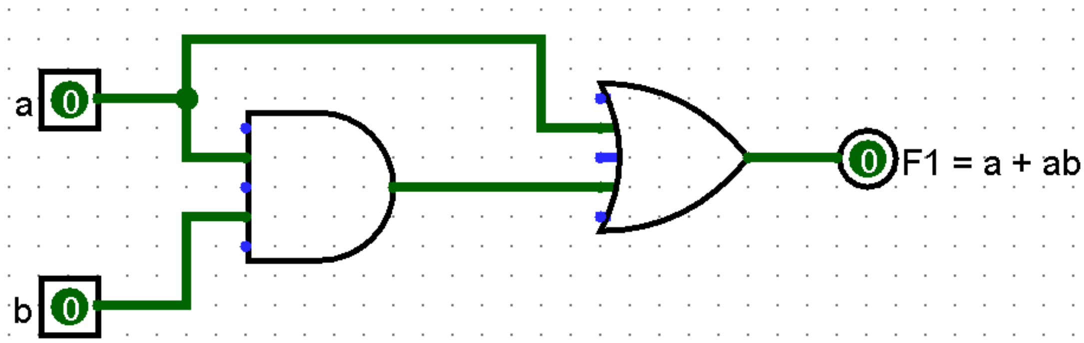

Figure 9: Design of F

a	b	F1AAb
0	0	0
0	1	0
1	0	1
1	1	1

Figure 10: Truth Table of F

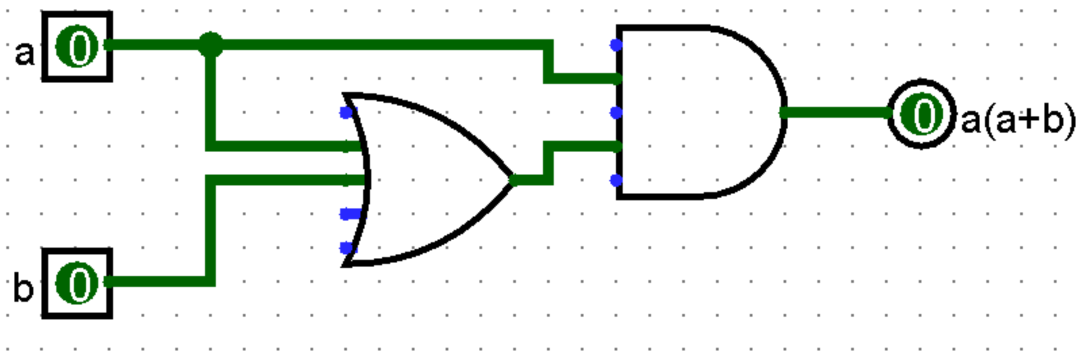

Figure 11: Design of Dual

a	b	aab
0	0	0
0	1	0
1	0	1
1	1	1

Figure 12: Truth Table of Dual

Moreover, these circuits are tested on C.A.D.E.T using a 7408 Quadruple 2-input Positive-AND Gate and a 7432 Quadruple 2-input Positive-OR Gate.

3.3 Part 3

In the third part of the experiment, we determined the complement of the given function:

$$F = ab + a'c$$

$$F' = (a' + b').(a + c')$$

and we implemented the complementary function using AND, OR and NOT gates. The circuit below is designed.

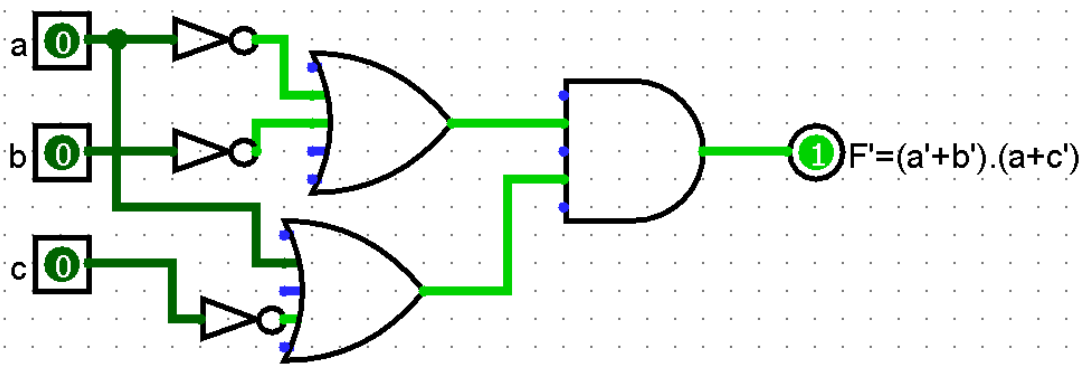

Figure 13: Design of F’

a	b	c	$(a \wedge b) \vee (\neg a \wedge c)$
1	1	1	1
1	1	0	1
1	0	1	0
1	0	0	0
0	1	1	1
0	1	0	0
0	0	1	1
0	0	0	0

Figure 14: Truth of F (created using the tool provided by emathhelp.net)

a	b	c	$(\neg a \vee \neg b) \wedge (a \vee \neg c)$
1	1	1	0
1	1	0	0
1	0	1	1
1	0	0	1
0	1	1	0
0	1	0	1
0	0	1	0
0	0	0	1

Figure 15: Truth of F' (created using the tool provided by emathhelp.net)

Moreover, these circuits are tested on C.A.D.E.T using a 7404 Hex Inverter, a 7408 Quadruple 2-input Positive-AND Gate and a 7432 Quadruple 2-input Positive-OR Gate.

3.4 Part 4

In the fourth part of the experiment, we simplified given function:

$$F(a,b,c,d) = \cup_1(1,2,5,6,9,10,13,14)$$

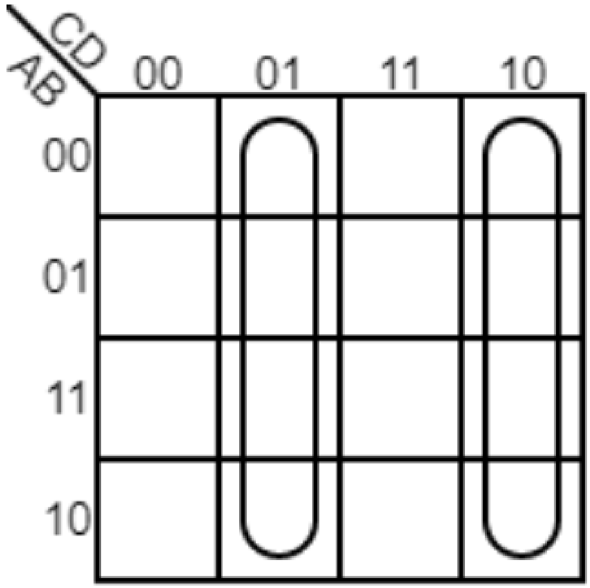

Figure 16: Karnaugh Map (created using the tool provided by boolean-algebra.com)

and we found the simplified expression:

$$F(a,b,c,d) = c'd + cd'$$

then, we implemented the simplified expression using AND, OR and NOT gates. The circuit below is designed.

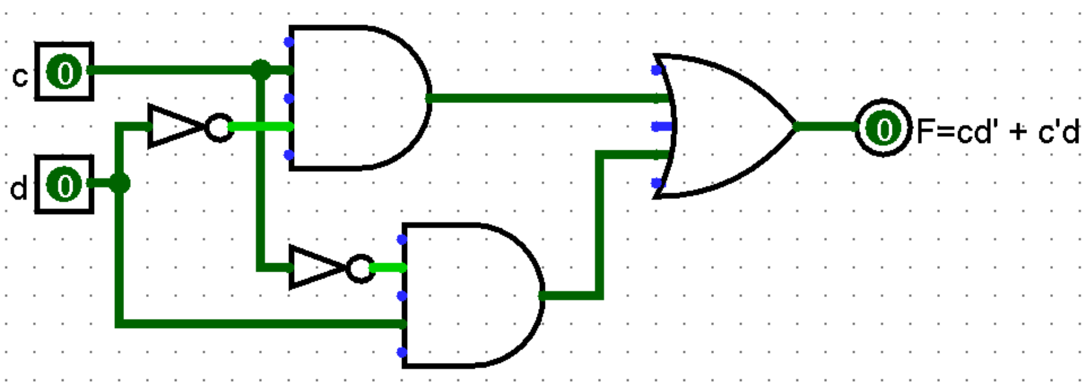

Figure 17: Design of F

c	d	$(c \wedge \neg d) \vee (\neg c \wedge d)$
1	1	0
1	0	1
0	1	1
0	0	0

Figure 18: Truth Table of F (created using the tool provided by emathhelp.net)

Moreover, these circuits are tested on C.A.D.E.T using a 7404 Hex Inverter, a 7408 Quadruple 2-input Positive-AND Gate and a 7432 Quadruple 2-input Positive-OR Gate.

3.5 Part 5

In the fifth part of the experiment, we observed some experimental environments.

Figure 19: Potentiometer

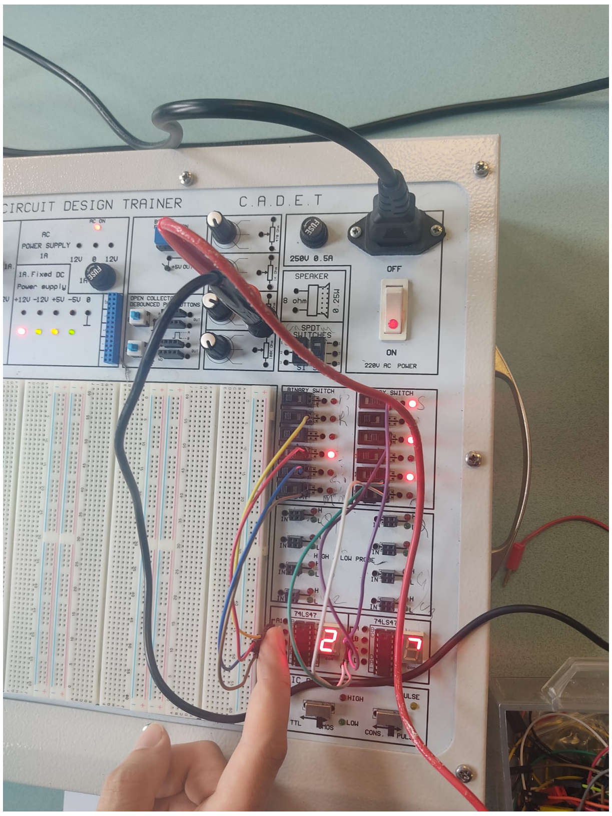

Figure 20: Display

3.6 Part 6

In the last part of the experiment, we obtained a basic knowledge of the use of the function generator and the oscilloscope.

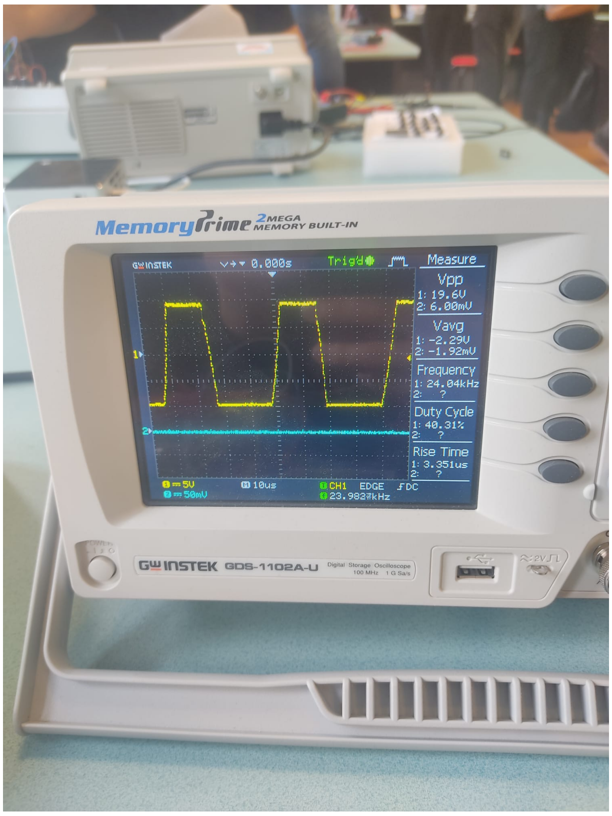

Figure 21: Oscilloscope

4 DISCUSSION

In the part 5, we were not able to show "7" number entirely in display due to a problem in our experimental environment.

5 CONCLUSION

In this experiment, we observed given axioms and theorems, implemented them in the experimental environments, and we obtained a basic knowledge of the use of the function generator and the oscilloscope.

REFERENCES