Quiz #1

1. The following questions are according to the memory map given on the side.

   a) Draw the chip select input of *BIOS*, *Main Memory*, and *Graphics Card* separately using the <u>NAND</u> circuit.

   b) Fill the following table according to the address input in which the chip selection area will be enabled or disabled.

Address Input	$\overline{CS_{BIOS}}$	$\overline{CS_{Memory}}$	$\overline{CS_{Graphics}}$
0x0523	1	1	1
0xE4C7	1	1	0
0xA4FF	1	1	1
0x6B20	1	0	1

Memory map:
- 0x0000
- 0x3400
- **BIOS**
- 0x37FF
- 0x6800
- **Main Memory**
- 0x6BFF
- 0xC000
- **Graphics Card**
- 0xFFFF

2. Build a memory that spans between $0000 and $3FFF with 4Kx8 memory chips for a CPU with 8-bit data bus and 16-bit address bus.

   a) Calculate the memory address range for all chips.

   b) How many 4K chips are needed?

   c) Draw the memory design by showing all necessary connections. (Address bus, Data bus, Chip select signals). Use an address decoder (determine its type) and logic gates (determine their types). Assume the decoder select signal and the memory chip select signals are active high.
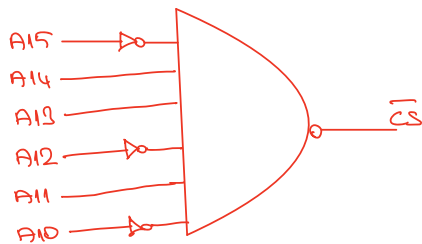
Duration: 40 minutes

(1)

a) **BIOS**

0x3400
0x37FF
$\Rightarrow$ 0011 0100 0000 0000
$\quad$ 0011 0111 1111 1111
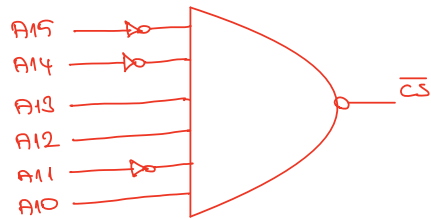
A15 —▷∘—
A14 —▷∘—
A13 ——
A12 ——
A11 —▷∘—
A10 ——
$\overline{CS}$

MAIN MEMORY

0x6800
0x68FF
$\Rightarrow$ 0110 1000 0000 0000
$\quad$ 0110 1011 1111 1111

A15 —▷∘—
A14 ——
A13 ——
A12 —▷∘—
A11 ——
A10 —▷∘—
$\overline{CS}$

GRAPHICS CARD

0x C000
0x FFFF
$\Rightarrow$ 1100 0000 0000 0000
$\quad$ 1111 1111 1111 1111

A15 ——
A14 ——
$\overline{CS}$
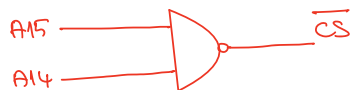
② a)

$0000	0000	0000	0000	0000
$0FFF	⇒	0000	1111	1111	1111
$1000		0001	0000	0000	0000
$1FFF	⇒	0001	1111	1111	1111
$2000		0010	0000	0000	0000
$2FFF	⇒	0010	1111	1111	1111
$3000		0011	0000	0000	0000
$3FFF	⇒	0011	1111	1111	1111

b) 4

c)

$D_0 - D_7$

Mem-4	Mem-3	Mem-2	Mem-1
$3FFF	$2FFF	$1FFF	$0FFF
$3000	$2000	$1000	$0000

$A_0 - A_{10}$

R/$\overline{W}$

2×4 Decoder $\overline{E}$

A13

A12

A15

A14