Quiz #1

1. The following questions are according to the memory map given on the side.

   a) Draw the chip select input of *BIOS*, *Main Memory*, and *Graphics Card* separately using the <u>NAND</u> circuit.

   b) Fill the following table according to the address input in which the chip selection area will be enabled or disabled.

Address Input	$\overline{CS_{BIOS}}$	$\overline{CS_{Memory}}$	$\overline{CS_{Graphics}}$
0x23FF	1	1	1
0xE4B7	1	1	0
0xC800	1	1	1
0x6B20	0	1	1

Memory map (right side):

| Address	Region
0x0000	
0x4000	**BIOS**
0x7FFF	
0xA400	**Main Memory**
0xA3FF	
0xE000	**Graphics Card**
0xFFFF	

2. Build a memory that spans between $3000 and $6FFF with 4Kx8 memory chips for a CPU with 8-bit data bus and 16-bit address bus.

   a) Calculate the memory address range for all chips.
   b) How many 4K chips are needed?
   c) Draw the memory design by showing all necessary connections. (Address bus, Data bus, Chip select signals). Use an address decoder (determine its type) and logic gates (determine their types). Assume the decoder select signal and the memory chip select signals are active high.
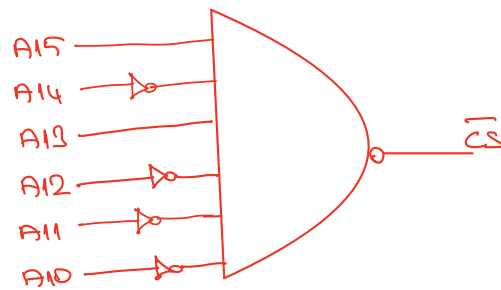
Duration: 40 minutes

1

a) **BIOS**

0x 4000

0x 7FFF

⇒ 01/00 0000 0000 0000
   01/11 1111 1111 1111

A15 ──▷∘─────╮
            ╲‾‾‾) ∘──── $\overline{CS}$
A14 ────────╱
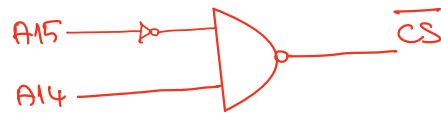
MAIN MEMORY

0x A000

0x A3FF

⇒ 1010 00/00 0000 0000
   1010 00/11 1111 1111

A15 ───────╮
A14 ──▷∘───┤
A13 ───────┤‾‾‾‾‾╲
A12 ──▷∘───┤   ) ∘──── $\overline{CS}$
A11 ──▷∘───┤
A10 ──▷∘───╯____╱

GRAPHICS CARD

0x E000 ⇒ 111/0 0000 0000 0000
0x FFFF   111/1 1111 1111 1111

A15 ───────╮
           ╲‾‾‾‾‾╲
A14 ───────┤   ) ∘──── $\overline{CS}$
           ╱_____╱
A13 ───────╯
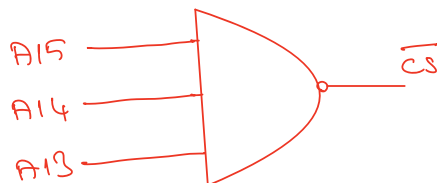
② a)

\$3000 ⟹	0011	0000 0000 0000	
\$3FFF ⟹	0011	1111 1111 1111	

\$4000 ⟹	0100	0000 0000 0000	
\$4FFF ⟹	0100	1111 1111 1111	

\$5000 ⟹	0101	0000 0000 0000	
\$5FFF ⟹	0101	1111 1111 1111	

\$6000 ⟹	0110	0000 0000 0000	
\$6FFF ⟹	0110	1111 1111 1111	

b) 4

c)

$D_0 - D_7$

Mem-4   Mem-3   Mem-2   Mem-1

\$6FFF \\ \$6000   \$5FFF \\ \$5000   \$4FFF \\ \$4000   \$3FFF \\ \$3000

$A_0 - A_{10}$

$R/\overline{W}$

3×8 Decoder $\overline{E}$

A14
A13
A12

A15