İTÜ Computer Engineering Dep.
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BLG 231E DIGITAL CIRCUITS FINAL EXAM SOLUTIONS

QUESTION 1 (20 Points):

a) [10 points]

8-bit integers that can be represented using 4 bits:
Positive: `0000 0000 - 0000 0111` (between 0 and +7)
Negative: `1111 1111 – 1111 1000` (between -1 and -8)

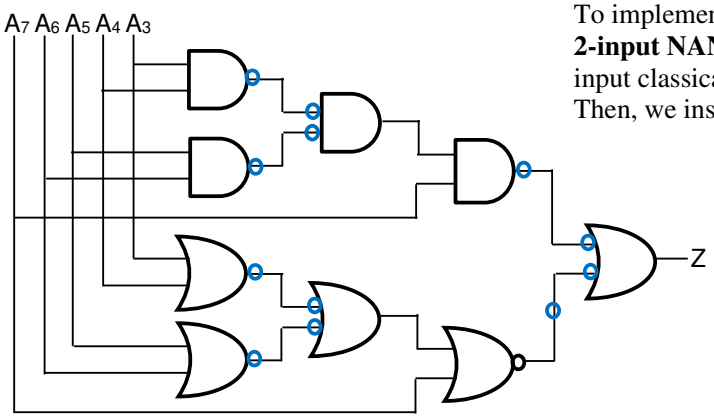
$$Z = A_7 \cdot A_6 \cdot A_5 \cdot A_4 \cdot A_3 + \overline{A_7 + A_6 + A_5 + A_4 + A_3}$$

$$Z = A_7 \cdot A_6 \cdot A_5 \cdot A_4 \cdot A_3 + \overline{A_7} \cdot \overline{A_6} \cdot \overline{A_5} \cdot \overline{A_4} \cdot \overline{A_3}$$

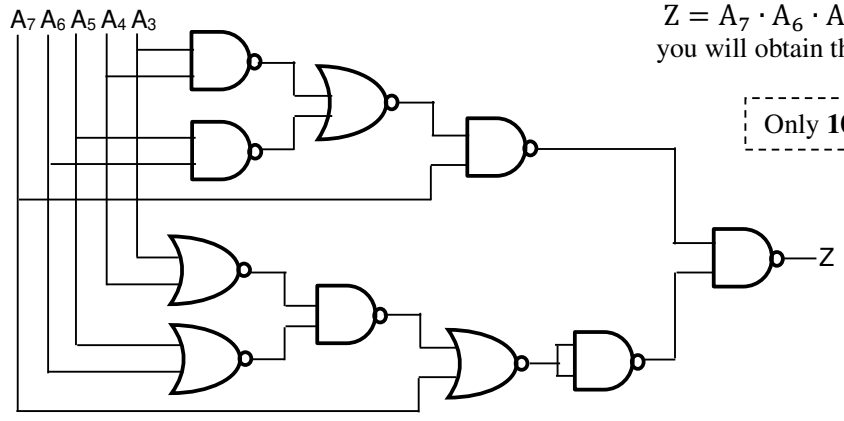
Notes:
The 5-input XOR (or XNOR) function is not correct.
$Z = A_7 \oplus A_6 \oplus A_5 \oplus A_4 \oplus A_3$ incorrect!
For example, $1 \oplus 0 \oplus 0 \oplus 0 \oplus 0 = 1$
There are also solutions that use XOR and AND gates but they are difficult to implement using NAND/NOR gates only.

b) [10 points]

$$Z = A_7 \cdot A_6 \cdot A_5 \cdot A_4 \cdot A_3 + \overline{A_7 + A_6 + A_5 + A_4 + A_3}$$



To implement the circuit using the **fewest possible** number of **2-input NAND** and **2-input NOR gates** only, we start using 2-input classical logic gates.
Then, we insert NOT gates represented by circles.



If you use the expression
$Z = A_7 \cdot A_6 \cdot A_5 \cdot A_4 \cdot A_3 + \overline{A_7} \cdot \overline{A_6} \cdot \overline{A_5} \cdot \overline{A_4} \cdot \overline{A_3}$,
you will obtain the same implementation.

Only **10 gates** are sufficient.

QUESTION 2 (30 Points):
Note: Parts (a) and (b) are not related and can be solved independently.

a) [15 points]

i. [10 points] Fill in the table given below for this device assuming the inputs are applied in the given order:

A	B	Y	Z
0	0	1	1
0	1	1	0
1	1	1	0
1	0	x	x

For these inputs, the circuit oscillates, it is not stable.

ii. [5 points]

Remember: A memory unit must have
1. two stable states,
2. control input(s), which can be used to change (set, reset) or preserve the state of the unit.

If we consider Z as the output of the circuit, we can conclude that we can set the device to Z=1 by applying AB=00 and reset it to Z=0 by applying AB=01.
Input combination AB=10 is forbidden. These values may not be applied to AB.
There is one important aspect of this device that is missing: it cannot preserve its previous state if Z=1. It acts as a NOT gate between B and Z.
After AB=01,Z=0 , we can apply 11 to AB to preserve the state. However, after AB=00,Z=1, it is not possible.
Therefore, this device cannot be used as a latch.
Note:
You will get partial credit, if you make reasonable comments as described above.

b) [15 points]

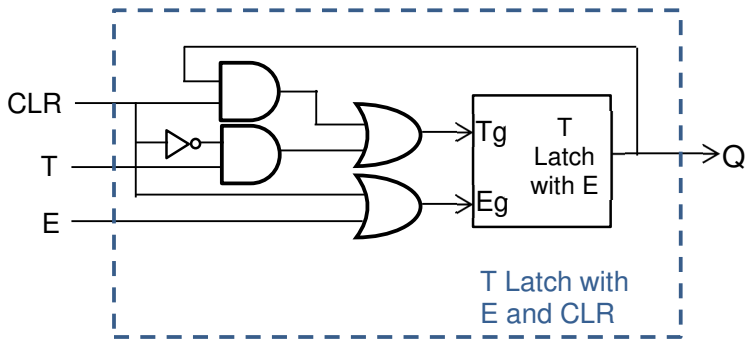
We label the inputs T and E of the given T latch as Tg and Eg, respectively.
If CLR=0:
The latch must work normally.

- Tg=T, Eg=E

If CLR=1:
The latch will be reset to Q=0 regardless of the values of T and Enable (E).

- Eg=1. To reset the latch, it must be enabled.
- If Q=0, then Tg=0 (don't change). We do not need to change the Q.
- If Q=1, then Tg=1 (toggle). We want reset the latch to Q=0.

$$Eg = CLR + E$$
$$Tg = CLR \cdot Q + \overline{CLR} \cdot T$$



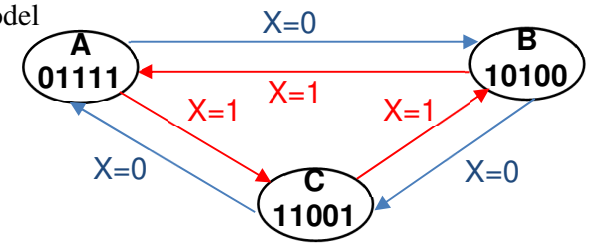
Note:
You cannot implement this circuit connecting some gates (for example AND) to the output only. In this way, you can only block the output but you cannot change the value (state) of the latch. When the CLR changes from 1 to 0, the original value (for example, 1), of the latch will appear at the output again. You cannot reset the latch in this way.

QUESTION 3 (30 Points):

a) [5 points]

A: 15_{10}= 01111_2 (Z4-Z0)
B: 20_{10}= 10100_2 (Z4-Z0)
C: 25_{10}= 11001_2 (Z4-Z0)

Moore Model



b) [5 points]

Q_1Q_0 \ X	0	1
A	B	C
B	C	A
C	A	B

State encoding:
A: 00
B: 01
C: 10
(Other encodings are possible)

State, output table

Q_1Q_0 \ X	0	1	Z_4	Z_3	Z_2	Z_1	Z_0
00	01	10	0	1	1	1	1
01	10	00	1	0	1	0	0
11	ØØ	ØØ	Ø	Ø	Ø	Ø	Ø
10	00	01	1	1	0	0	1

c) [15 points]

Q_1 transitions

Q_1Q_0 \ X	0	1
00	00	01
01	01	00
11	ØØ	ØØ
10	10	10

Q_0 transitions

Q_1Q_0 \ X	0	1
00	01	00
01	10	10
11	ØØ	ØØ
10	00	01

Transition table for JK flip-flop:

symbol	QQ^+	J	K
0	00	0	ø
α	01	1	ø
β	10	ø	1
1	11	ø	0

Inputs of J-K FF 1

J_1

Q_1Q_0 \ X	0	1
00	0	1
01	1	0
11	ϕ	ϕ
10	ϕ	ϕ

J_1= Q_0X'+ $Q_0'X$
= $Q_0 \oplus X$
(XOR)

K_1

Q_1Q_0 \ X	0	1
00	ϕ	ϕ
01	ϕ	ϕ
11	ϕ	ϕ
10	1	1

K_1= 1

Inputs of J-K FF 0

J_0

Q_1Q_0 \ X	0	1
00	1	0
01	ϕ	ϕ
11	ϕ	ϕ
10	0	1

J_0= $Q_1'X'$+ Q_1X
= $Q_0 \odot X$
(XNOR)

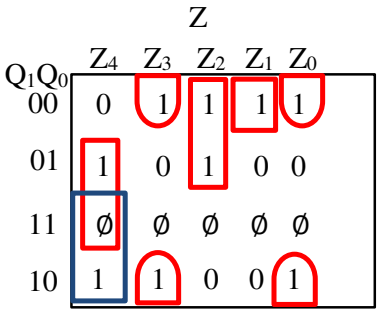
K_0

Q_1Q_0 \ X	0	1
00	ϕ	ϕ
01	1	1
11	ϕ	ϕ
10	ϕ	ϕ

K_0= 1

d) [5 points] Write the expression of the output function G.

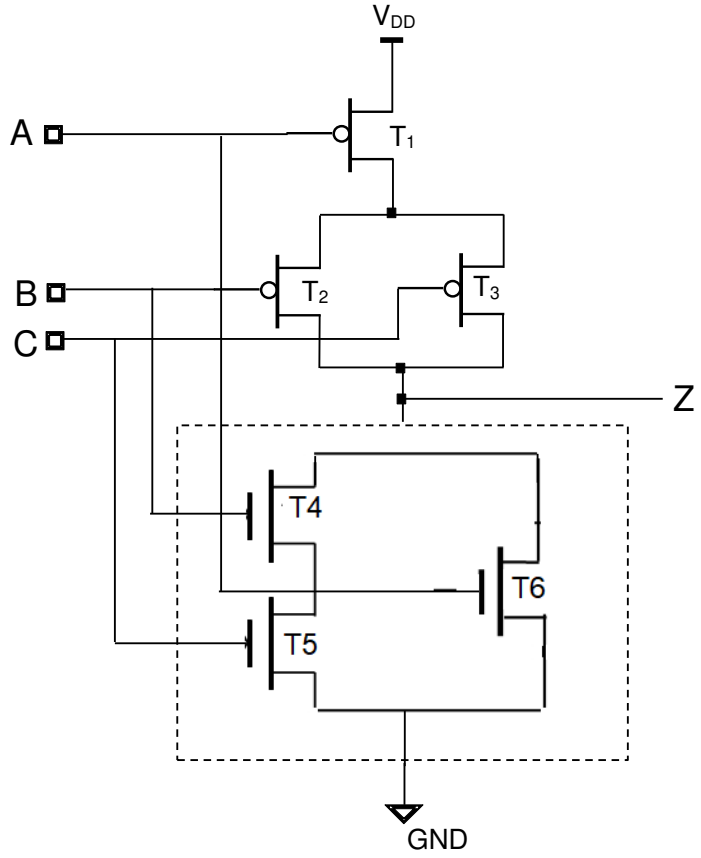
Output table



$Z_4 = Q_1 + Q_0$, $Z_3 = Q_0'$, $Z_2 = Q_1'$, $Z_1 = Q_1'Q_0'$, $Z_0 = Q_0'$

QUESTION 4 (20 Points):

a) [10 points]



b) [10 points]

			Transistors						
A	**B**	**C**	**T1**	**T2**	**T3**	**T4**	**T5**	**T6**	**Z**
L	H	H	ON	OFF	OFF	ON	ON	OFF	L
H	L	L	OFF	ON	ON	OFF	OFF	ON	L
H	L	H	OFF	ON	OFF	OFF	ON	ON	L
H	H	L	OFF	OFF	ON	ON	OFF	ON	L
H	H	H	OFF	OFF	OFF	ON	ON	ON	L