İTÜ Computer Engineering Dep.
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Student ID:
First Name and Last Name:
Signature:

BLG 322E COMPUTER ARCHITECTURE FINAL EXAM

Regulations:

1. The duration for this question is **25 minutes**.
2. **You may not ask any questions during the exam.** If you think something is missing in a question, explain it, make the necessary assumption, and solve the question.
3. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings.
4. Your solution must **be all hand-written and signed by you**.
5. Please **show all your work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT.

QUESTION 2 (Total 25 points):

For a shared memory multiprocessor system, the states of **two caches** on **two separate cores** (P0 and P1) are shown below. Assume that the caches are **direct mapped caches,** and the **MESI** snooping protocol maintains cache coherency.

P0:

	Tag	Data Word 1	Data Word 2	Data Word 3	Data Word 4	Coherency State
Frame 0	1000	100	200	300	400	E
Frame 1	4000	500	600	700	800	S
...						
Frame N	3000	200	400	600	800	I

P1:

	Tag	Data Word 1	Data Word 2	Data Word 3	Data Word 4	Coherency State
Frame 0	2000	100	100	100	100	I
Frame 1	8000	500	600	700	800	S
...						
Frame N	3000	200	400	600	800	M

Answer the three questions below:

a) If **P0** wants to write **Frame 0**, what happens to its coherency state?
b) If **P1** writes to **Frame 1**, is **Frame 1** on **P0** invalidated? Why or why not?
c) If **P1** brings in a new data block into **Frame M** for reading, and there are other caches that have a copy, what state is it cached in **P1**?