Istanbul Technical University

Department of Computer Engineering

BLG 322E - COMPUTER ARCHITECTURE

Assignment 1

Due Date: Wednesday, March 16, 2025, 23:00.

- Please **write and draw** <u>neatly</u>.

- <u>You may draw the circuits by hand. PLEASE BE NEAT! If we cannot read or follow your solution, no partial credit will be given.</u>

- Please **write your full name** (first name and last name) **and Student ID** at the top of your solution.

- Please <u>show ALL your work</u>. Answers with no supporting explanations or work will not receive any partial credit. Your homework is <u>not just a final report</u> of your results; we want to see your <u>steps</u>. <u>Upload all</u> the papers you worked on to get to the solution.

- **Submissions:** Submit your solution as a PDF file to Ninova before the deadline.

- **No late submissions** will be accepted. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official Ninova e-learning system before the deadline. Do not risk leaving your submission to the last few minutes.

- **Consequences of plagiarism/cheating:** Assignments have to be done individually. Any cheating will be subject to disciplinary action.

- **AI usage:** Language and reasoning models (ChatGPT, o1, o3, Claude, etc.) are tested on the questions. They hallucinate on architecture images and give the wrong answers. You can use them to test alternative ideas, but <u>you should always check the results.</u>

If you have any questions, please e-mail **Mustafa Abdullah Hakkoz (hakkozm22@itu.edu.tr).**

QUESTION:

A task **T** that will be executed on integers consists of <u>nine suboperations</u> X_i (i =1,2,3,4,5), Y_i (i=1,2) and Z_i (i=1,2).
These suboperations are implemented using combinational digital circuits with the following propagation delays:
X_1=**5**, X_2=**10ns**, X_3=**30ns**, X_4=**40ns**, X_5=**15ns**, Y_1=**30ns**,
Y_2=**20ns,** Z_1=**35ns**, Z_2=**40ns**
Fig. 1 on the right shows the block diagram of the circuit.
- The arrows between the suboperations indicate the dependencies between them. Therefore, the suboperations should be executed in the given order.
- Suboperation Y_1 can execute in parallel with X_2 or X_3.
- Similarly, suboperation Y_2 can also execute in parallel with X_3 or X_4.
- Suboperation Z_1 can execute in parallel with X_3 or X_4.
- Similarly, suboperation Z_2 can also execute in parallel with X_3 or X_4.

To execute task **T** faster on elements of an array, we construct pipeline P_A with <u>five stages</u> (S1, S2, S3, S4, S5) as shown in Fig. 2 below. After each stage, we place a register with a delay of 5ns.
a) How long does it take to execute the task only on the first element of array using the pipeline P_A? (T_1 = ?) **[10pt]**
b) What is the duration of execution of the task **T** for once without the pipeline? (t_n = ?) **[10pt]**
c) What is the minimum number of elements the array should have to achieve any speedup with this pipeline? **[10pt]**
d) Calculate the highest possible speedup pipeline P_A can achieve when it executes a task **T** on an array with an <u>infinite</u> number of elements. **[10pt]**
e) Design an alternative pipeline P_B that executes task **T** and meets the following constraints: **[40pt]**
- The speedup P_B achieves on an array with an <u>infinite</u> number of elements should not be lower than that achieved by P_A.
- Use as few registers as possible.
- Use the units given in the original circuit (X_i(i=1,2,3,4,5) Y_i (i=1,2) and Z_i (i=1,2)).
- **Do not submit** incomprehensible, unreadable, or sloppy drawings. These will incur a **-5pt penalty.**
f) How long does it take to execute the task only on the first element using pipeline P_B you designed in **Part (e)** (T_1= ?)? **[10pt]**
g) When executing task **T** on an array with an <u>infinite</u> number of elements, what speedup does the pipeline P_B you designed in **Part (e)** achieve? **[10pt]**
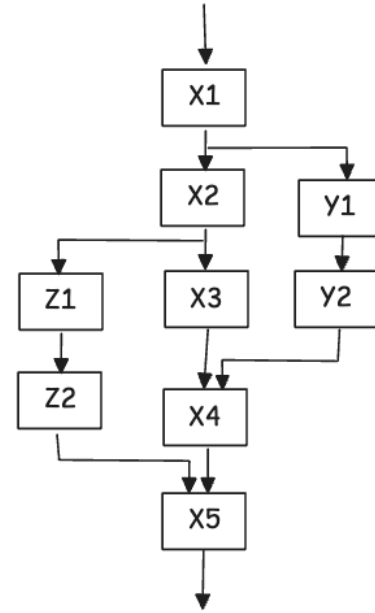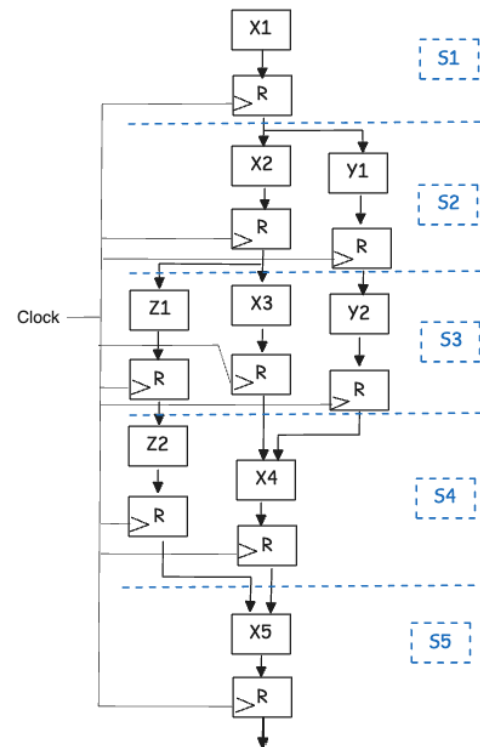

Fig. 1: Dependency diagram of the circuit.

Fig. 2: Pipeline with 5 stages.