Istanbul Technical University

Department of Computer Engineering

BLG 322E - COMPUTER ARCHITECTURE

Assignment 3

Due Date: Monday, May 3, 2025, 23:59.

- Please **type your full name** (first name and last name) **and Student ID** at the top of your solution.
- Please **draw the diagrams using a computer program**. PLEASE BE NEAT! If we cannot read or follow your solution, no partial credit will be given.
- Please show ALL your work. Answers with no supporting explanations or work will not receive any partial credit. Your homework is not just a final report of your results; we want to see your steps. Upload all the papers you worked on to get to the solution.
- **Submissions:** Submit your solution as a **PDF file** to Ninova before the deadline.
- **No late submissions** will be accepted. Do not send your solutions by e-mail. We will only accept files that have been uploaded to the official Ninova e-learning system before the deadline. Do not risk leaving your submission to the last few minutes.
- **Consequences of plagiarism/cheating:** Assignments have to be done individually. Any cheating will be subject to disciplinary action.

If you have any questions, please e-mail **M. Alpaslan Tavukçu (tavukcu22@itu.edu.tr)**.

QUESTION 1 (100 points):

The instruction cycle of a CPU has the following 5 states (cycles) with the given durations:

1. Instruction fetch and decode: **50** ns,
2. Operand fetch: **60** ns,
3. Execution: **50** ns and
4. Result write: **50** ns
5. Interrupt housekeeping: **200** ns.
6. TAS instruction Execution state time : **100 ns** (TAS instruction consists of IF + DECODE + Execution, there is no RW etc.)
   (Note: The CPU enters the interrupt cycle only if there are interrupt requests.
   For simplicity, 'interrupt housekeeping' is treated as a single block operation and cannot be executed in parallel with DMA operations. Housekeeping operations (saving the return address, reading the vector address, etc.) in the interrupt cycle take **200** ns.)

- The CPU does not access memory only in "3. Execution" cycle; it uses memory in all other cycles **(1, 2, 4, 5).**
- Memory access time and I/O interface access times are **50 ns** each.
- Two vectored interrupt sources (devices) A and B are connected over a priority interrupt controller to the CPU. Device B has higher priority than device A (B > A). **For simplicity,** the interrupt service routine (including the RTI (Return from Interrupt) instruction) for device **A runs 2 instructions**, also the interrupt service routine (ISR) for device **B runs 1 instruction.**
- Two DMACs ($DMAC_1$, $DMAC_2$) are connected to this processor over a bus arbiter. $DMAC_1$ works in **cycle-stealing** mode, while $DMAC_2$ works in **burst** mode. The order of precedence is **$DMAC_2$ > $DMAC_1$**. $DMAC_1$ is configured to transfer **5 words** from I/O interface to memory for each attempt. $DMAC_2$ is configured to transfer **3 words** from I/O interface to memory for each attempt. The DMACs types are **fly-by (implicit),** data does not pass through the DMAC.

Assume that

- We start a clock (Clock = 0) when the CPU begins to run the program.
- The I/O interface is always ready to transfer.
- At Clock = 2**0 ns,** device A sends an interrupt request.
- At Clock = **40 ns,** $DMAC_1$ attempts to start the data transfer from the I/O interface to memory.
- At Clock = **260 ns,** CPU reaches a TAS instruction.
- At Clock = **570 ns,** device B sends an interrupt request.
- At Clock = **580 ns,** $DMAC_2$ attempts to start the data transfer from the I/O interface to memory.
- At Clock = **880 ns,** $DMAC_2$ attempts to start the data transfer from the I/O interface to memory.

Draw a timeline and mark (and label) the activities of the CPU and the arrivals of the interrupts, DMACs attempts etc. and answer the following questions using the diagram. (check lecture notes, DMA and Interrupt Example, slide 5.15)

a) When (Clock =?) will the $DMAC_1$ complete the transfer of the **first, second, third, fourth and fifth** words? Show your calculations and mark on timeline diagram properly.

b) When (Clock =?) will the $DMAC_2$ complete the transfer of first attempt? Show your calculations and mark on timeline diagram properly.

c) When (Clock =?) will the $DMAC_2$ complete the transfer of second attempt? Show your calculations and mark on timeline diagram properly.

d) When (Clock =?) will the CPU finish the interrupt service routine for device A triggered at Clock = 2**0 ns**? Show your calculations and mark on timeline diagram properly.

e) When (Clock =?) will the CPU finish the interrupt service routine for device B triggered at Clock = **570 ns**? Show your calculations and mark on timeline diagram properly.