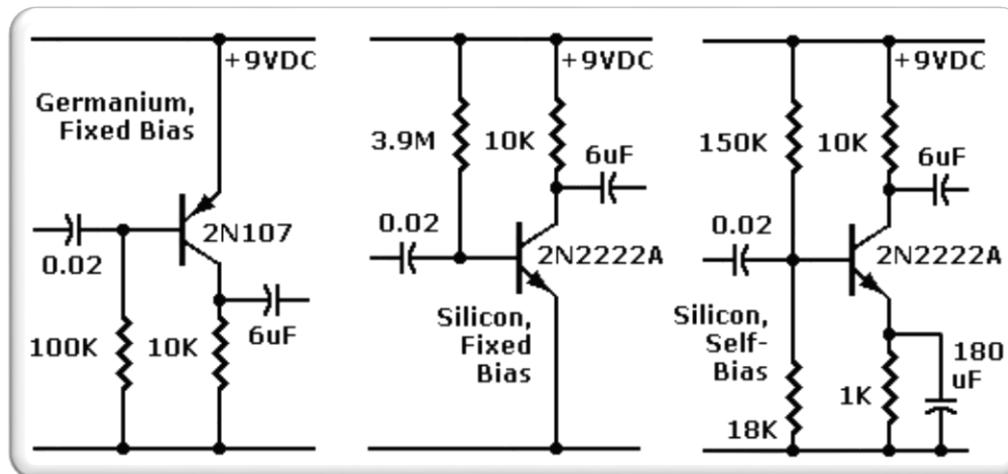
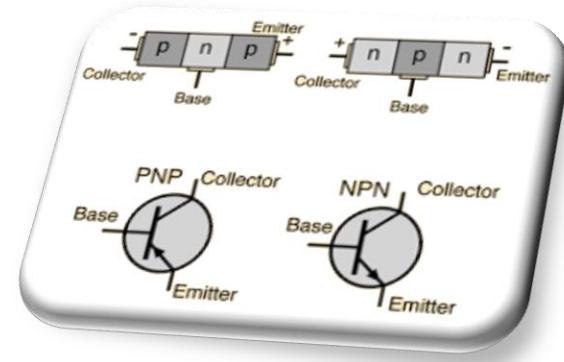
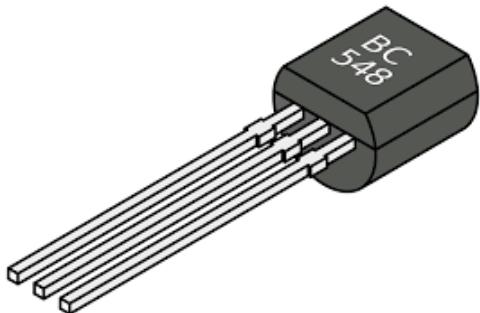


# BJT (Bipolar Junction Transistor)



# Point-Contact Transistor - first transistor ever made

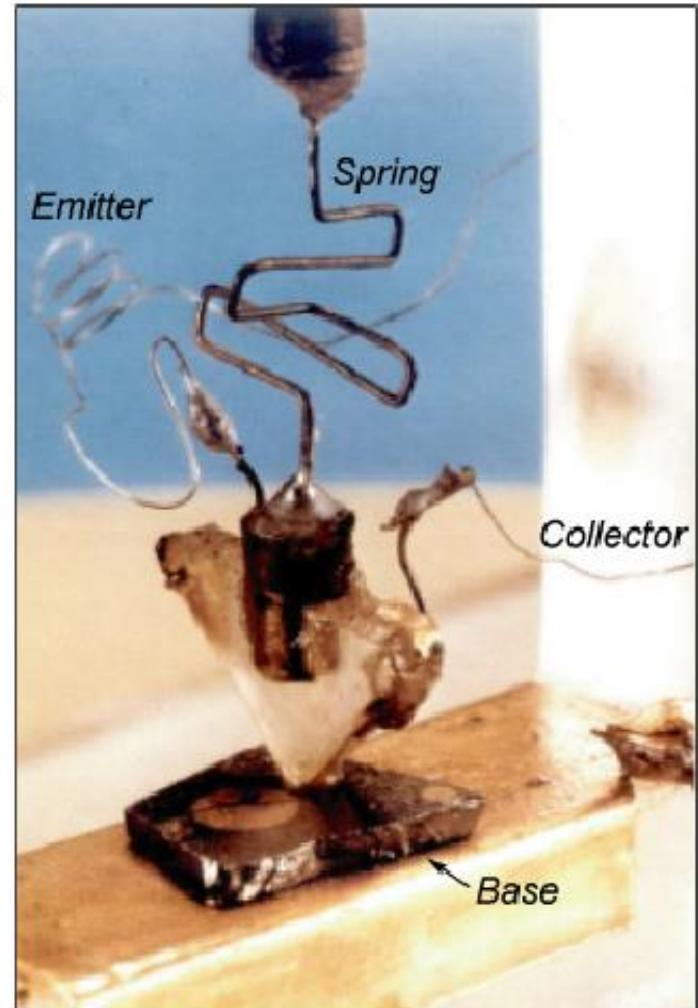
The first transistor was a point-contact transistor

## *The first point-contact transistor*

*John Bardeen, Walter Brattain, and William Shockley  
Bell Laboratories, Murray Hill, New Jersey (1947)*



Shockley



# First - BJTs

The transistor was probably the most important invention of the 20th Century.

The story behind the invention is one of clashing egos and top secret research.



Reference:

Bell Labs Museum

B. G. Streetman & S. Banerjee 'Solid State Electronic Devices', Prentice Hall 1999.

# Interesting story...

Picture shows the workbench of John Bardeen (Stocker Professor at OU) and Walter Brattain at Bell Laboratories.

The experimental results hadn't been very good. Their boss, William Shockley, came near to canceling the project. But in 1947, they built the circuit in the picture.

It was a working amplifier! John and Walter submitted a patent for the first working point contact transistor.



# Interesting story...

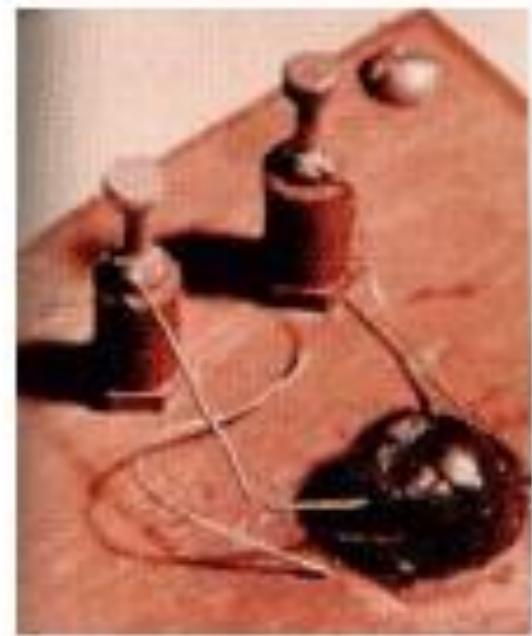
Shockley was furious and took their work and invented the junction transistor and submitted a patent for it 9 days later.

The three shared a **Nobel Prize in 1955**.

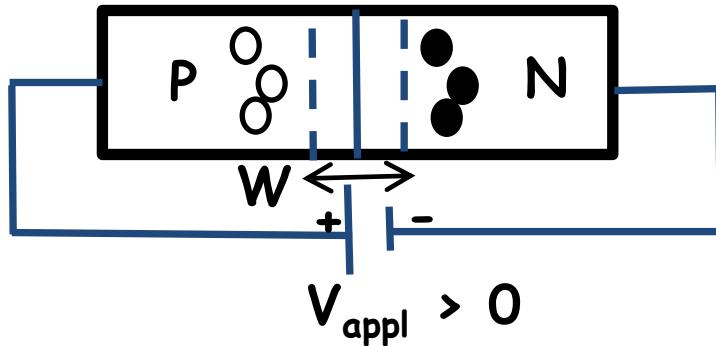
Bardeen and Brattain continued in research (and Bardeen later won another Nobel).

Shockley quit to start a semiconductor company in Palo Alto. It folded, but its staff went on to invent the integrated circuit (the "chip") and to found **Intel Corporation**.

By 1960, all important computers used transistors for logic, and ferrite cores for memory.



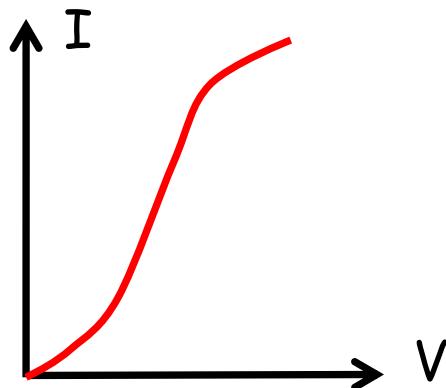
## Recall p-n junction



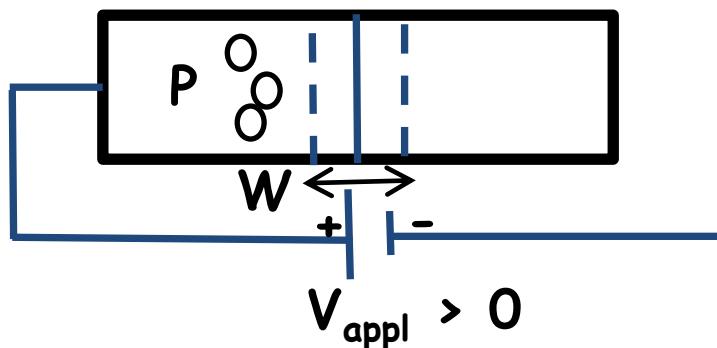
Forward bias, + on P, - on N

(Depletion region shrinks and then disappears.)

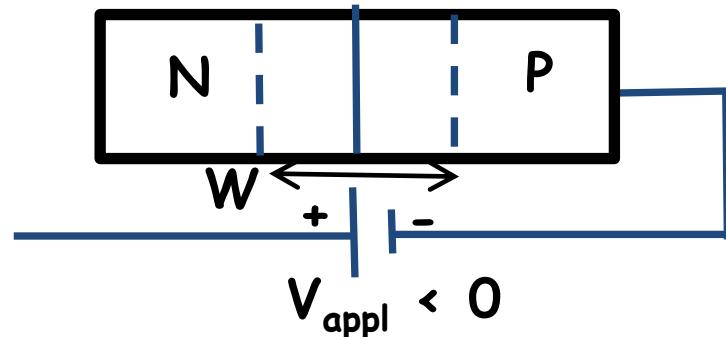
Allow holes to jump over barrier into N region.



So if we combine these by fusing their terminals...



Forward Bias



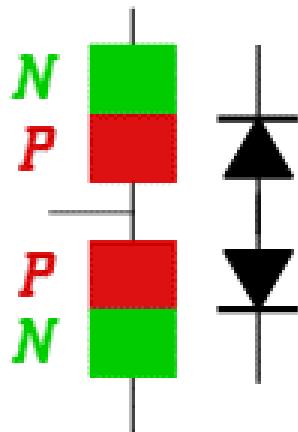
Reverse Bias

Holes from P region of 1<sup>st</sup> PN junction are driven by Forward Bias of 1<sup>st</sup> PN junction into central N region

Holes in the central N region are attracted by the negative terminal of the Reverse Bias of the 2<sup>nd</sup> junction.

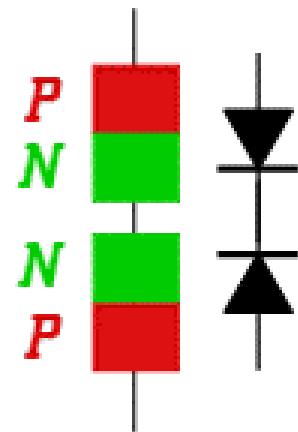
# Basic models of BJT

Diode



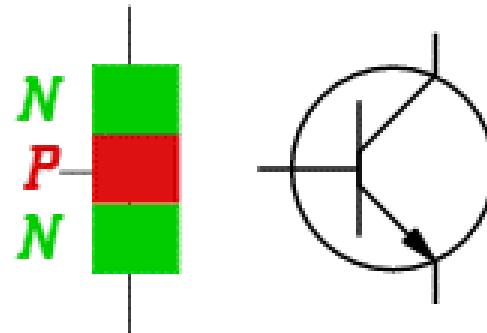
Diode

Diode

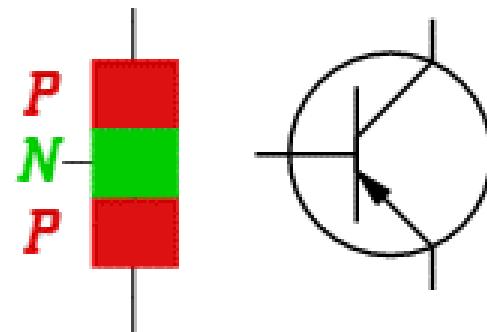


Diode

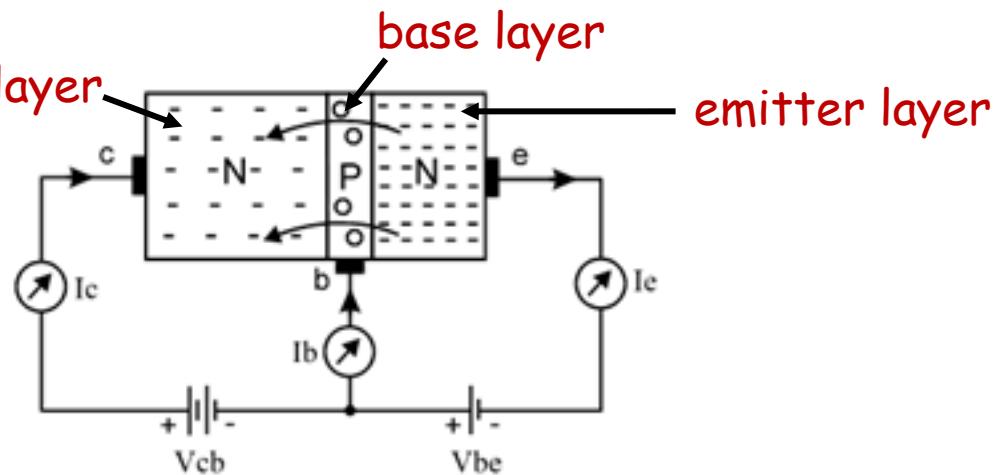
npn transistor



pnp transistor



## npn BJTs



It contains three semiconductor layers: one p-layer and two n-layers.

The area of collector layer is largest. So it can dissipate heat quickly.

Area of base layer is smallest and it is very thin.

Area of emitter layer is medium.

Collector layer is moderately doped. So it has medium number of charges (electrons).

Base layer is lightly doped. So it has a very few number of charges (holes).

Emitter layer is heavily doped. So it has largest number of charges (electrons).

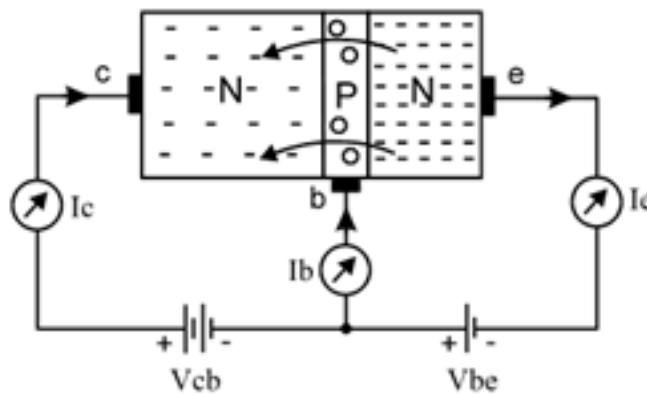
**THE P-LAYER IS SANDWICCHED BETWEEN TWO N-LAYERS.**

The junction between collector layer and base layer is called as collector-base junction or c-b junction.

The junction between base layer and emitter layer is called as base-emitter junction or b-e junction.

The two junctions have almost same potential barrier voltage of 0.6V to 0.7V, just like in a general purpose diode.

## npn BJTs



The collector is connected to high positive voltage with respect to base i.e.  $V_{cb}$  is very high. So c-b junction is reverse biased.

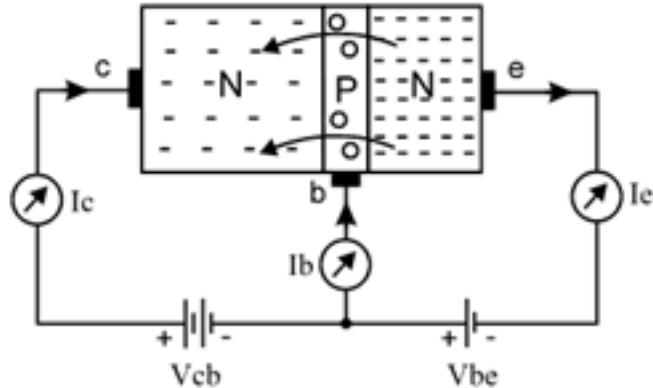
When we increase  $V_{be} \geq 0.7V$  (the value 0.7V is a typical value of potential barrier voltage) the **transistor** (b-e junction) is forward biased.

Now large number of electrons in emitter layer is repelled by negative terminal of  $V_{be}$  and they flow towards b-e junction.

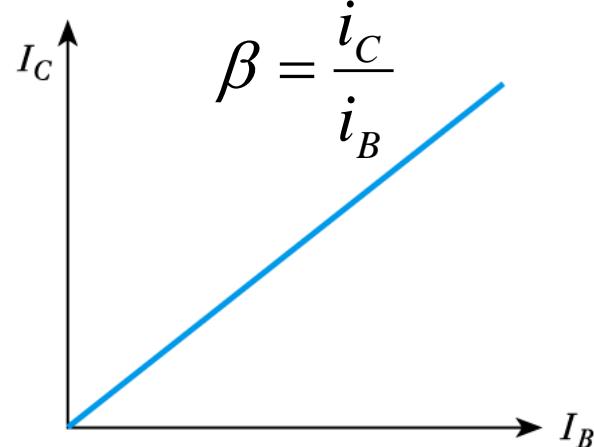
They cross the junction and enter into small base layer. Here some electrons combine with holes. Also some of them are attracted by positive terminal of  $V_{be}$  and remaining maximum number of electrons flow into collector layer, crossing the second junction i.e. c-b junction.

The resident electrons of collector are repelled by these (guest) electrons and thus, then all the electrons are present in collector layer are attracted by positive terminal of  $V_{cb}$ . Thus, all these electrons complete their journey back into emitter layer and produce conventional currents in the transistor as shown in the above circuit.

# npn BJTs



Now when  $V_{be}$  is still increased, more electrons are repelled by negative terminal of  $V_{be}$ . So base-emitter junction is more and more forward biased. Thus, base ( $I_b$ ) and collector currents ( $I_c$ ) increase.

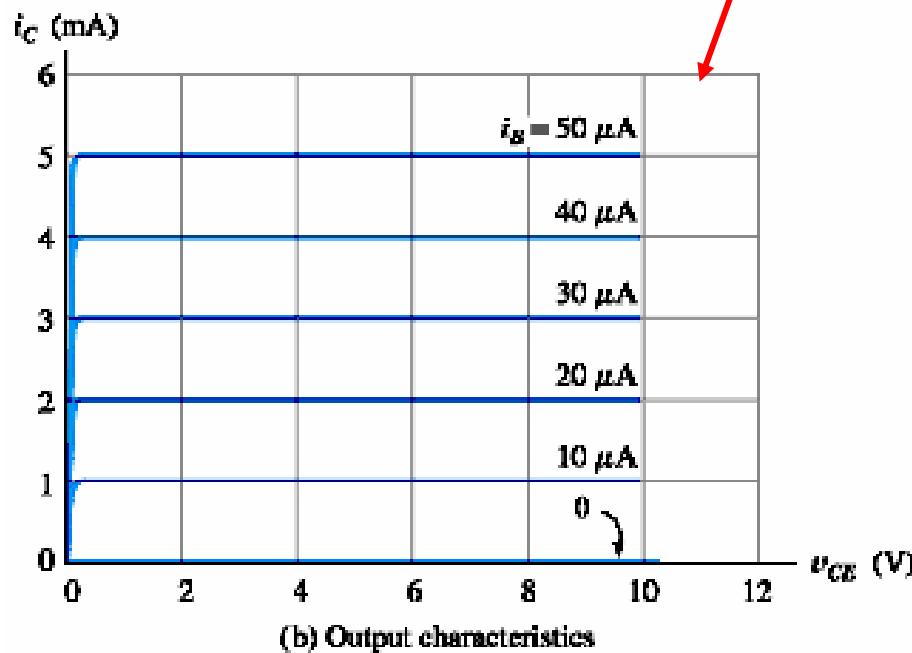


Collector current ( $I_c$ ) is the function of base current ( $I_b$ ) **in active mode**. Characteristic is approximately linear.

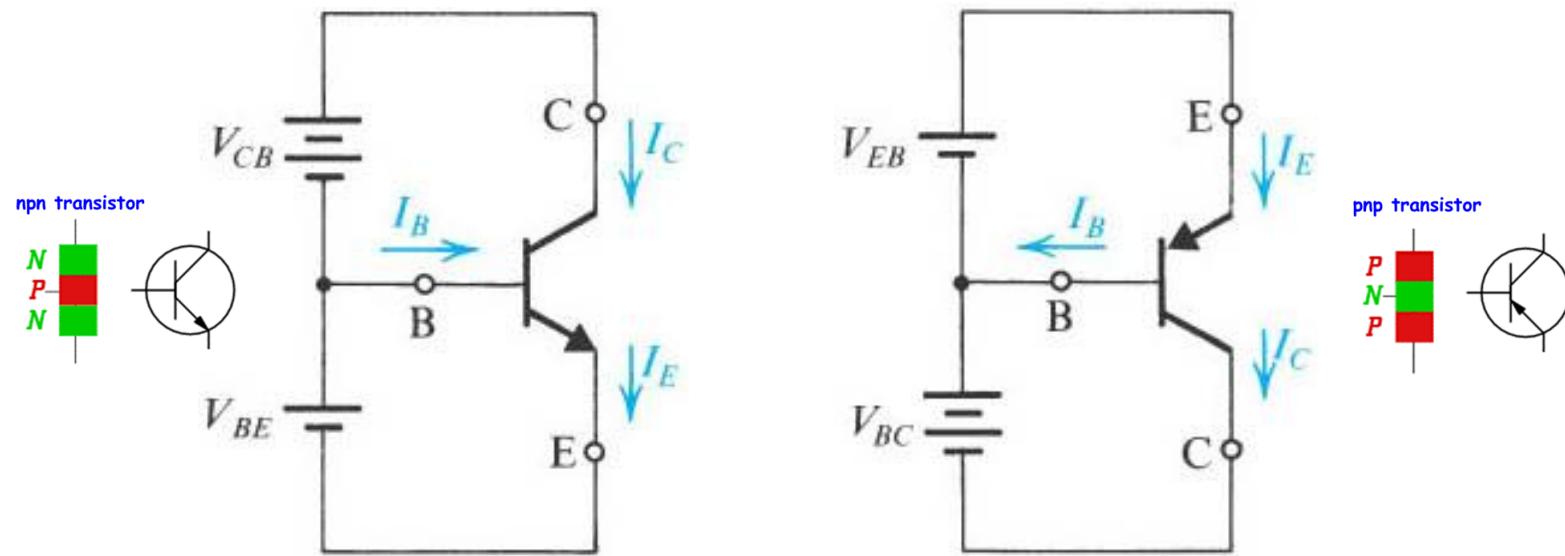
## Example:

Please calculate the current gain ( $\beta$ ) of this transistor

$$i_C = \beta i_B$$



# BJT Currents

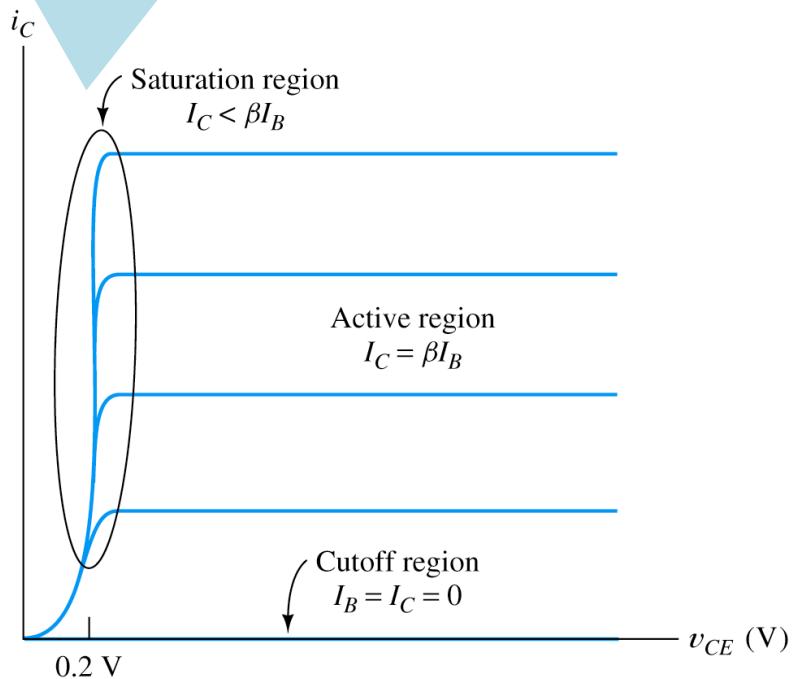


$$i_E = i_C + i_B$$

# BJT Operating Regions and I V Curves

## Output characteristics

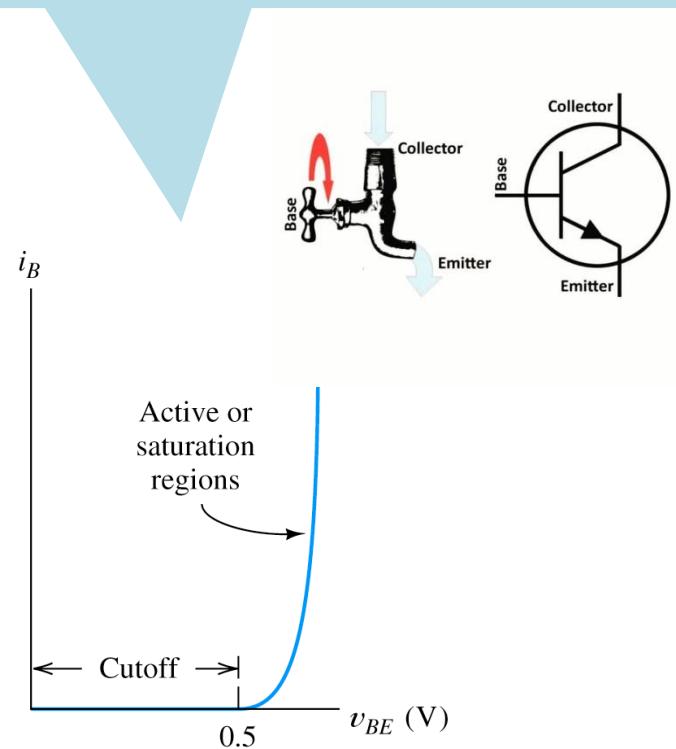
- region near to the origin is the saturation region
- this is normally avoided in linear circuits



(a) Output characteristic

## Input characteristics

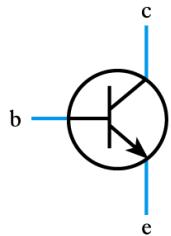
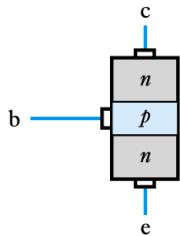
- the input takes the form of a forward-biased  $pn$  junction
- the input characteristics are similar to a semiconductor diode



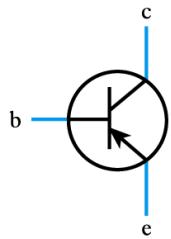
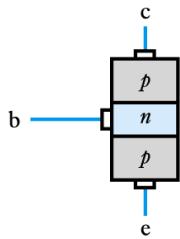
(b) Input characteristic

Regions of operation on the characteristics of an  $npn$  BJT.

# Bipolar Junction Transistors: Operation Modes



(a) An *n-p-n* transistor



(b) An *p-n-p* transistor

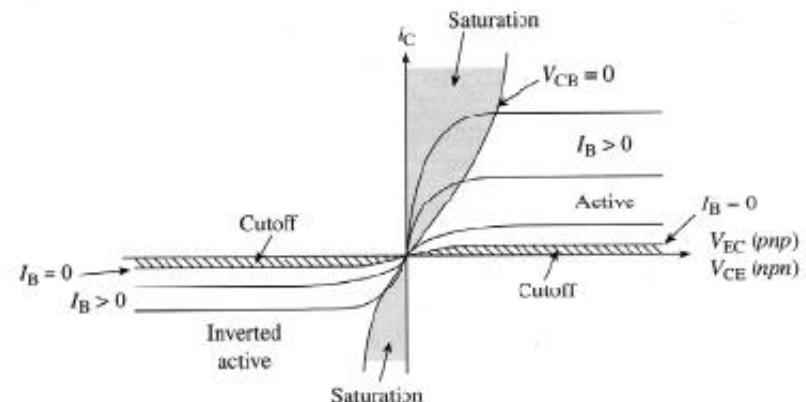
<i>Bias Mode</i>	<i>E-B Junction</i>	<i>C-B Junction</i>
Saturation	Forward	Forward
Active	Forward	Reverse
Cutoff	Reverse	Reverse

Operational modes are defined based on  $V_{BE}$  and  $V_{BC}$

- Saturation :** In this mode, both the junctions are forward biased. This method is not useful as the transistor is in "saturation" and the current cannot be controlled easily.

- Cutoff:** In this mode, both the junctions are reverse biased. This method is also not useful as the transistor is in "cut-off" state since current is zero.

- Active:** This is the most common and popular mode used in transistor biasing. In this mode, the **base-emitter junction** is forward biased and **collector-base junction** is reverse biased. So by adjusting base voltage we can control total current in the transistor easily.



# BJTs - Current & Voltage Relationships

Operation mode:  $v_{BE}$  is forward &  $v_{BC}$  is reverse (Active mode)

The Shockley equation:  $i_E = I_{ES} \left[ \exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right]$

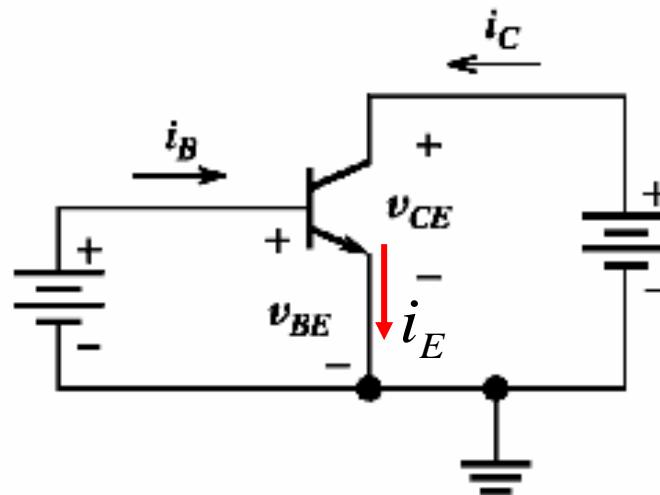
$I_{ES}$ =saturation current ( $10^{-12}$ - $10^{-16}$ A);

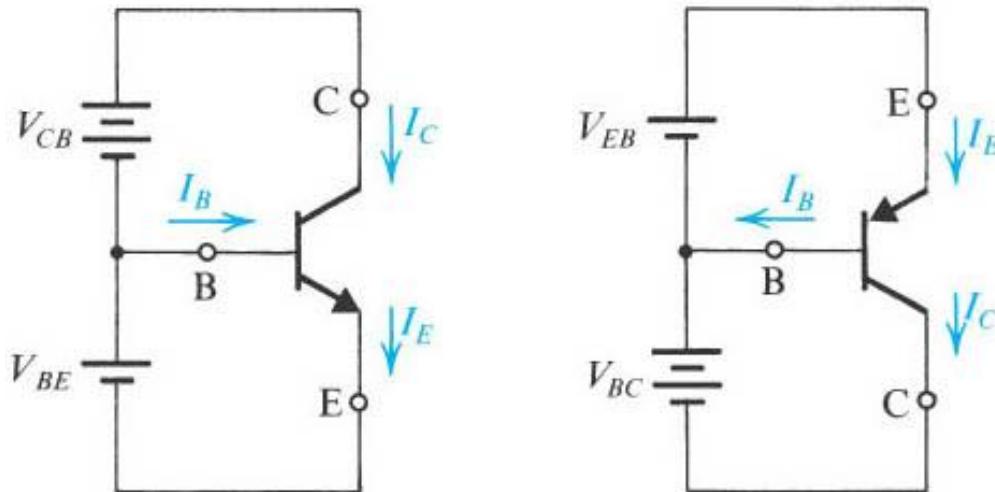
$V_T=kT/q$  -thermal voltage (26mV)

The Kirchhoff's laws

$$i_E = i_C + i_B$$

Active Mode:  $\beta = \frac{i_C}{i_B}$

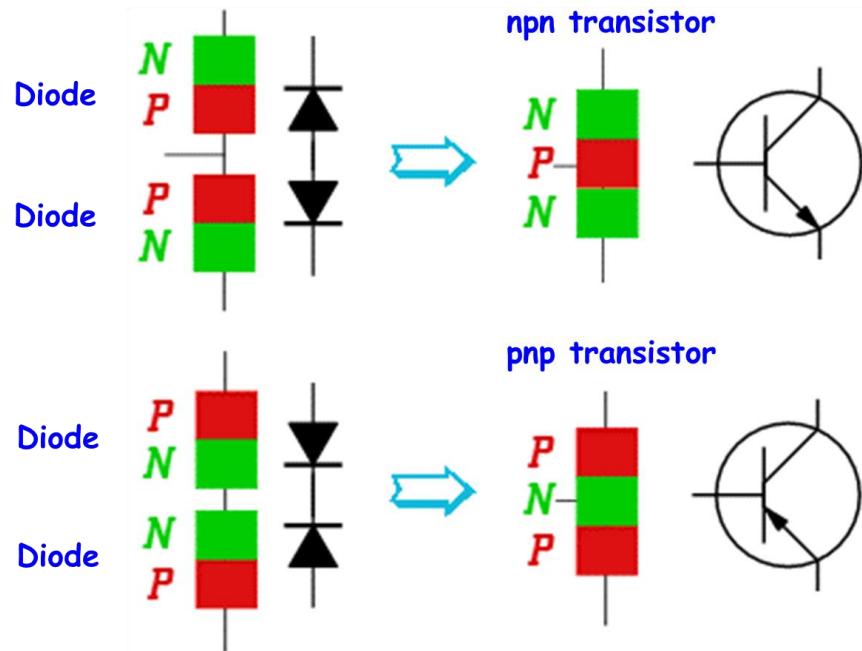




Voltage polarities and current flow  
if transistors are biased in the active mode.

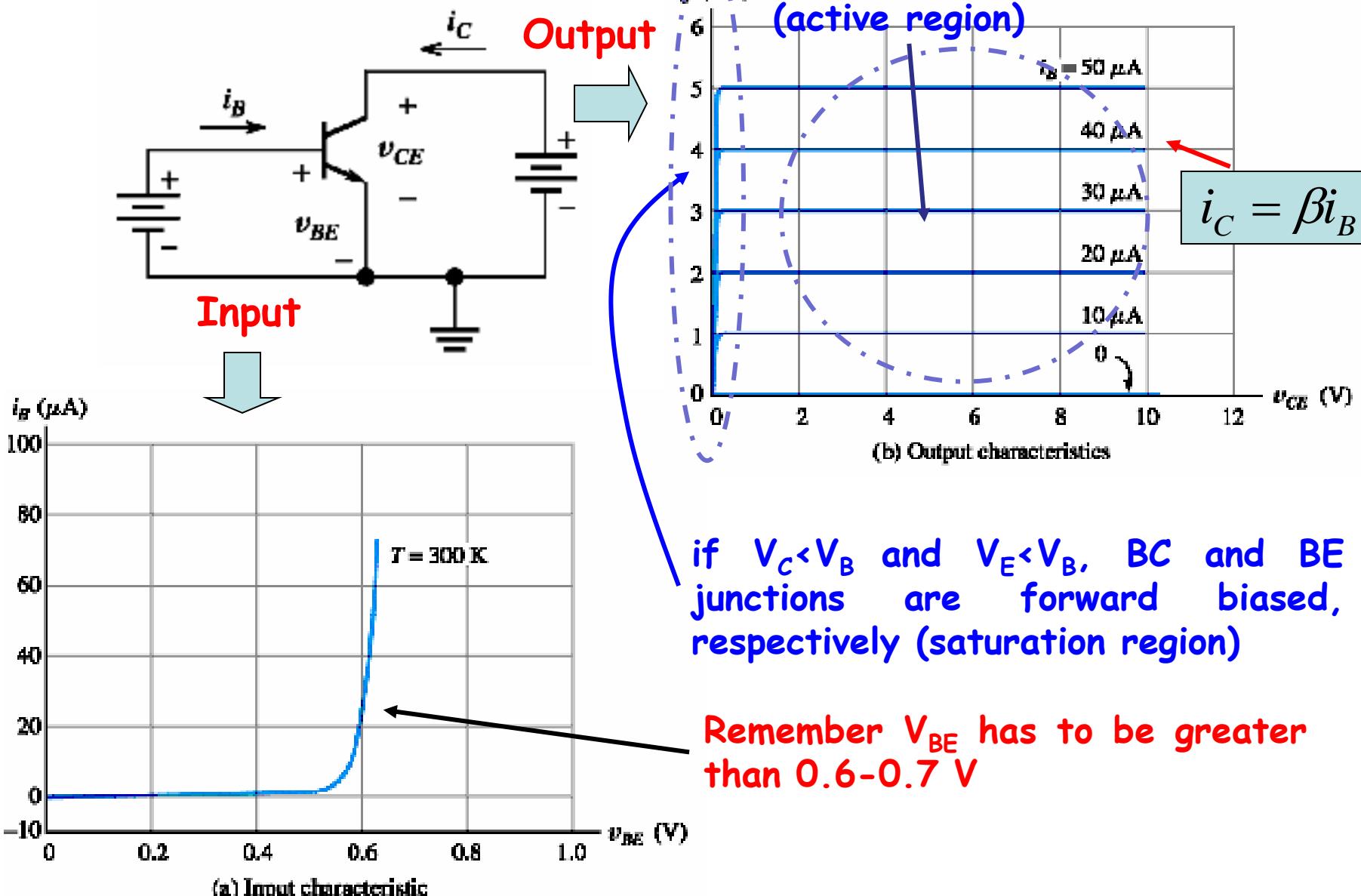
$$i_C = \beta i_B$$

$$i_E = i_B + i_C = i_B + \beta i_B = i_B (\beta + 1)$$

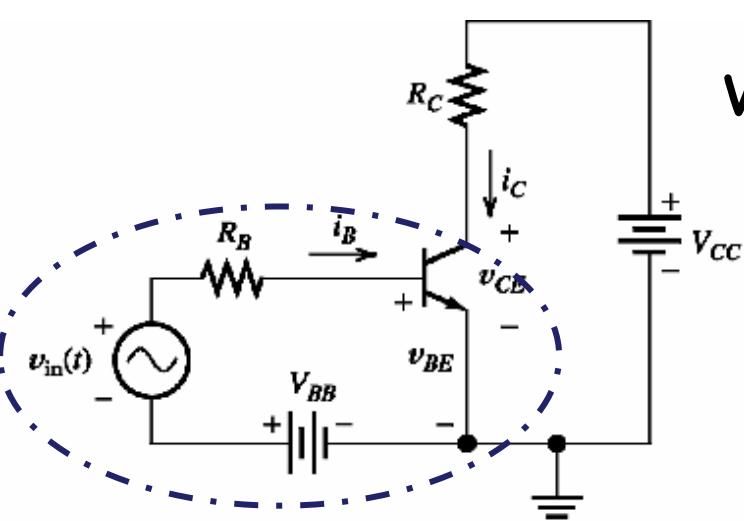


# BJTs - Characteristics

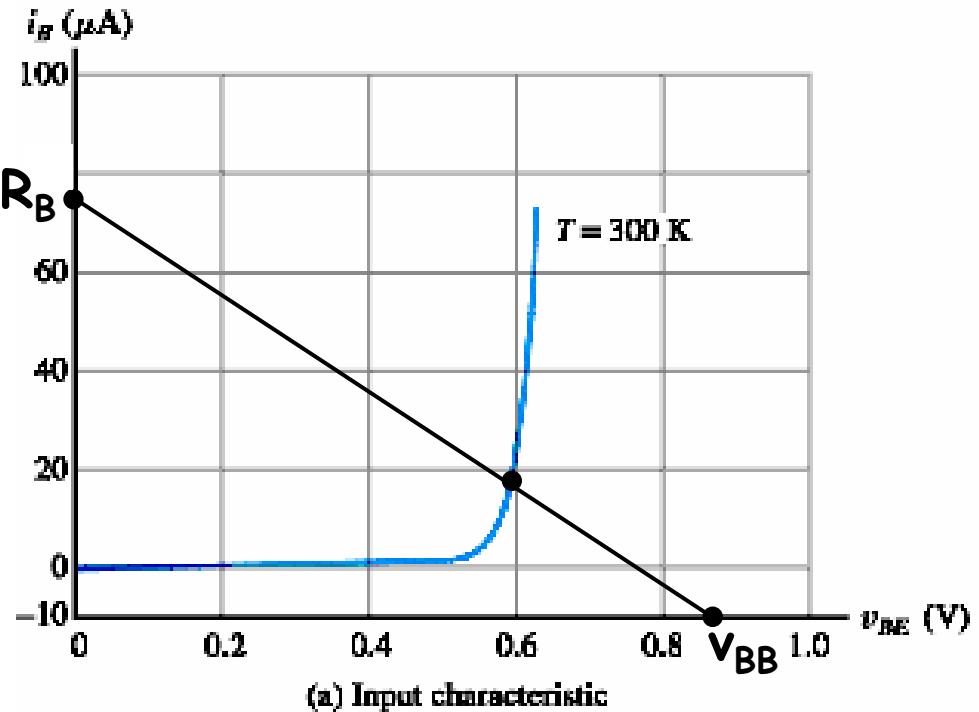
## npn transistor



# BJTs - Load line analysis



Input loop



$$V_{BB} = R_B i_B + V_{BE}$$

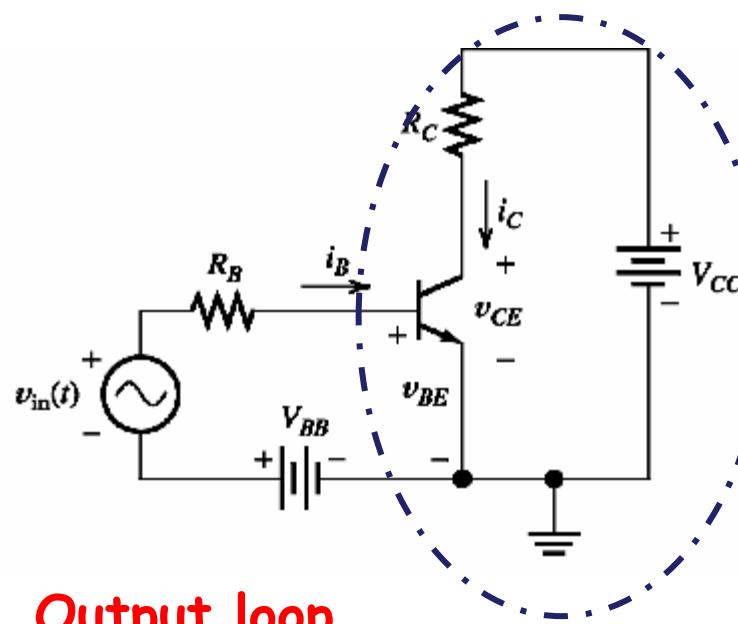
if  $i_B=0$

$$V_{BE} = V_{BB}$$

if  $v_{BE}=0$

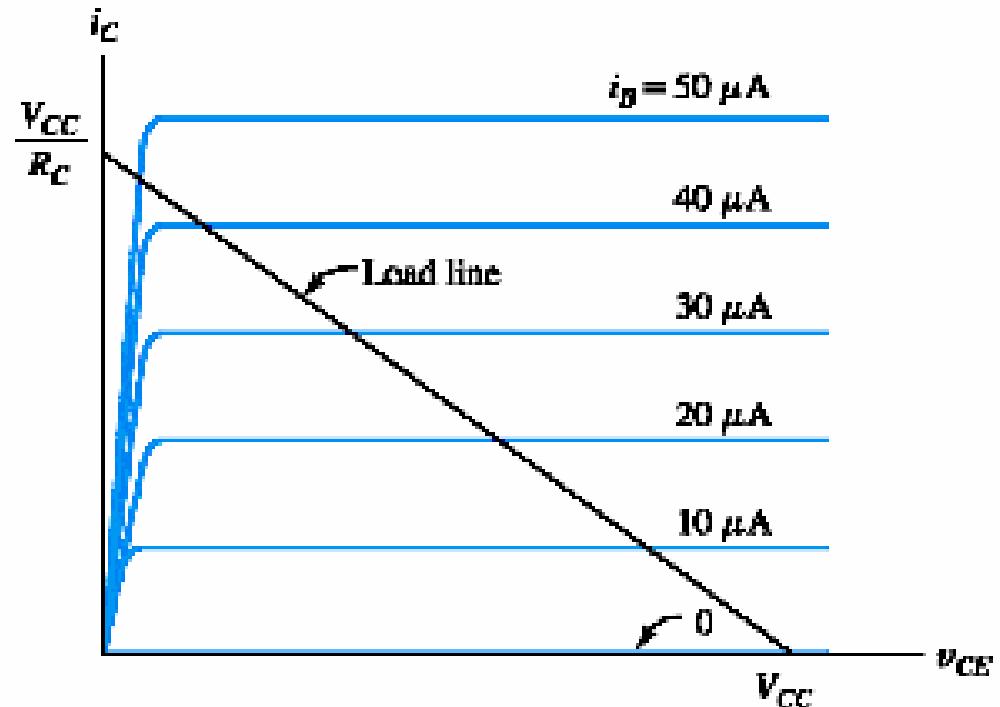
$$i_B = V_{BB} / R_B$$

# BJTs - Load line analysis



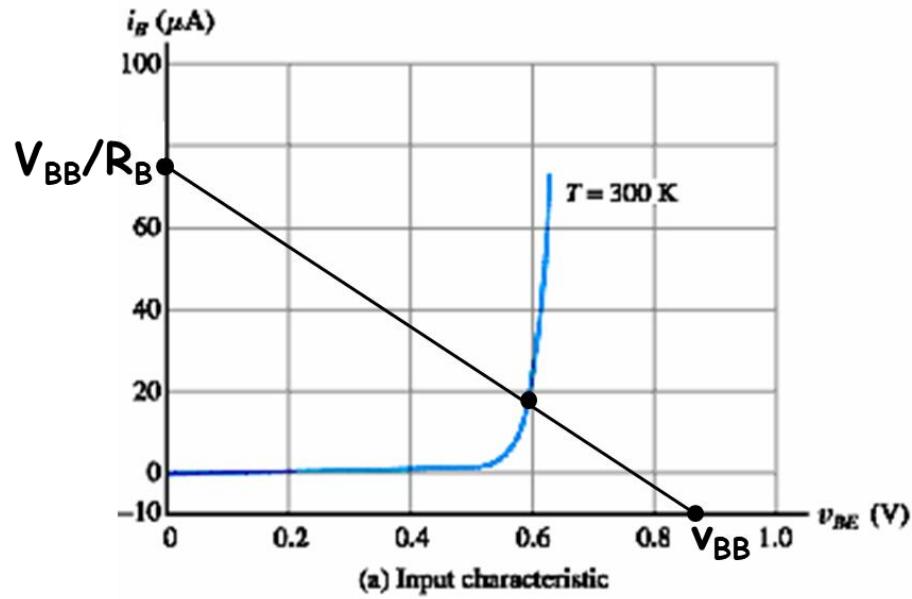
Output loop

$$V_{CC} = R_C i_C + v_{CE}$$



## Load Line Analysis:

Can be performed in order to determine  $|V_{BE}|$  value of transistor in the active and saturation regions.



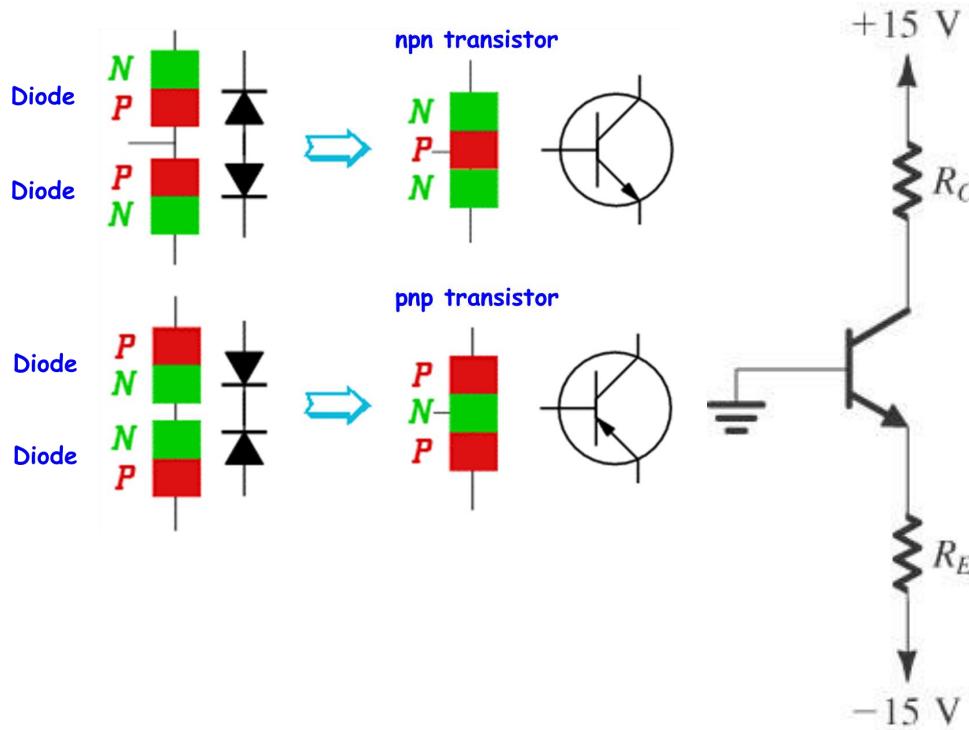
or

Assumption:

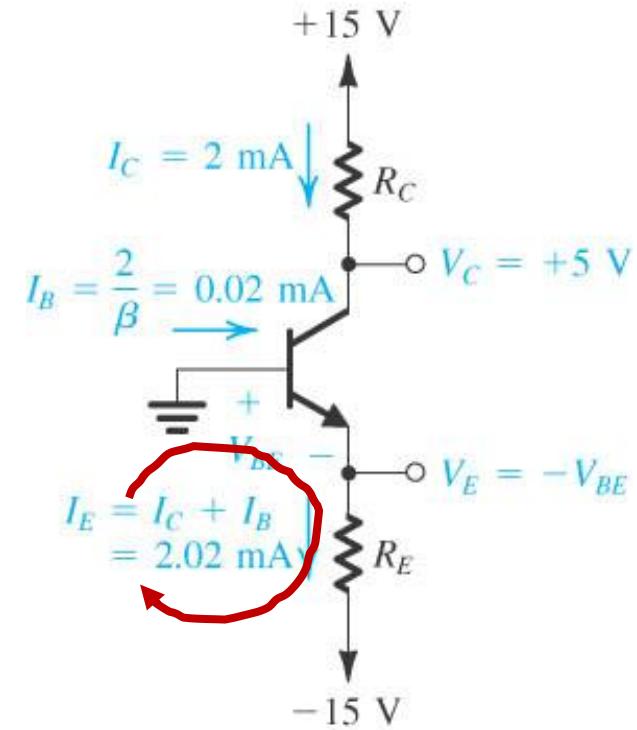
It is assumed that  $|V_{BE}| = 0.7\text{ V}$  in the active and saturation regions.

## Problem :

Analyze the circuit shown in figure to determine current ( $I$ ) and voltage ( $V$ ) values. For the transistor,  $\beta = 100$  and assume that  $|V_{BE}| = 0.7V$  in the active region. ( $R_C = 5k\Omega$ ,  $R_E = 7.07k\Omega$ )



(a)



(b)

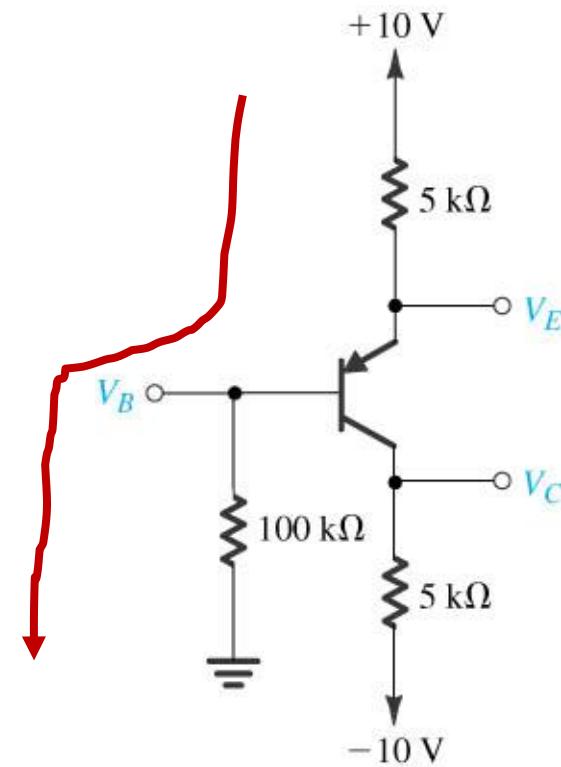
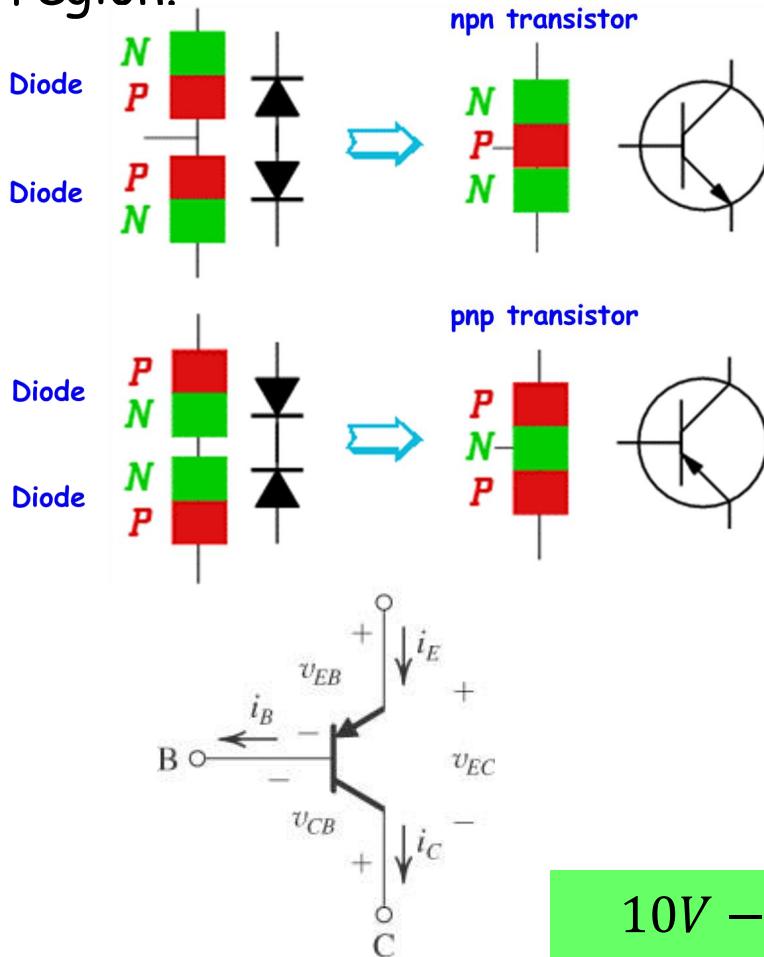
$$0 - V_{BE} - I_B(h_{FE} + 1) R_E = -15V$$

$$I_C = \beta I_B$$

$$I_E = I_B(h_{FE} + 1)$$

## Problem :

Analyze the circuit shown in Figure to determine I and V values. For the transistor, assume that  $\beta = 100$  and  $|V_{BE}| = 0.7V$  in the active region.

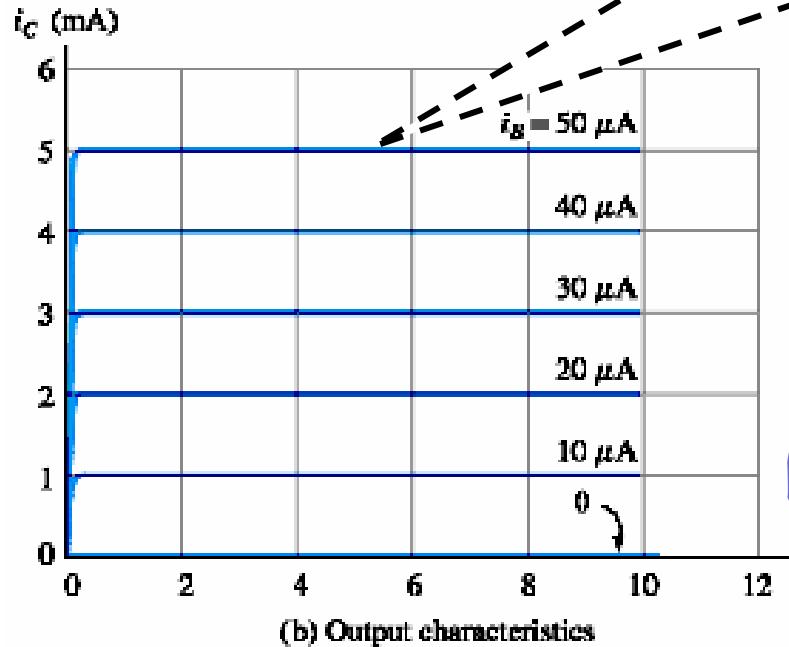


$$10V - I_B(h_{FE} + 1) 5k\Omega - V_{EB} - I_B 100\Omega k = 0$$

$$I_C = \beta I_B$$

# Early Effect

Ideal: Slope is zero



(b) Output characteristics

$$I_C = I_S \exp\left(\frac{V_{BE}}{V_T} - 1\right)$$

$$I_B = \frac{I_S}{\beta} \exp\left(\frac{V_{BE}}{V_T} - 1\right)$$

$$I_{CQ} = I_C + \Delta I_C = I_C + I_C \frac{\Delta V_{CE}}{V_A}$$

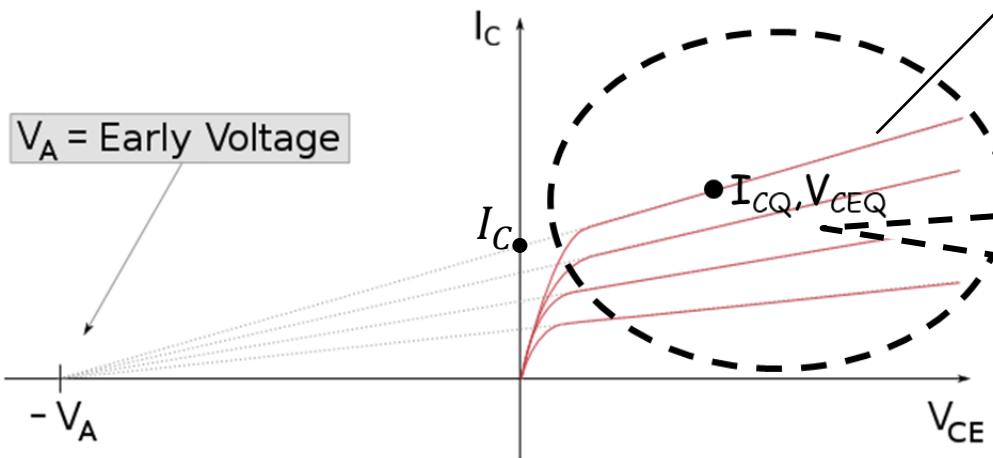
Early Effect

$$\rightarrow I_{CQ} = \left( I_S \exp\left(\frac{V_{BE}}{V_T} - 1\right) \right) \left( 1 + \frac{V_{CEQ}}{V_A} \right)$$

$$\text{slope} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{I_C}{V_A}$$

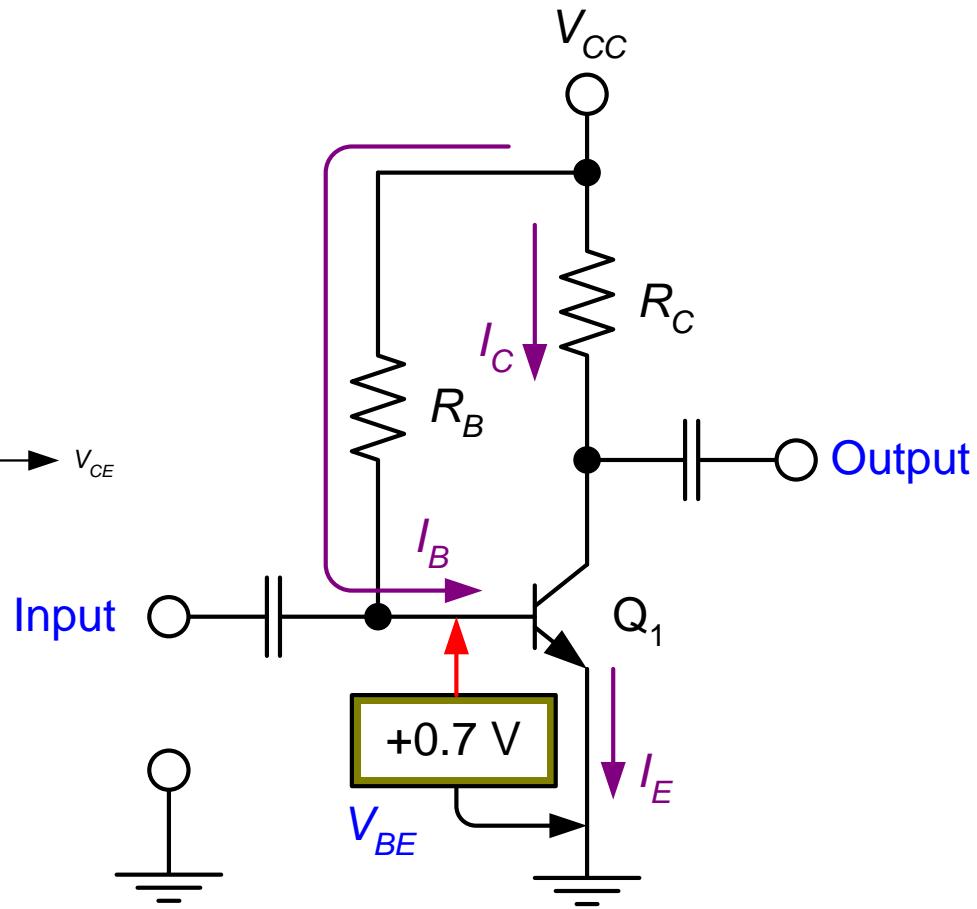
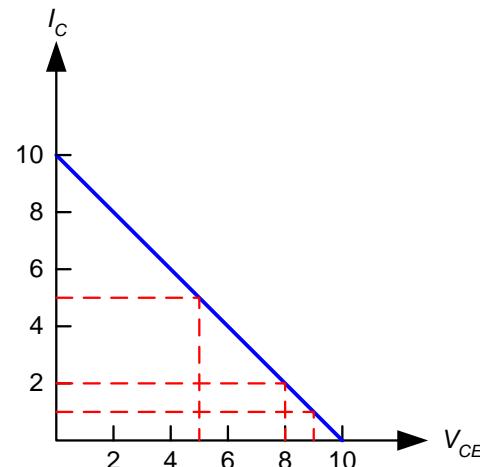
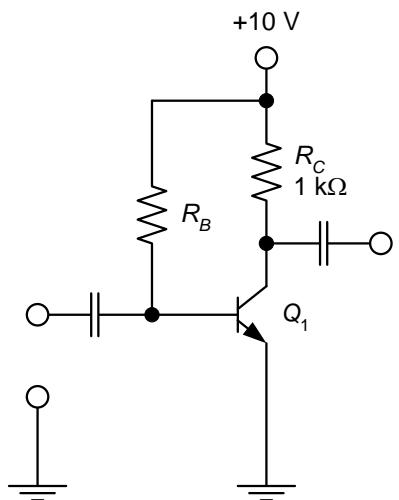
$$\Delta I_C = \Delta V_{CE} \frac{I_C}{V_A} = I_C \frac{\Delta V_{CE}}{V_A}$$

$V_A$  = Early Voltage



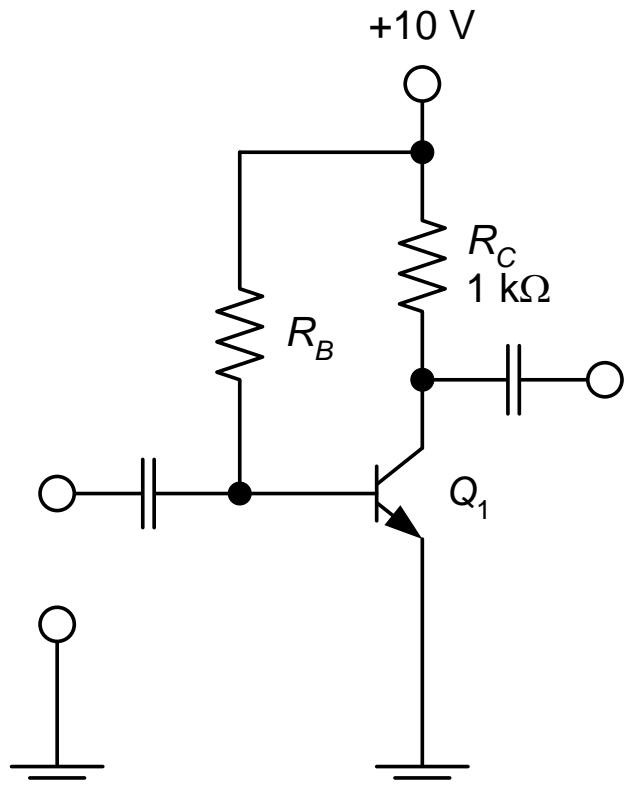
Reality: Slope is not zero.  
This nonlinear behaviour is modeled by 'Early Voltage' ( $V_A$ ).

# DC Biasing Circuits of BJTs



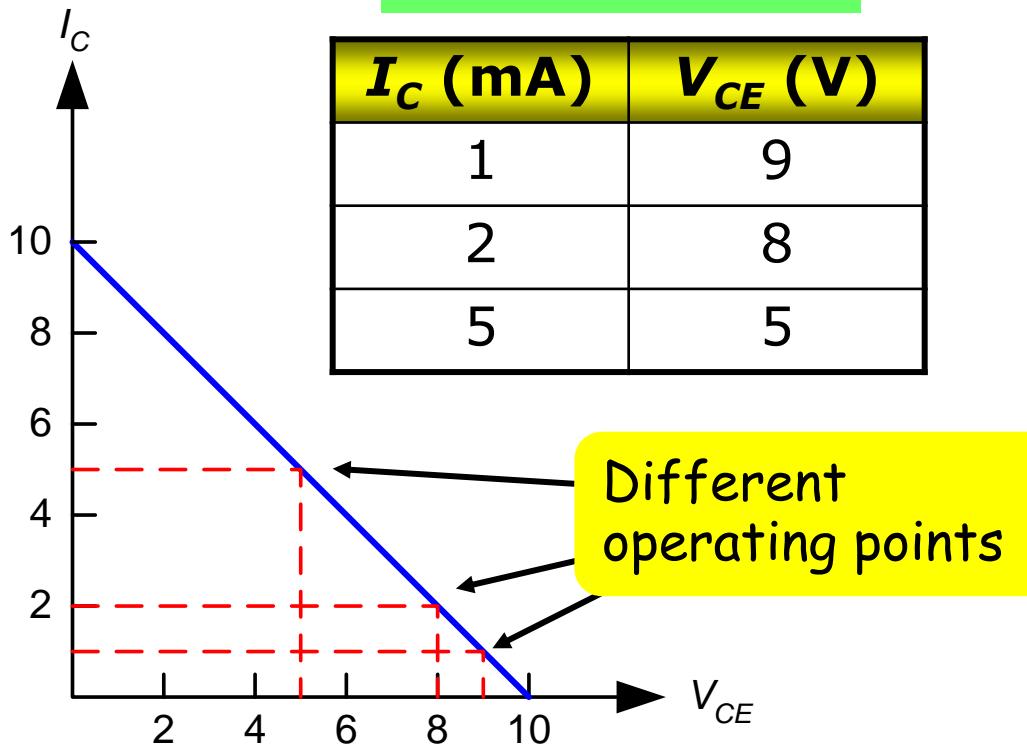
# Example

Plot the DC load line for the circuit shown in Fig. Then, find the values of  $V_{CE}$  for  $I_C = 1, 2, 5 \text{ mA}$  respectively.



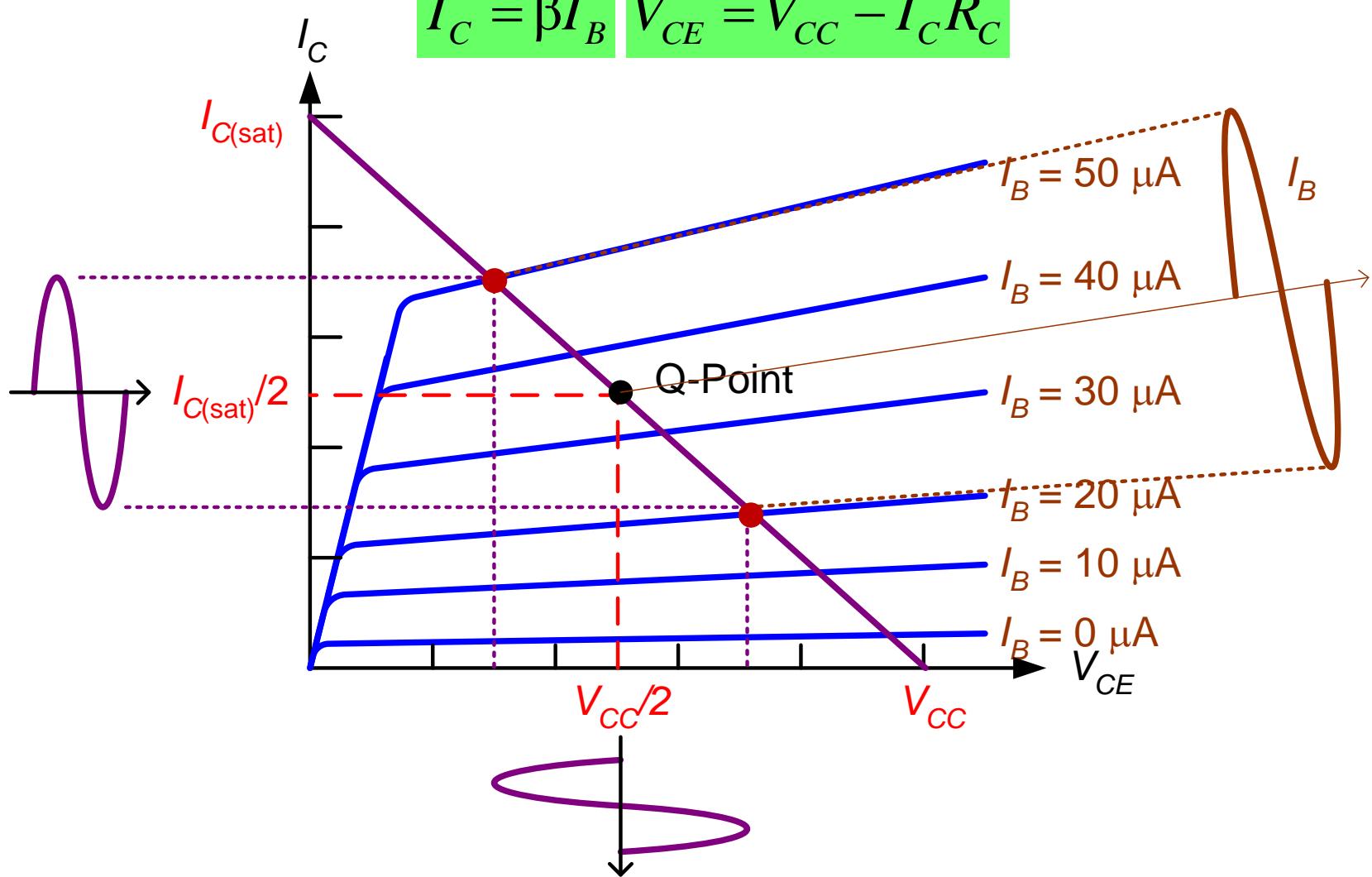
$$V_{CE} = V_{CC} - I_C R_C$$

$I_C (\text{mA})$	$V_{CE} (\text{V})$
1	9
2	8
5	5

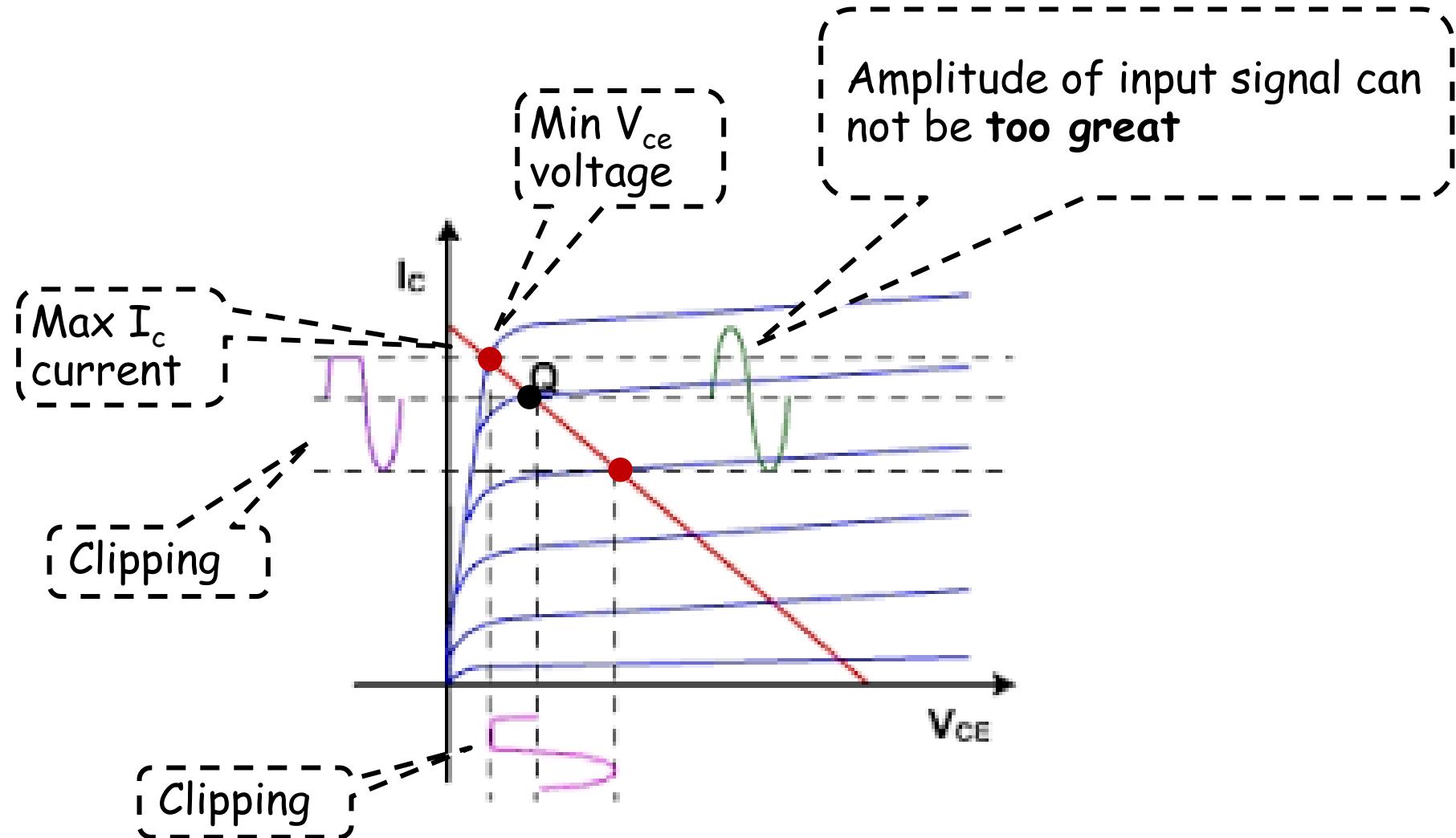


# Optimum Q-point with amplifier operation.

$$I_C = \beta I_B \quad V_{CE} = V_{CC} - I_C R_C$$



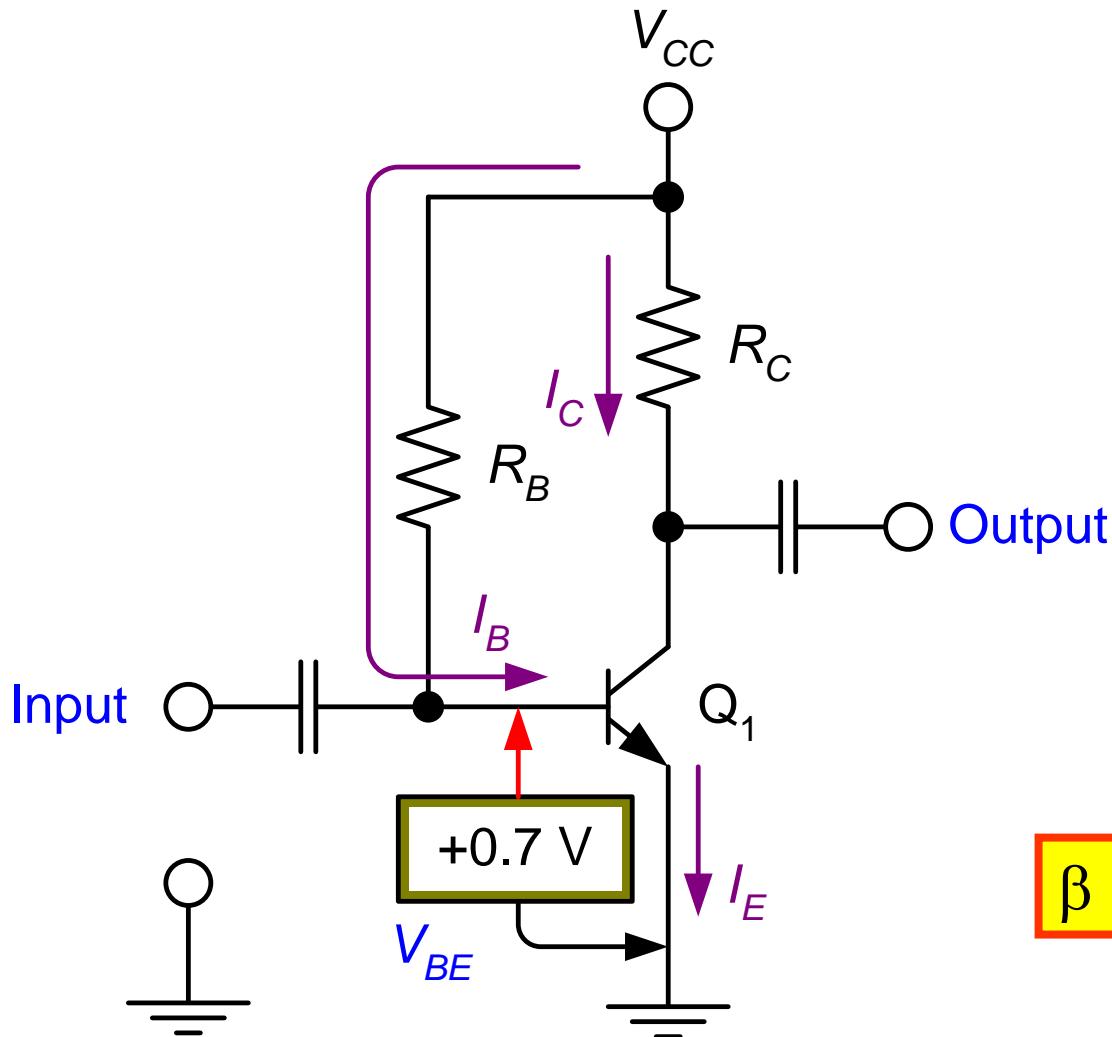
# Q-point is not at optimum location



# BIAS CIRCUITS

Assumption:  
 $|V_{BE}| = 0.7V$

## 1. Base bias (fixed bias).



$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

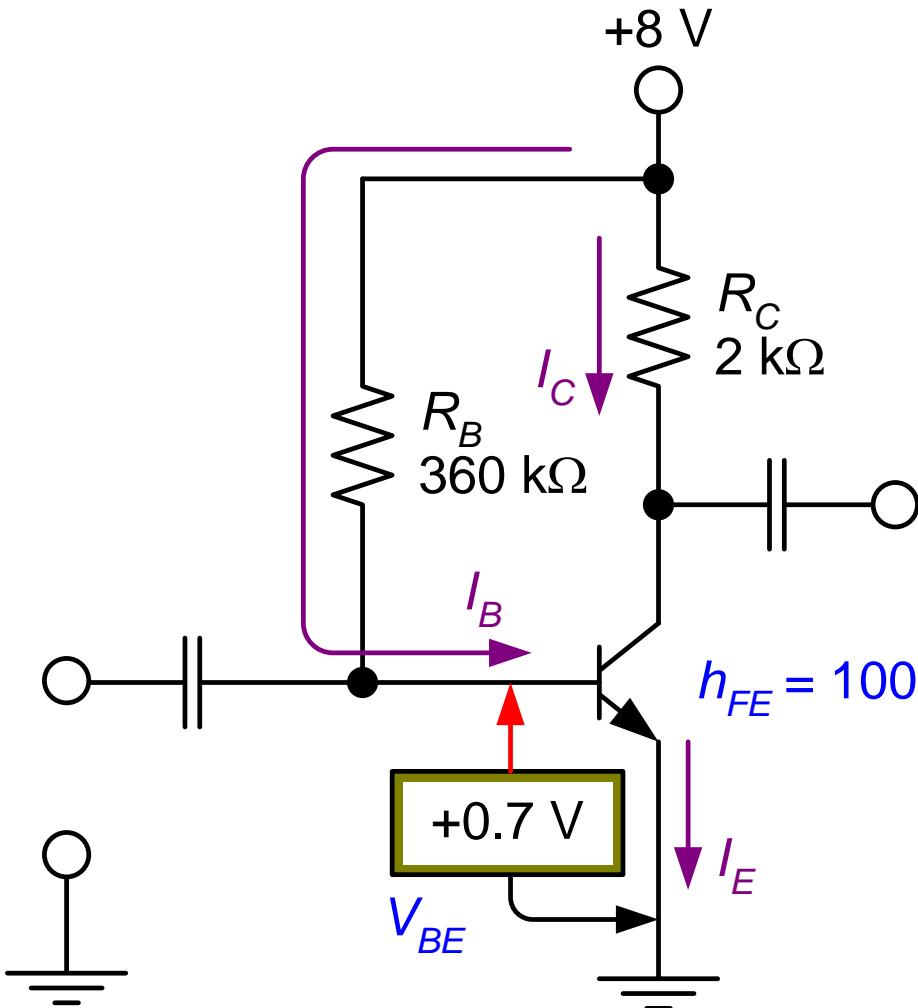
$$I_C = \beta I_B$$

$$V_{CE} = V_{CC} - I_C R_C$$

$\beta = \text{DC current gain} = h_{FE}$

# Example

Construct the DC load line for the circuit and plot the Q-point. Determine whether the circuit is midpoint biased.



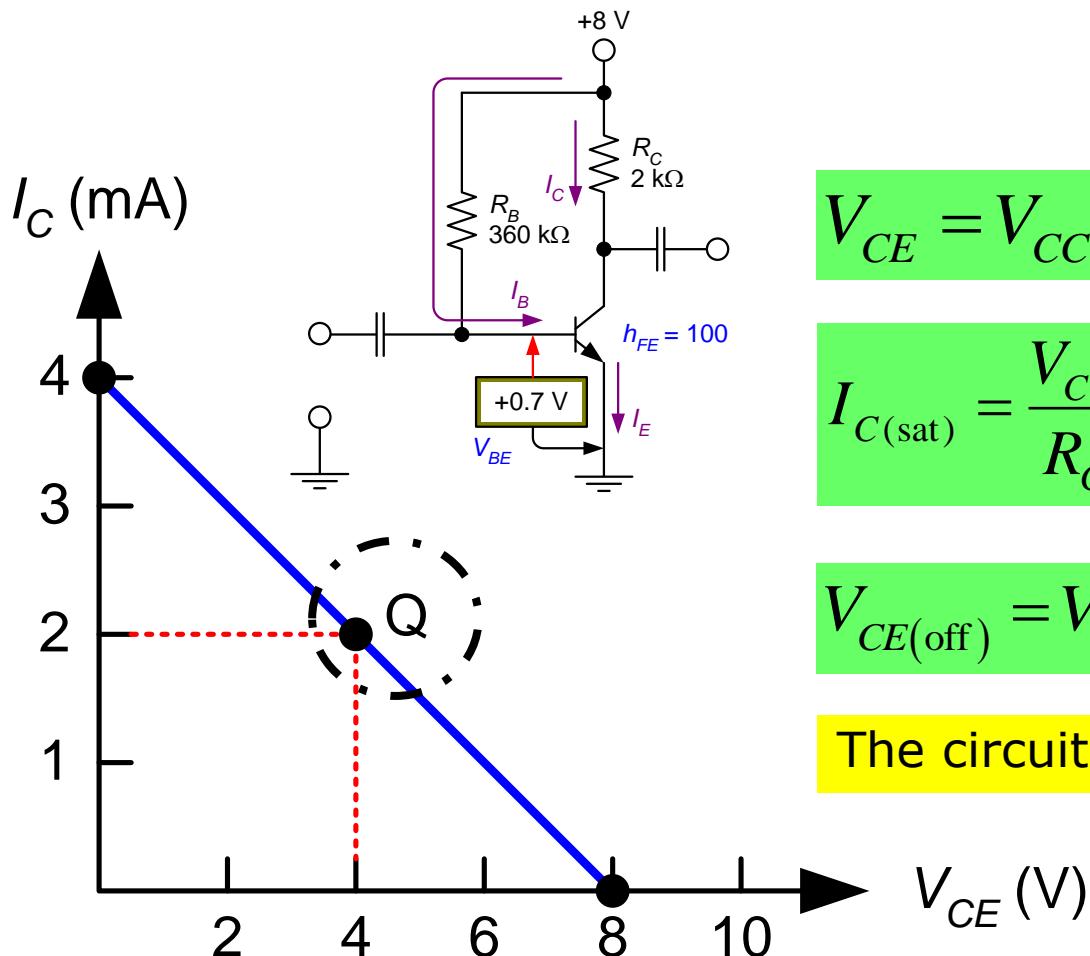
$$I_B = \frac{V_{CC} - 0.7V}{R_B} = \frac{8V - 0.7V}{360k\Omega}$$
$$= 20.28\mu A$$

$$I_C = h_{FE} I_B = (100)(20.28\mu A)$$
$$= 2.028mA$$

$$V_{CE} = V_{CC} - I_C R_C$$
$$= 8V - (2.028mA)(2k\Omega)$$
$$= 3.94V$$

# Example

Construct the DC load line for the circuit



$$V_{CE} = V_{CC} - I_C R_C$$

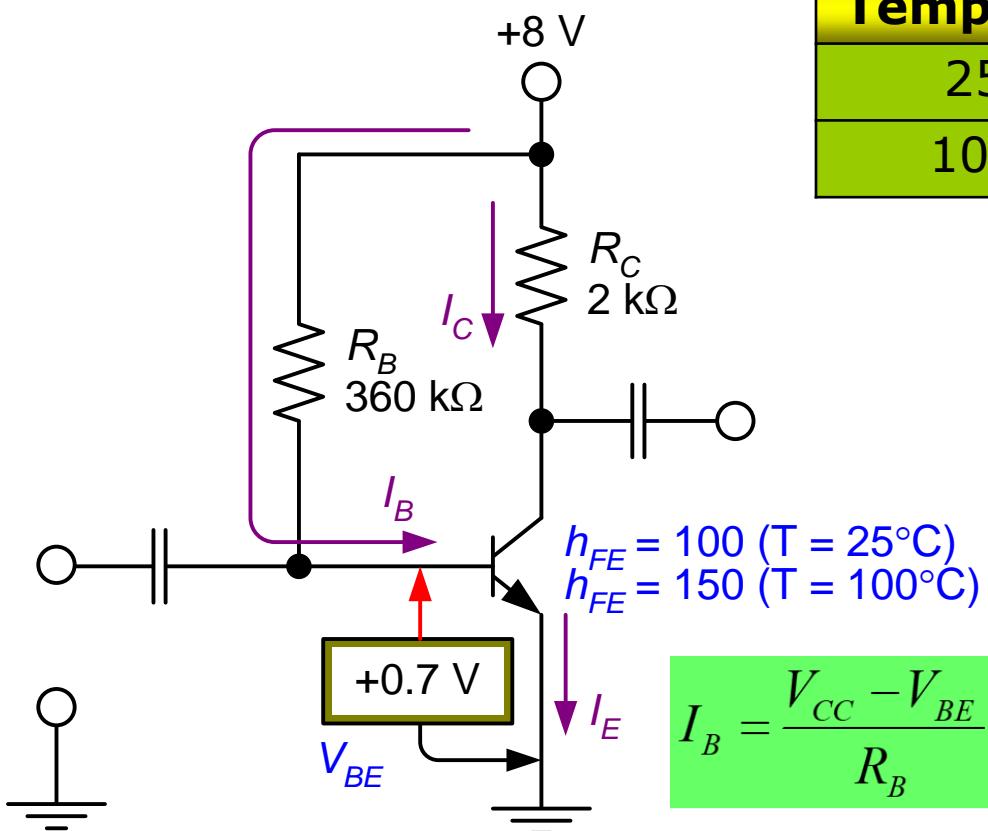
$$I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{8\text{V}}{2\text{k}\Omega} = 4\text{mA}$$

$$V_{CE(\text{off})} = V_{CC} = 8\text{V}$$

The circuit is midpoint biased.

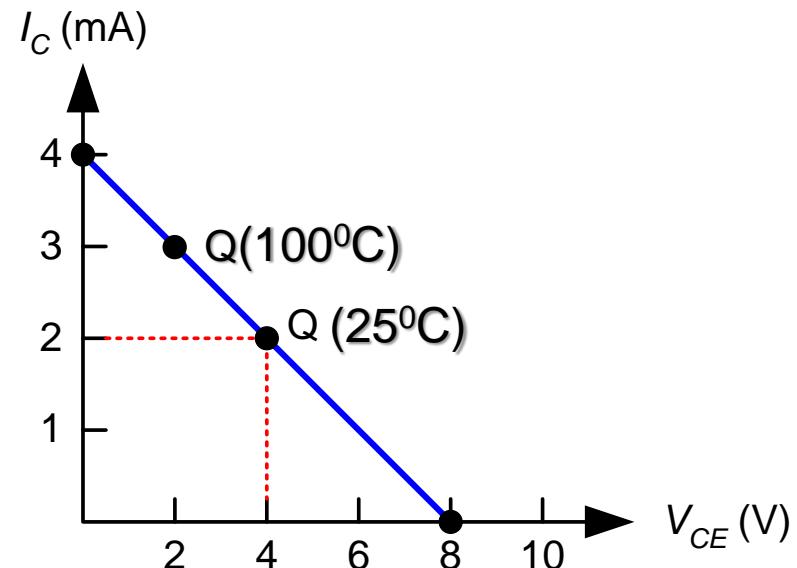
# (Q-point shift)

The transistor has values of  $h_{FE} = 100$  when  $T = 25^\circ\text{C}$  and  $h_{FE} = 150$  when  $T = 100^\circ\text{C}$ . Determine the Q-point values of  $I_C$  and  $V_{CE}$  at both of these temperatures.  $V_{BE}=0.7\text{V}$

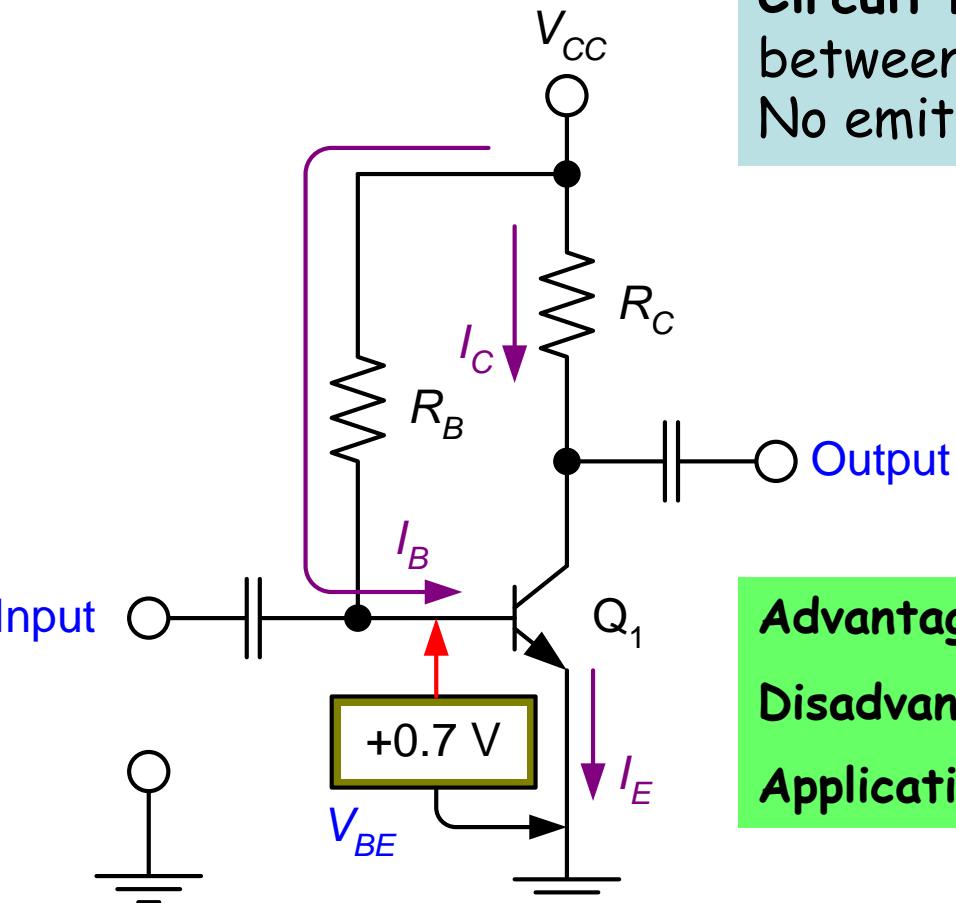


Temp( $^\circ\text{C}$ )	$I_B$ ( $\mu\text{A}$ )	$I_C$ (mA)	$V_{CE}$ (V)
25	20.28	2.028	3.94
100	20.28	3.04	1.92

$$I_C = \beta I_B$$



# Base bias characteristics.



**Circuit recognition:** A single resistor ( $R_B$ ) between the base terminal and  $V_{CC}$ . No emitter resistor.

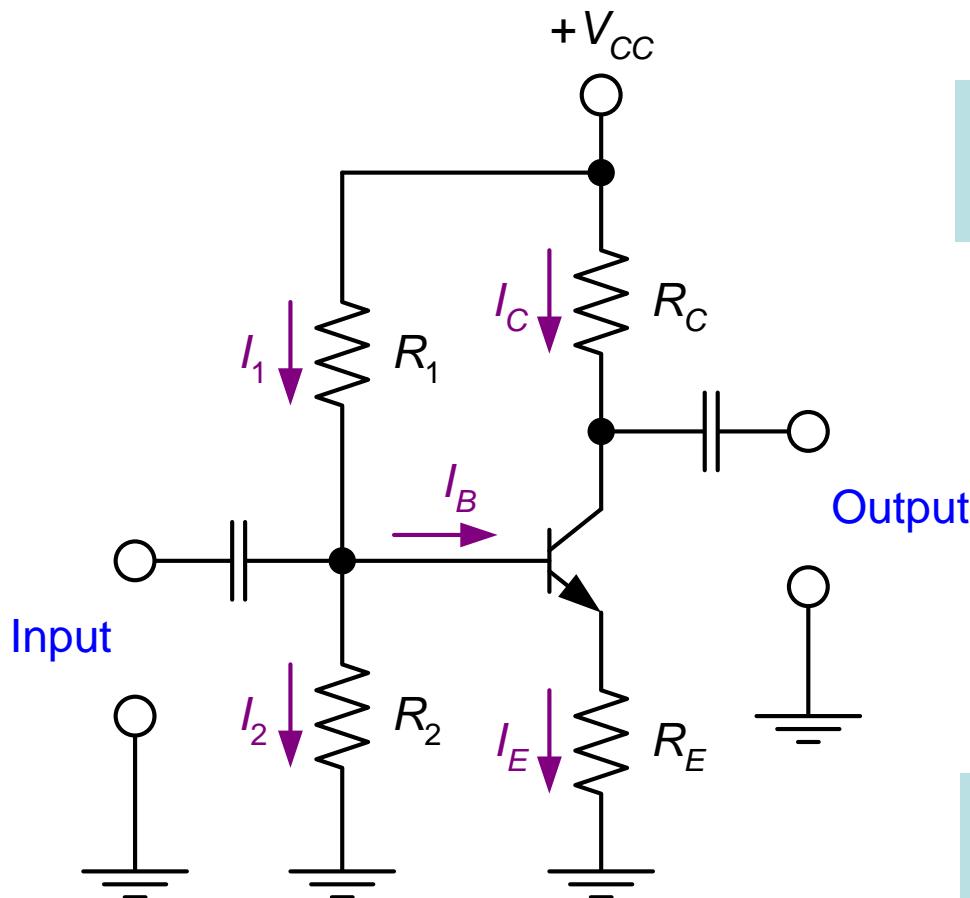
**Advantage:** Circuit simplicity.

**Disadvantage:** Q-point shift with temp.

**Applications:** Switching circuits only.

## 2. Voltage divider bias.

Assumption:  
 $|V_{BE}| = 0.7V$



Assume that  $I_2 > 10I_B$ .  
Therefore, we can neglect  $I_B$

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$V_E = V_B - 0.7V$$

$$I_E = \frac{V_E}{R_E}$$

Assume that  $I_{CQ} \approx I_E$   
( $h_{FE} \gg 1$ ). Then

$$V_{CEQ} = V_{CC} - I_{CQ} (R_C + R_E)$$

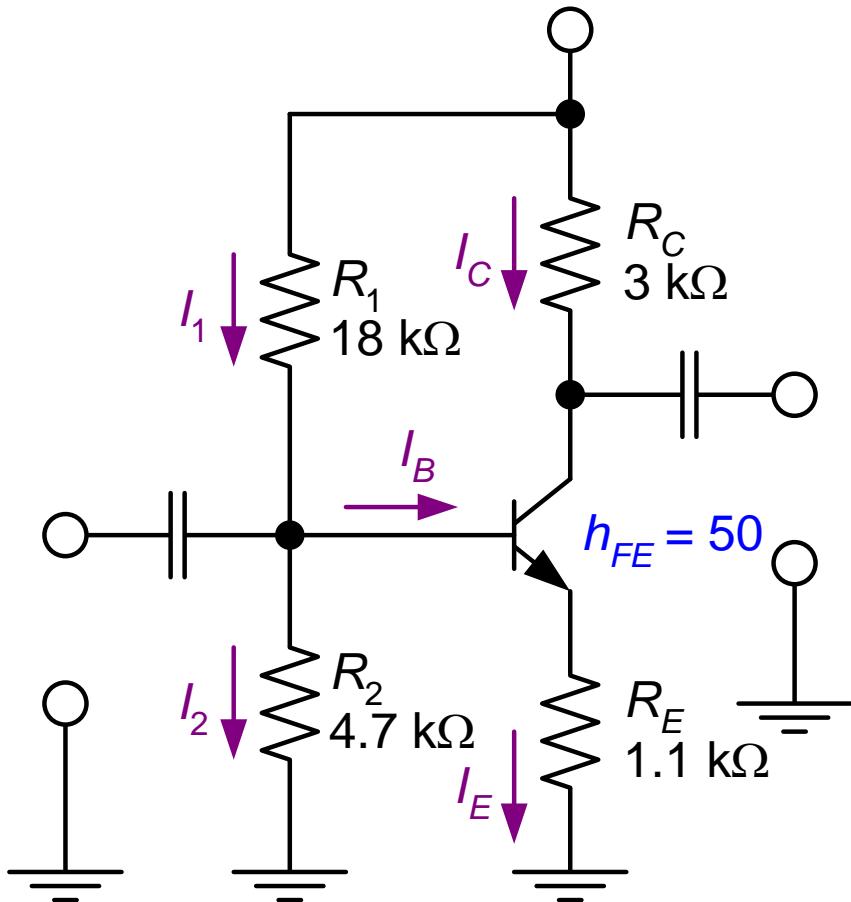
Operating point

# Example

Assumption:  
 $|V_{BE}| = 0.7V$

Determine the values of  $I_{CQ}$  and  $V_{CEQ}$  for the circuit shown in Fig.

+10 V



$$V_B = V_{CC} \frac{R_2}{R_1 + R_2}$$

$$= (10V) \frac{4.7k\Omega}{22.7k\Omega} = 2.07V$$

$$V_E = V_B - 0.7V$$

$$= 2.07V - 0.7V = 1.37V$$

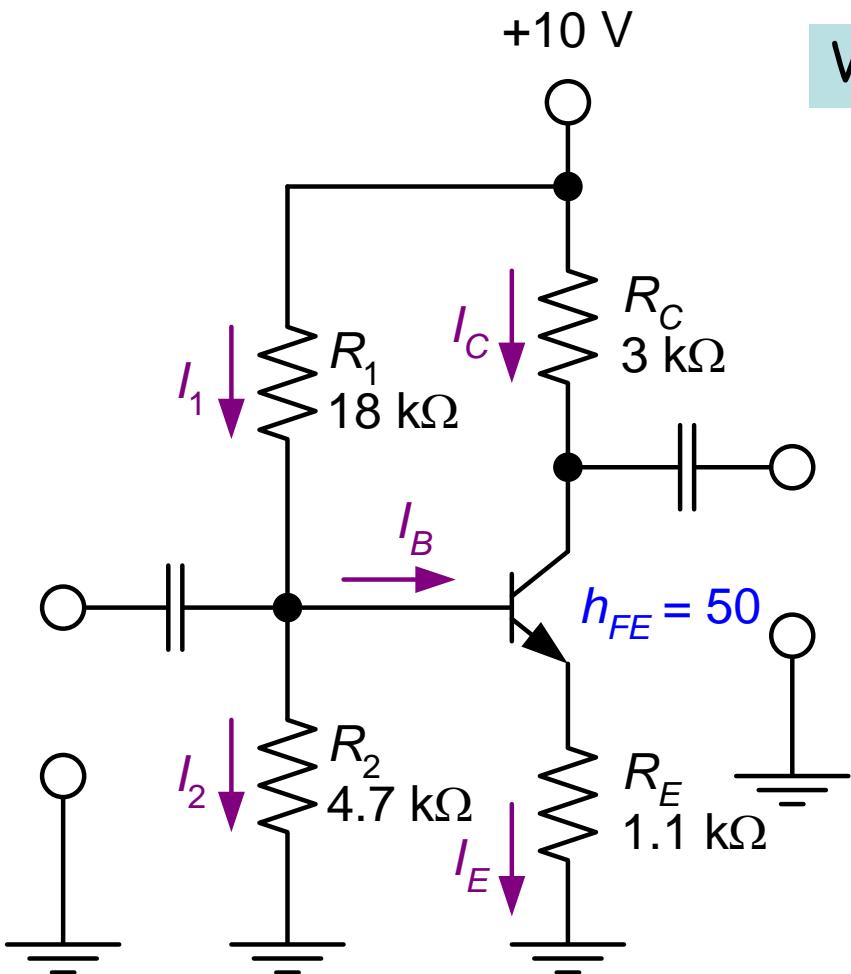
Because  $I_{CQ} @ I_E$  (or  $h_{FE} \gg 1$ ),

$$I_{CQ} \cong \frac{V_E}{R_E} = \frac{1.37V}{1.1k\Omega} = 1.25mA$$

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$$

$$= 10V - (1.25mA)(4.1k\Omega) = 4.87V$$

# Example



Verify that  $I_2 > 10 I_B$

$$I_2 = \frac{V_B}{R_2} = \frac{2.07\text{V}}{4.7\text{k}\Omega} = 440.4\mu\text{A}$$

$$\begin{aligned} I_B &= \frac{I_E}{h_{FE} + 1} = \frac{1.25\text{mA}}{50+1} \\ &= 24.51\mu\text{A} \end{aligned}$$

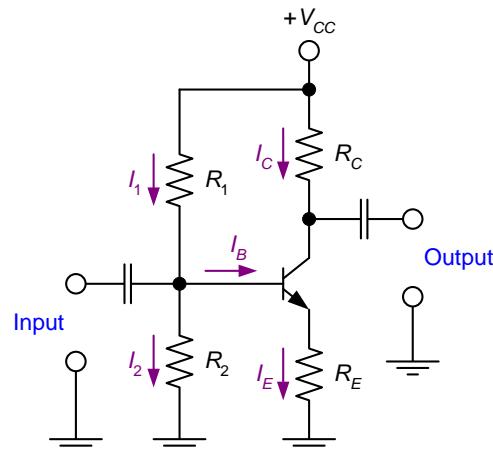
$$\therefore I_2 > 10I_B$$

# Stability of Voltage Divider Bias Circuit

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$V_E = V_B - 0.7V$$

$$I_E = \frac{V_E}{R_E}$$



$I_E$  is determined by  $V_{CC}$ ,  $R_1$ ,  $R_2$  and  $V_{BE}$  voltage of transistor. Their values hardly change with the change of temperature.

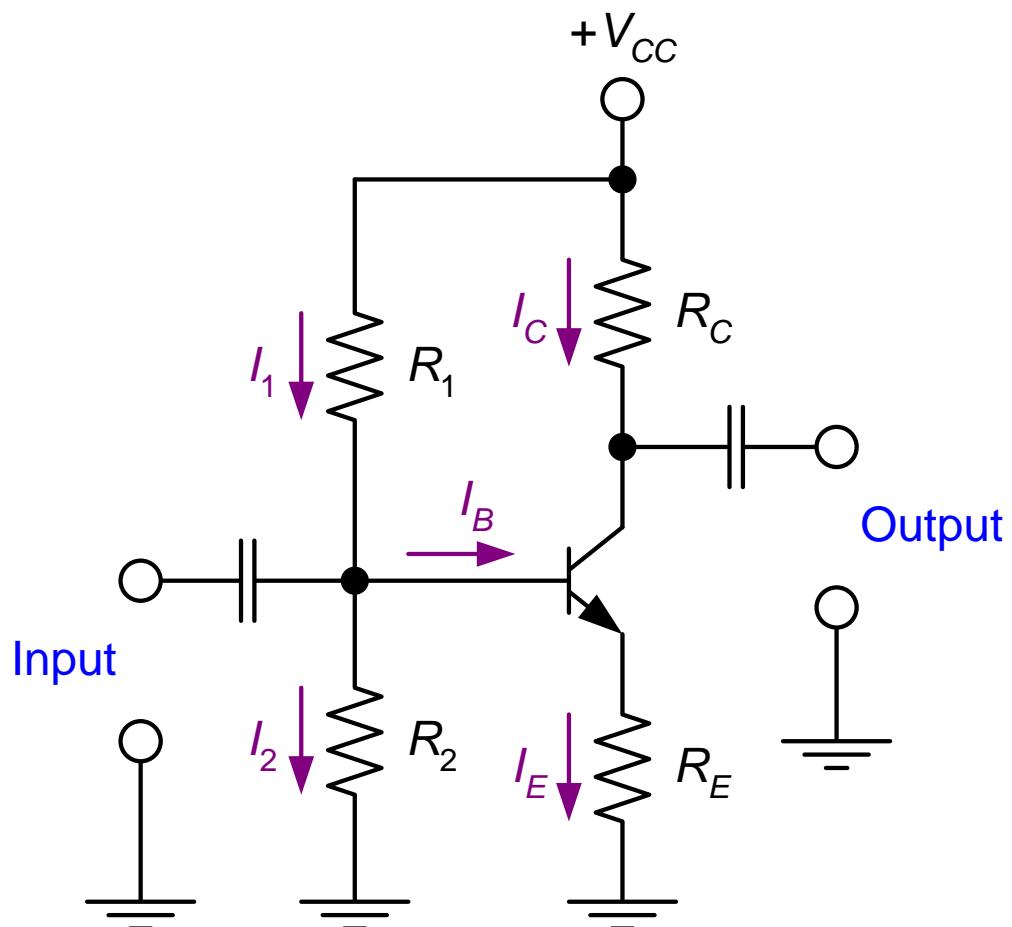
For example, if  $I_E$  is exactly 10 mA and the range of  $h_{FE}$  is from 100 to 300. Then,

$$\text{At } h_{FE} = 100, I_B = \frac{I_E}{h_{FE} + 1} = \frac{10\text{mA}}{101} \cong 100\mu\text{A} \text{ and } I_{CQ} = I_E - I_B \cong 9.90\text{mA}$$

$$\text{At } h_{FE} = 300, I_B = \frac{I_E}{h_{FE} + 1} = \frac{10\text{mA}}{301} \cong 33\mu\text{A} \text{ and } I_{CQ} = I_E - I_B \cong 9.97\text{mA}$$

$I_{CQ}$  hardly changes over the entire range of  $h_{FE}$ .

# Voltage-divider bias characteristics.



**Circuit recognition:** The voltage divider in the base circuit.

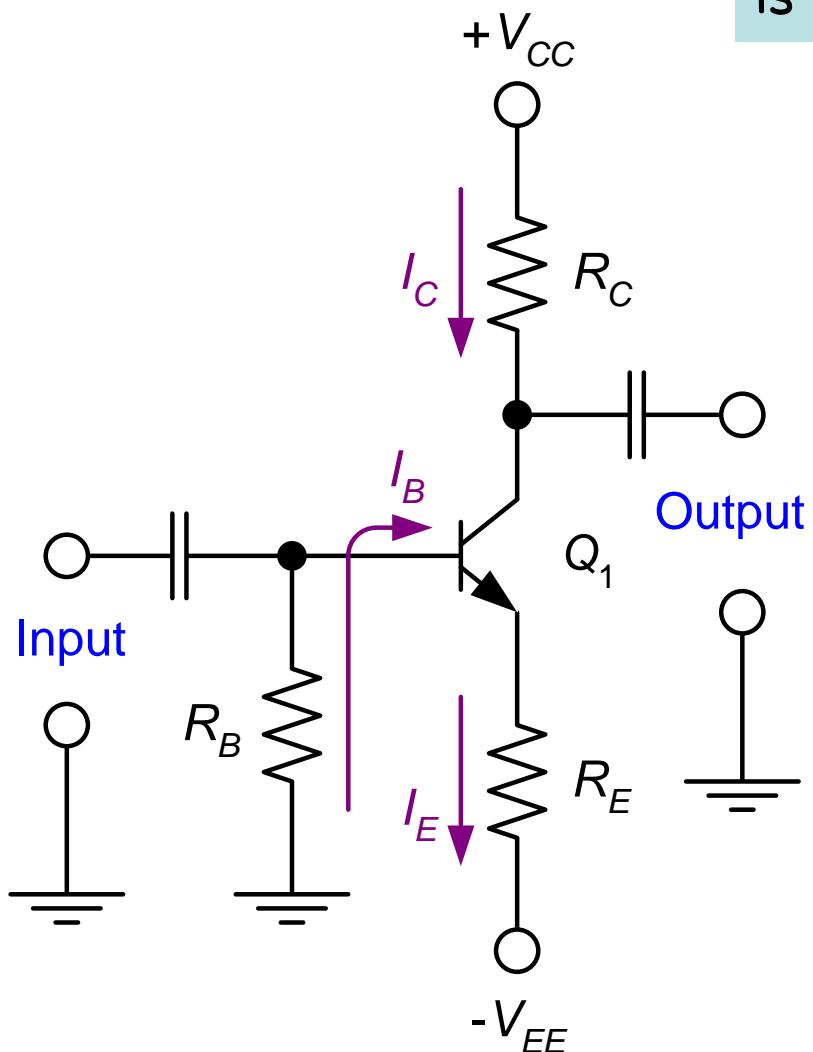
**Advantages:** The circuit Q-point values are stable against changes in  $h_{FE}$ .

**Disadvantages:** Requires more components than most other biasing circuits.

**Applications:** Used primarily to bias linear amplifier.

### 3. Emitter bias.

Assume that the transistor operation is in active region and  $V_{BE}=0.7V$ .



$$0V - I_B R_B - V_{BE} - I_B (h_{FE} + 1) R_E = -V_{EE}$$

$$I_B = \frac{V_{EE} - 0.7V}{R_B + (h_{FE} + 1) R_E}$$

$$I_C = h_{FE} I_B$$

$$I_E = (h_{FE} + 1) I_B$$

$$+V_{CC} - I_C R_C - V_{CE} - I_E R_E = -V_{EE}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E + V_{EE}$$

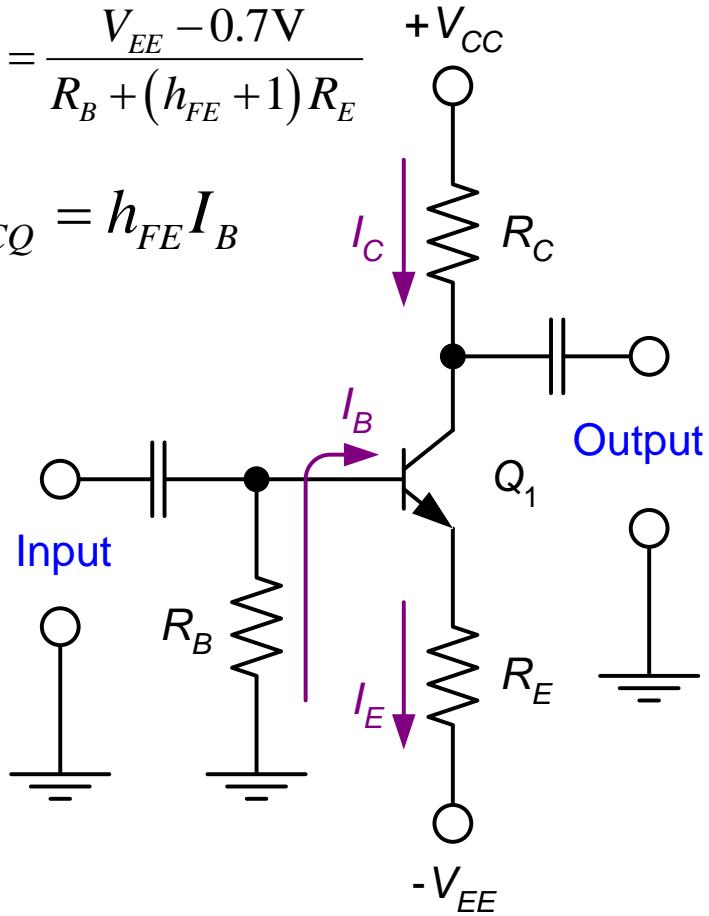
Assume that  $h_{FE} \gg 1$ .

$$V_{CE} \cong V_{CC} - I_C (R_C + R_E) + V_{EE}$$

# Circuit Stability of Emitter-Bias Circuit

$$I_B = \frac{V_{EE} - 0.7V}{R_B + (h_{FE} + 1)R_E}$$

$$I_{CQ} = h_{FE} I_B$$



$h_{FE}$  increases

$I_C$  and  $I_E$  increase (if  $I_B$  is the same)

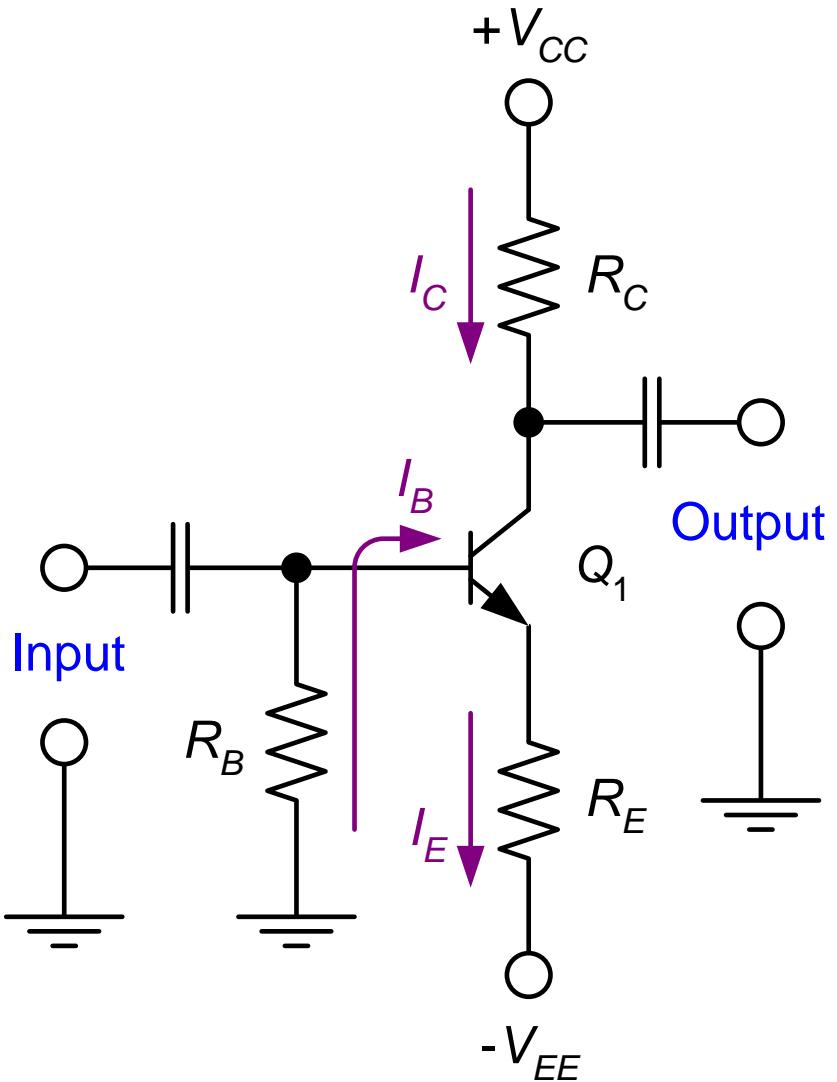
$V_E$  and then  $V_B$  increase

$I_B$  decreases

$I_C$  does not increase that much.

Good Stability. Less dependent on  $h_{FE}$  and temperature.

# Emitter-bias characteristics.



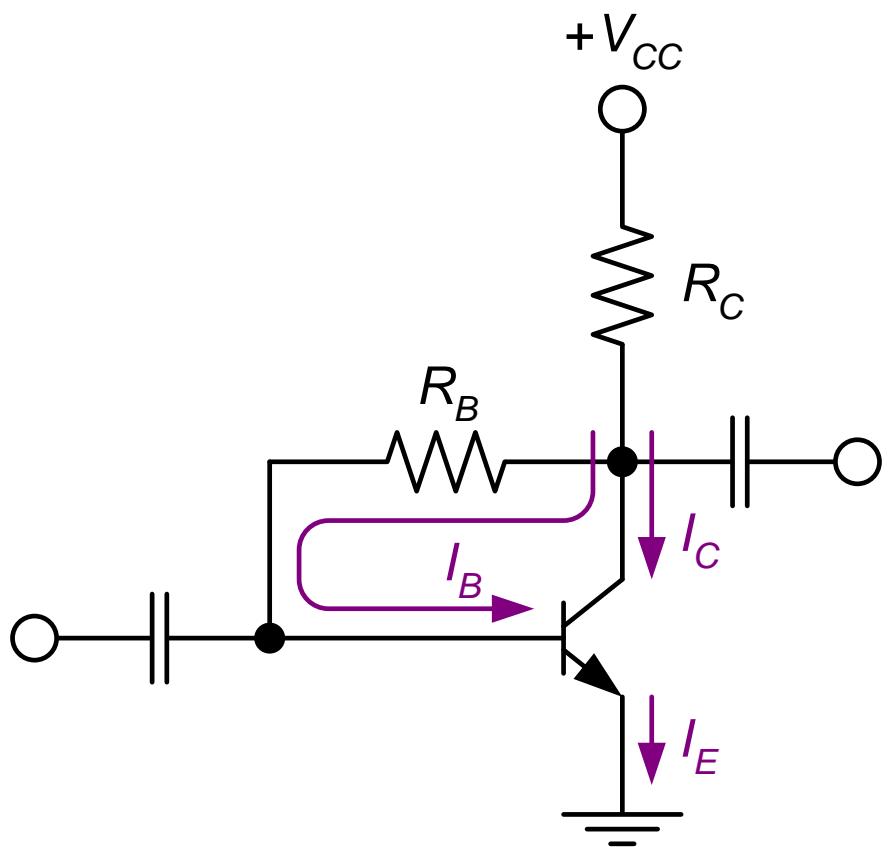
**Circuit recognition:** A split (dual-polarity) power supply and the base resistor is connected to ground.

**Advantage:** The circuit Q-point values are stable against changes in  $h_{FE}$ .

**Disadvantage:** Requires the use of dual-polarity power supply.

**Applications:** Used primarily to bias linear amplifiers.

## 4. Collector-feedback bias.



$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{(h_{FE} + 1)R_C + R_B}$$

$$I_{CQ} = h_{FE} I_B$$

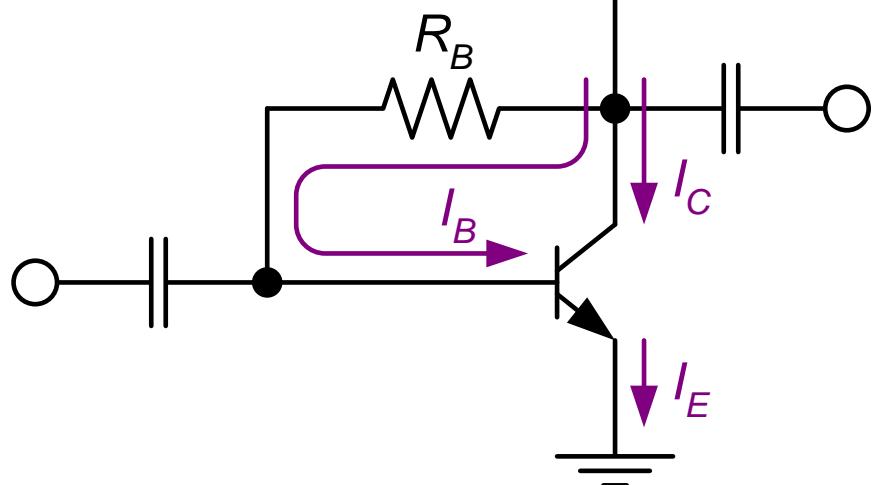
$$V_{CEQ} = V_{CC} - (h_{FE} + 1) I_B R_C$$

$$\cong V_{CC} - I_{CQ} R_C$$

# Circuit Stability of Collector-Feedback Bias

$$I_B = \frac{V_{CC} - V_{BE}}{(h_{FE} + 1)R_C + R_B}$$

$$I_{CQ} = h_{FE} I_B$$



$$V_C - I_B R_B - V_{BE} = 0$$

$h_{FE}$  increases



$I_C$  increases (if  $I_B$  is the same)



$V_{CE}$  and  $V_C$  decreases



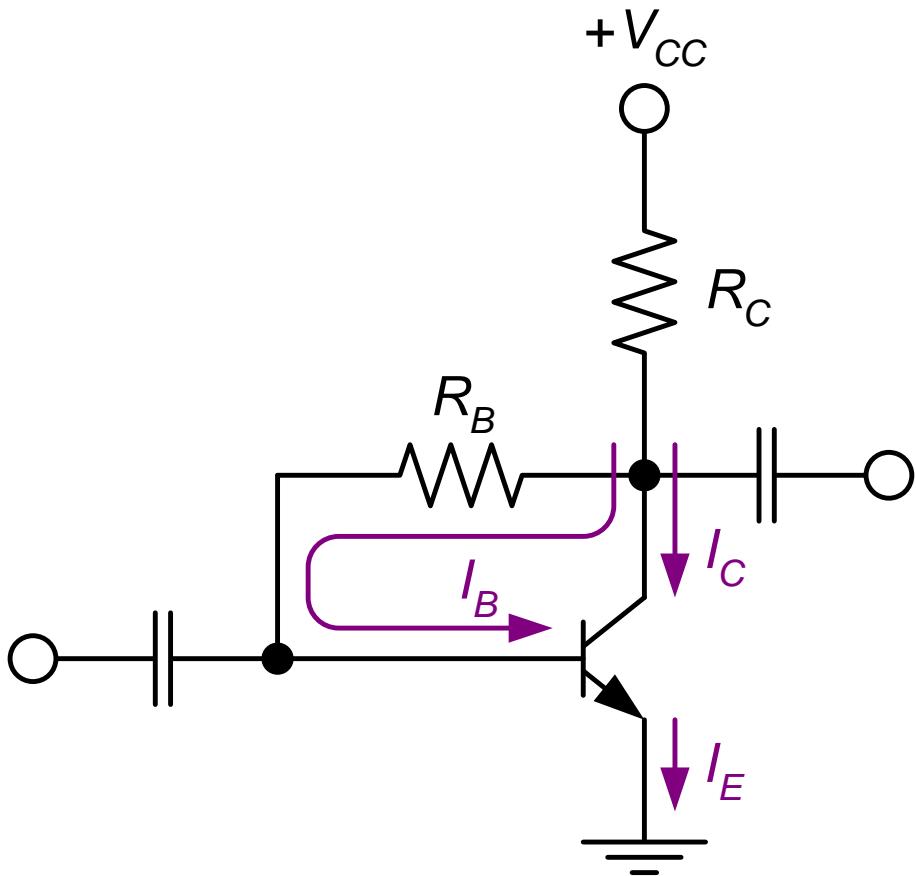
$I_B$  decreases



$I_C$  does not increase that much.

Good Stability. Less dependent  
on  $h_{FE}$  and temperature.

# Collector-Feedback Characteristics



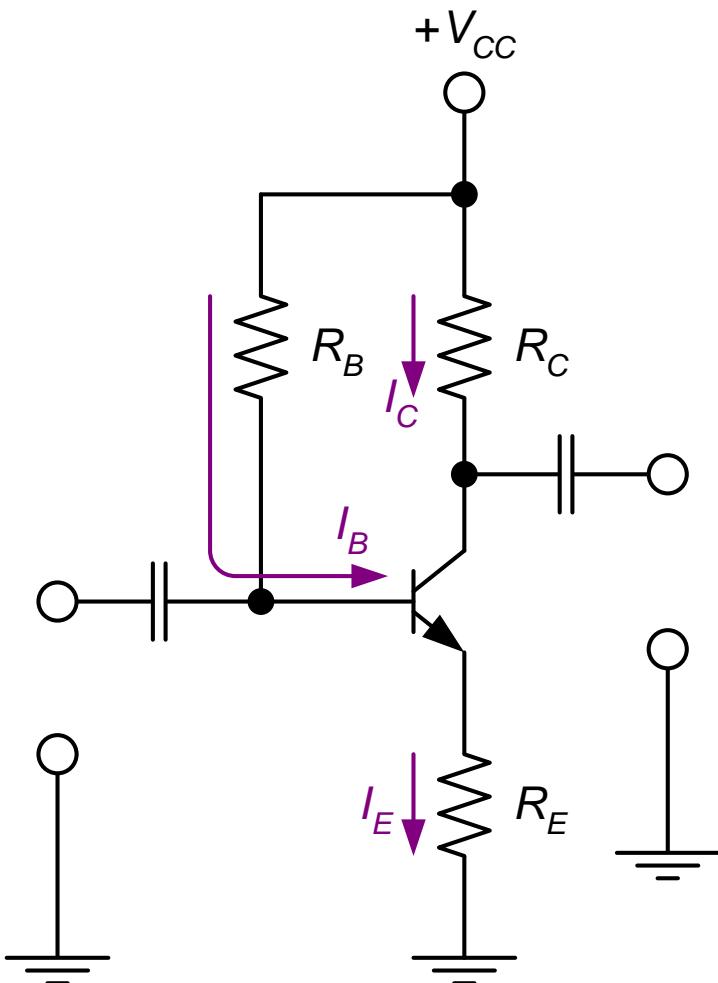
**Circuit recognition:** The base resistor is connected between the base and the collector terminals of the transistor.

**Advantage:** A simple circuit with relatively stable Q-point.

**Disadvantage:** Relatively poor AC characteristics.

**Applications:** Used primarily to bias linear amplifiers.

## 5. Emitter-feedback bias.



$$V_{CC} - I_B R_B - V_{BE} - I_B (h_{FE} + 1) R_E = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (h_{FE} + 1) R_E}$$

$$I_{CQ} = h_{FE} I_B$$

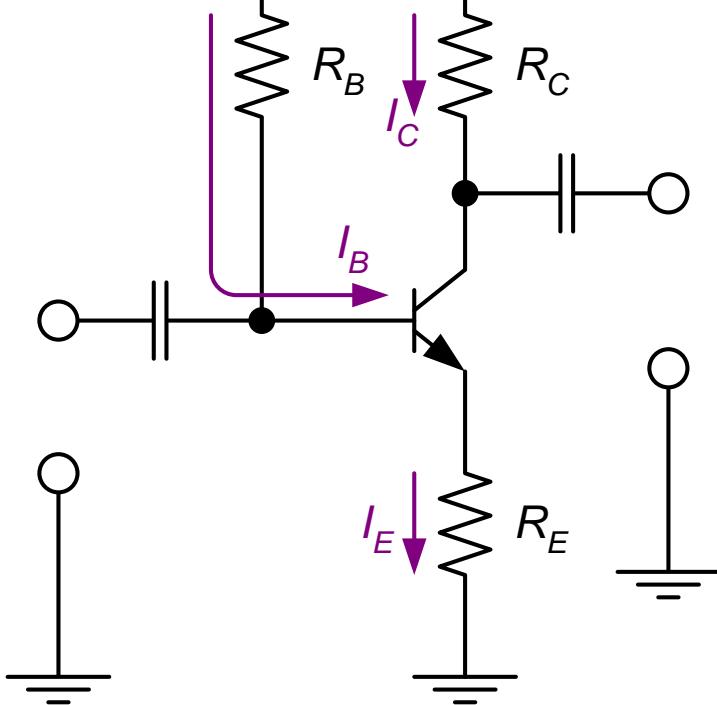
$$I_E = (h_{FE} + 1) I_B$$

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_C R_C - I_E R_E \\ &\cong V_{CC} - I_{CQ} (R_C + R_E) \end{aligned}$$

# Circuit Stability of Emitter-Feedback Bias

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (h_{FE} + 1)R_E}$$

$$I_{CQ} = h_{FE} I_B$$



$$V_{CC} - I_B R_B = V_B$$

$h_{FE}$  increases



$I_C, I_E$  increases (if  $I_B$  is the same)



$V_E, V_B$  increases



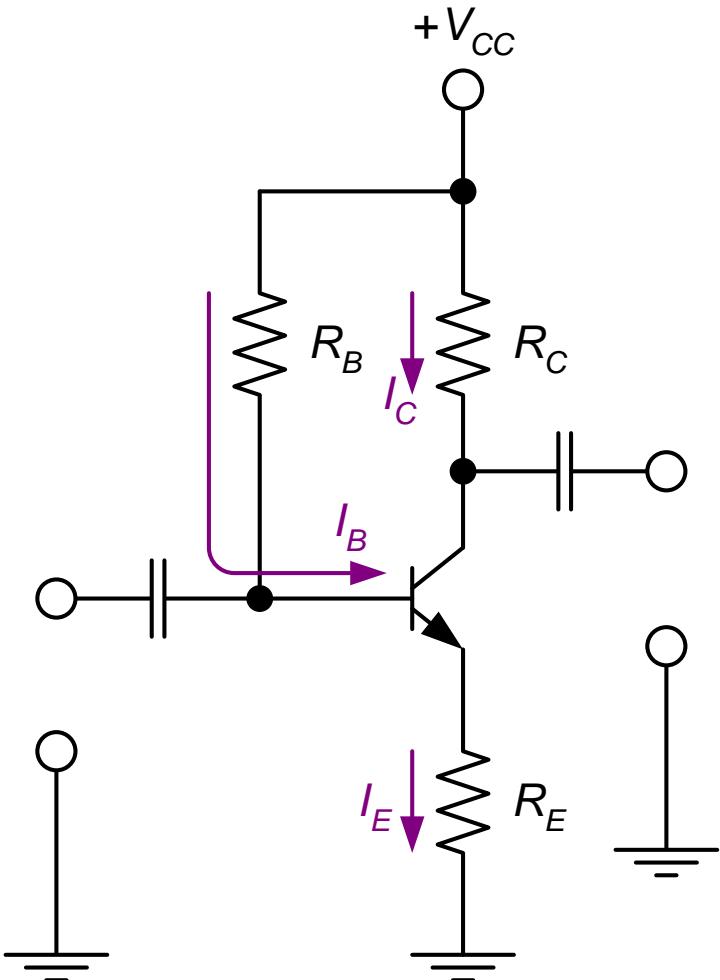
$I_B$  decreases



$I_C$  does not increase that much.

$I_C$  is less dependent on  $h_{FE}$  and temperature.

# Emitter-Feedback Characteristics



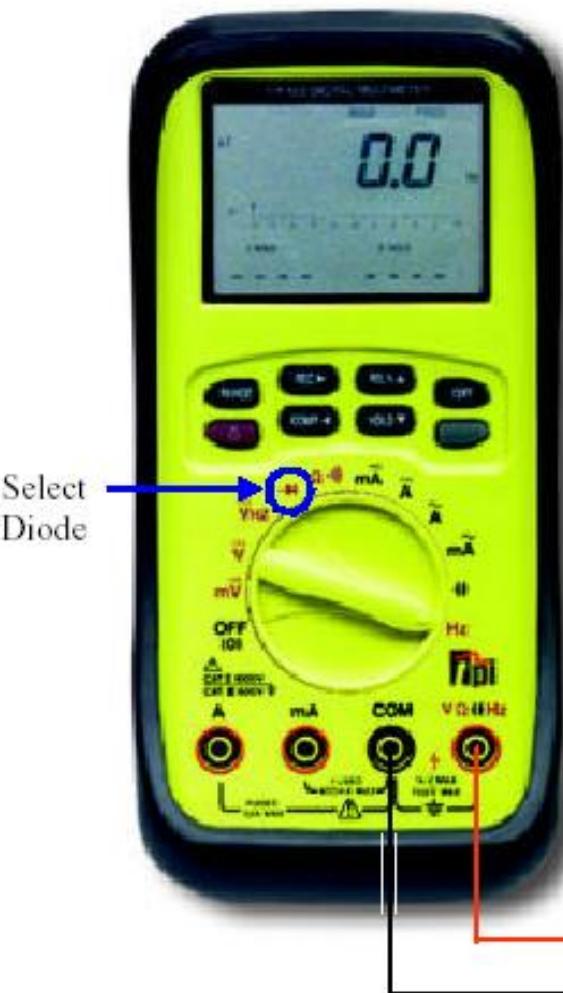
**Circuit recognition:** Similar to voltage divider bias with  $R_2$  missing (or base bias with  $R_E$  added).

**Advantage:** A simple circuit with relatively stable Q-point.

**Disadvantage:** Requires more components than collector-feedback bias.

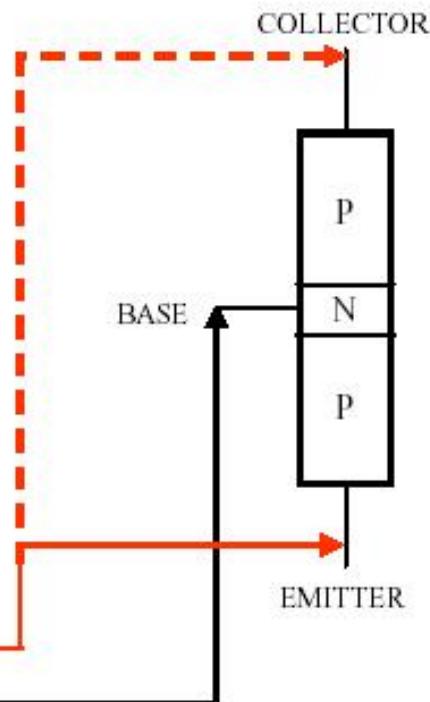
**Applications:** Used primarily to bias linear amplifiers.

# BJTs - Testing



TPI 183 Digital Multimeter

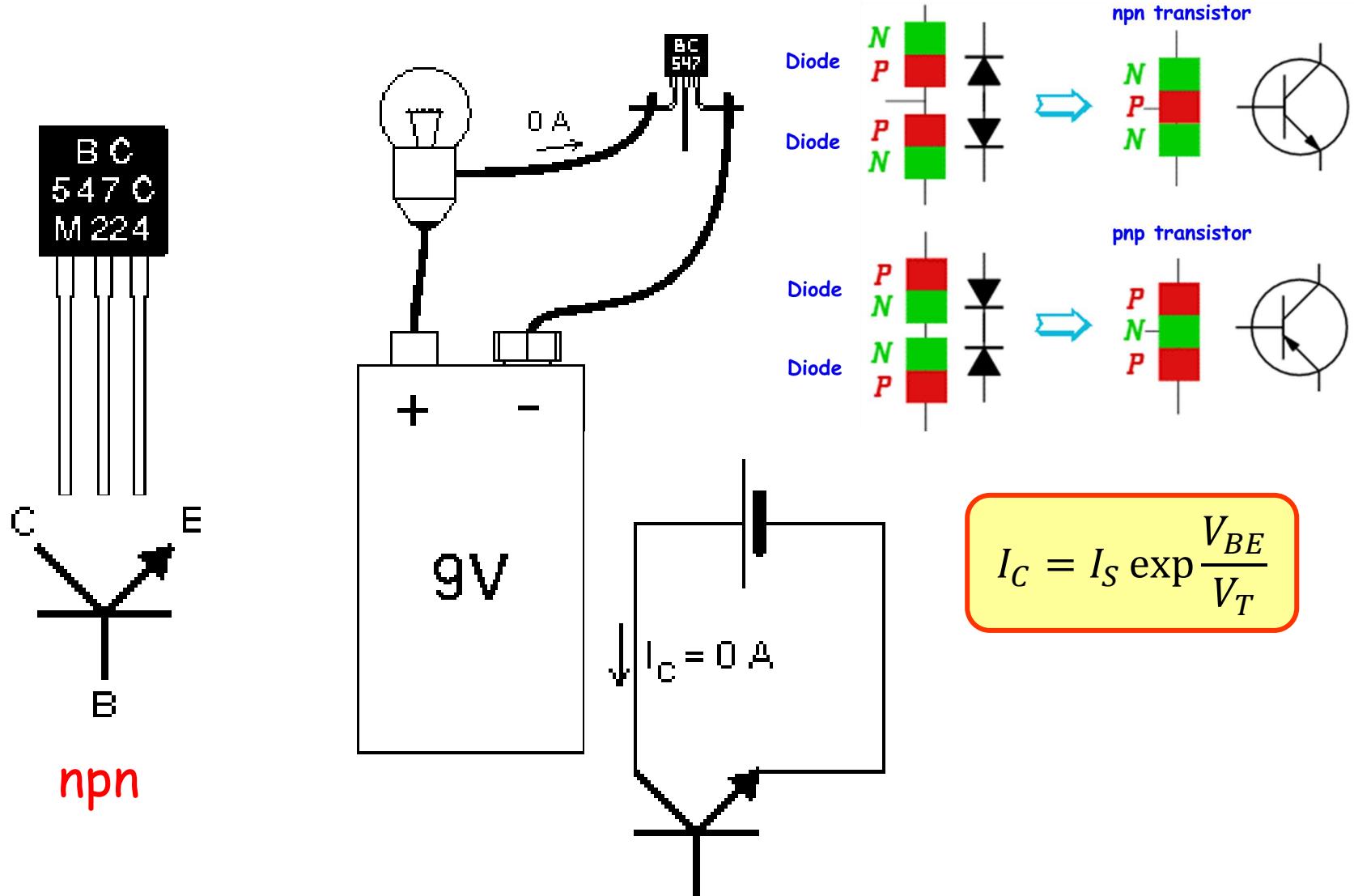
## PNP Transistor Simplified Diagram

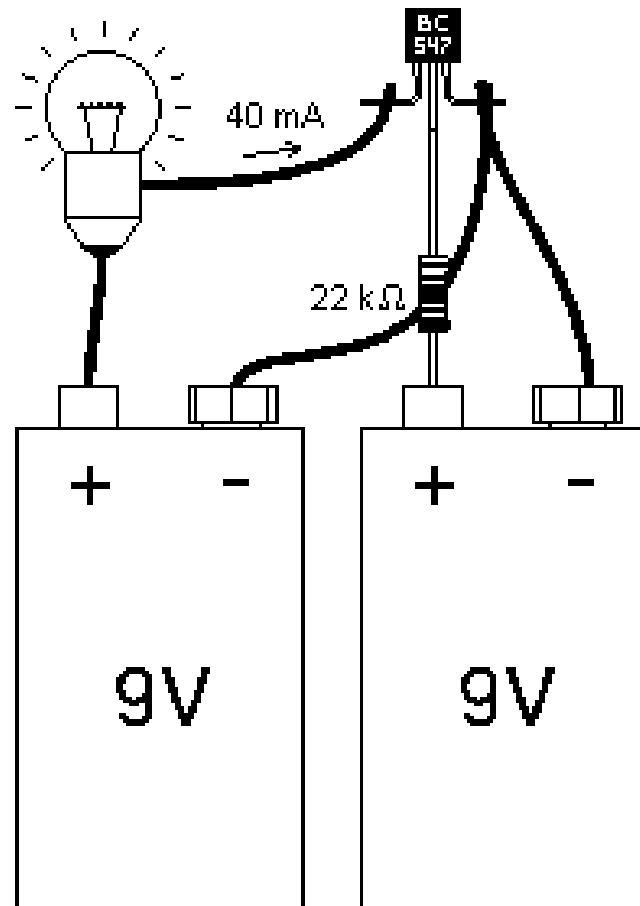
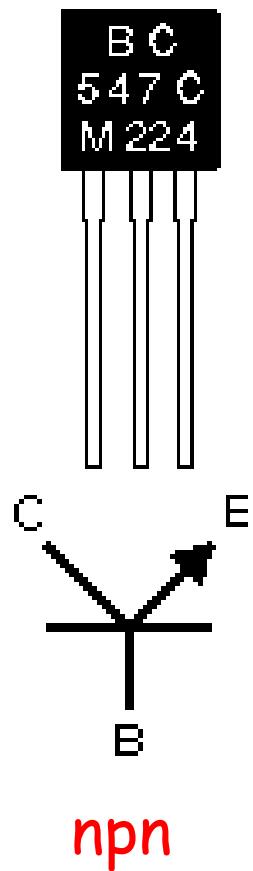


## PNP Test Procedure

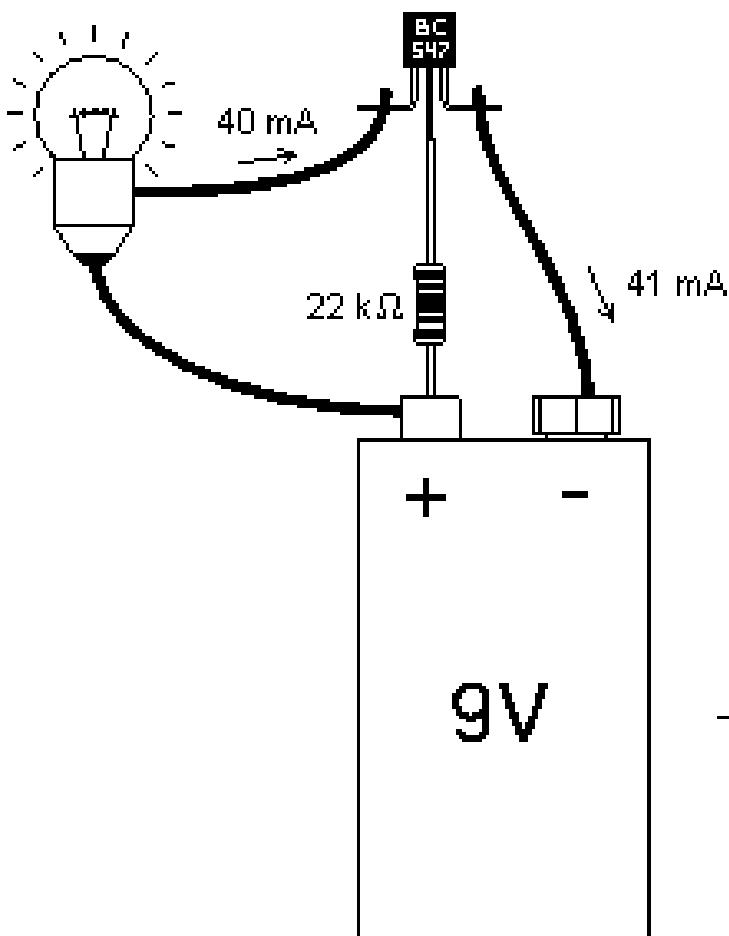
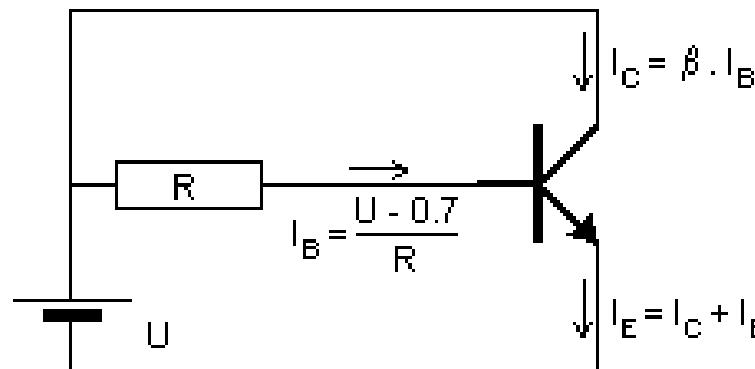
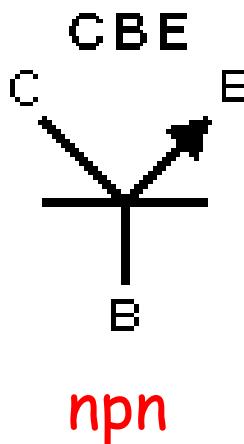
Connect the meter leads with the polarity as shown and verify that the base-to-emitter and base-to-collector junctions read as a forward biased diode: 0.5 to 0.8 VDC.

# BJTs - Practical Aspects



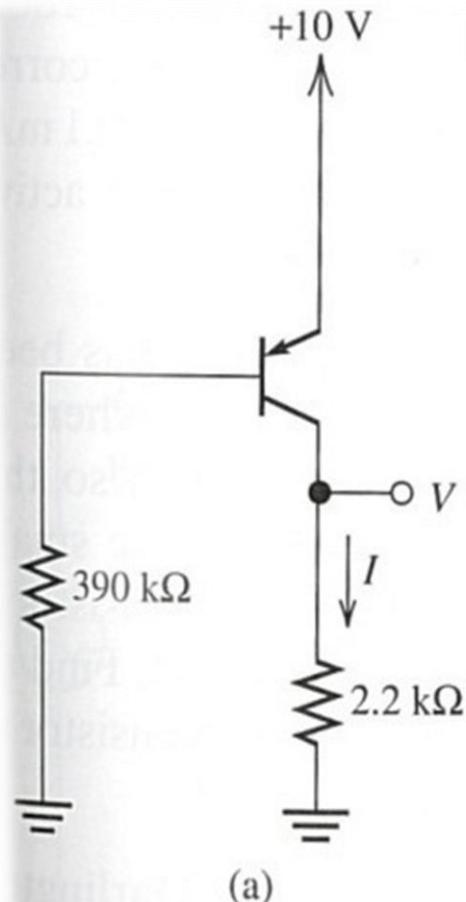


B C  
547 C  
M 224



## Problem :

Analyze the circuits shown in Figure to determine I and V. For all transistors  $\beta = 100$  and assume that  $|V_{BE}| = 0.7V$  in the active region.

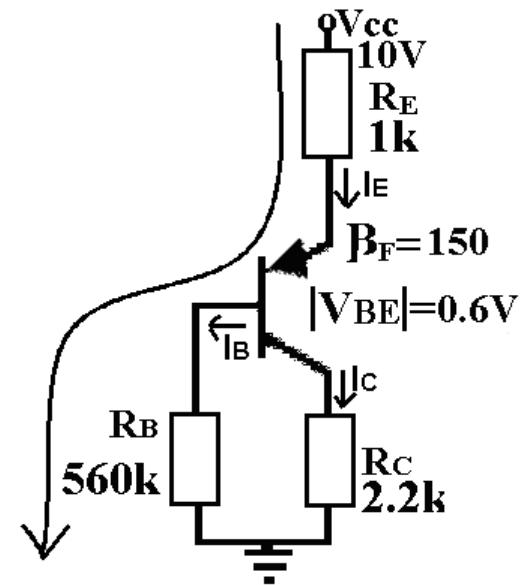
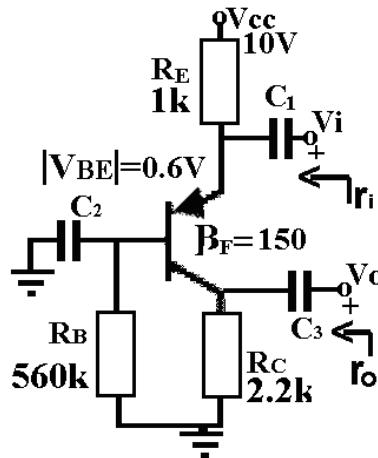


$$(a) \text{ for } \beta = 100$$

$$|V_{BE}| = 0.7 \Rightarrow V_B = 9.3V$$

$$I_B = \frac{9.3}{390k} = 23.8\mu A$$

$$I_C = \beta I_B = 2.38mA \Rightarrow V = I_C * 2.2k = 5.236 V$$



Consider the amplifier circuit shown on the left. Use the following parameters for your calculations. Transistor parameters :  $\beta=150$ ,  $|V_{BE}|=0.6V$

- a. Perform DC analysis and calculate DC operating values of the transistor.

$$V_{CC} - I_E R_E - V_{EB} - I_B R_B = 0$$

$$V_{CC} - (\beta + 1)I_B R_E - V_{EB} - I_B R_B = 0$$

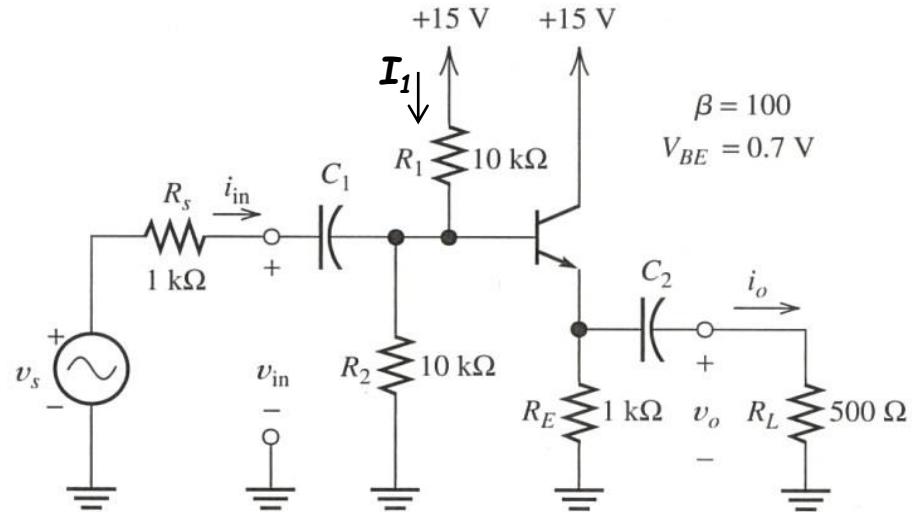
$$I_B \cong \frac{V_{CC} - V_{EB}}{\beta R_E - R_B} = \frac{10V - 0.6V}{150 * 1k - 560k} = 13.24\mu A$$

$$I_C = \beta I_B \cong 2mA$$

## Problem:

Consider the circuit below. Calculate  $I_{CQ}$  ( $\beta = 100$ ,  $V_{BE} = 0.7V$ ).

$$(I_1 = I_B + I_{R2})$$



$$15V - I_1 * 10k + (I_1 - I_B) * 10k = 0 \Rightarrow I_1 * 20k - I_B * 10k = 15 V$$

$$15 - I_1 * 10k - 0.7 = (1 + \beta) * I_B * 1k\Omega \Rightarrow I_1 * 10k + I_B * 101k = 14.3 V$$

*multiply 2nd equation by 2 and subtract the first one*

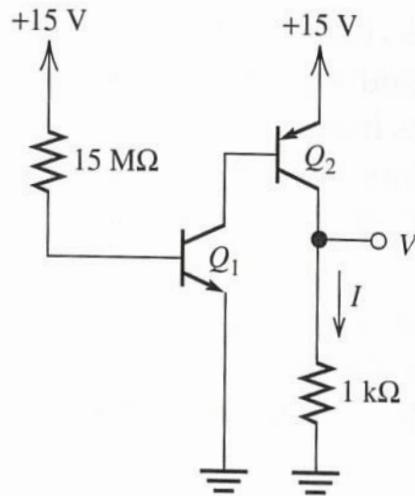
$$I_B * (202k + 10k) = 28.6 - 15$$

$$I_B = \frac{13.6}{212k} = 64.2\mu A$$

$$I_{CQ} = I_B * \beta = 6.42mA$$

## Problem :

Analyze the circuits shown in figure to determine I and V. For all transistors, assume that  $\beta = 100$  and  $|V_{BE}| = 0.7V$  in the active region.



For  $\beta = 100$

$$I_{B1} = \frac{14.3}{15M\Omega} = 0.9533\mu A$$

$$I_{C1} = \beta I_{B1} = 95.33\mu A = I_{B2}$$

$$I = I_{C2} = I_{B2} * \beta = 9.533mA$$

$$V = I * 1k = 9.533 V$$

## Problem:

Suppose that npn transistor has  $V_{BE} = 0.7V$ . Determine  $I_C$  and  $V_{CE}$  and output voltage.

Assume that Base current is small, so

$$V_B \approx V_{CC} \frac{R_2}{R_1 + R_2} = 10 \frac{10 \text{ k}\Omega}{27 \text{ k}\Omega + 10 \text{ k}\Omega} = 2.7 \text{ V}$$

Emitter voltage

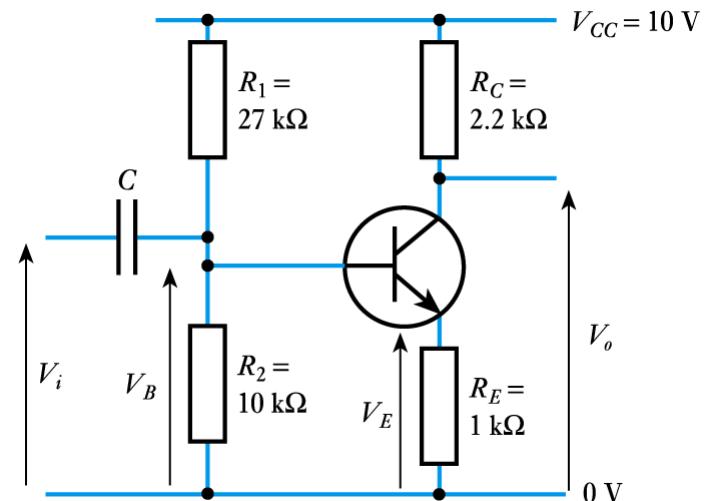
$$V_E = V_B - V_{BE} = 2.7 - 0.7 = 2.0 \text{ V}$$

Emitter current

$$I_E = \frac{V_E}{R_E} = \frac{2.0 \text{ V}}{1 \text{ k}\Omega} = 2 \text{ mA}$$

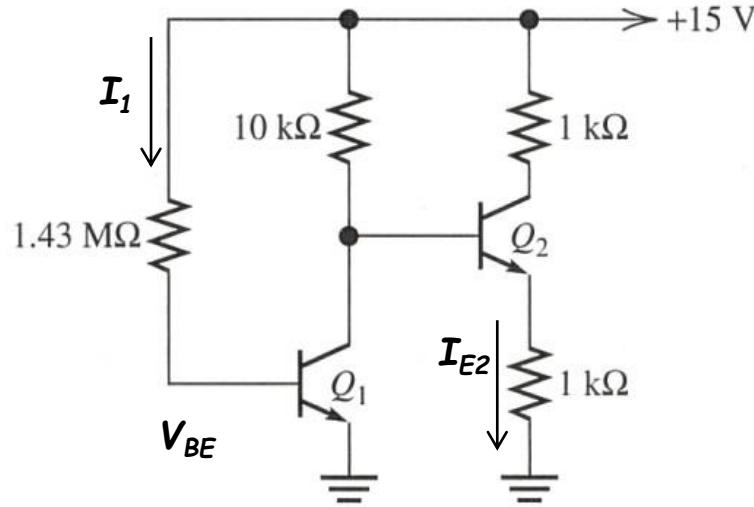
Since  $I_B$  is small, collector current  $I_C \approx I_E = 2 \text{ mA}$

Output voltage =  $V_{CC} - I_C R_C = 10 - 2 \text{ mA} \times 2.2 \text{ k}\Omega = 5.6 \text{ V}$



## Problem:

The transistors shown in figure operate in active region and have  $\beta = 100$ ,  $V_{BE} = 0.7V$ . Determine  $I_C$  and  $V_{CE}$  for each transistor.



$$I_{C1} = \beta I_{B1} = 1\text{ mA}$$

$$I_{C2} = 3.8735\text{ mA}$$

$$V_{CE2} = 7.213\text{ V}$$

$$V_{CE1} = 4.6126\text{ V}$$

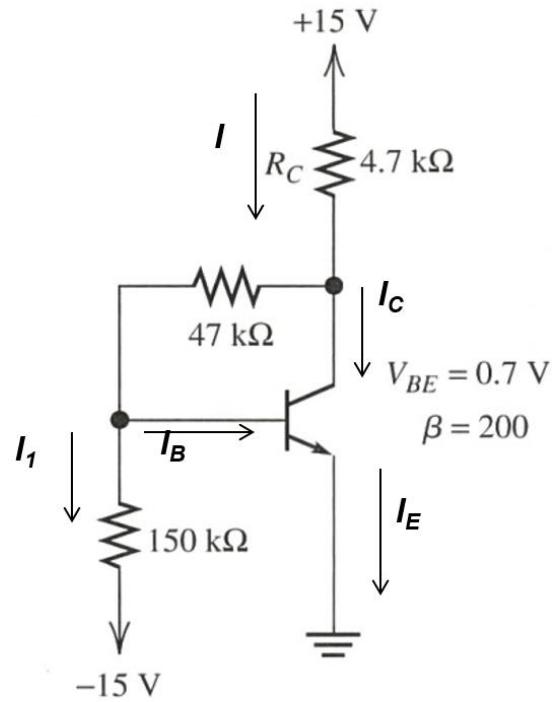
$$15V - I_{B1} 1.43M\Omega - V_{BE1} = 0 \Rightarrow I_{B1} \text{ SOLVED}$$

$$15V - (I_{C1} + I_{B2}) 10k\Omega - V_{BE2} - (\beta + 1) I_{B2} 1k\Omega = 0 \Rightarrow I_{B2} \text{ SOLVED}$$

$$15V - I_{C2} 1k\Omega - V_{CE2} - (\beta + 1) I_{B2} 1k\Omega = 0 \Rightarrow V_{CE2} \text{ SOLVED}$$

## Problem:

Analyze the circuit of figure and determine  $I_C$  and  $V_{CE}$ . ( $\beta = 100$ ,  $V_{BE} = 0.7V$ )



$$V_B = 0.7V$$

$$V_B - I_1 150k\Omega = -15V \Rightarrow I_1 \text{ SOLVED}$$

$$15V - (I_B + \beta I_B + I_1) 4.7k\Omega - (I_B + I_1) 47k\Omega = V_B \\ \Rightarrow I_B \text{ SOLVED}$$

$$15V - (I_B + \beta I_B + I_1) 4.7k\Omega - V_{CE} = 0 \\ \Rightarrow V_{CE} \text{ SOLVED}$$

$$I_1 = 0.1047mA$$

$$I_E = (\beta + 1)I_B$$

$$I_B = 9.0\mu A$$

$$I_C = 1.8mA$$

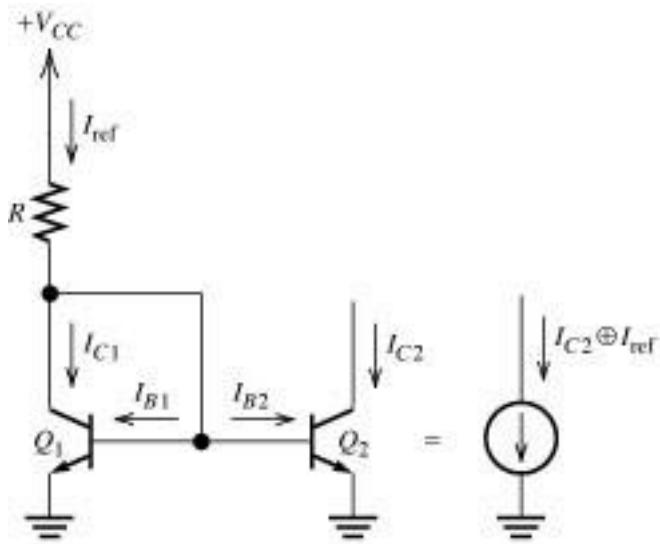
$$V_{CE} = 6.04V$$

An **ideal current source** supplies **constant current** to a circuit despite any other conditions present in the circuit.

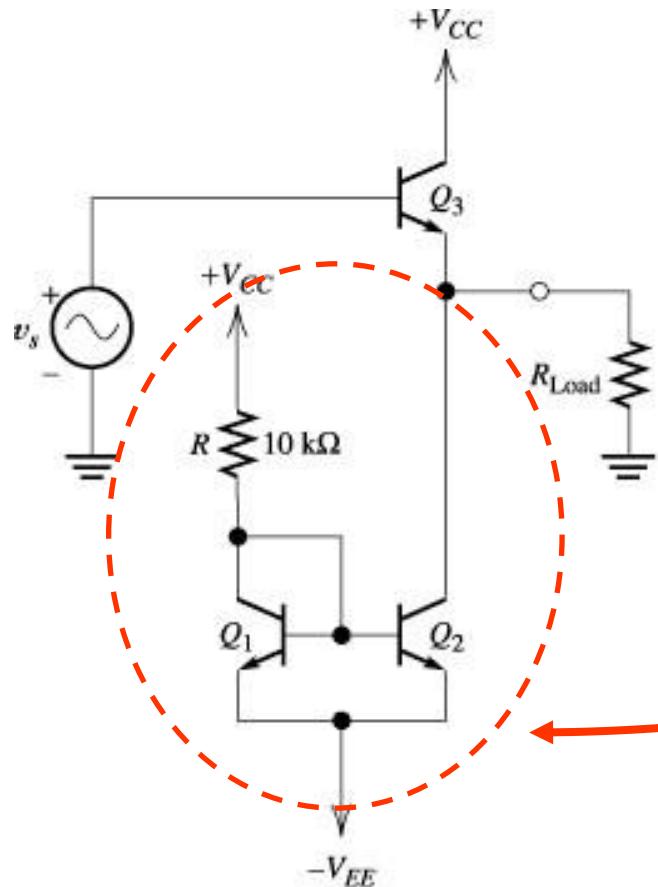
Thus, if an ideal current source is a 12mA current source, the load will receive the entire 12mA, without any being lost.

## Current Mirror (current source circuit)

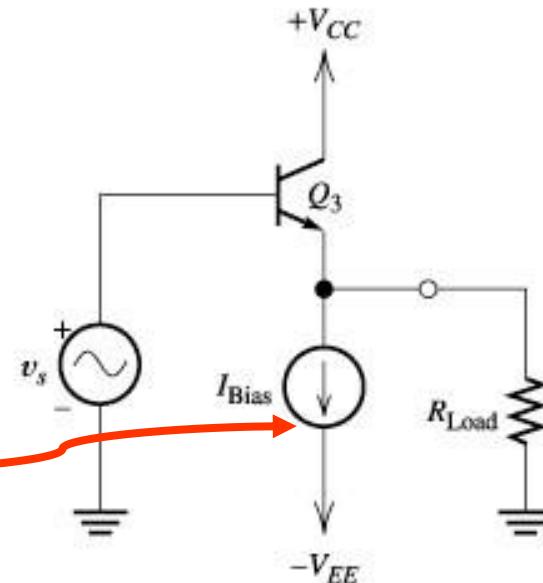
A **current mirror** is a current source circuit. Output current ( $I_{C2}$ ) is a copy of reference current ( $I_{REF}$ ) regardless of loading.



# Current Mirror



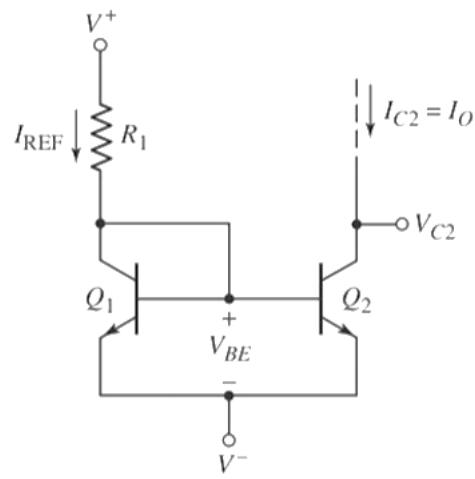
(a) Detailed diagram



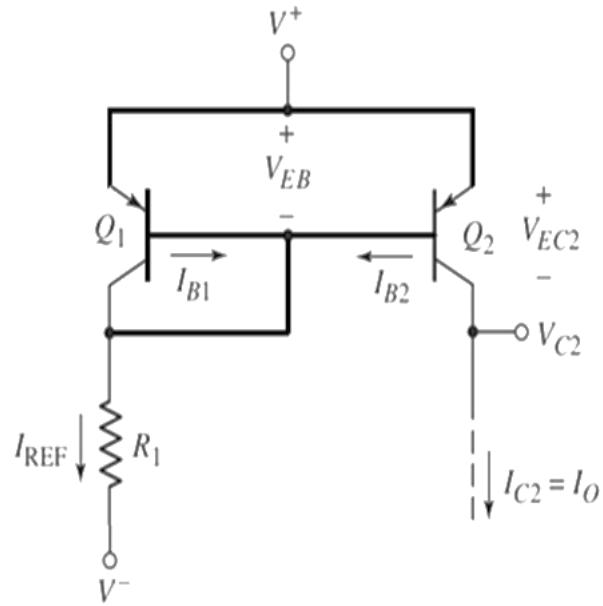
(b) Simplified diagram

# Current Mirror (current source circuit)

A current mirror is a current source circuit. Output current ( $I_o$ ) is a copy of reference current ( $I_{REF}$ ) regardless of loading.

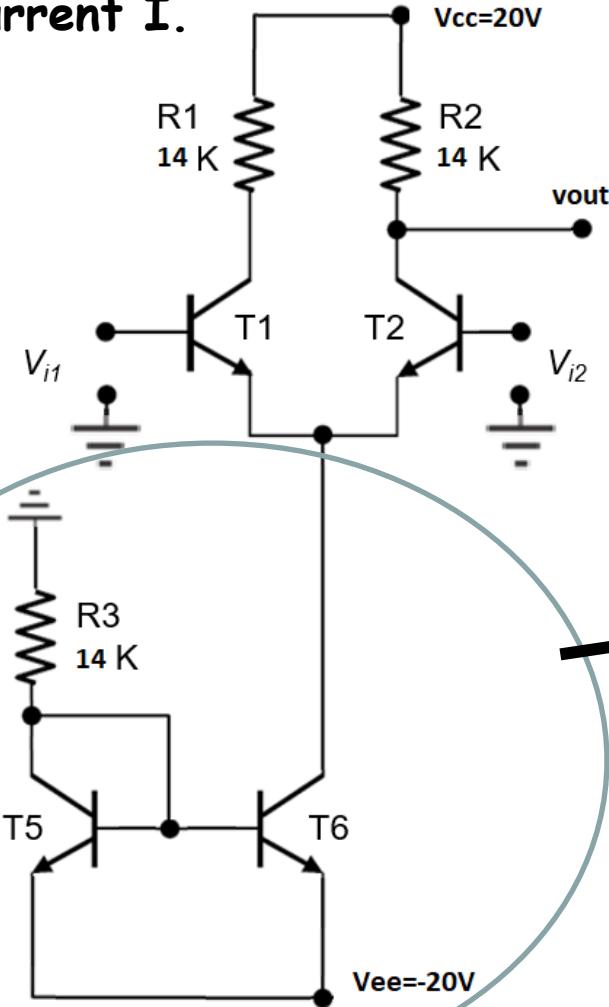


(a) Using npn transistors

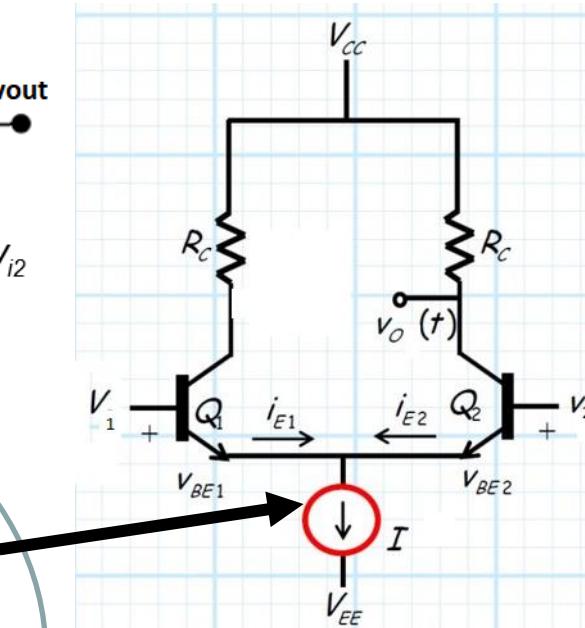


(b) Using pnp transistors

For the transistors shown below  $\beta = h_{fe} = h_{FE} = 100$ ,  $V_{BE} = 0.7V$ . Calculate current I.



$$I_C = I_S \exp \frac{V_{BE}}{V_T}$$



$$0 - I_{R3} R_3 - V_{BE} = V_{ee}$$

$$0 - I_{R3} 14k - 0.7V = -20V$$

$$I_{R3} = (20 - 0.7) / 14k = 1.37mA$$

$$V_{BE5} = V_{BE6} \Rightarrow I_{C5} = I_{C6} = I_C$$

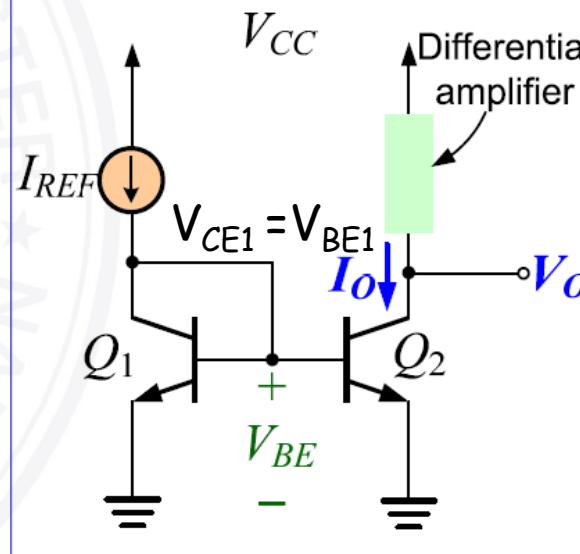
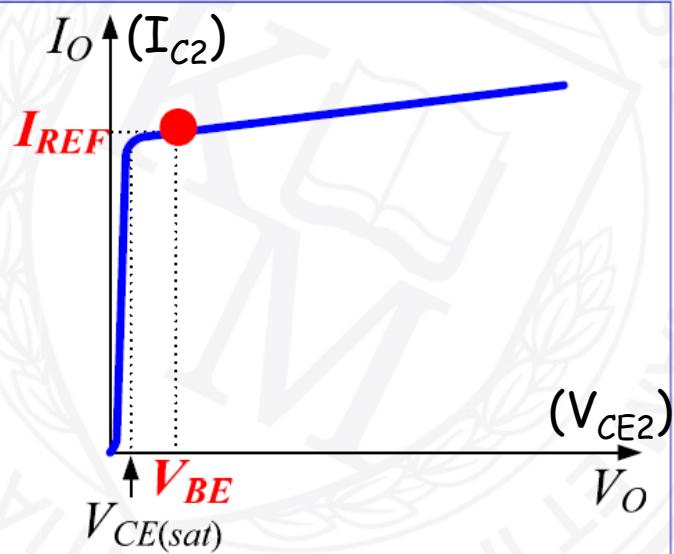
$$I_{R3} = I_C + 2 I_B = \beta I_B + 2 I_B = 102 I_B$$

$$I = I_C = 1.34mA$$

# Current Mirror Equations considering Early Effect

$$I_{REF} \cong I_{C1} = I_s e^{V_{BE}/V_T} \left( 1 + \frac{V_{BE}}{V_A} \right)$$

$$I_O = I_{C2} = I_s e^{V_{BE}/V_T} \left( 1 + \frac{V_O}{V_A} \right)$$

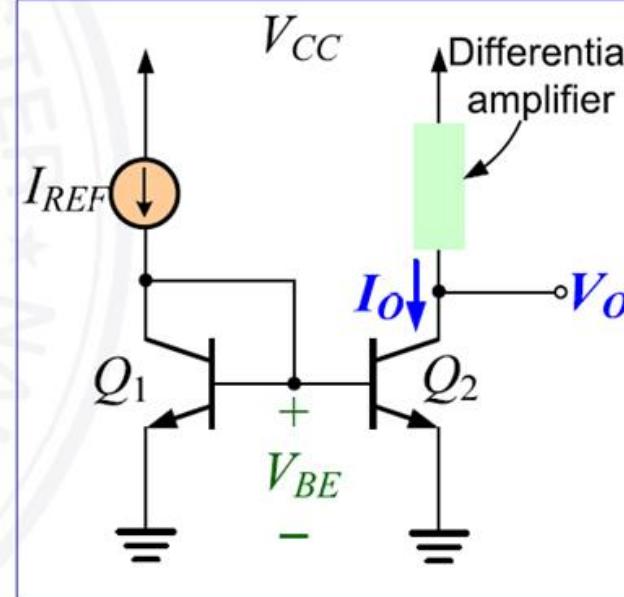
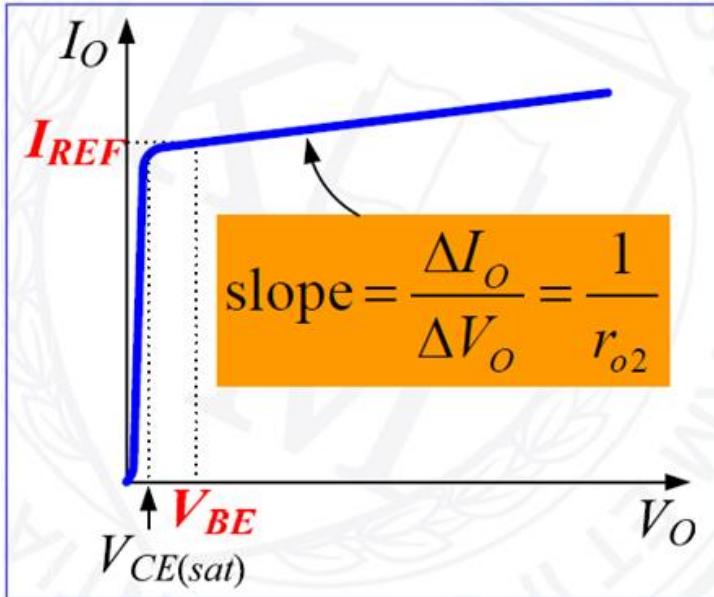


$$V_{CE1} = V_{BE}$$

$$V_{CE2} = V_O$$

Early effect will result in different  $I_C$ 's for the two transistors unless  $V_O = V_{BE}$ .

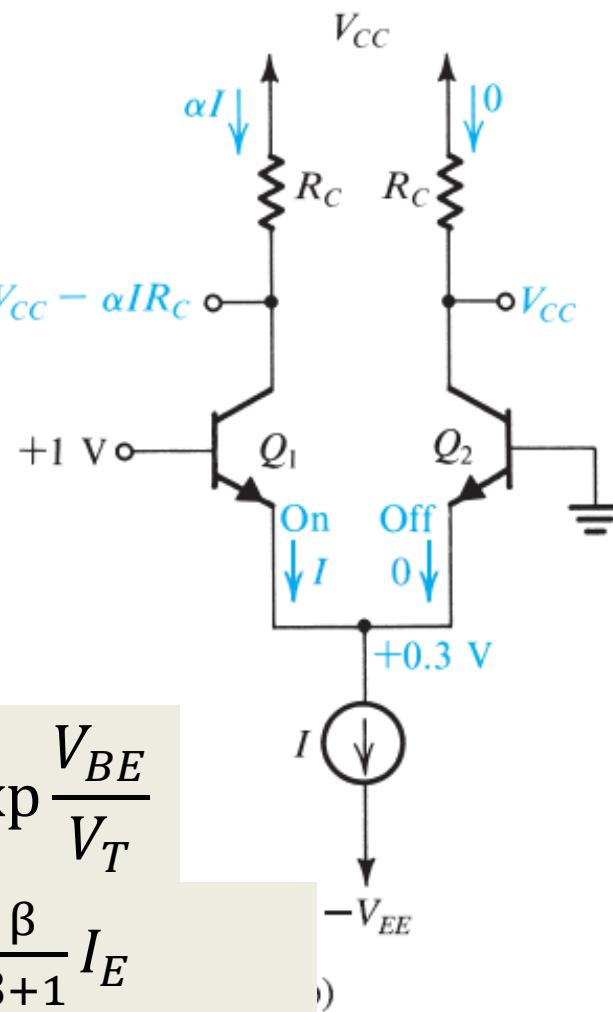
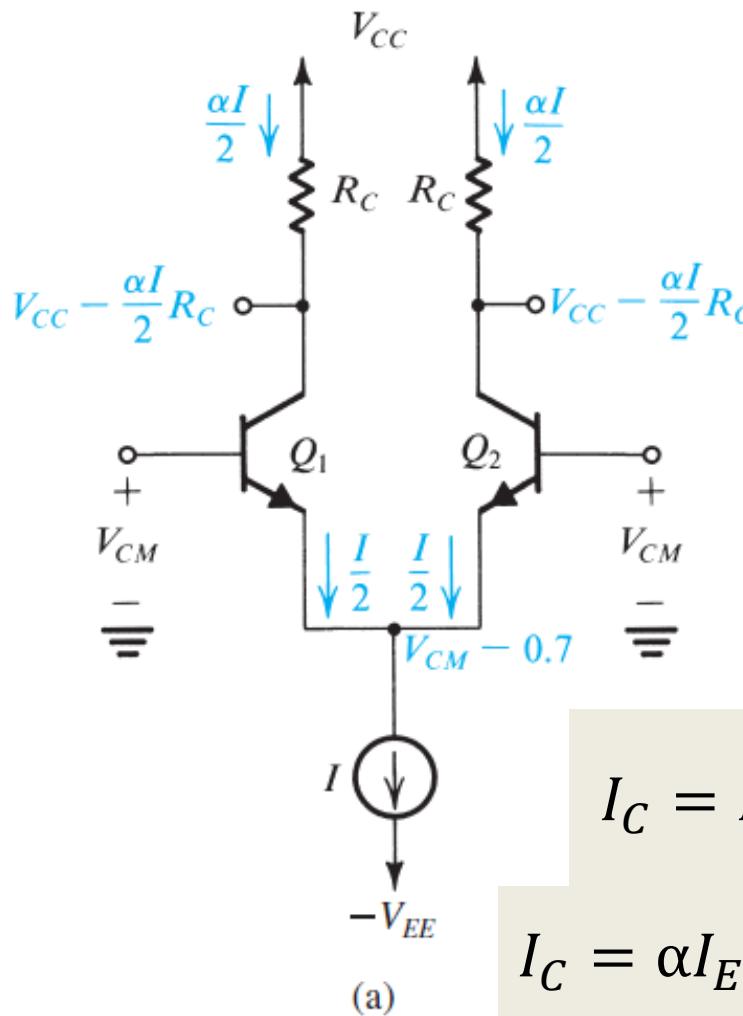
# Finite output resistance



$r_{o2}$ : internal resistance of current source (current mirror)

# Differential Amplifiers

For the transistors  $V_{BE} = 0.7V$

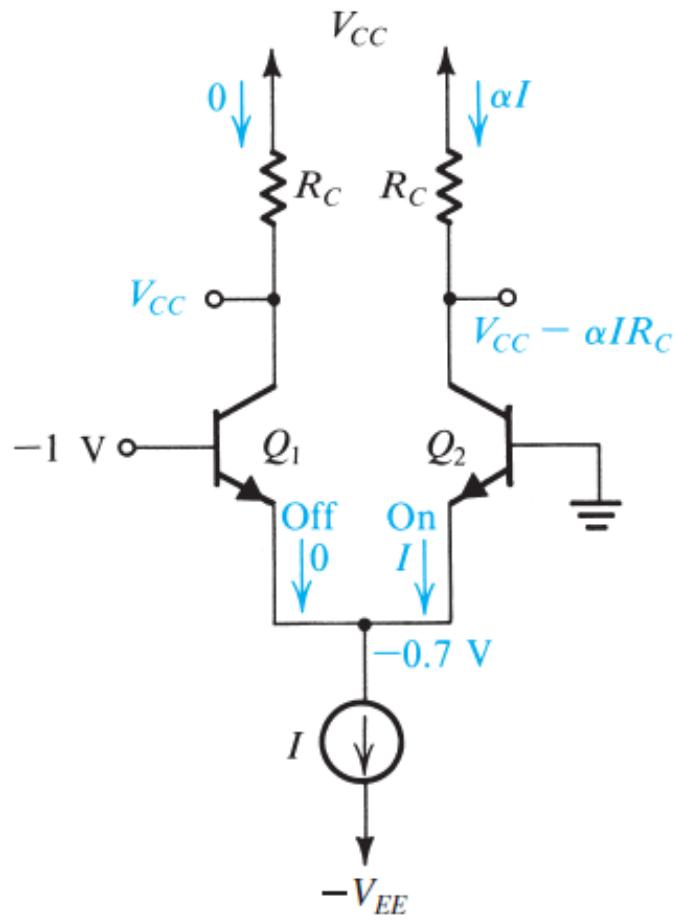


$$V_{BE\ Q1} = V_{BE\ Q2} \Rightarrow I_{CQ1} = I_{CQ2} = I/2$$

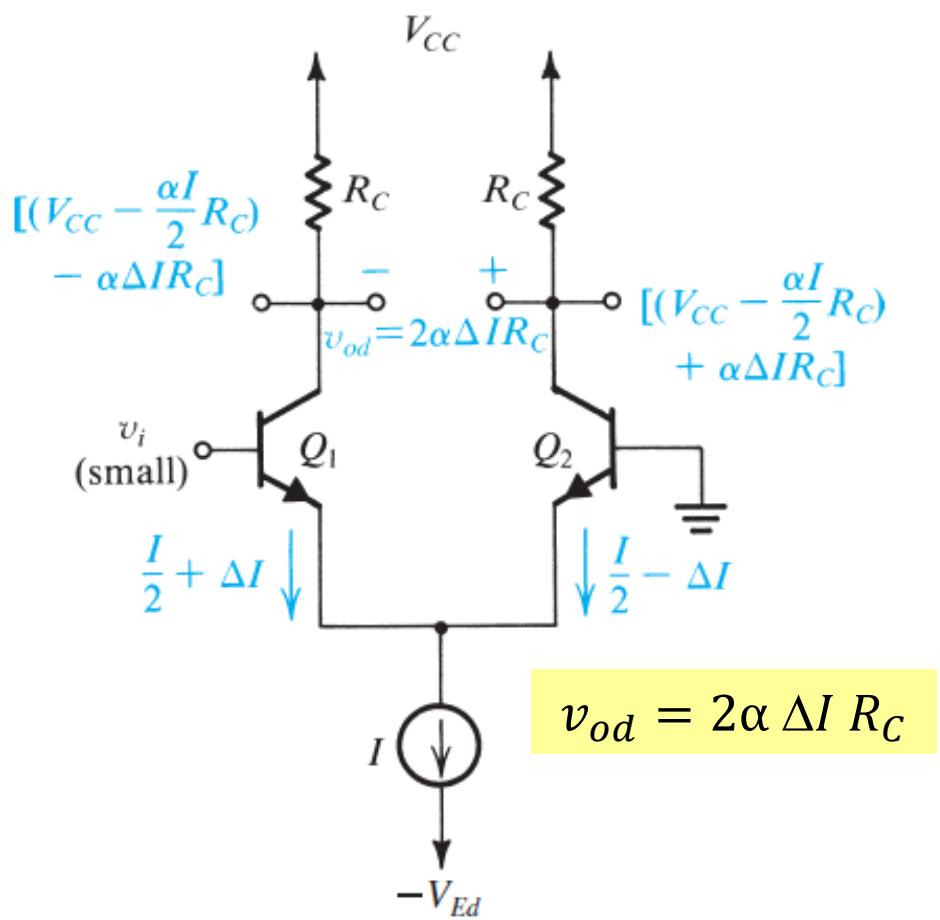
Transistors are exactly same.

# Differential Amplifiers

$$I_C = \alpha I_E$$

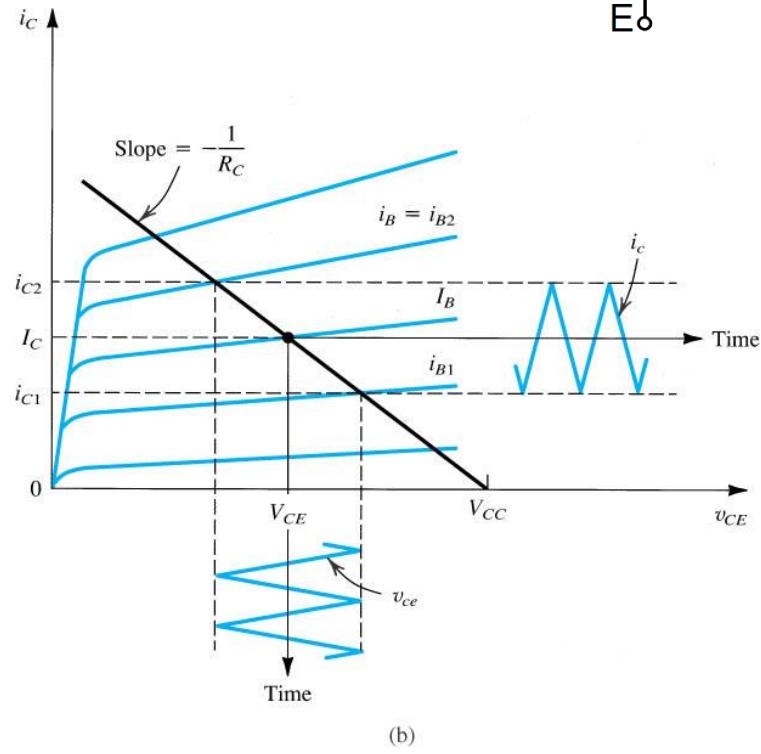
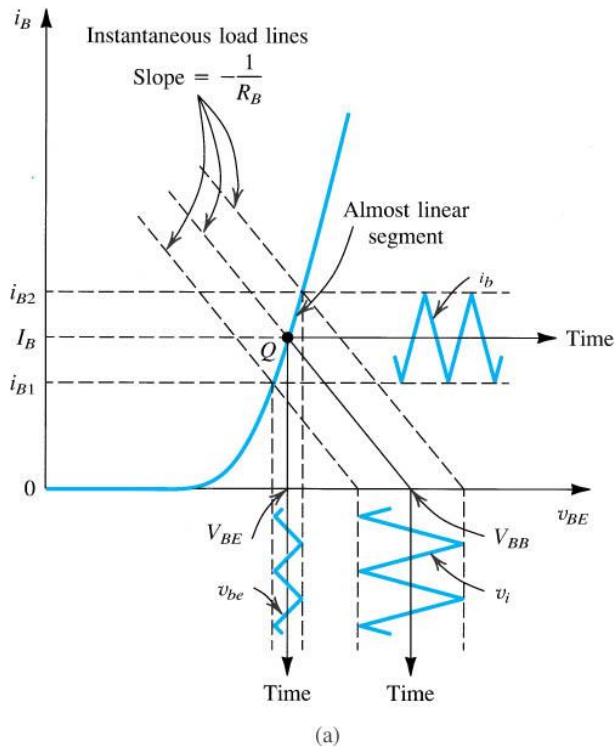
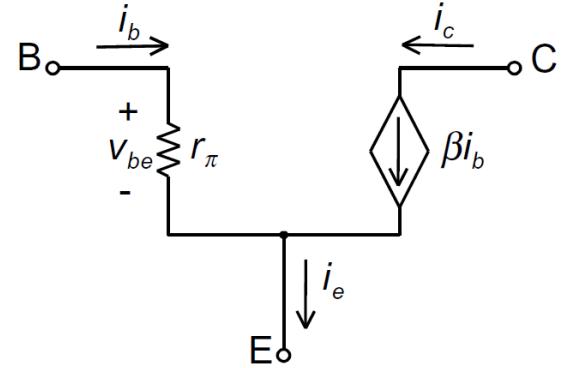


(c)



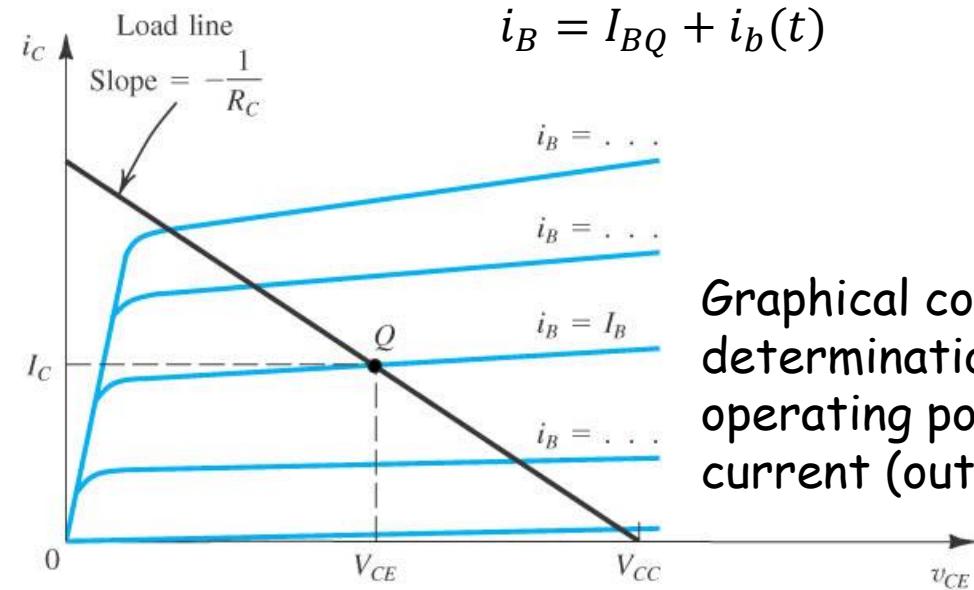
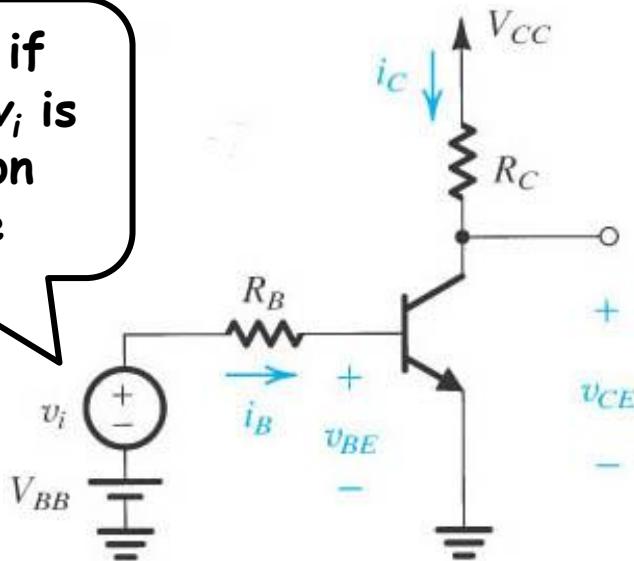
(d)

# BJT (Small Signal Analyses)

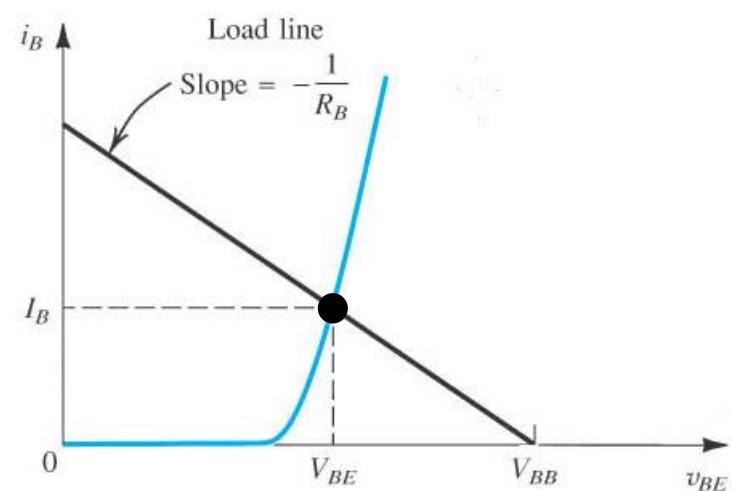


# Small-Signal Analysis

What happens if a small signal  $v_i$  is superimposed on the DC voltage



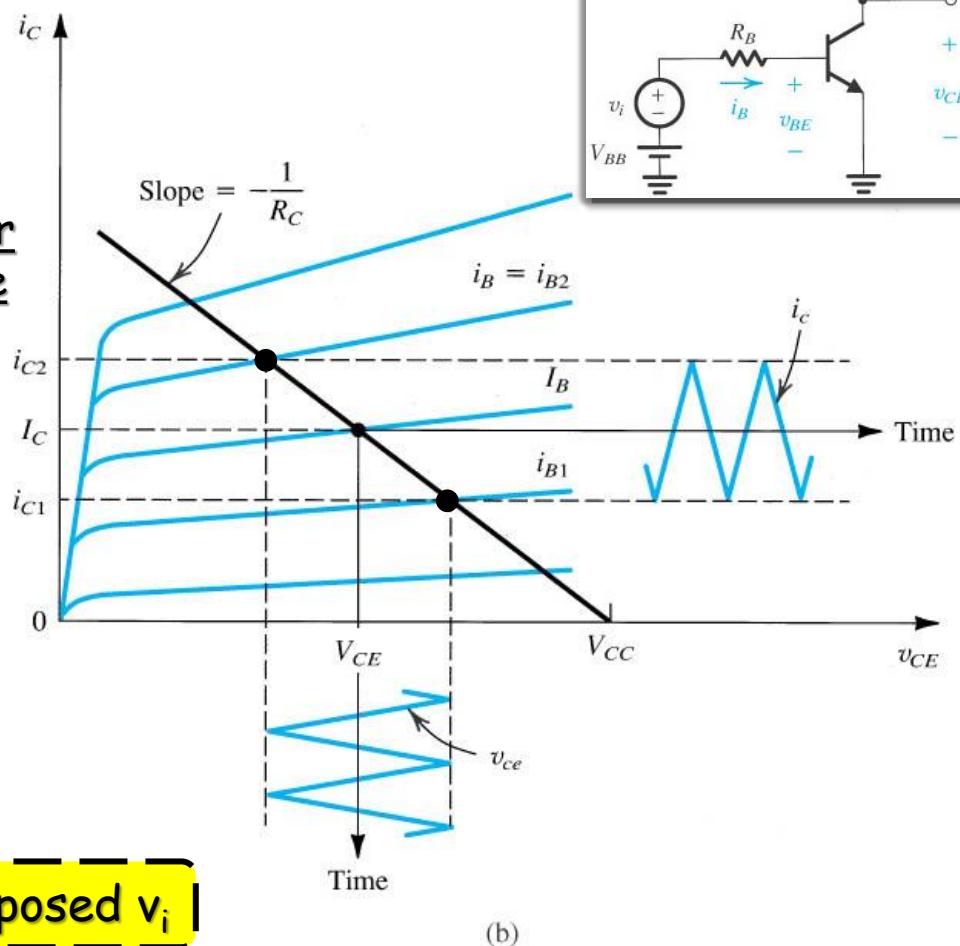
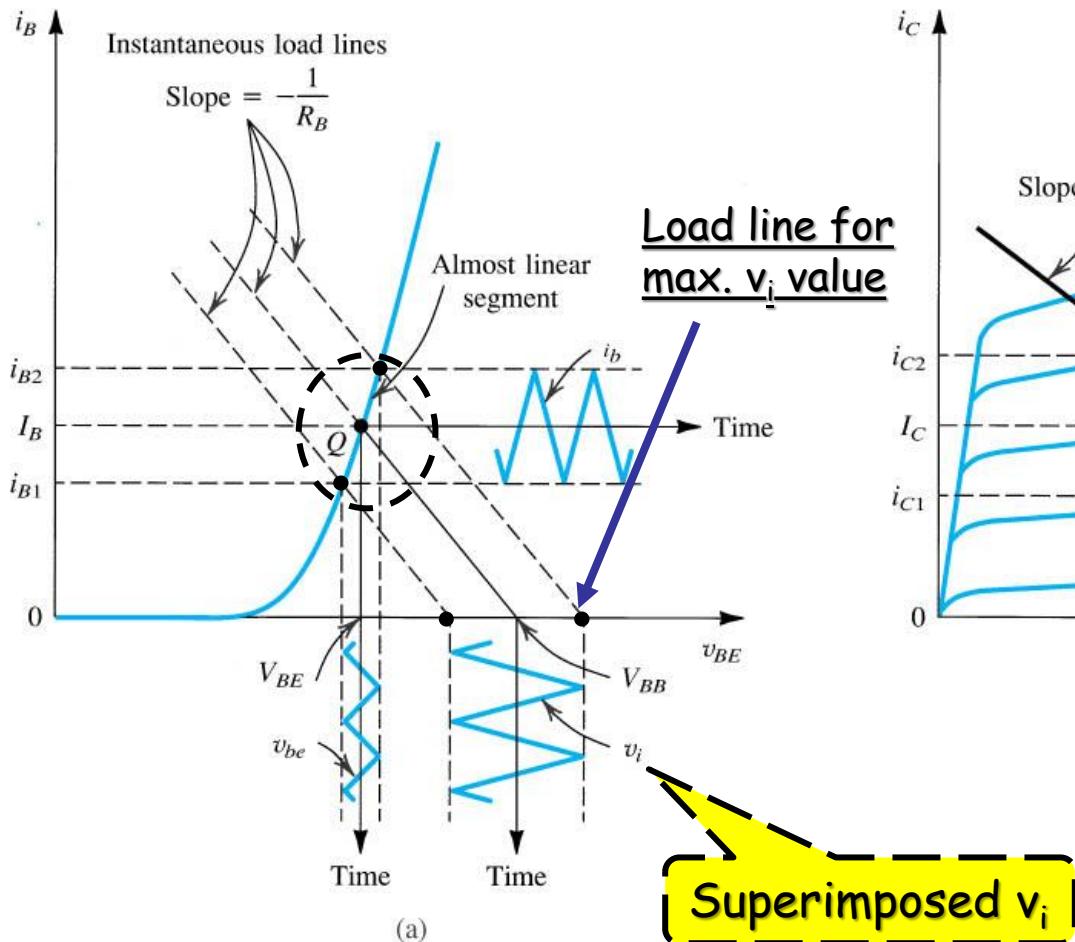
Graphical construction for the determination of the operating point collector current (output)



Graphical construction for the determination of the base operating point current (input)

# Small-Signal Analysis

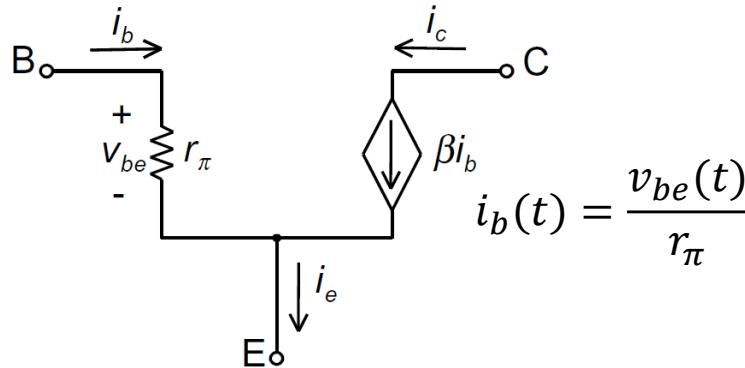
$$V_{BB} + v_i(t) - R_B i_B = v_{BE}$$



Graphical determination of the signal components  $v_{be}$ ,  $i_b$ ,  $i_c$ , and  $v_{ce}$  when a signal component  $v_i$  is superimposed on the dc voltage  $V_{BB}$

# Small-Signal Equivalent Circuit (hybrid- $\pi$ small-signal model)

Small signal equivalent circuit  
for npn BJT:



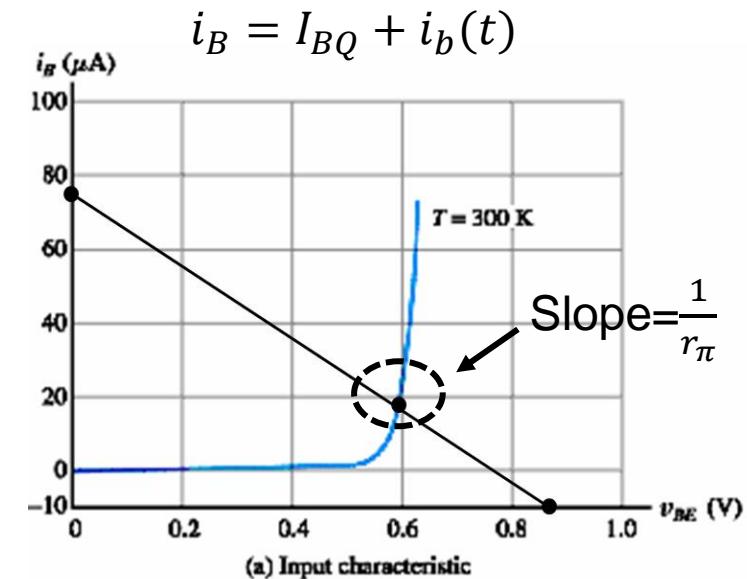
Transistor is modeled by using  
input resistance and output current

$$i_{EQ} = I_{ES} \left[ \exp\left(\frac{v_{BEQ}}{V_T}\right) - 1 \right]$$

$$i_{BQ} = I_{ES} \left[ \exp\left(\frac{v_{BEQ}}{V_T}\right) - 1 \right] / (\beta + 1)$$

$$\left[ \frac{di_B(t)}{dv_{BE}(t)} \right]_Q = \frac{i_{BQ}}{V_T} \quad \Rightarrow \quad r_\pi = \left[ \frac{di_B(t)}{dv_{BE}(t)} \right]_Q^{-1} = \frac{V_T}{i_{BQ}}$$

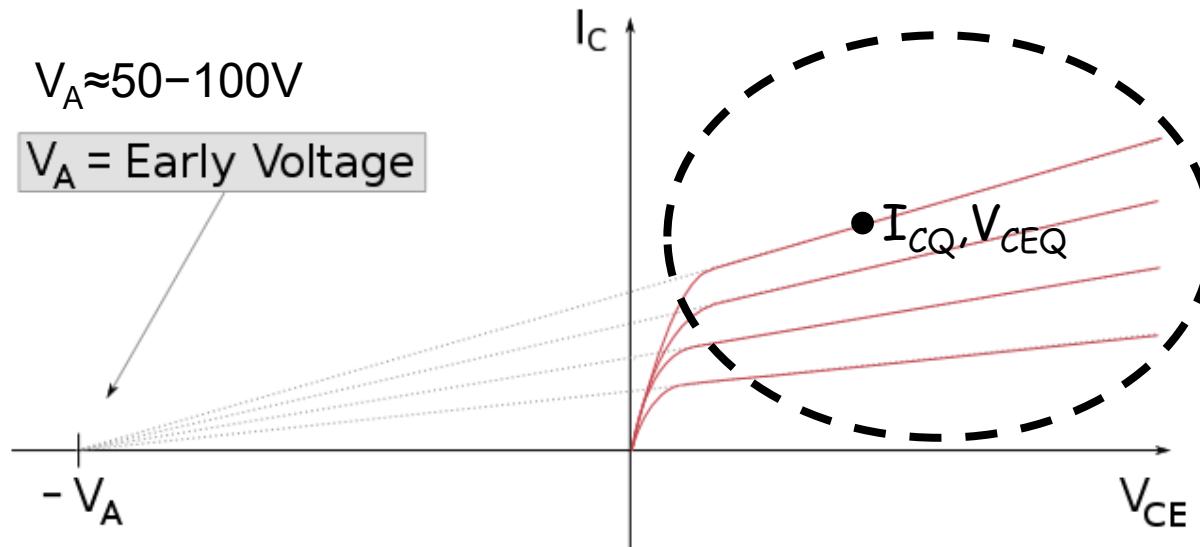
Assumption: Early  
Voltage ( $V_A$ ) is infinite.



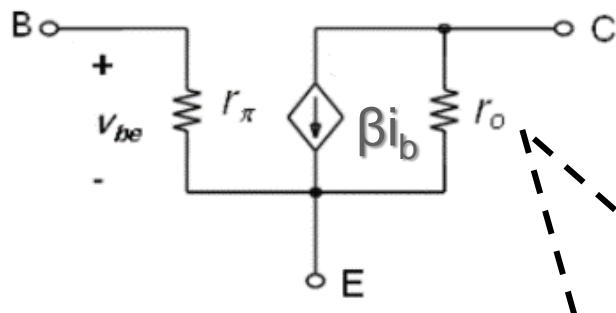
# Early Effect

$V_A \approx 50-100V$

$V_A = \text{Early Voltage}$



Small signal equivalent circuit



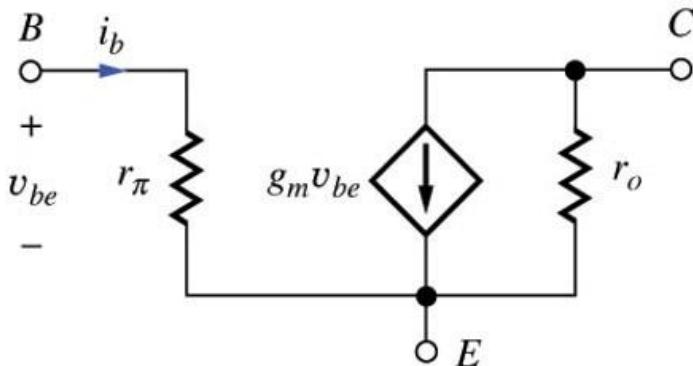
This behaviour is modeled by a resistor.

$$I_{CQ} = \left( I_S \exp \left( \frac{V_{BE}}{V_T} \right) \right) \left( 1 + \frac{V_{CEQ}}{V_A} \right)$$

$$\left( \frac{\partial I_C}{\partial V_{CE}} \right)_Q = \frac{I_{CQ}}{V_A}$$

$$\text{output resistance: } r_0 \equiv \left( \frac{\partial I_C}{\partial V_{CE}} \right)_Q^{-1} \equiv \frac{V_A}{I_{CQ}}$$

# The two versions of the hybrid- $\pi$ small-signal model



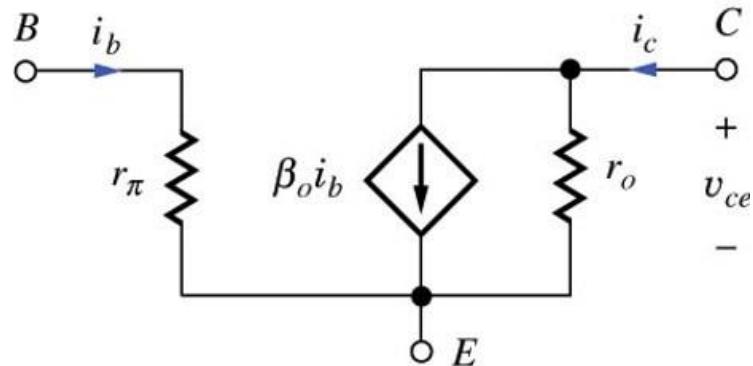
$$v_{be} = r_\pi i_b$$

$$i_c = g_m v_{be} + \frac{1}{r_o} v_{ce}$$

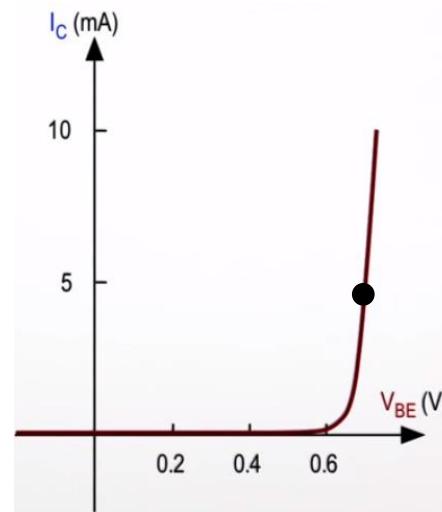
$$g_m = \frac{d}{dV_{BE}} \left( I_S \exp \left( \frac{V_{BE}}{V_T} \right) \right)_Q$$

$$g_m = \frac{1}{V_T} I_S \exp \left( \frac{V_{BE}}{V_T} \right)$$

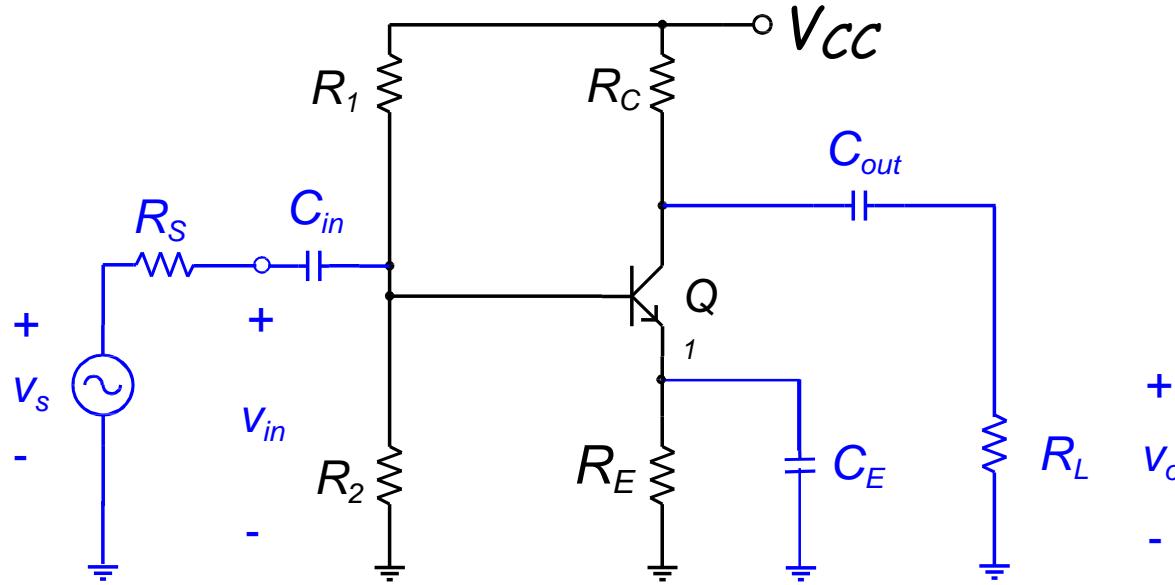
$$g_m = \frac{I_{CQ}}{V_T}$$



$$r_\pi = \frac{V_T}{I_{BQ}} \quad g_m = \frac{I_{CQ}}{V_T} = \frac{I_{CQ}}{I_{BQ} r_\pi} = \frac{\beta}{r_\pi} \quad r_0 \approx \frac{V_A}{I_{CQ}}$$

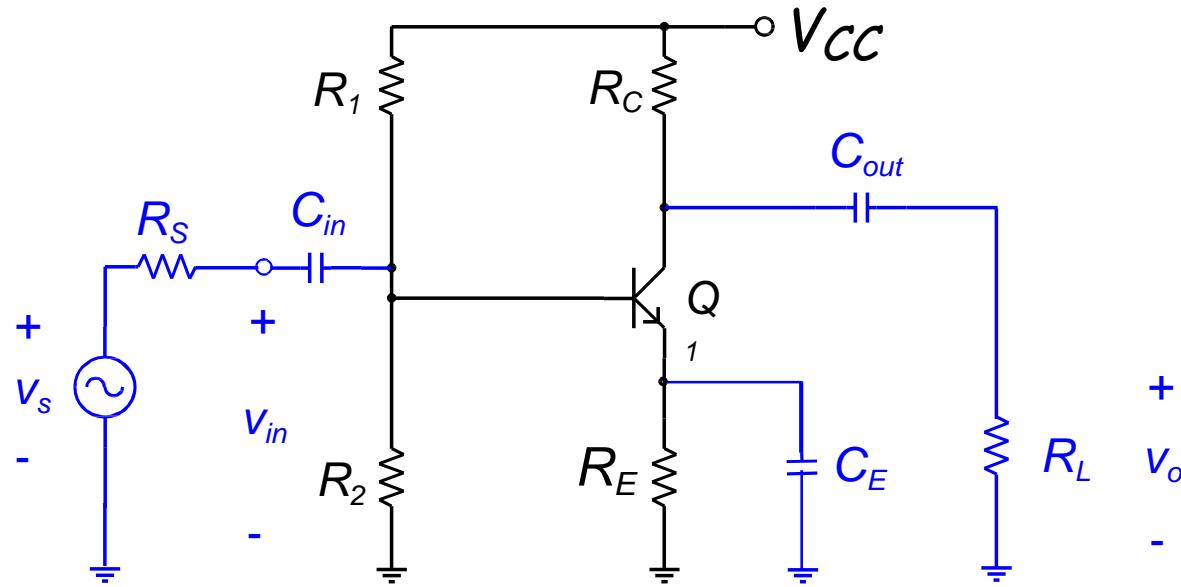


# DC ANALYSIS



1. Replace all capacitors with OPEN circuits.
2. Set all AC sources to zero, because they have zero signal component!!!

# Constructing the Small-Signal Equivalent Circuit

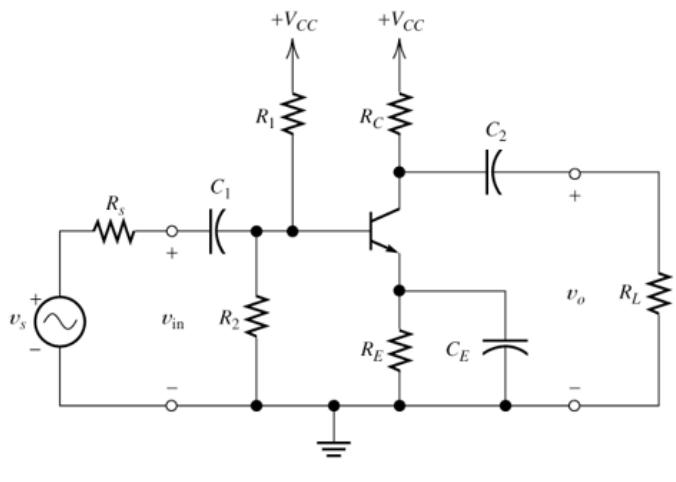


To construct small-signal equivalent circuit for entire amplifier, we:

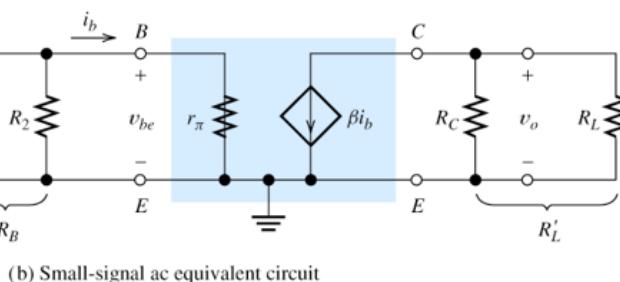
1. Replace the BJT by its small-signal model.
2. Replace all capacitors with short circuits.
3. Set all DC sources to zero, because they have zero signal component!!!

The result is the small-signal equivalent circuit of the amplifier:

# Small-Signal Analysis



(a) Actual circuit



(b) Small-signal ac equivalent circuit

The result is the small-signal equivalent circuit of the amplifier.

First perform DC analysis to find small-signal equivalent parameters at the **operating point**.

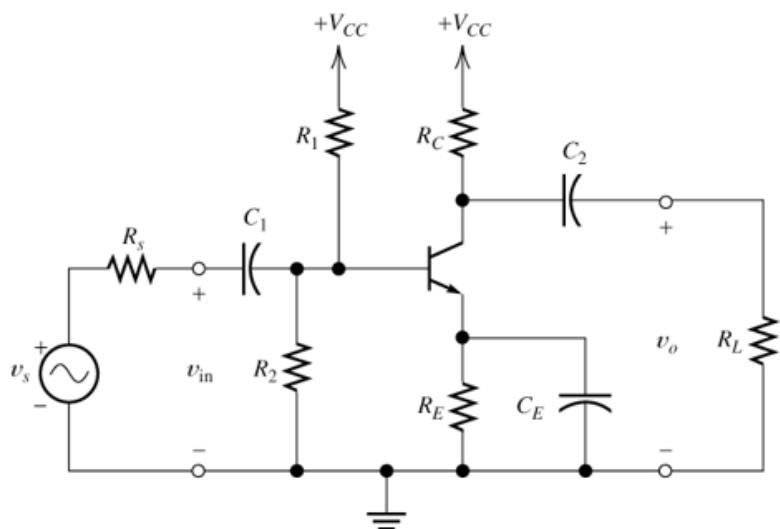
Then:

To construct small-signal equivalent circuit for entire amplifier, we:

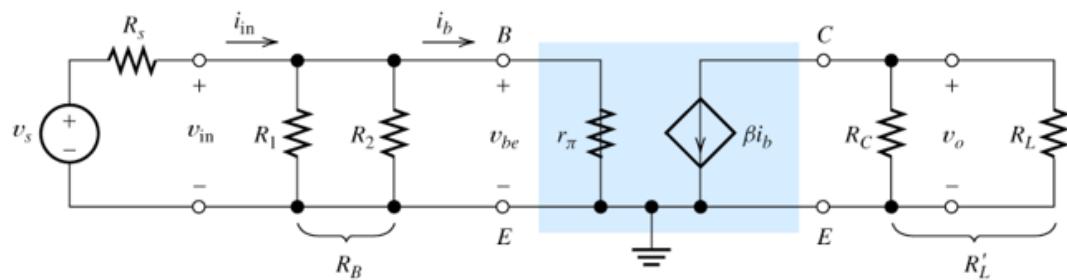
1. Replace the BJT by its small-signal model.
2. Replace all capacitors with short circuits.
3. Set all DC sources to zero, because they have zero signal component!!!

Assume that:  
 $V_A = \infty$

# Small-Signal Analysis



(a) Actual circuit



(b) Small-signal ac equivalent circuit

Find voltage gain:

$$v_{in} = v_{be} = r_\pi i_b$$

$$v_o = -R' L \beta i_b$$

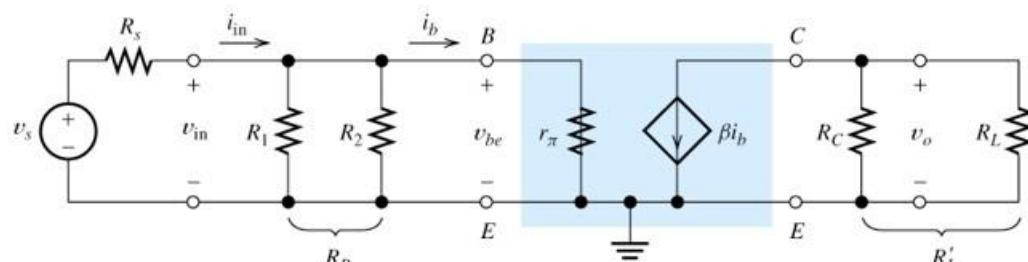
$$A_v = \frac{v_o}{v_{in}} = -\frac{R' L \beta}{r_\pi}$$

$$A_{voc} = \frac{v_o}{v_{in}} = -\frac{R_C \beta}{r_\pi}$$

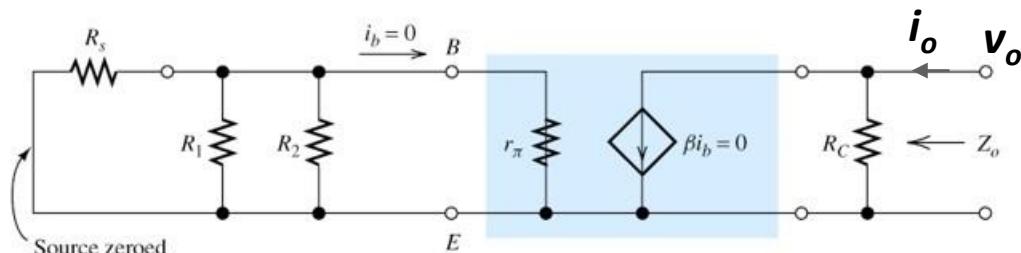
$A_{voc}$ : Open circuit gain.  
 Gain without 'Load'

Assume that:  
 $V_A = \infty$

# Small-Signal Analysis



(b) Small-signal ac equivalent circuit



(c) Equivalent circuit used to find  $Z_o$

Find input impedance:

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{1}{\frac{1}{R_B} + \frac{1}{r_\pi}}$$

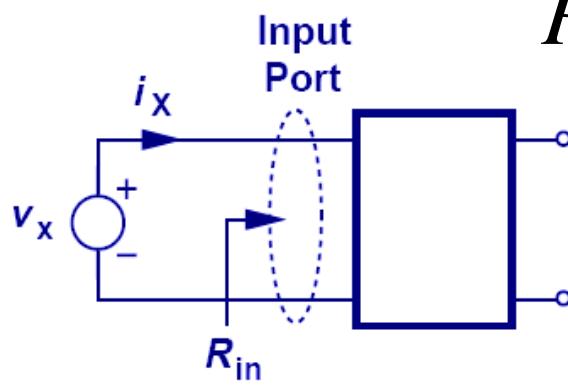
Find output impedance:

$$Z_o = v_o / i_o = R_c$$

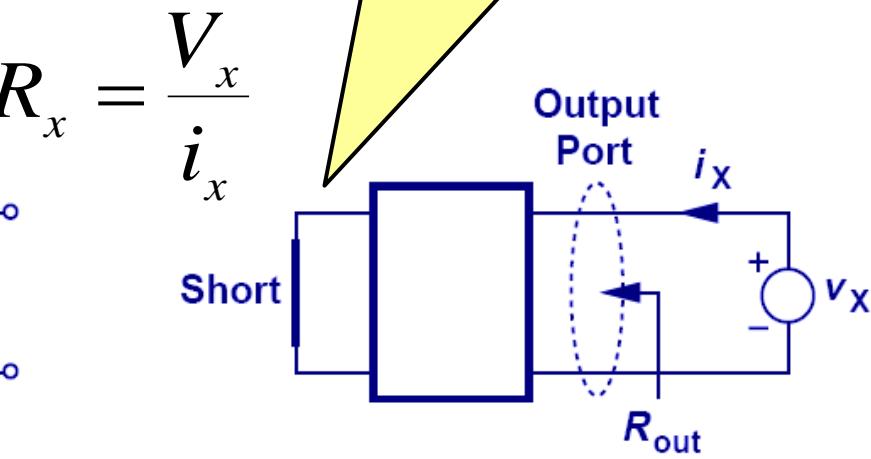
Assume that:  
 $V_A = \infty$

# Input/Output Impedances

When measuring **output impedance**, the input port has to be grounded.



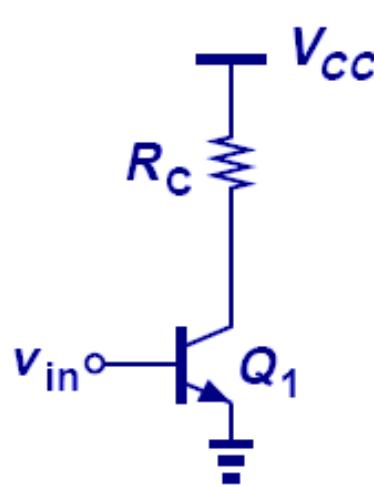
(a)



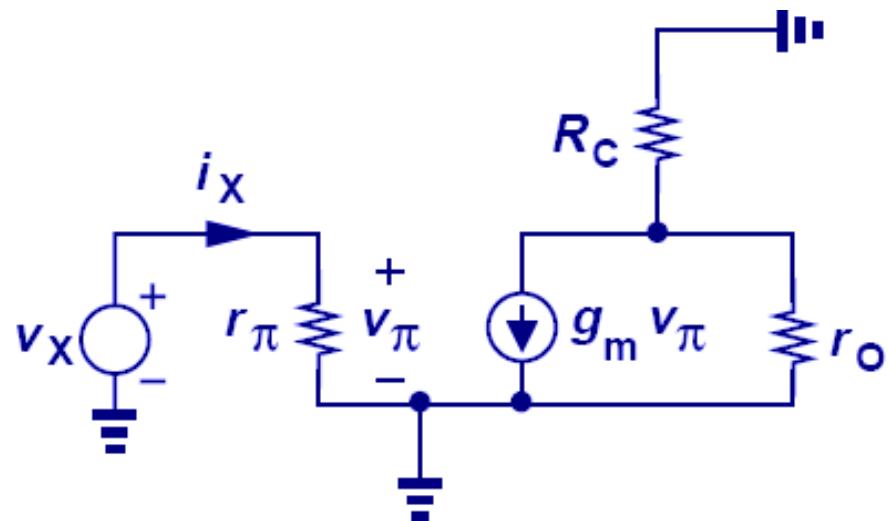
(b)

- The figure above shows the techniques of measuring input and output impedances.

# Input Impedance Example I



(a)

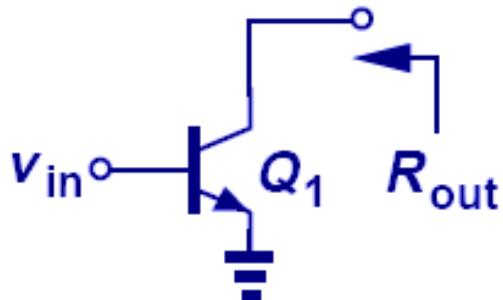


(b)

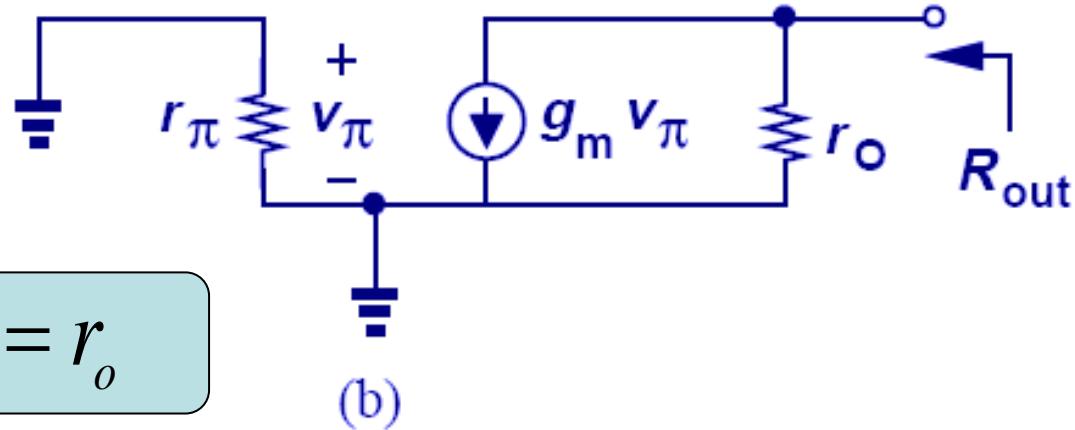
$$\frac{v_x}{i_x} = r_\pi$$

When calculating input/output impedance, small-signal analysis is assumed.

# Output Impedance Example I

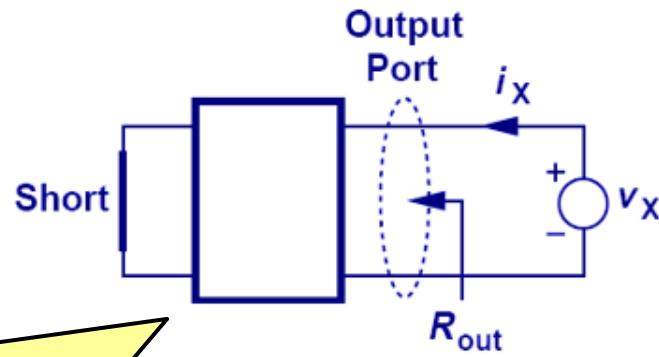


(a)



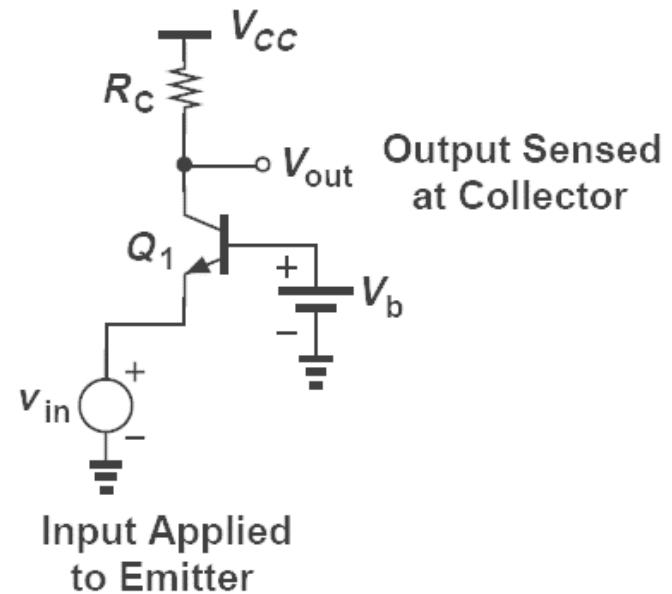
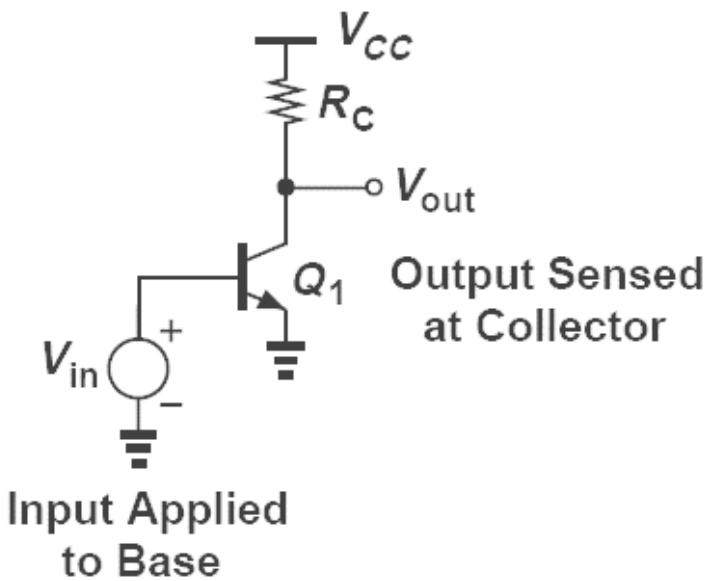
(b)

$$R_{out} = r_o$$

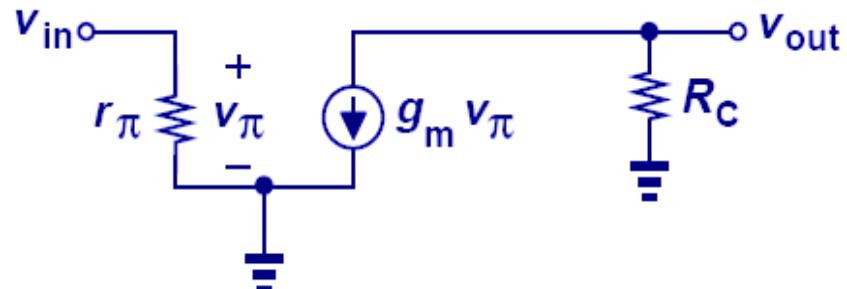
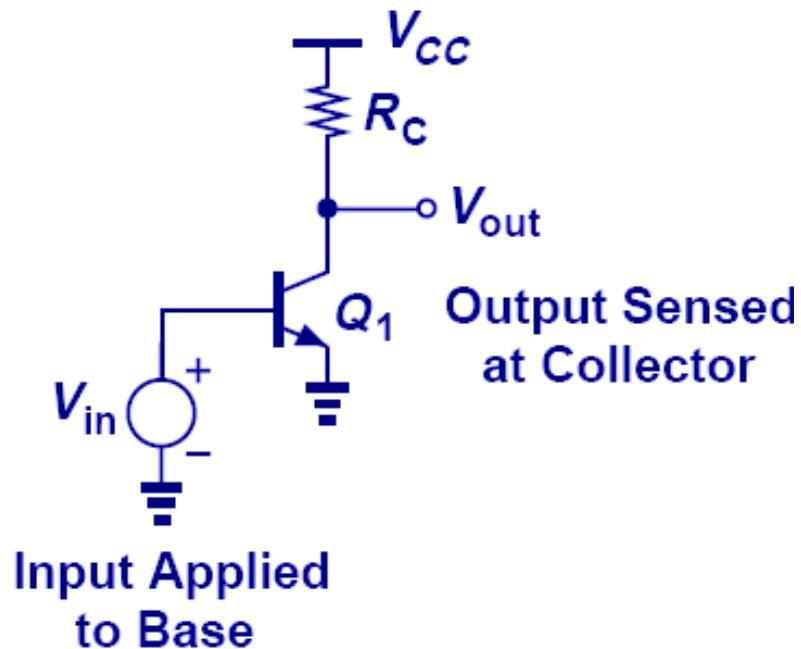


When measuring **output impedance**, the input port has to be grounded.

# Amplifier Circuits



# Common-Emitter (CE) Amplifier



$$v_{out} = -R_c g_m v_\pi$$

$$v_{in} = v_\pi$$

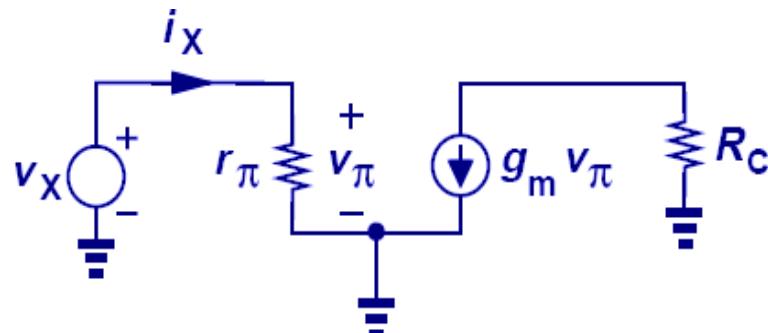
$$A_v = \frac{v_{out}}{v_{in}}$$

$$A_v = -g_m R_c$$

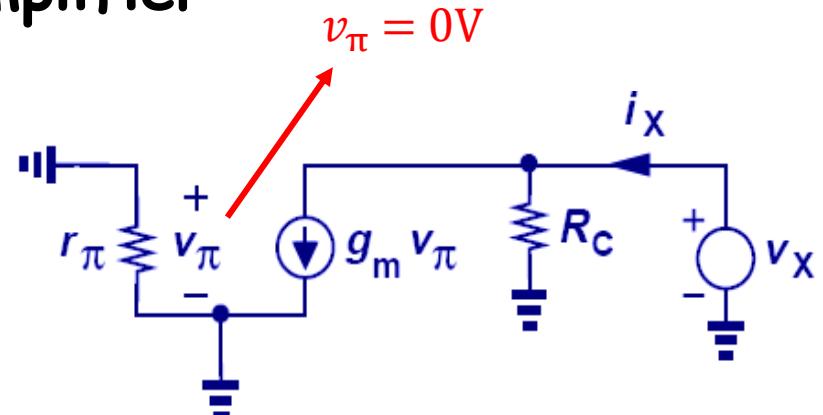
Assume that:  $V_A = \infty$

$$r_0 \approx \frac{V_A}{I_{CQ}}$$

# I/O Impedances of CE Amplifier



(a)



(b)

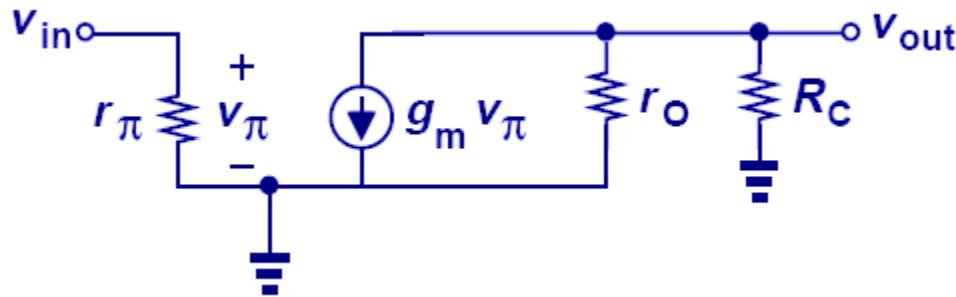
$$R_{in} = \frac{v_x}{i_x} = r_\pi$$

$$R_{out} = \frac{v_x}{i_x} = R_c$$

- When measuring output impedance, the input port has to be grounded so that  $V_{in} = 0$ .

Assume that:  
 $V_A = \infty$

# Inclusion of Early Effect



$$A_v = -g_m (R_C \parallel r_o)$$

$$R_{out} = R_C \parallel r_o$$

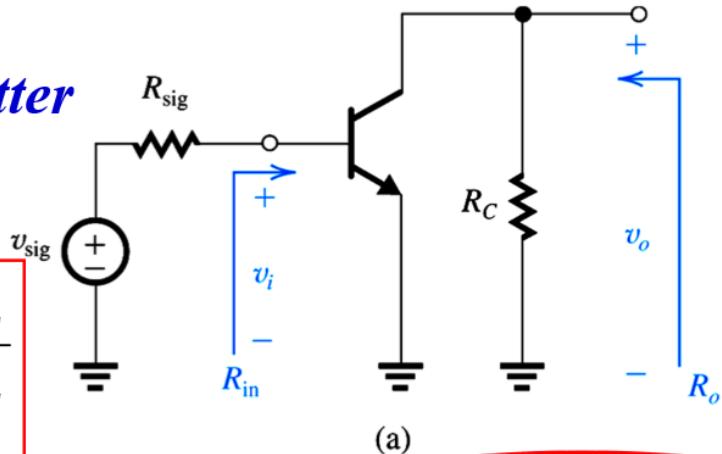
Early effect will lower the gain of the CE amplifier, as it appears in parallel with  $R_C$ .

# Summary

## The Common-Emitter (CE) Amplifier

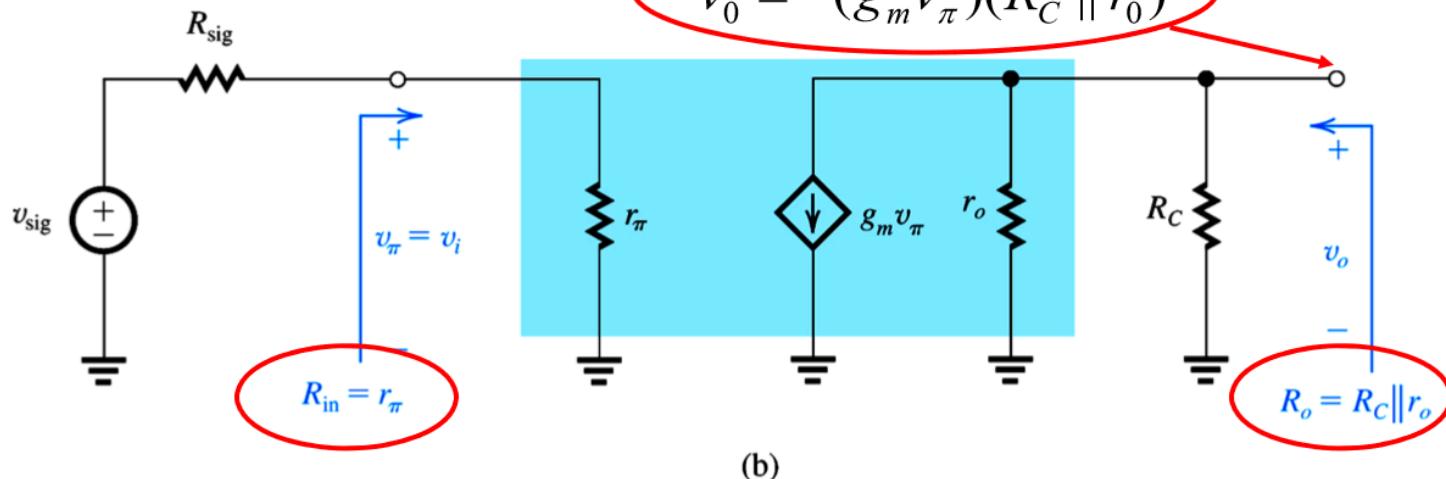
$$r_\pi = \frac{\beta}{g_m}$$

$$r_o = |V_A| / I_C$$

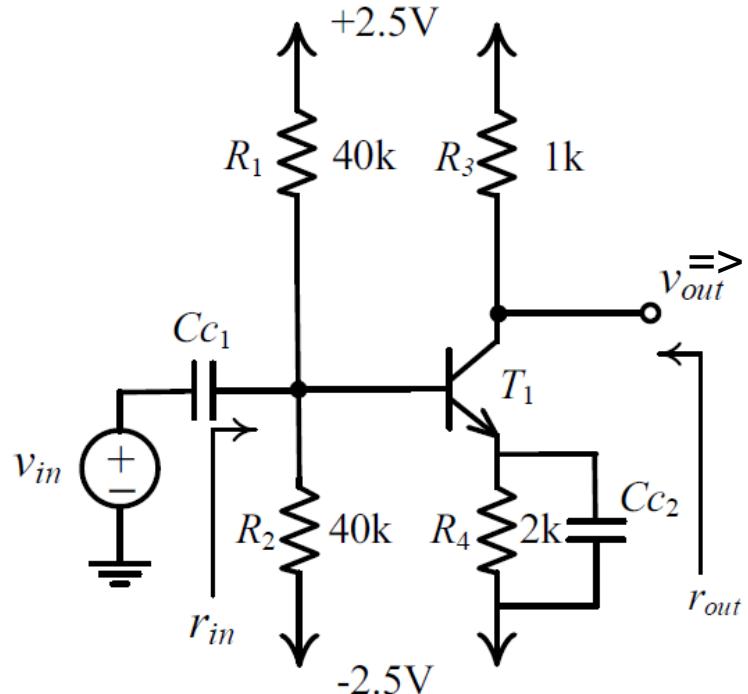


$$A_{v0} = -g_m(R_C \parallel r_0)$$

$$v_0 = -(g_m v_\pi)(R_C \parallel r_0)$$

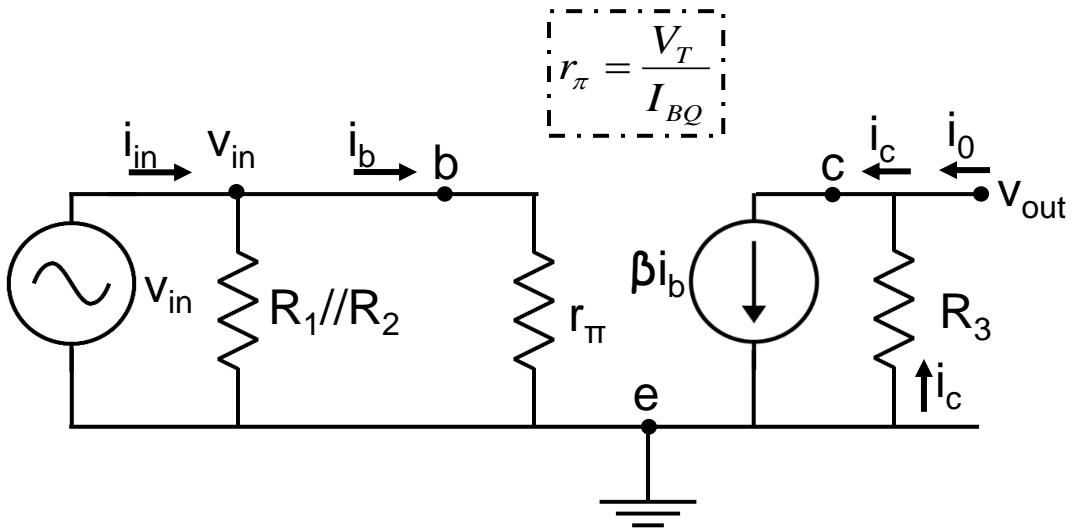


Consider an amplifier shown below. Suppose that the value of the coupling capacitors  $C_{c1}$  and  $C_{c2}$  are high enough, so they can be considered shorted in small signal analysis. Find the small signal values of  $Z_{in}$ ,  $Z_{out}$ , and  $v_{out}/v_{in}$ .  
 NPN Transistor Parameters:  $V_{BE} = 0.7$ ,  $\beta = 40$ ,  $V_A = \infty$ ,  $V_T = 25$  mV.



$$Z_{in} = \frac{v_{in}}{i_{in}} = R_1 // R_2 // r_\pi$$

$$Z_{out} = \frac{v_0}{i_0} = R_3$$



$$v_{be} = v_{in} = i_b \quad r_\pi = i_{in}(R_1 // R_2 // r_\pi)$$

$$v_{out} = -R_3 \beta i_b$$

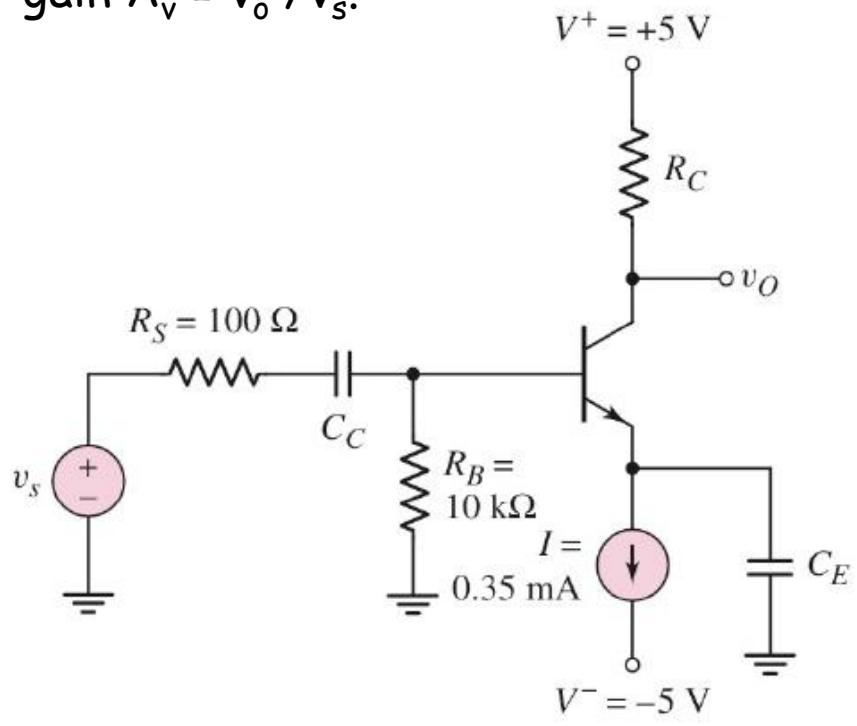
$$\frac{v_{out}}{v_{in}} = \frac{-R_3 \beta}{r_\pi}$$

The parameters of the transistor are  $\beta = 100$ ,  $V_{BE}=0.7V$  and  $V_A = \infty$ .

(a) Find the DC voltages at the base and emitter terminals.

(b) Find  $R_C$  such that  $V_{CEQ} = 3.5$  V.

(c) Assuming  $C_C$  and  $C_E$  act as short circuits, determine the small-signal voltage gain  $A_v = v_o / v_s$ .



$$I_{CQ} = \frac{\beta}{1+\beta} I_{EQ} = \left( \frac{100}{1+100} \right) (0.35) = 0.347 \text{ (mA)}$$

$$I_{BQ} = \frac{I_{EQ}}{1+\beta} = \frac{0.35}{1+100} = 3.47 \text{ (\mu A)}$$

$$V_B = 0 - I_{BQ} R_B = -(3.47 \times 10^{-3})(10) = -0.0347 \text{ (V)}$$

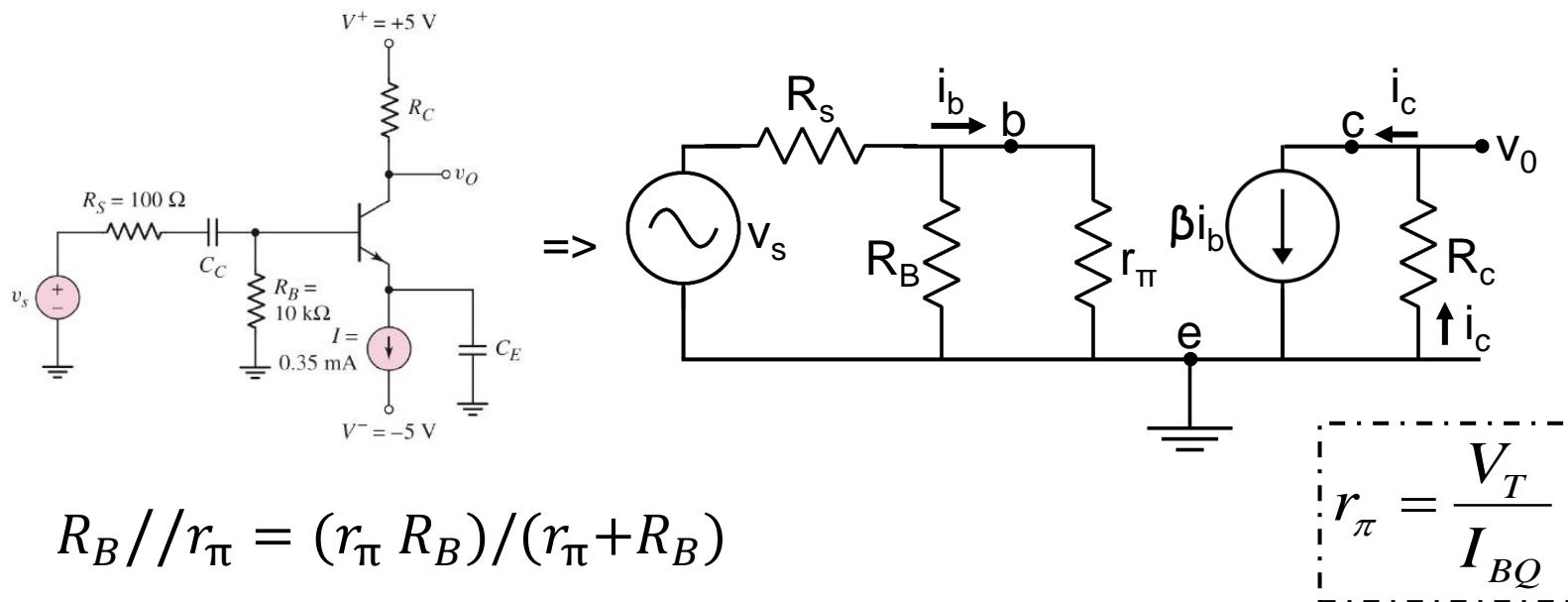
$$V_E = V_B - V_{BE(\text{on})} = -0.7347 \text{ (V)}$$

$$V^+ = V_E + V_{CEQ} + I_{CQ} R_C$$

$$R_C = \frac{V^+ - V_E - V_{CEQ}}{I_{CQ}}$$

$$= \frac{5 - (-0.737) - 3.5}{0.347} = 6.45 \text{ (k}\Omega\text{)}$$

Continue: The parameters of the transistor are  $\beta = 100$ ,  $V_{BE}=0.7V$  and  $V_A = \infty$ .



$$R_B // r_\pi = (r_\pi R_B) / (r_\pi + R_B)$$

$$r_\pi = \frac{V_T}{I_{BQ}}$$

$$v_{be} = \frac{R_B // r_\pi}{R_S + R_B // r_\pi} v_s = i_b r_\pi$$

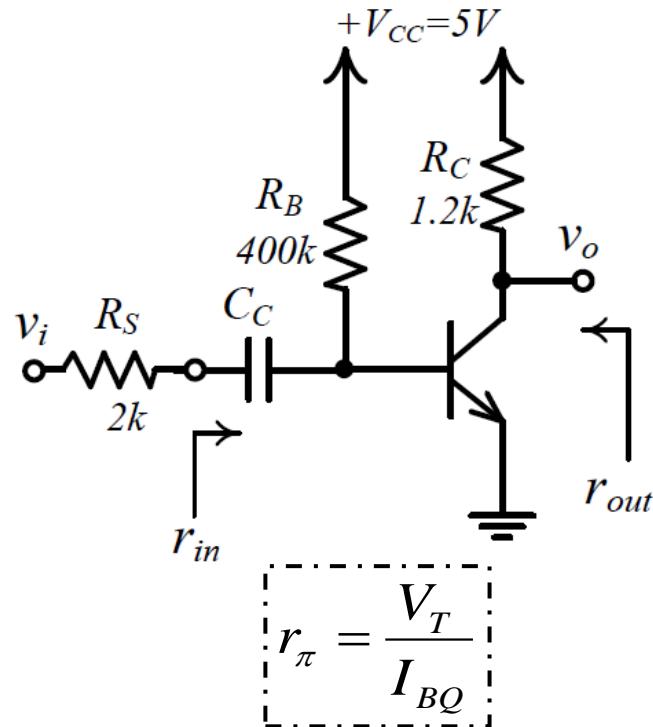
$$v_0 = -R_c \beta i_b \quad \frac{v_0}{v_{be}} = \frac{-R_c \beta}{r_\pi}$$

$$\frac{v_0}{v_s} = \frac{v_0}{v_{be}} \frac{v_{be}}{v_s} = \frac{-R_c \beta}{r_\pi} \frac{R_B // r_\pi}{R_S + R_B // r_\pi} = \frac{-R_B // r_\pi}{r_\pi (R_S + R_B // r_\pi)} R_c \beta$$

Consider the amplifier shown above. Use the following parameters for your calculations. Transistor parameters :  $\beta=200$ ,  $V_{BE}=0.7V$ ,  $V_T=25mV$ ,  $V_A=\infty$

a. Find  $V_B$  and  $V_o$  of the transistor by performing DC analysis.

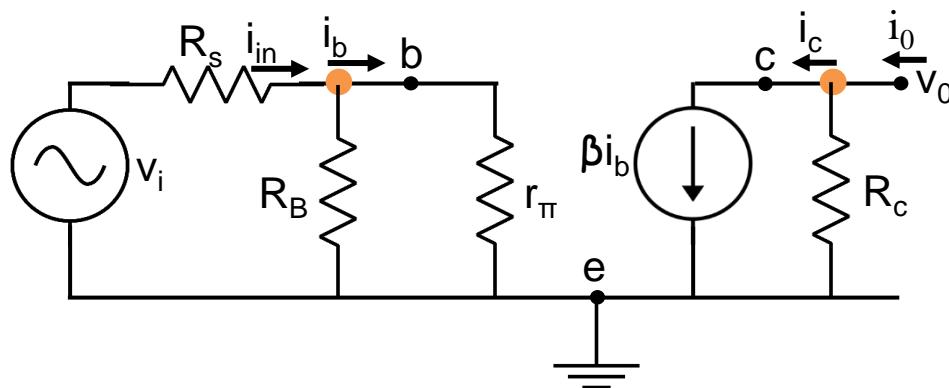
b. Find the small signal values of  $Z_{in}$ ,  $Z_{out}$ , and  $v_o/v_{in}$ .



$$5V - I_B 400k\Omega - V_{BE} = 0 \Rightarrow I_B \text{ SOLVED}$$

$$V_{BE} = V_B = 0.7V$$

$$5V - \beta I_B 1.2k\Omega = V_o \Rightarrow V_o \text{ SOLVED}$$



$$v_{be} = \frac{R_B // r_\pi}{R_s + R_B // r_\pi} v_i = i_b r_\pi$$

$$v_o = -R_c \beta i_b$$

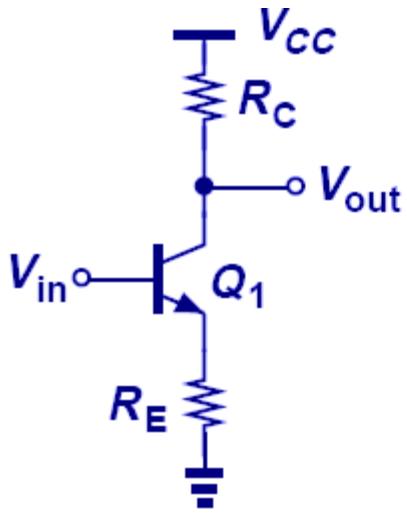
$$\frac{v_o}{v_i} = \frac{-R_B // r_\pi}{r_\pi (R_s + R_B // r_\pi)} R_c \beta$$

$$\frac{v_o}{v_i} = \frac{v_0}{v_{be}} \frac{v_{be}}{v_i}$$

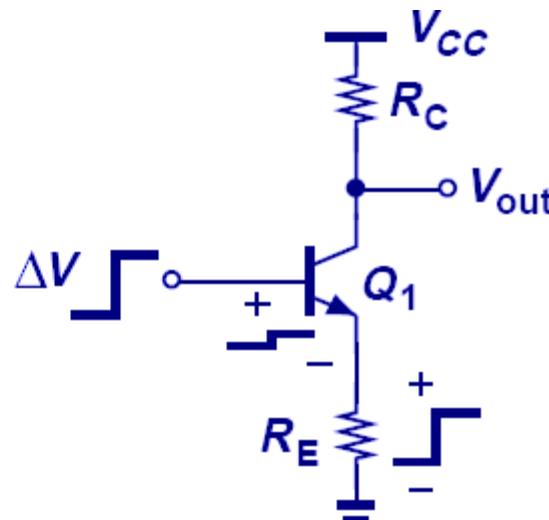
$$Z_{in} = \frac{v_{in}}{i_{in}} = R_B // r_\pi$$

$$Z_{out} = \frac{v_0}{i_0} = R_c$$

# Emitter Degeneration



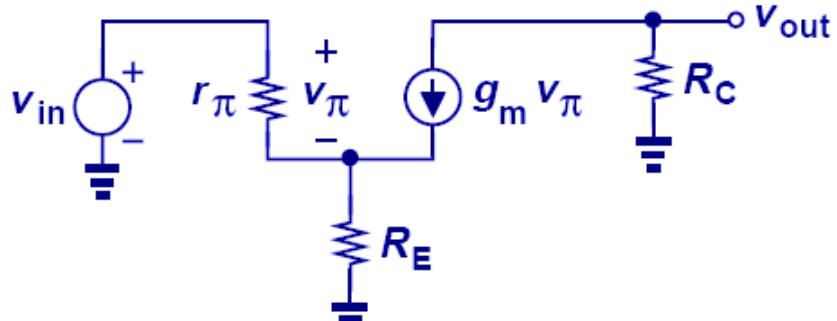
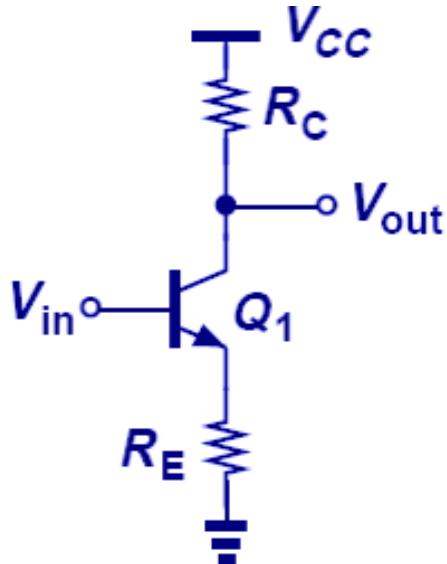
(a)



(b)

- By inserting a resistor in series with the emitter, this topology will decrease the gain of the amplifier but improve other aspects, such as linearity, and input impedance.

# Small-Signal Model



$$v_{out} = -R_c g_m v_\pi$$

$$v_{in} = v_\pi + R_E \left( g_m v_\pi + \frac{v_\pi}{r_\pi} \right)$$

$$A_v = -\frac{g_m R_C}{1 + R_E(g_m + \frac{1}{r_\pi})}$$

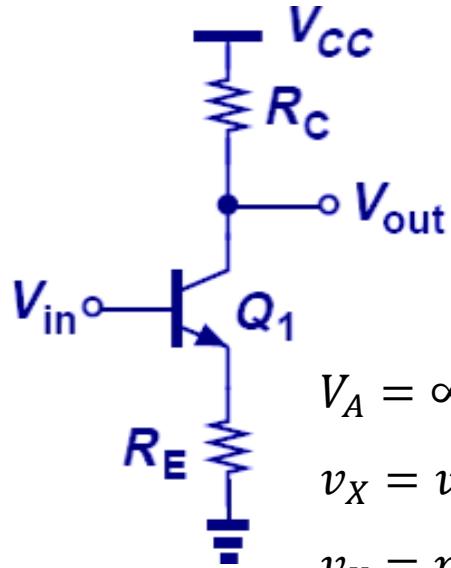
$$A_v = -\frac{g_m R_C}{1 + g_m R_E}$$

$$A_v = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

Base current is neglected

Assume that:  
 $V_A = \infty$

# Input Impedance of Degenerated CE Stage



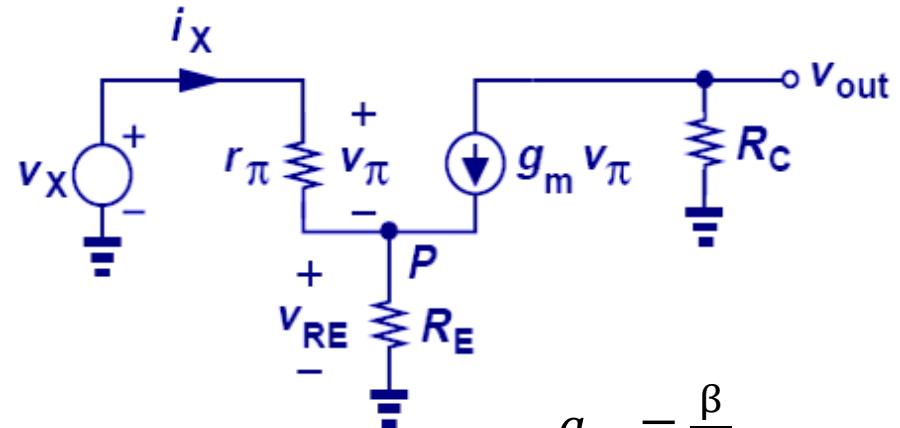
$$V_A = \infty, \quad v_\pi = r_\pi i_X$$

$$v_X = v_\pi + (i_X + g_m v_\pi) R_E$$

$$v_X = r_\pi i_X + (i_X + g_m r_\pi i_X) R_E$$

$$R_{in} = \frac{v_X}{i_X} = r_\pi + (1 + g_m r_\pi) R_E$$

$$R_{in} = \frac{v_X}{i_X} = r_\pi + (\beta + 1) R_E$$

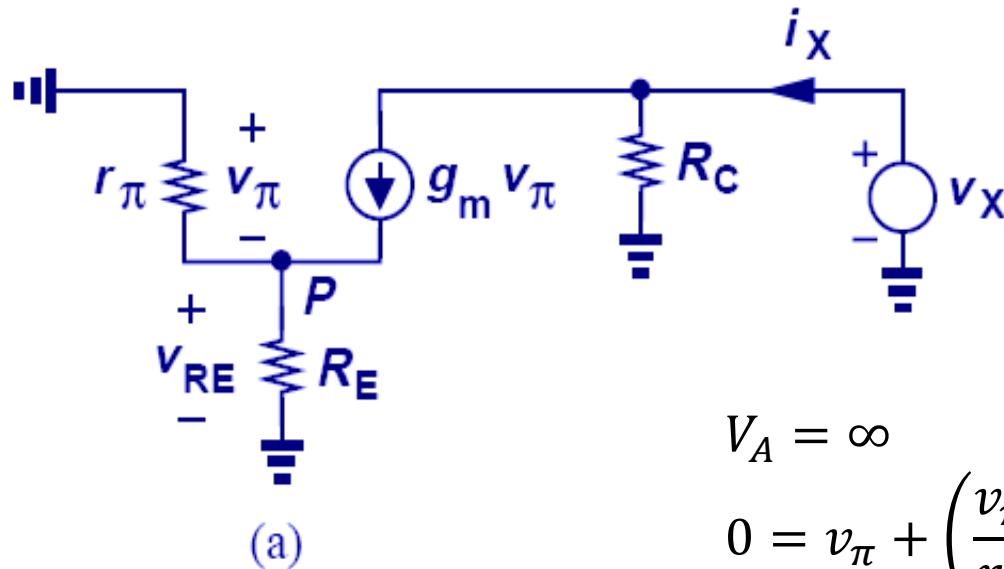


$$g_m = \frac{\beta}{r_\pi}$$

Assume that:  
 $V_A = \infty$

With emitter degeneration, the input impedance is **increased** from  $r_\pi$  to  $r_\pi + (\beta + 1) R_E$ ; a desirable effect.

# Output Impedance of Degenerated CE Stage



$$V_A = \infty$$

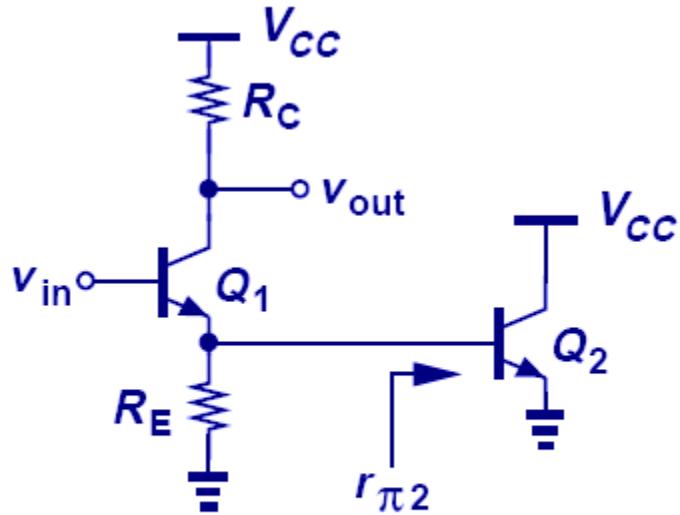
$$0 = v_\pi + \left( \frac{v_\pi}{r_\pi} + g_m v_\pi \right) R_E \Rightarrow v_\pi = 0$$

$$R_{out} = \frac{v_X}{i_X} = R_C$$

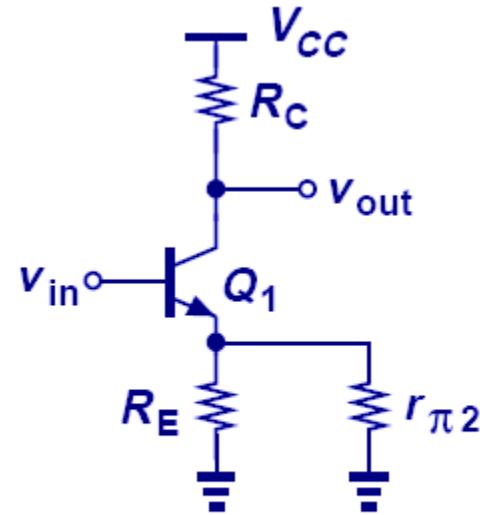
Emitter degeneration does not alter the output impedance in this case.

Assume that:  
 $V_A = \infty$

# Emitter Degeneration Example I



(a)

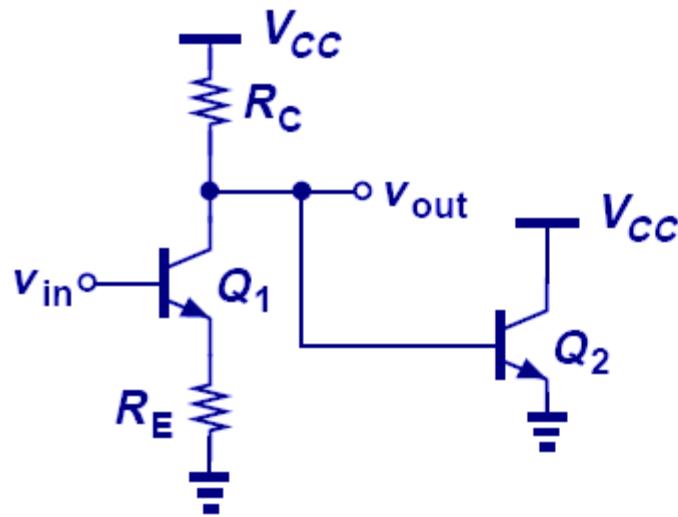


(b)

$$A_v = - \frac{R_C}{\frac{1}{g_m 1} + R_E || r_{\pi 2}}$$

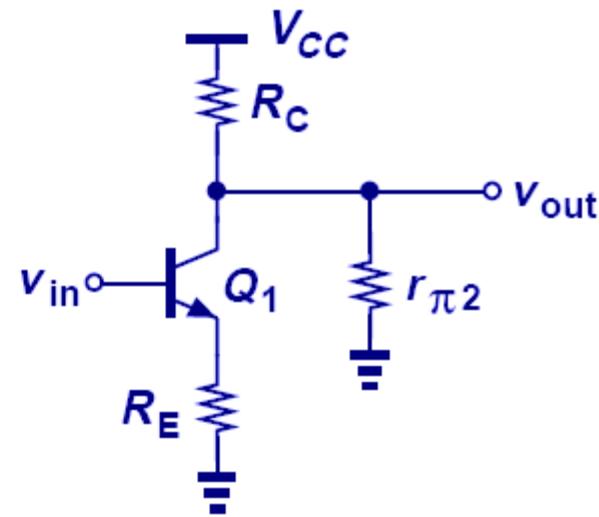
The input impedance of  $Q_2$  can be combined in parallel with  $R_E$  to yield an equivalent impedance that degenerates  $Q_1$ .

# Emitter Degeneration Example II



(a)

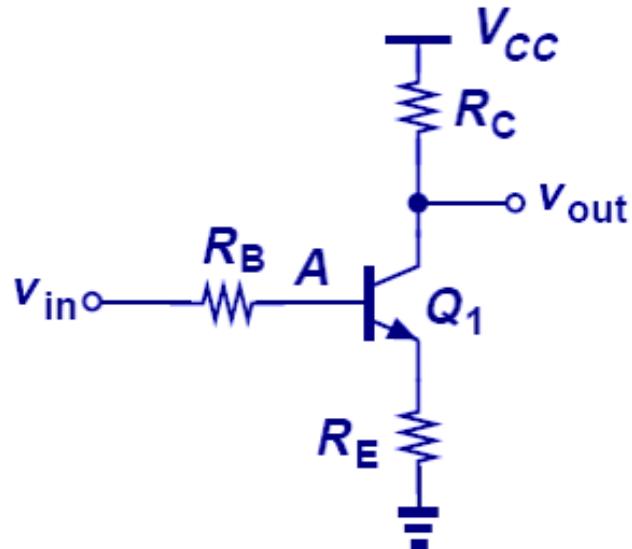
$$A_v = -\frac{R_C \parallel r_{\pi 2}}{\frac{1}{g_{m1}} + R_E}$$



(b)

In this example, the input impedance of  $Q_2$  can be combined in parallel with  $R_C$  to yield an equivalent collector impedance to ground.

# Degenerated CE with Base Resistance



$$V_A = \infty$$

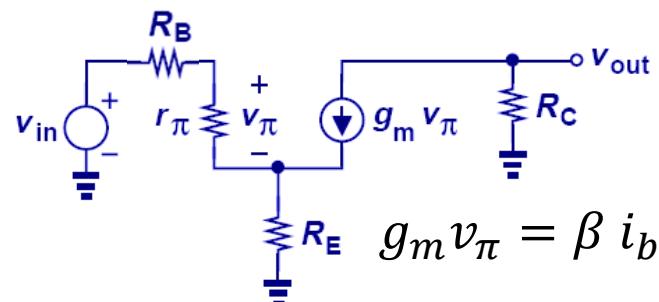
$$v_{out} = -\beta i_b R_c$$

$$v_{in} = (r_\pi + R_B)i_b + (i_b + g_m v_\pi) R_E$$

$$v_{in} = (r_\pi + R_B)i_b + (i_b + g_m r_\pi i_b) R_E$$

$$v_{in} = (r_\pi + R_B)i_b + i_b(1 + g_m r_\pi) R_E$$

$$v_{in} = (r_\pi + R_B)i_b + i_b(1 + \beta) R_E$$

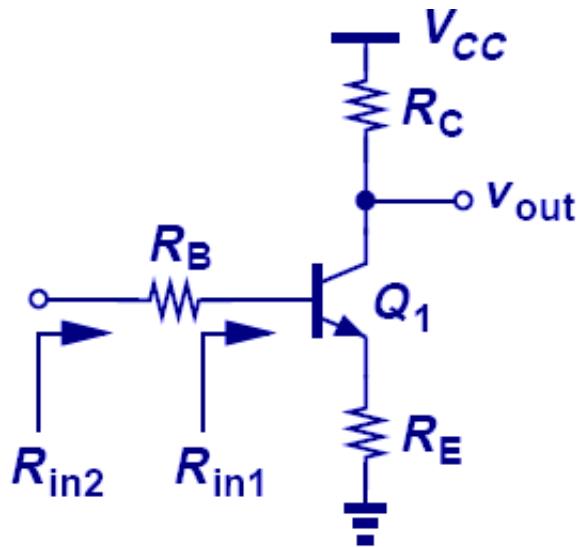


$$\frac{v_{out}}{v_{in}} = \frac{-\beta R_C}{r_\pi + (\beta + 1)R_E + R_B}$$

$$A_v \approx \frac{-R_C}{\frac{1}{g_m} + R_E + \frac{R_B}{\beta}}$$

Assume that:  
 $V_A = \infty$

# Input/Output Impedances



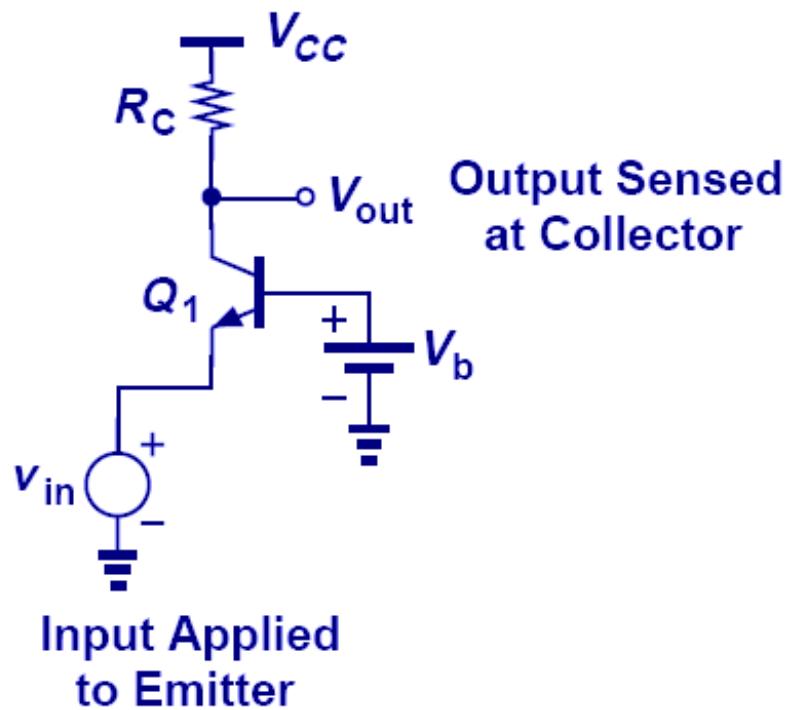
$$V_A = \infty$$

$$R_{in1} = r_\pi + (\beta + 1)R_E$$

$$R_{in2} = R_B + r_\pi + (\beta + 1)R_E$$

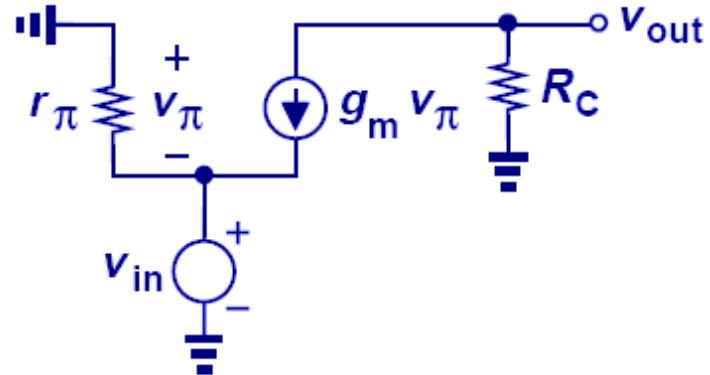
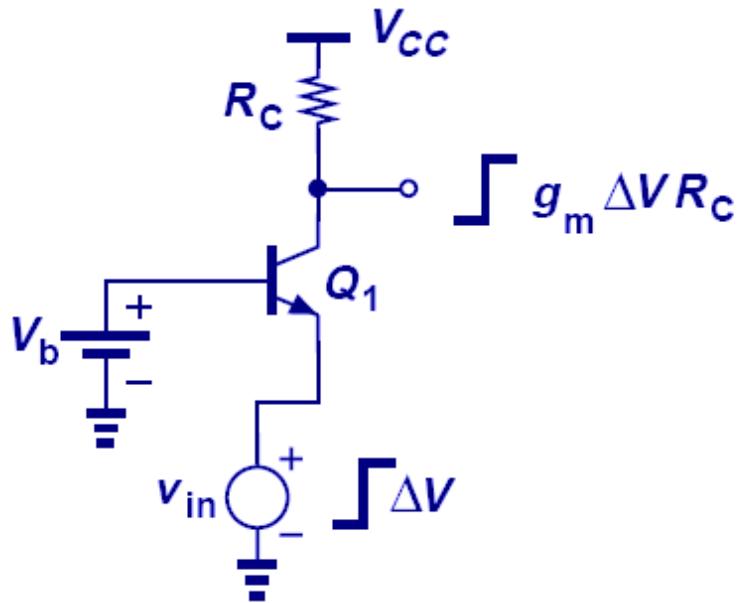
$$R_{out} = R_C$$

# Common Base (CB) Amplifier



In common base topology, where the **base terminal is biased with a fixed voltage**, emitter is fed with a signal, and collector is the output.

# Common Base (CB) Amplifier



$$v_{out} = -R_c g_m v_\pi$$

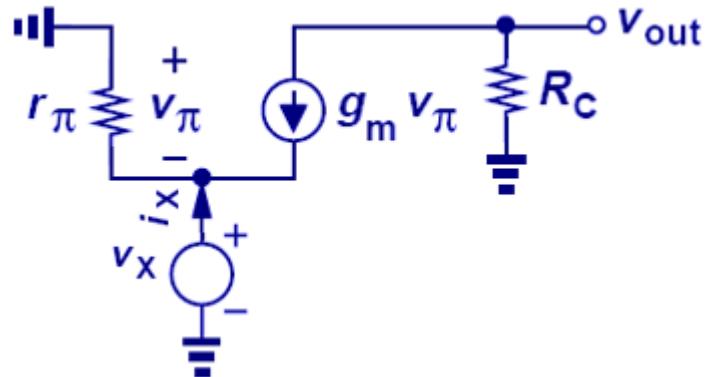
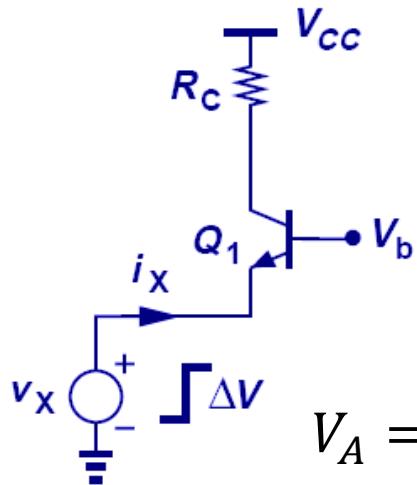
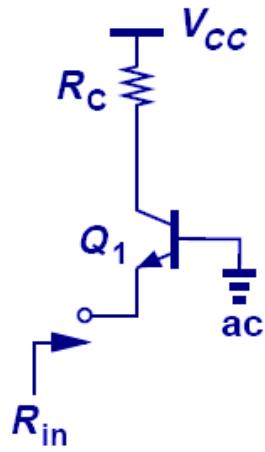
$$v_{in} = -v_\pi$$

$$A_v = g_m R_C$$

The voltage gain of CB stage is  $g_m R_C$ , which is identical to that of CE stage in magnitude and opposite in phase.

Assume that:  
 $V_A = \infty$

# Input Impedance of CB Amplifier



$$V_A = \infty, v_x = -v_\pi$$

$$R_{in} = \frac{v_x}{i_x} = \frac{v_x}{-(g_m(-v_x) + \frac{(-v_x)}{r_\pi})}$$

$$R_{in} = \frac{v_x}{i_x} = \frac{1}{g_m + \frac{1}{r_\pi}}$$

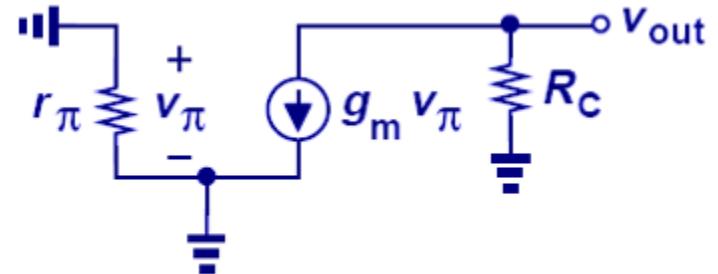
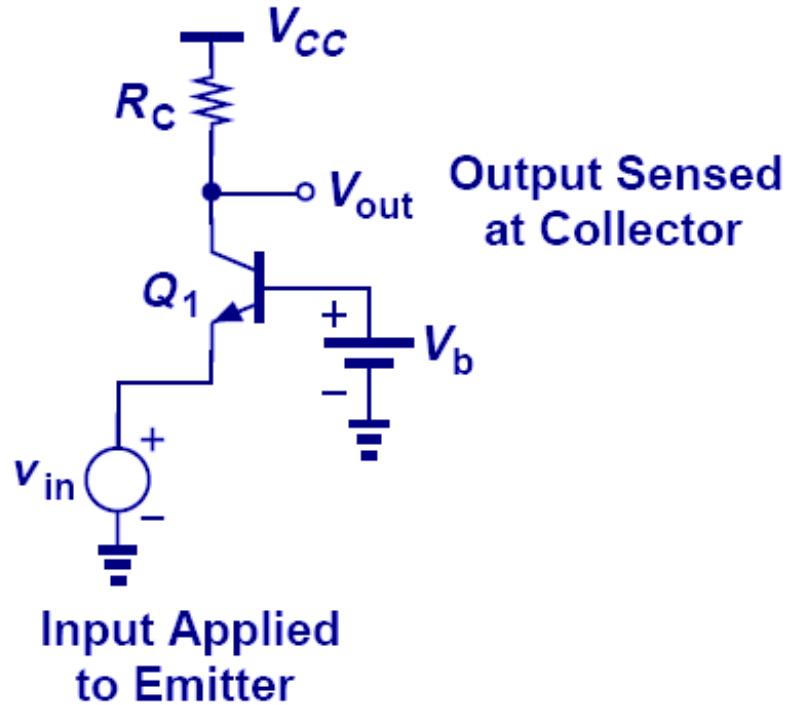
The input impedance of CB stage is much smaller than that of the CE stage.

Assume that:  
 $V_A = \infty$

$\frac{1}{r_\pi}$  is neglected

$$R_{in} = \frac{1}{g_m}$$

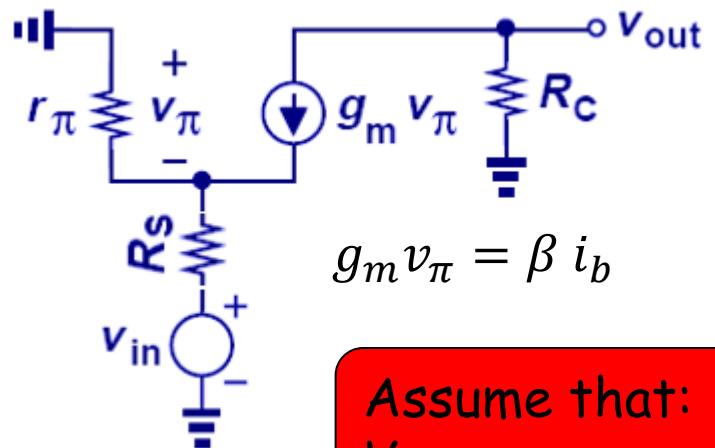
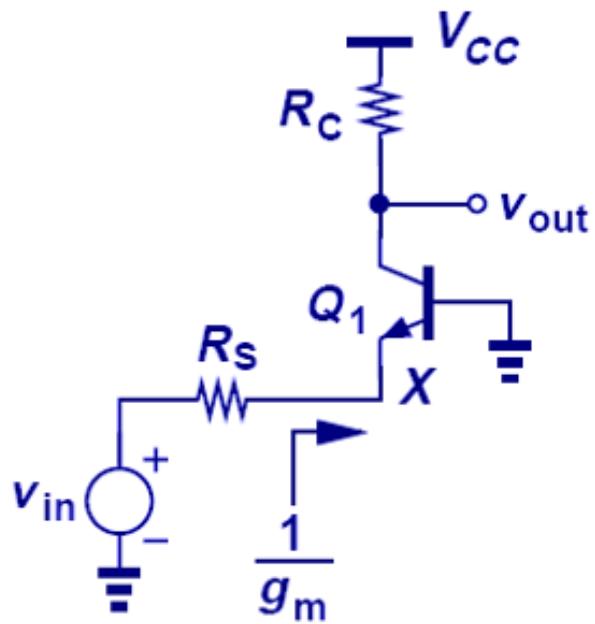
# Output Impedance of CB Stage



$$R_{out} = R_C$$

Assume that:  
 $V_A = \infty$

# CB with Source Resistance



$$V_A = \infty$$

$$v_{out} = -R_c g_m v_\pi$$

$$v_{in} = -(v_\pi + v_{R_s})$$

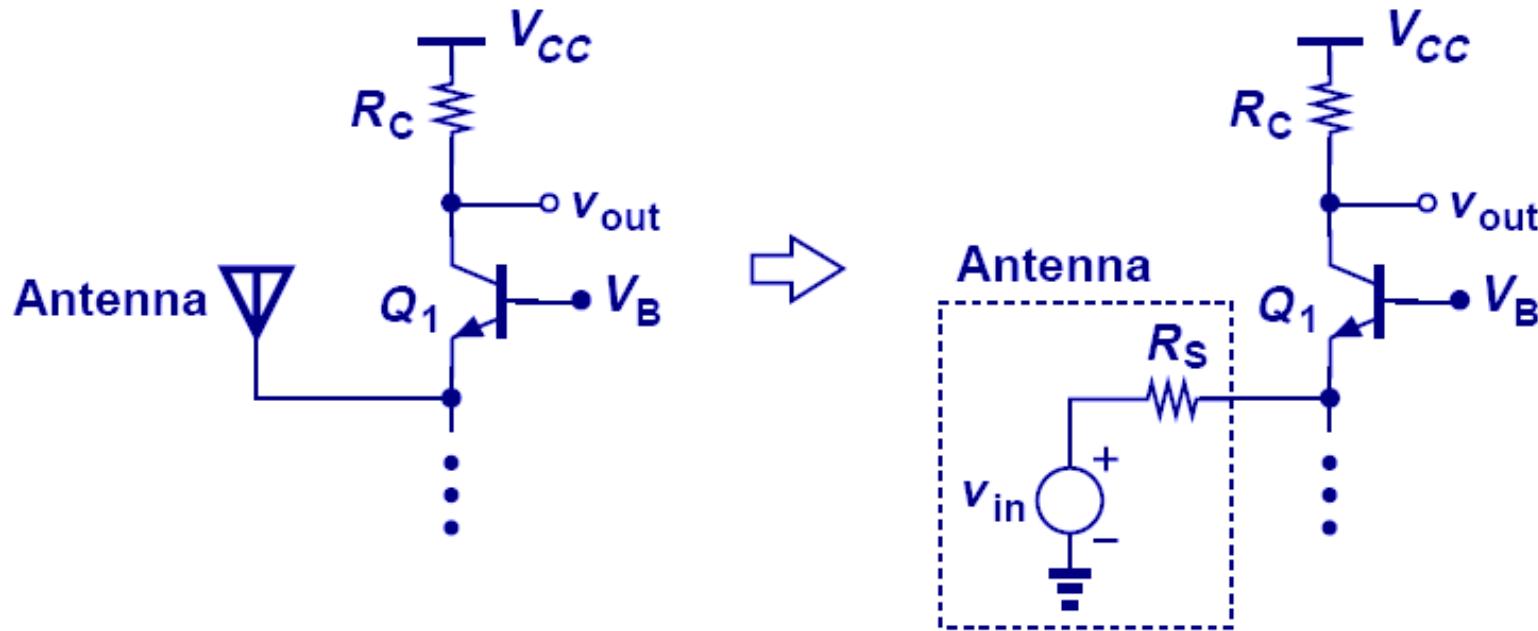
$$v_{in} = -(v_\pi + R_s (g_m v_\pi + \frac{v_\pi}{r_\pi}))$$

$$A_v = \frac{R_c}{\frac{1}{g_m} + R_s (1 + \frac{1}{g_m r_\pi})} \approx \frac{R_c}{\frac{1}{g_m} + R_s}$$

Assume that:  
 $V_A = \infty$

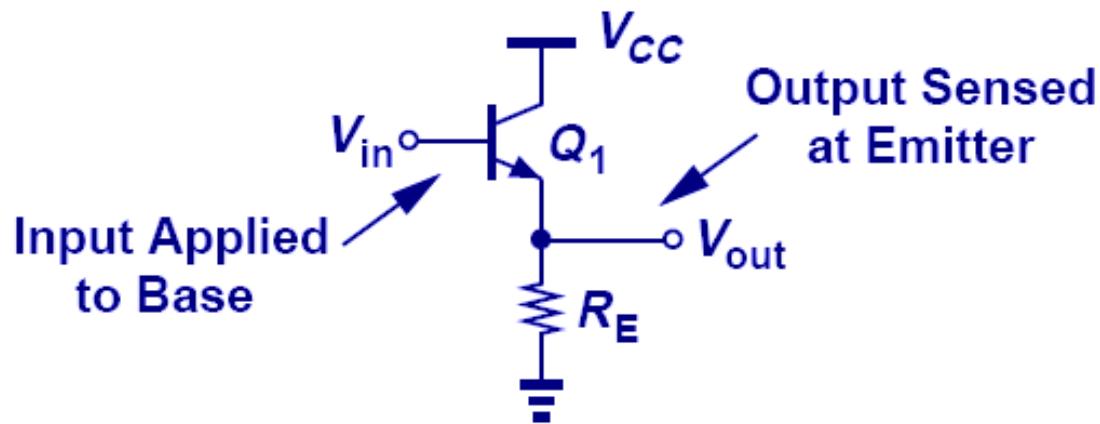
With an inclusion of a source resistor, the input signal is attenuated before it reaches the emitter of the amplifier; therefore, we see a lower voltage gain.

# Practical Example of CB Stage

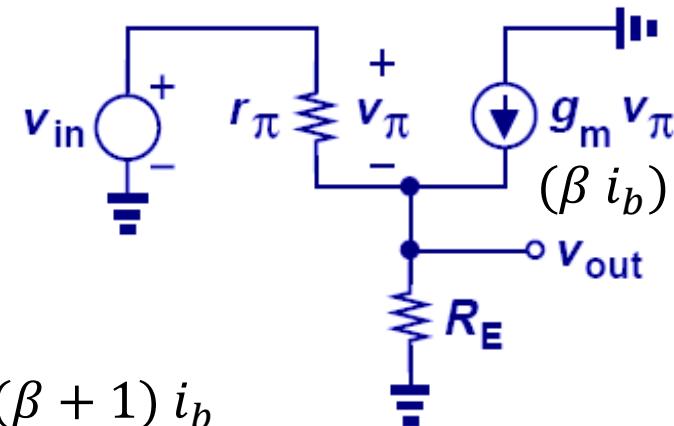
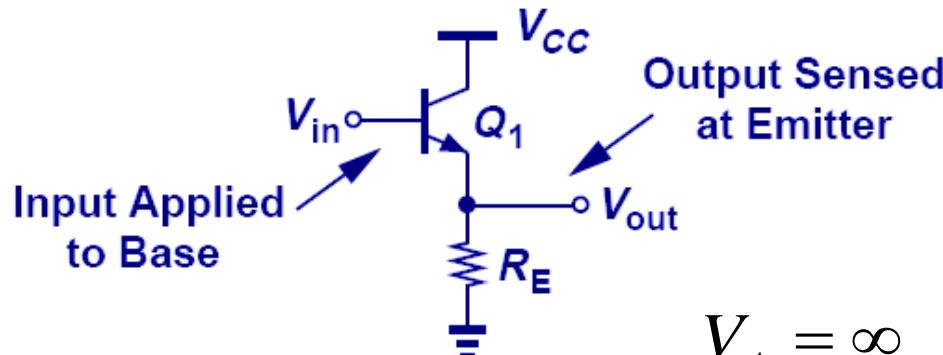


An antenna usually has **low output impedance**; therefore, a correspondingly **low input impedance** is required for the following stage.

# Emitter Follower (Common Collector Amplifier)



# Small-Signal Model of Emitter Follower (Common Collector)



$$V_A = \infty$$

$$v_{out} = R_E (\beta + 1) i_b$$

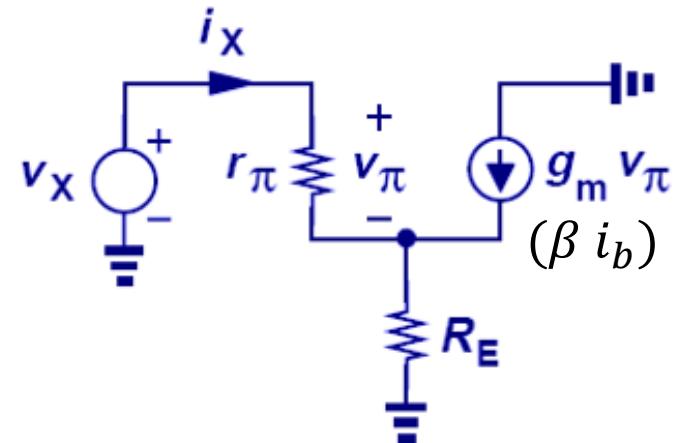
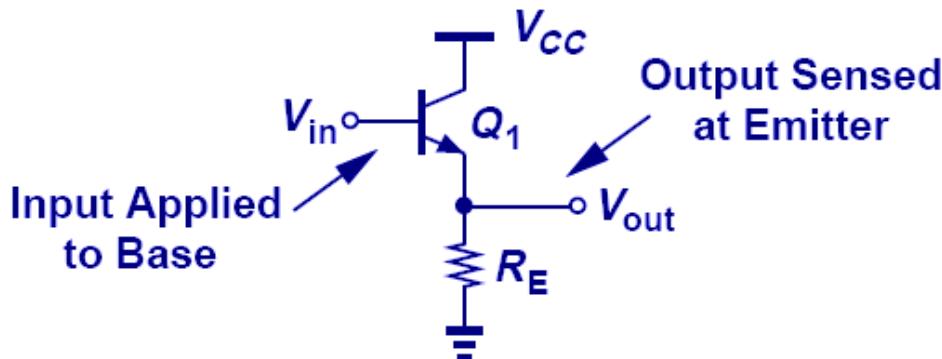
$$v_{in} = r_\pi i_b + R_E (\beta + 1) i_b$$

$$\frac{v_{out}}{v_{in}} = \frac{1}{1 + \frac{r_\pi}{\beta + 1} \cdot \frac{1}{R_E}} \approx \frac{R_E}{R_E + \frac{1}{g_m}}$$

As shown above, the voltage gain is less than unity and positive.

Assume that:  
 $V_A = \infty$

# Input Impedance of Emitter Follower



$$V_A = \infty$$

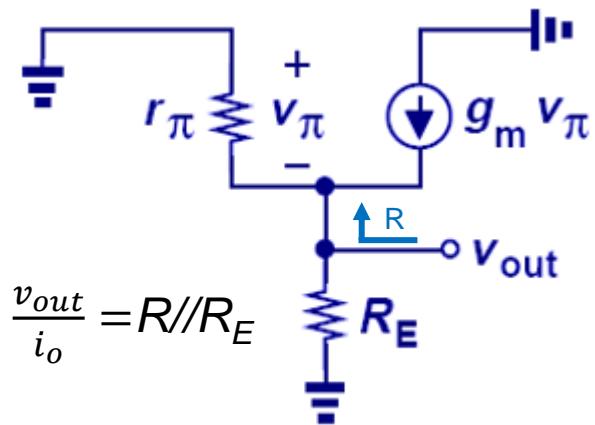
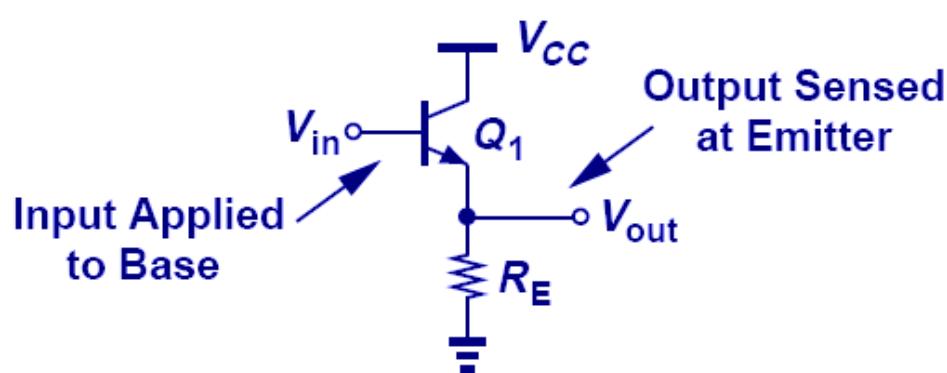
$$v_x = r_\pi i_x + R_E (1 + \beta) i_x$$

$$R_{in} = \frac{v_x}{i_x} = r_\pi + (\beta + 1) R_E$$

The input impedance of emitter follower is exactly the same as that of CE stage with emitter degeneration. This is not surprising because the input impedance of CE with emitter degeneration does not depend on the collector resistance.

Assume that:  
 $V_A = \infty$

# Output Impedance of Emitter Follower



$$\frac{v_{out}}{i_o} = R // R_E$$

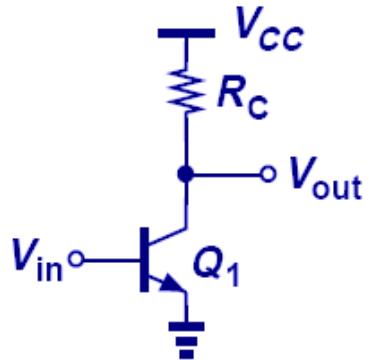
$$v_{out} = -v_\pi \quad i_e = (g_m v_\pi + \frac{v_\pi}{r_\pi}) \quad R = \frac{v_{out}}{-i_e}$$

$$\frac{v_{out}}{i_o} = R_E // \frac{-v_\pi}{-(g_m v_\pi + \frac{v_\pi}{r_\pi})} = R_E // \frac{1}{(g_m + \frac{1}{r_\pi})}$$

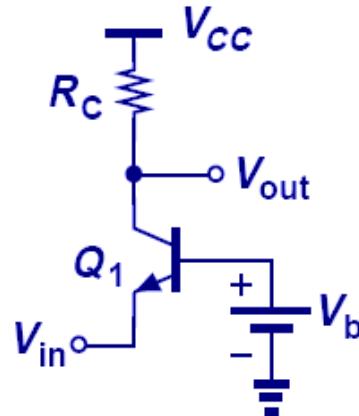
Assume that:  
 $V_A = \infty$

# Summary of Amplifier Topologies

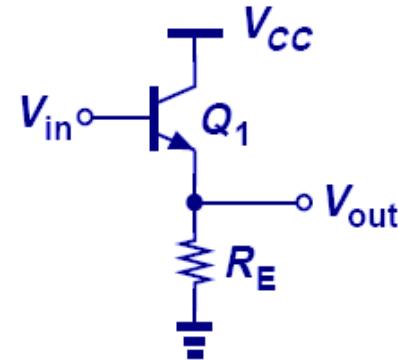
CE Stage



CB Stage



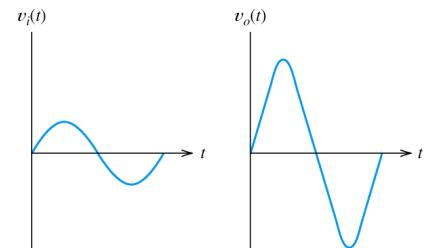
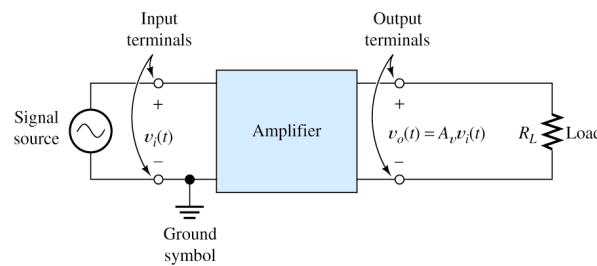
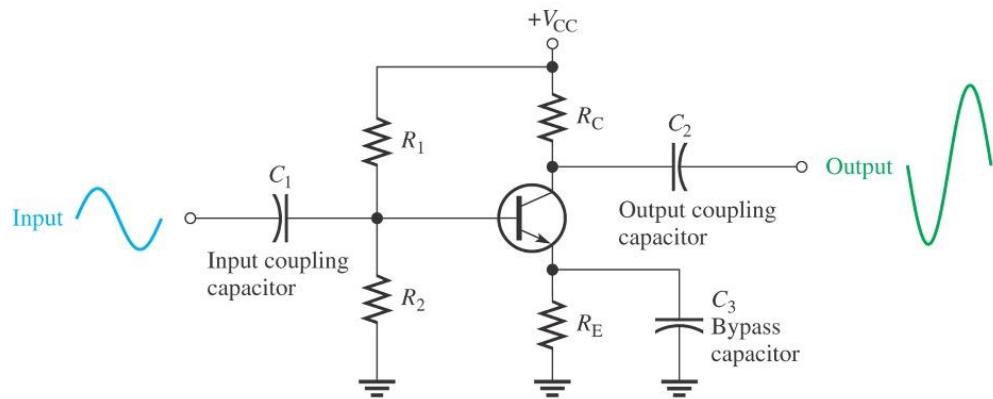
Follower



The three amplifier topologies studied so far have different properties and are used on different occasions.

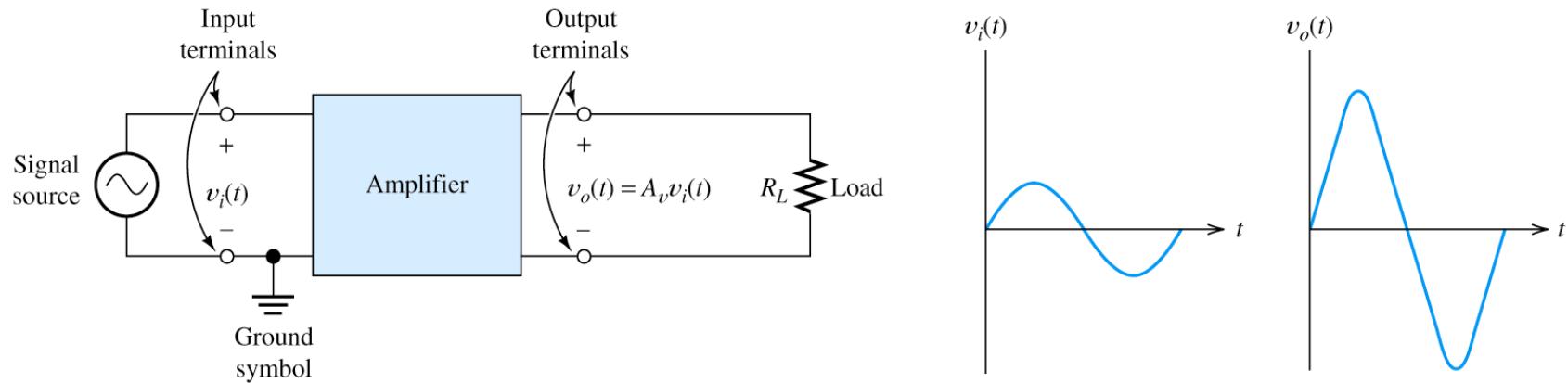
- CE and CB have voltage gain with magnitude greater than one, while follower's voltage gain is at most one.

# Amplifiers - Basic Amplifier Concepts



# Amplifiers - Basic Amplifier Concepts

Ideally, an *amplifier* produces an output signal with identical wave-shape as the input signal but with a larger amplitude.

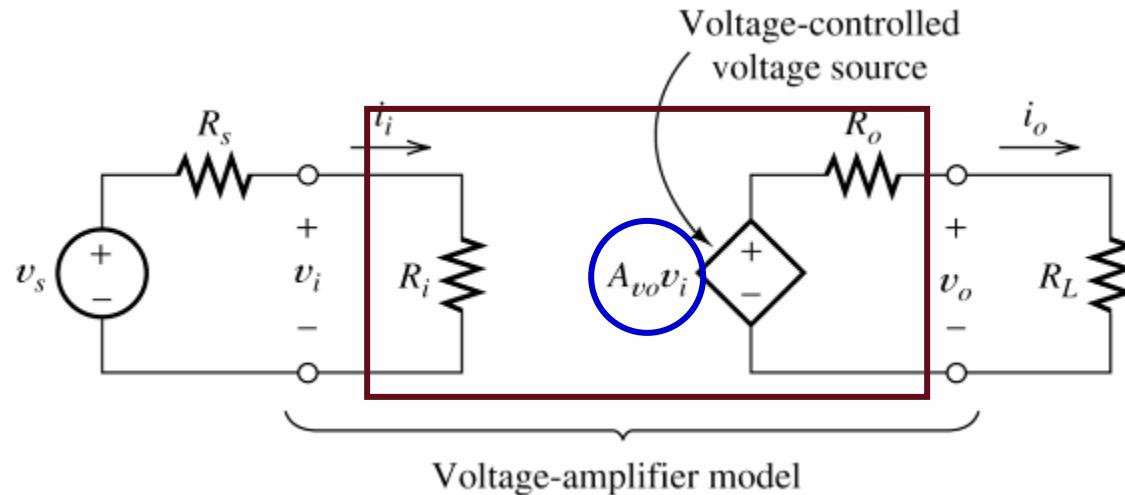


$$v_o(t) = A_v v_i(t)$$

$A_v$  is the Voltage Gain

# Amplifiers - Amplifier Model

Amplification can be modeled by a controlled source.



$R_i$ : the input resistance (or impedance), is the equivalent resistance seen when looking into the input terminals.

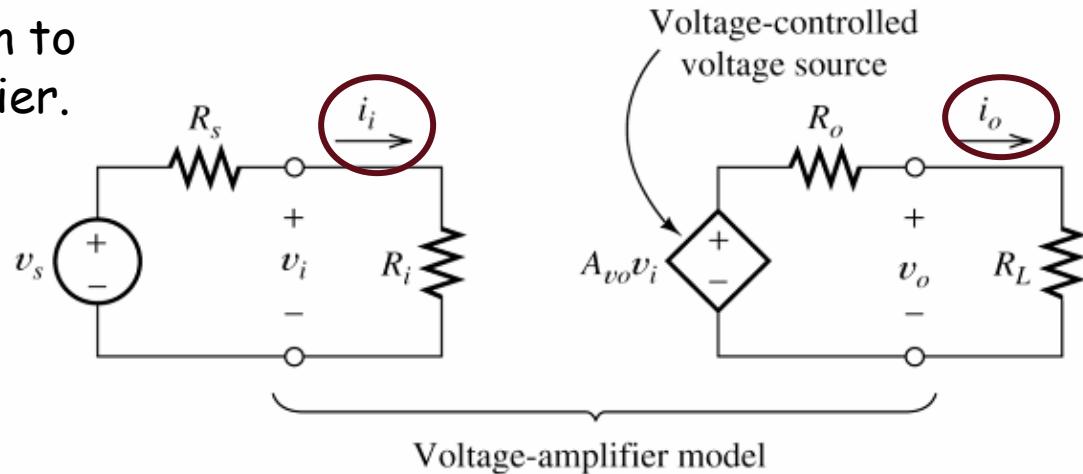
$R_o$ : in series with the output terminals, is the output resistance (or impedance)

$A_{vo} = v_{oc}/v_i$  : the open-circuit voltage gain (**gain without load**)  
(note: the real gain is smaller than  $A_{vo}$ )

# Amplifiers - Current and Voltage Gains

$i_i$  is the current delivered in to the terminals of the amplifier.

$i_o$  is the current flowing through the load.



*The current gain  $A_i$  is the ratio between output and input currents :  $A_i = \frac{i_o}{i_i}$*

*Furthermore,  $A_i = \frac{i_o}{i_i} = \frac{v_o/R_L}{v_i/R_i} = A_v \frac{R_i}{R_L}$ , where  $A_v = \frac{v_o}{v_i}$  is the voltage gain*

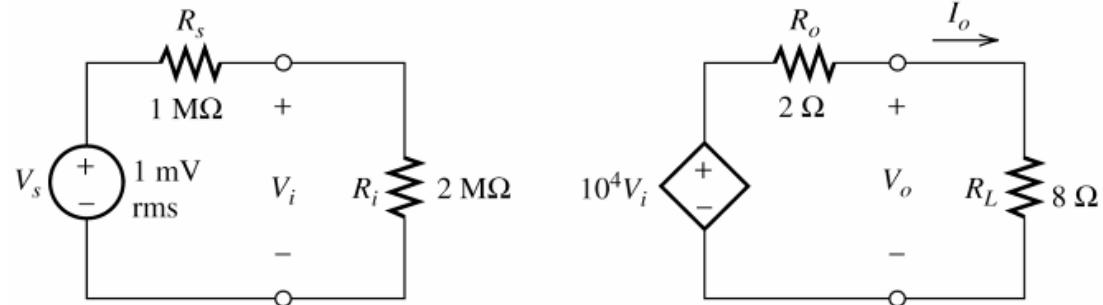
*The voltage gain  $A_v$  is usually smaller than the open-circuit voltage gain  $A_{vo}$*

# Example

**Find the voltage gains**

$$A_{vs} = V_o / V_s \text{ and } A_v = V_o / V_i$$

**Also, find the current gain**



$$V_i = V_s \frac{R_i}{R_i + R_s} \quad V_o = A_{vo} V_i \frac{R_L}{R_o + R_L} \quad A_v = \frac{V_o}{V_i} = A_{vo} \frac{R_L}{R_o + R_L}$$

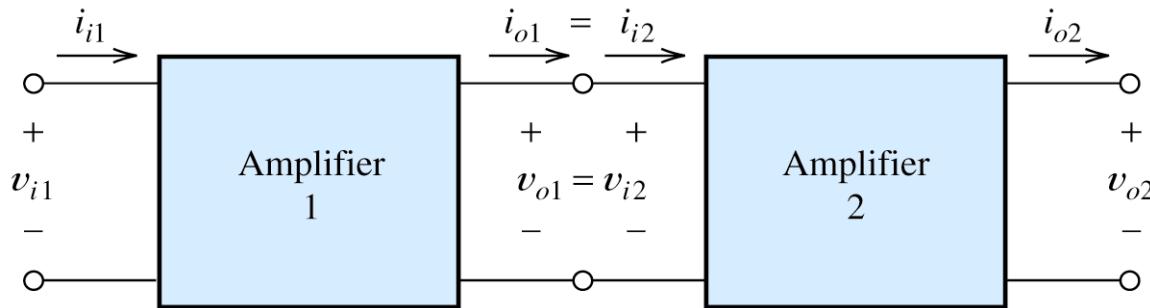
$$A_v = \frac{V_o}{V_i} = A_{vo} \frac{R_L}{R_o + R_L} = 10^4 \frac{8}{2 + 8} = 8000$$

$$A_{vs} = \frac{V_o}{V_s} = \frac{V_i}{V_s} \frac{V_o}{V_i} = \frac{R_i}{(R_i + R_s)} \frac{V_o}{V_i} = A_v \frac{R_i}{R_i + R_s} = 5333$$

(Note: due to the loading effect,  $A_{VS} < A_v < A_{vo}$ )

$$A_i = A_v \frac{R_i}{R_L} = 2 \times 10^9$$

# Amplifiers - Cascade Amplifiers



Cascade connection of two amplifiers.

$$A_{vo2} = v_{oc2}/v_{i2} : \text{the open-circuit voltage gain}$$

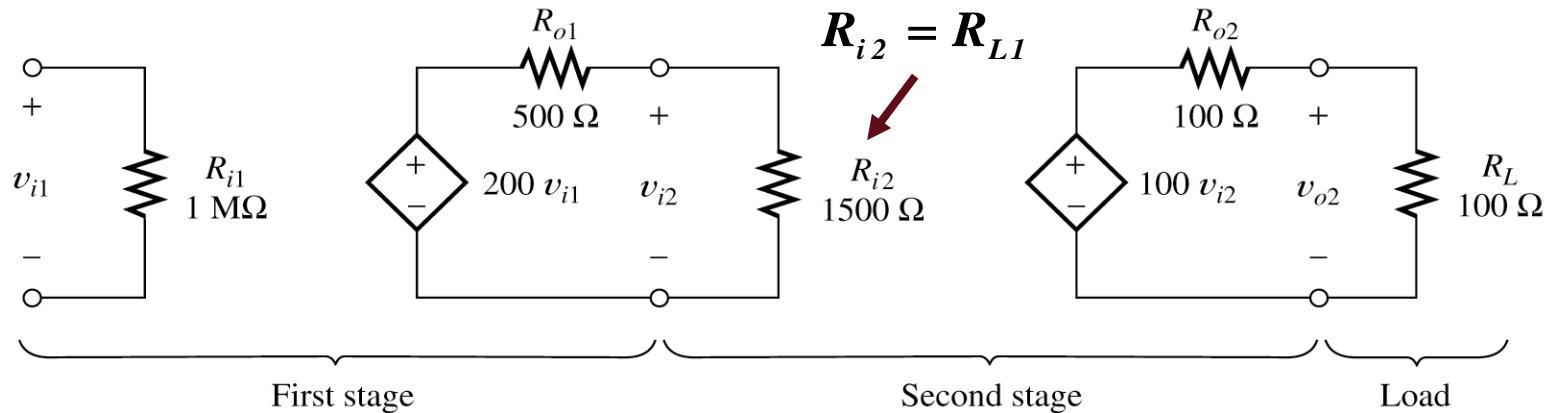
$$A_v = \frac{v_{o2}}{v_{i1}} = \frac{v_{o1}}{v_{i1}} \times \frac{v_{o2}}{v_{o1}} = \frac{v_{o1}}{v_{i1}} \times \frac{v_{o2}}{v_{i2}} \Rightarrow A_v = A_{v1}A_{v2}$$

$$A_{vo} = \frac{v_{oc2}}{v_{i1}} = \frac{v_{o1}}{v_{i1}} \times \frac{v_{oc2}}{v_{i2}} \Rightarrow A_{vo} = A_{v1}A_{vo2}$$

$$\text{In addition, } A_i = A_{i1} A_{i2}$$

gain without load

# Example



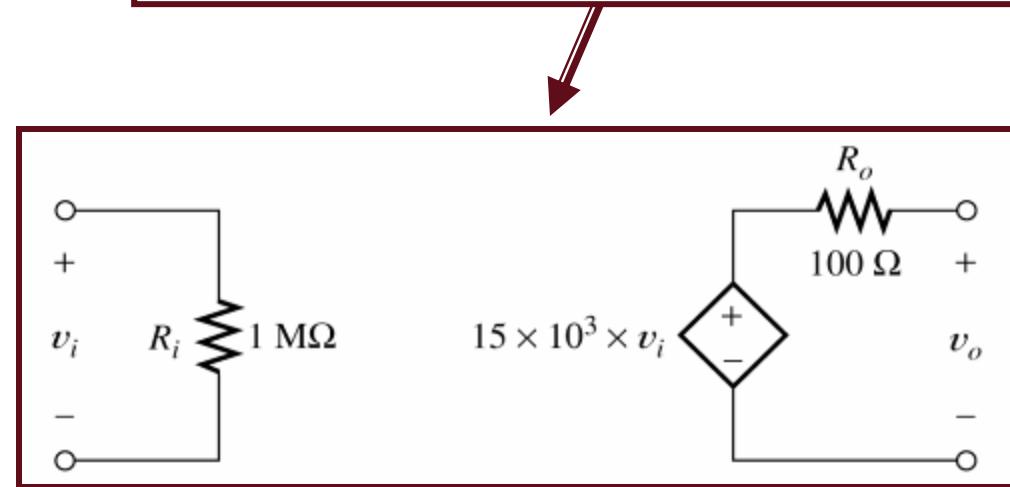
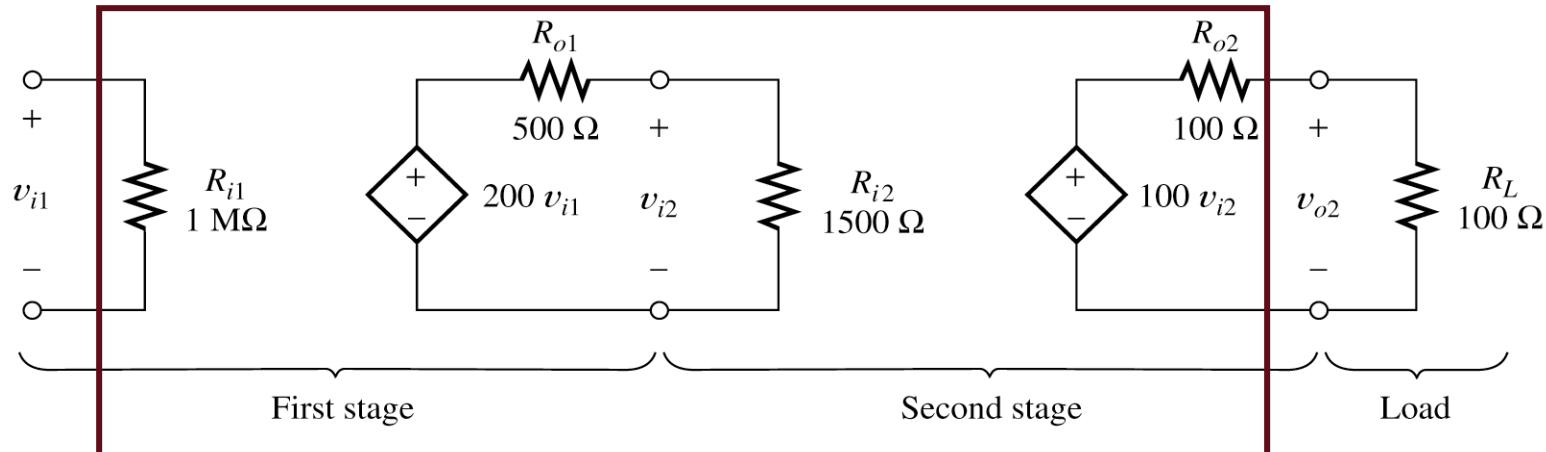
$$A_{v1} = A_{vo1} \frac{R_{i2}}{R_{i2} + R_{o1}} = 150,$$

$$A_{v2} = A_{vo2} \frac{R_L}{R_L + R_{o2}} = 50 \quad \Rightarrow \quad A_v = A_{v1}A_{v2} = 7500$$

$$A_{i1} = A_{v1} \frac{R_{i1}}{R_{i2}} = 10^5,$$

$$A_{i2} = A_{v2} \frac{R_{i2}}{R_L} = 750 \quad \Rightarrow \quad A_i = A_{i1}A_{i2} = 75 \times 10^6$$

# Example



$$A_{v1} = A_{vo1} \frac{R_{i2}}{R_{i2} + R_{o1}} = 150$$

$$A_{vo2} = 100$$

$$A_{vo} = A_{v1} A_{vo2} = 15 \times 10^3$$

# Amplifiers - Ideal Amplifiers

**Voltage Amplifier :**

$$R_i \rightarrow \infty, v_i \approx v_s \text{ max.}$$

$$R_o \rightarrow 0, v_o \approx A_{vo} v_i \text{ max}$$

**$\Rightarrow$  Maximum Voltage Gain!**

$$A_v = A_{vo} \frac{R_L}{R_0 + R_L}$$

