İTÜ Computer Engineering Dep.
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Student ID:
First Name and Last Name:
Signature:

BLG 322E COMPUTER ARCHITECTURE FINAL EXAM

Regulations:

1. The duration for this question is **40 minutes**.
2. **You may not ask any questions during the exam.** If you think something is missing in a question, explain it, make the necessary assumption, and solve the question.
3. Any cheating or any attempt to cheat will be subject to the University disciplinary proceedings.
4. Your solution must **be all hand-written and signed by you.**
5. Please **show all your work**. Answers with no supporting explanations or work will be given no partial credit. If we cannot read or follow your solution, no partial credit will be given. PLEASE BE NEAT.

QUESTION 1 (Total 45 points):

A. **(15 points)** Two Computer Architects are working on designing a cache memory for the first level cache. They have two choices for the organization. In one case, there are 32 data words per block and 1024 blocks in total. In another case, there are 128 data words per block but 256 blocks in total.

Can you discuss the advantages and disadvantages of both design choices? (At least, list one advantage and one disadvantage for each design choice. What type of data accesses benefit from which design choice?

B. **(15 points)** For this part, assume that, a processor has a direct mapped L1 data cache with a word size of 16 bits and the memory is word accessible. The physical memory address size is 24 bits long. In the given data cache, the tag size is 12 bits and each cache block is composed of 16 bytes.

How many blocks are in this data cache? Show all your work clearly.

C. **(15 points)** Now, consider a 16-way set-associative L2 cache. In this cache, data words are 32 bits long and the data is accessible (therefore addressable) at the half-word granularity. This cache holds total of 4 Mbytes of data. Each block in this cache holds totally 32 data words. The physical addresses are 32 bits.

How many bits of tag, index, and offset are needed to support data accesses to this cache? Show all your work clearly.