BLG 322E Computer Architecture
Spring 2025

Instructor: Assistant Prof. Ayse Yilmazer, Office: BBB 224, yilmazerayse@itu.edu.tr

Course meeting times: Thursday 8:30 am - 11:20 am, at BBB Z-16

Office Hours: Thursday 11:30am-12:30pm or by appointment

Teaching Assistant:

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Prerequisites: BLG222E, Computer Organization with a grade of at least DD

Textbook and Other References:

- Computer Organization and Architecture, William Stallings, Prentice Hall, 2016. 10th ed.
- Computer Architecture, A Quantitative Approach, John L. Hennessy and David A. Patterson, Morgan Kaufmann, 2017. 6th ed.
- Motorola, MC68000 16/32-bit Microprocessor User's Manual

Course Description: Pipeline. Instruction-level parallelism. RISC pipeline. Input-output organization. Interrupts. Direct memory access (DMA). Memory hierarchy, cache memory, virtual memory. RAID: (Redundant Array of Independent/ Inexpensive Disks). Multiprocessor systems: Interconnection networks, cache coherence.

Grading (subject to change):

- 4 Homeworks (Take home exams) – Total 20% (each has 5%)
- Midterm exam & quizzes – Total 40% (30%+10%)
- Final exam – 40%

Eligibility to take the final exam:

Students must meet the following criteria to take the final exam:

- Attend at least 70% of the lectures throughout the semester
- Students must have a mid-semester average grade of at least 35/100.

The average mid-semester grade is computed using the formula below:

Avg. mid-semester grade = (0.20 × Homeworks + 0.4 × (Midterm exam & quizzes)*100/60

Any student who gets a grade lower than the required grade on any of these assessments will fail the course with a grade of VF and not be allowed to take the final exam.

Course Material and Announcements: Students are expected to check the Ninova web site and their ITU e-mail for homeworks and announcements.

In addition, they are responsible for all announcements that may be made on the course web site and in class.

Tentative Schedule:

- Introduction: layered logical model of a computer system, CPU, CPU performance, computer evolution, binary prefixes
- Pipeline: general structure, space-time diagram, throughput, speedup, instruction pipeline (**(HW1)**
- Pipeline: instruction pipeline, hazards (conflicts) and solutions, dealing with branches (branch prediction) (Recitation if time allows) **(Short Exam/Quiz)**
- Pipeline: hazards, dealing with branches (branch prediction)
- Pipeline: hazards, dealing with branches (branch prediction) (Recitation)
- I/O organization & bus operations: CPU-I/O interface, data transfer modes, 68000 bus operations **((HW2)**
- Interrupts: Systems, vector address, priority interrupt hardware, processing, exceptions (Recitation)
- Direct Memory Access (DMA): overview, controllers, transfer modes, 3-wire DMA, I/O processor **(HW3)**
- (Recitation) & **Midterm Exam**
- Memory organization (internal/external): memory hierarchy, memory gap, cache memory **(HW4)**
- Memory organization: cache memory (Recitation if time allows)
- External memory: magnetic disk, RAID, error detection/correction in memories
- Multi-proc./core/computer: shared memory, dist. systems, cache coherence **(Short Exam/Quiz)**
- Multi-proc./core/computer: cache coherence (Recitation)

Academic honesty:

You are expected to read the Undergraduate Education Regulations (http://www.sis.itu.edu.tr/tr/yonetmelik/lisansyonetmelik.html) and ITU Academic Honesty.

Pledge (http://www.sis.itu.edu.tr/tr/yonetmelik/AkademikOnurSozuEsaslar.html) and behave accordingly.

Cheating on the exams or on homework will be punished in the most severe manner, and Disciplinary regulations of The Council of Higher Education and of the university are applied.

Every piece of work that you turn in with your name on it must be yours and yours alone. No collaboration is allowed on any test or homework. You must not turn in work that is not yours.

Disclaimer:

The instructor reserves to right to make changes to the syllabus, including due dates and topics to be covered. Important changes will be announced as early as possible.