Lab 4: Synchronous Sequential Circuits

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Part Ia

2. Export the subcircuit schematic as an image and include it in your report.

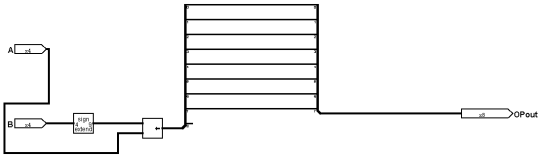

Figure 1: A schematic of op5.

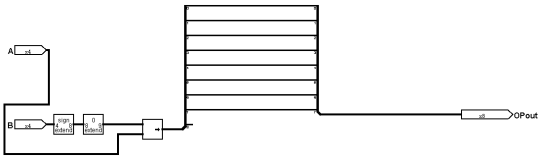

Figure 2: A schematic of op6.

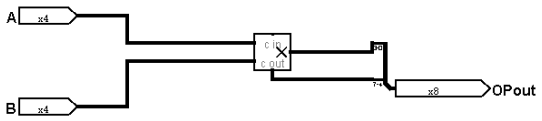

Figure 3: A schematic of op7.

3. Include a screenshot of your simulated test vectors for op5, op6, and op7.

Part Ib

3. Include a screenshot of your simulated timing diagram demonstrating ALUreg starting at 0x0 and increasing by 1 until 0x0f.
4. Include a screenshot of your simulated timing diagram demonstrating a shifting operation where ALUreg goes from at 0x01 and doubling until 0x00.

Part II

2. Export the subcircuit schematic as an image and include it in your report.
3. Include a screenshot of your simulated timing diagram demonstrating that the output can take on values from either input.

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	1011	1111 0110
pass	0011	1011	1101 1000
pass	0100	1011	1011 0000
pass	0101	1011	0110 0000
pass	1000	1011	0000 0000
pass	1011	1011	0000 0000
pass	1111	1011	0000 0000
pass	0001	0111	0000 1110
pass	0011	0111	0011 1000
pass	0100	0111	0111 0000
pass	0101	0111	1110 0000
pass	1000	0111	0000 0000
pass	1011	0111	0000 0000
pass	1111	0111	0000 0000

Figure 4: A simulation of op5.

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	1011	0111 1101
pass	0011	1011	0001 1111
pass	0100	1011	0000 1111
pass	0101	1011	0000 0111
pass	1000	1011	0000 0000
pass	1011	1011	0000 0000
pass	1111	1011	0000 0000
pass	0000	0111	0000 0111
pass	0001	0111	0000 0011
pass	0010	0111	0000 0001
pass	0011	0111	0000 0000
pass	0100	0111	0000 0000
pass	0101	0111	0000 0000
pass	1000	0111	0000 0000
pass	1011	0111	0000 0000
pass	1111	0111	0000 0000

Figure 5: A simulation of op6.

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0000	1111	0000 0000
pass	0000	1011	0000 0000
pass	0000	0010	0000 0000
pass	0001	1001	0000 1001
pass	0001	0101	0000 0101
pass	0110	1011	0100 0010
pass	1010	0010	0001 0100
pass	1001	1101	0111 0101
pass	0101	1110	0100 0110
pass	1111	1111	1110 0001

Figure 6: A simulation of op7.

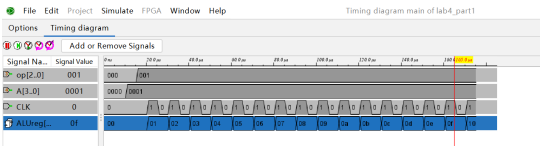

Figure 7: A timing simulation demonstrating incrementing.

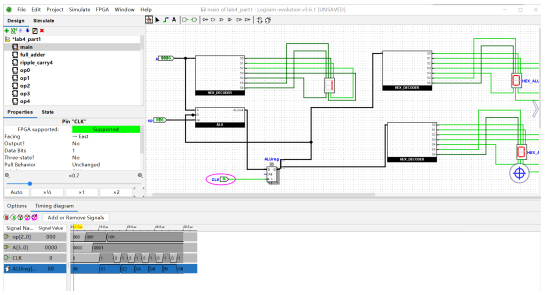

Figure 8: A timing simulation demonstrating doubling.

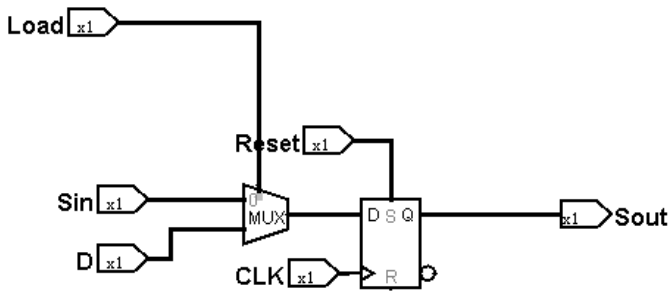

Figure 9: A schematic of the shifter_bit.

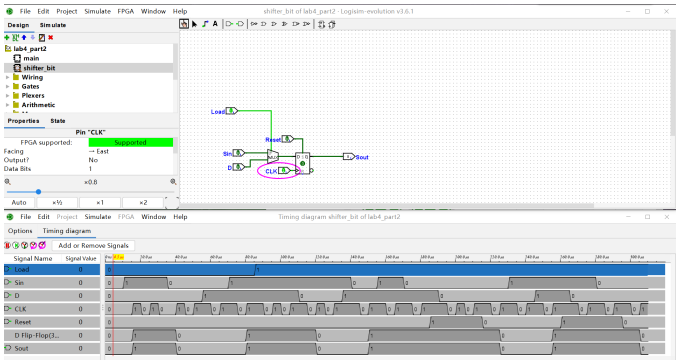

Figure 10: A timing simulation of the shifter_bit.