# Lab 6: Finite State Machines

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November 1, 2022

## 1 Part I

1. Complete Table 1 below.

Table 1: State Encodings

| State | Encoding |
|---|---|
| A | 0000001 |
| B | 0000010 |
| C | 0000100 |
| D | 0001000 |
| E | 0010000 |
| F | 0100000 |
| G | 1000000 |

2. Complete Table 2 below.

Table 2: Encoded State Transition Table for Robo-Snail II

| Current State | W | Next State |
|---|---|---|
| 0000001 | 0 | 0000001 |
| 0000001 | 1 | 0000010 |
| 0000010 | 0 | 0000001 |
| 0000010 | 1 | 0000100 |
| 0000100 | 0 | 0010000 |
| 0000100 | 1 | 0001000 |
| 0001000 | 0 | 0010000 |
| 0001000 | 1 | 0100000 |
| 0010000 | 0 | 0000001 |
| 0010000 | 1 | 1000000 |
| 0100000 | 0 | 0010000 |
| 0100000 | 1 | 0100000 |
| 1000000 | 0 | 0000001 |
| 1000000 | 1 | 0000100 |

3. Derive equations for each of your next state outputs below.

$$
\begin{aligned}
S_0' &= S_0\bar{W} + S_1\bar{W} + S_4\bar{W} + S_6\bar{W} \\
S_1' &= S_0W \\
S_2' &= S_1W + S_6W \\
S_3' &= S_2W \\
S_4' &= S_2\bar{W} + S_3\bar{W} + S_5\bar{W} \\
S_5' &= S_3W + S_5W \\
S_6' &= S_4W
\end{aligned}
$$

4. Export the subcircuit schematic as an image and include it in your report.

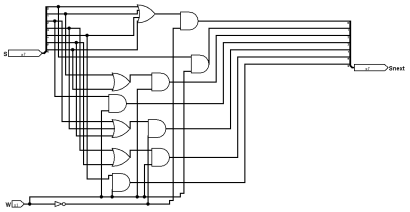

Figure 1: A schematic of Part I's next_state.

5. Complete Table 3 below.

Table 3: Encoded Output Table for Robo-Snail II

| State | Output |
|---|---|
| 0000001 | 0 |
| 0000010 | 0 |
| 0000100 | 0 |
| 0001000 | 0 |
| 0010000 | 0 |
| 0100000 | 1 |
| 1000000 | 1 |

6. Derive the equation for your output logic below.

$$Z = S_5 + S_6$$

7. Export the subcircuit schematic as an image and include it in your report.

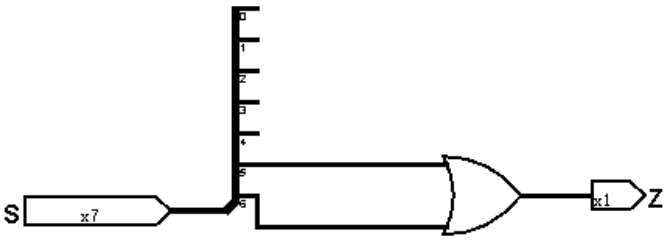


Figure 2: A schematic of Part I's output_logic.

# 2 Part II

1. Complete Table 4 below.

Table 4: Encoded State Transition Table for Part II

| Current State | Next State |
|---|---|
| 0000 | 0001 |
| 0001 | 0010 |
| 0010 | 0011 |
| 0011 | 0100 |
| 0100 | 0000 |

2. Complete Table 5 below.

Table 5: Output Table for Part II

| S | ALUSelB | ALUop | LoadC | LoadALUout | LoadA | LoadB | LoadR |
|---|---|---|---|---|---|---|---|
| 0000 | 00 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0001 | 00 | 0 | 0 | 0 | 1 | 0 | 0 |
| 0010 | 00 | 1 | 0 | 1 | 1 | 0 | 0 |
| 0011 | 10 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0100 | 01 | 0 | 0 | 0 | 0 | 0 | 1 |

3. Draw the state transition diagram and include it in Figure 3.

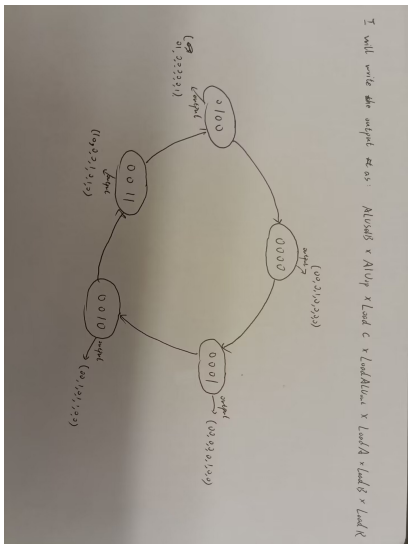


Figure 3: The state transition diagram for Part II

4. Describe how each state controls the datapath from Part II in Table 6.

Table 6: A description of how a state controls the datapath

| State | Description |
|---|---|
| 0000 | Load the value of Input(C) to RegC |
| 0001 | Load the value of Input(A) to RegA |
| 0010 | RegA and RegA are two operands and the operation of ALU is *, and then the output ($A^2$) is loaded in RegA |
| 0011 | RegA and RegC are two operands and the operation of ALU is +, and then the output ($A^2 + C$) is loaded in RegB |
| 0100 | RegA and RegB are two operands and the operation of ALU is +, and then the output ($2A^2 + C$) is loaded in RegR |

5. Export the timing diagram as an image and include it in your report.

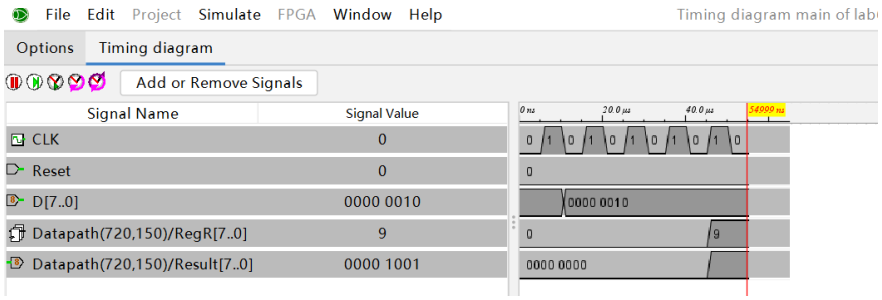


Figure 4: A timing simulation of the main schematic in Part II.