Lab 3: The Arithmetic Logic Unit

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October 10, 2022

Part I

2. Export the subcircuit schematic as an image and include it in your report.

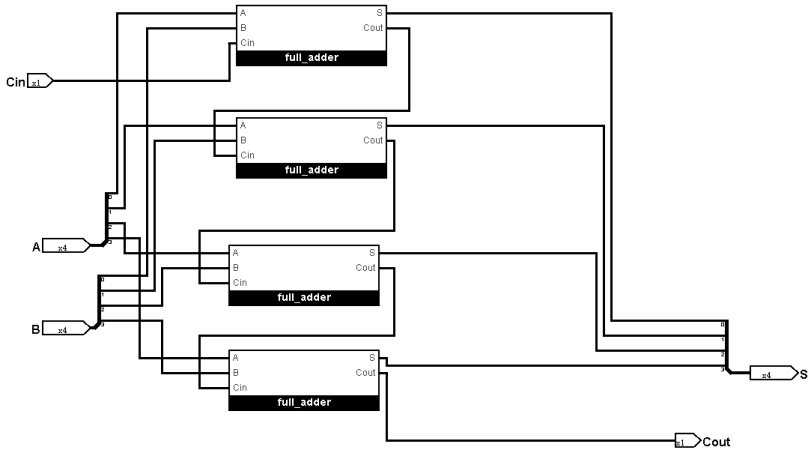

Figure 1: A schematic of ripple_carry4.

3. Include a screenshot of your simulated test vector for the 4-bit Ripple Carry Adder.

Passed: 14 Failed: 0

Status	Cin	A	B	S	Cout
pass	0	0000	0000	0000	0
pass	0	0000	0001	0001	0
pass	0	0001	0001	0010	0
pass	0	0010	0010	0100	0
pass	0	0100	0100	1000	0
pass	0	1000	1000	0000	1
pass	0	1111	1111	1110	1
pass	1	0000	0000	0001	0
pass	1	0000	0001	0010	0
pass	1	0001	0001	0011	0
pass	1	0010	0010	0101	0
pass	1	0100	0100	1001	0
pass	1	1000	1000	0001	1
pass	1	1111	1111	1111	1

Figure 2: A simulation ripple_carry4.

Part II

1. Export the subcircuit schematic of each operation as an image and include it in your report.

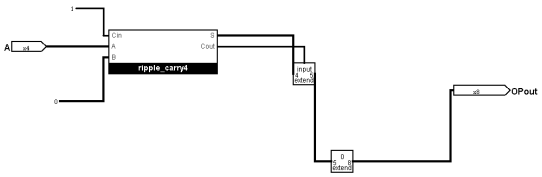

Figure 3: A schematic of op0.

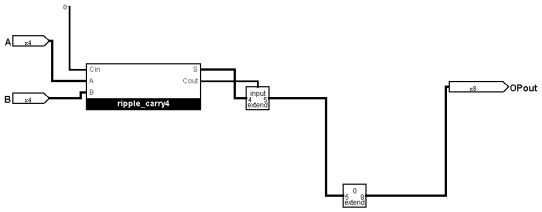

Figure 4: A schematic of op1.

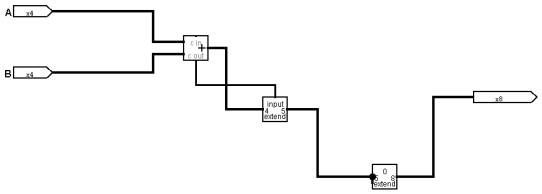

Figure 5: A schematic of op2.

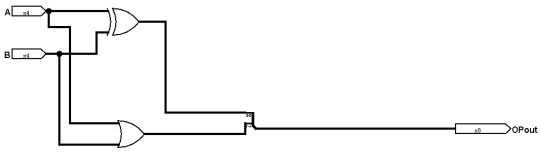

Figure 6: A schematic of op3.

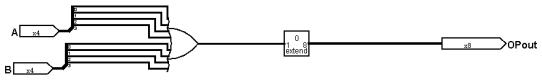

Figure 7: A schematic of op4.

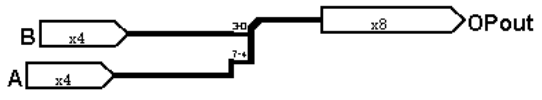

Figure 8: A schematic of op5.

2. Include a screenshot of your simulated test vectors for op3, op4, and op5.
3. Export the ALU schematic as an image and include it in your report.

Passed: 13 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	0000	0001 0001
pass	0001	0001	0001 0000
pass	0000	0001	0001 0001
pass	0010	0000	0010 0010
pass	0000	0010	0010 0010
pass	0010	0010	0010 0000
pass	0100	0000	0100 0100
pass	0000	0100	0100 0100
pass	0100	0100	0100 0000
pass	1000	0000	1000 1000
pass	0000	1000	1000 1000
pass	1000	1000	1000 0000

Figure 9: A simulation of op3.

Passed: 13 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	0000	0000 0001
pass	0000	0001	0000 0001
pass	0001	0001	0000 0001
pass	0010	0010	0000 0001
pass	0010	0000	0000 0001
pass	0000	0010	0000 0001
pass	0100	0000	0000 0001
pass	0000	0100	0000 0001
pass	0100	0100	0000 0001
pass	1000	0000	0000 0001
pass	0000	1000	0000 0001
pass	1000	1000	0000 0001

Figure 10: A simulation of op4.

Passed: 9 Failed: 0

Status	A	B	OPout
pass	0000	0000	0000 0000
pass	0001	0000	0001 0000
pass	0010	0000	0010 0000
pass	0100	0000	0100 0000
pass	1000	0000	1000 0000
pass	0000	0001	0000 0001
pass	0000	0010	0000 0010
pass	0000	0100	0000 0100
pass	0000	1000	0000 1000

Figure 11: A simulation of op5.

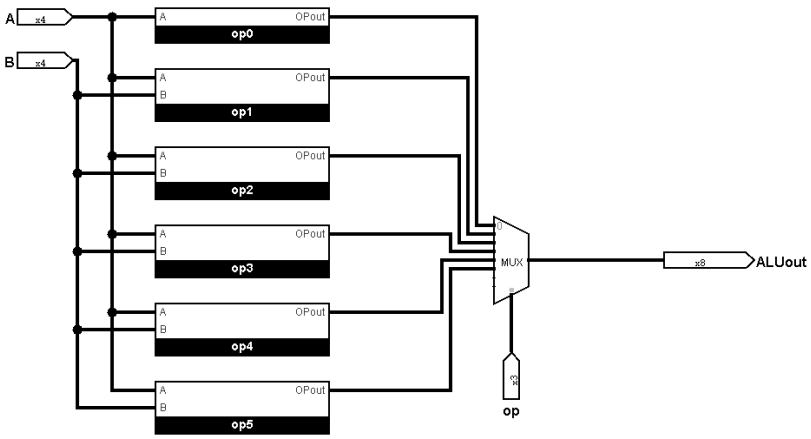

Figure 12: A schematic of the ALU.