

Final Projects

2023

Project 1 : Implement CNN on FPGA

1. Description

Research simple Neural network in image processing, recognize handwritten digits by using Verilog language and upload design to FPGA kit.

2. References and Documents

- Paper : [FPGA Implementation of Convolutional Neural Networks with Fixed-Point Calculations](#)
- Source code : [Verilog Generator of Neural Net Digit Detector for FPGA](#)

3. Requirements

1. Learn about CNN theory, simulate, evaluate design results when implementing on software (Python)
2. Design, verify modules when switching to Verilog code.
3. Implement your design on hardware: FPGA kit, camera, monitor.

Project 2 : Design I2C controller core

1. Description

I2C protocol was invented by Philips semiconductors in the 1980s, to provide easy onboard communications between a CPU and various peripheral chips. I2C stands for Inter-Integrated Circuit. It is used for attaching lower-speed peripheral ICs to microcontrollers in short-distance communication. Low-speed peripherals include external EEPROMs, digital sensors, I2C LCD, and temperature sensors.

Design I2C Master Core: provides an interface between a Wishbone Master and an I2C bus, compatible with Philips I2C bus standard and Wishbone bus.

2. References and Documents

- [I2C Bus Specification, Philips Semiconductor, version 2.1, January 2000](#)
- Paper : [Implementation of I2C master bus controller on FPGA](#)
- Source code : [I2C controller core](#)

3. Requirements

1. Build Specification of the design based on the documentations provided: I2C bus standard, Wishbone bus.
 - ⇒ System modeling / design by using diagram, FSM, ASM, FSMD, ASMD,...
 - ⇒ Describe the input / output signals of each module / block.
2. Design I2C Master Core: provides an interface between a Wishbone Master and an I2C bus.
 - ⇒ Compatible with Philips I2C bus standard.
 - ⇒ Compatible with Wishbone bus.
3. Verify your design.
4. Evaluate the results of the device when deployed on FPGA: by simulation, FPGA board, evaluate resource consumption.

Project 3 : Design FFT/IFFT 128 points IP core

1. Description

FFT is an algorithm for the effective Discrete Fourier Transform calculation.

2. References and Documentations

- [Pipelined FFT/IFFT 128 points \(Fast Fourier Transform\) IP Core User Manual](#)
- Source code : [Pipelined FFT/IFFT 128 points processor](#)

3. Requirements

1. Build Specification of the design
 - System modeling / design by using diagram, FSM, ASM, FSMD, ASMD,...
 - Describe the input / output signals of each module / block.
2. Implement Algorithm on C++ / Python
3. Verify your RTL design.
4. Evaluate the results of the device when deployed on FPGA: by simulation, FPGA board, evaluate resource consumption.

Project 4 : Design a RISC Stored-Program Machine

1. Description

Reduced instruction-set computers (RISC) are designed to have a small set of instructions that execute in short clock cycles, with a small number of cycles per instruction. RISC machines are optimized to achieve efficient pipelining of their instruction streams. The machine also serves as a starting point for developing architectural variants and a more robust instruction set. Designers make high-level tradeoffs in selecting an architecture that serves an application. Once an architecture has been selected, a circuit that has sufficient performance (speed) must be synthesized. Hardware description languages (HDLs) play a key role in this process by modeling the system and serving as a descriptive medium that can be used by a synthesis tool.

2. References and Documents

- Book : Advanced Digital Design with Verilog HDL - Chapter 7. Design and Synthesis of Datapath Controller - Section 7.3 Design and Synthesis of a RISC Stored Program Machine (Page 355)
- Source code : in the book

3. Requirements

1. Implement the design according to the instructions in the document.
2. Build Specification of the design based on the documentations provided.
 - System modeling/design by diagram, FSM, ASM, ASMD, FSMD,...
 - Describe the input/output signals of each module.
3. Verify your design.
4. Evaluate the results of the device when deployed on FPGA: by simulation, FPGA kit, evaluate resource consumption.

Project 5 : Implement a UART modem

1. Description

UART, or Universal Asynchronous Receiver-Transmitter is a computer hardware device for asynchronous serial communication capable of both receive and transmit data.

2. References and Documents

- Book : Advanced Digital Design with Verilog HDL - Chapter 7. Design and Synthesis of Datapath Controller - Section 7.4 Design Example: UART (Page 378)
- Source code : in the book

3. Requirements

1. Modeling both UART's receiver and transmitter, follow the instructions in the document
2. Build Specification of the design based on the documentations provided.
 - System modeling/design by diagram, FSM, ASM, ASMD, FSMD,...
 - Describe the input/output signals of each module.
3. Verify your design.
4. Evaluate the results of the device when deployed on FPGA: by simulation, FPGA kit, evaluate resource consumption.