Assignment 9

November 13, 2023

For each group, design the givin module, write testbench, and simulate your design.
The group leaders need to upload the report and/or slide to Teams folder. Each group will be presenting infront of the class in the upcoming lessons.

1. 4.3.1 Shift register (Free-running shift register - Universal shift register) (Group 9, 10, 11)
2. 4.3.2 Binary counter and variant (Free-running binary counter - Universal binary counter - Mod-m counter)(Group 12, 13, 14)
3. 4.4 Testbench for Sequential Circuit(Group 15, 16)
4. 4.5.1 LED time-multiplexing circuit (Time multiplexing with LED patterns)(Group 1, 2)
5. 4.5.1 LED time-multiplexing circuit (Time multiplexing with hexadecimal digits)(Group 3, 4, 17)
6. 4.5.2 Stopwatch (Group 5, 6)
7. 4.5.3 FIFO Buffer (Group 7, 8)

NOTE : FPGA PROTOTYPING BY VERILOG EXAMPLES - Chapter 4 Regular Sequential Circuit - Section 4.3 Simple Design Examples - Page 91