Assignment 8

November 6, 2023

Problem 1 : For each student

1. Compare blocking and nonblocking assignments.
2. How to use case, casex, casez in Behavioral model.
3. Describe sequential circuit with mixed blocking and nonblocking assignments

NOTE : FPGA PROTOTYPING BY VERILOG EXAMPLES - Section 7.1.4 - Page 180

Problem 2 : For each group

Design the givin module, write testbench, and simulate your design.
The group leaders need to upload the report to Teams folder. Each group will be presenting infront of the class in the next lessons.
Besides well understand your own topic, every team members should also need to understand others group's topic.

1. Example 3.9.1 Hexadecimal digit to seven-segment LED decoder (Group 1, 2, 3, 4)
2. Example 3.9.2 Sign - magnitude adder (Group 5, 6, 7, 8)
3. Example 3.9.3 Barrel shifter (Group 9, 10, 11, 12)
4. Example 3.9.4 Simplified floating - point adder (Group 13, 14, 15, 16)

NOTE : FPGA PROTOTYPING BY VERILOG EXAMPLES - Section 3.9 - Page 67