

## Assignment 3 : Structural Model

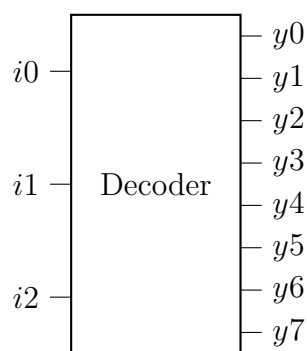
October 2, 2023

### Problem 1 : Write testbench for all problems in Assignment 2

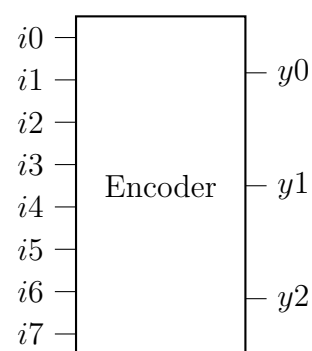
1. Problem 1
2. 4-to-1 Multiplexer
3. Half Adder
4. Full Adder
5. 4-bit Ripple Carry Full Adder

### Problem 2 : 8-to-3 Encoder and 3-to-8 Decoder

1. Construct truth table.
2. Determine output function.
3. Write Verilog code and testbench for that circuit.



(a) 3-to-8 Decoder



(b) 8-to-3 Encoder

Figure 1: Encoder and Decoder

**Problem 3 : Flip-flops : D-FF, T-FF, JK-FF, SR-FF**

1. Construct truth table.
2. Determine output function.
3. Write Verilog code and testbench for that circuit.

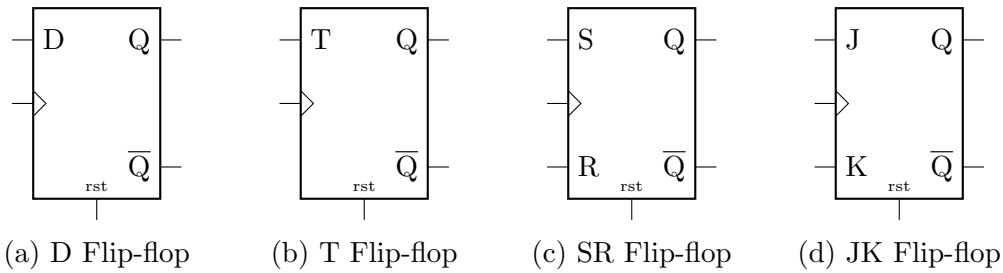


Figure 2: Flip-flops

*NOTE : Using structural model. Flip flops include reset signal.*