Assignment 2 Solution

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Problem 1

$F(A, B, C, D) = \sum m(0, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15)$

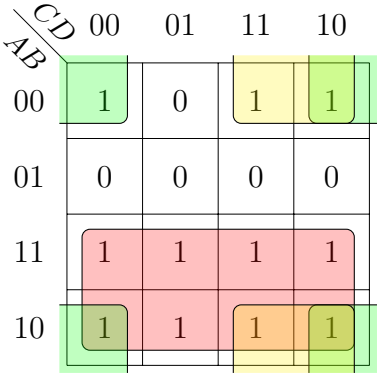

Figure 1: Karnaugh map

$\Rightarrow F = A + B'D' + B'C$

A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 1: Truth Table

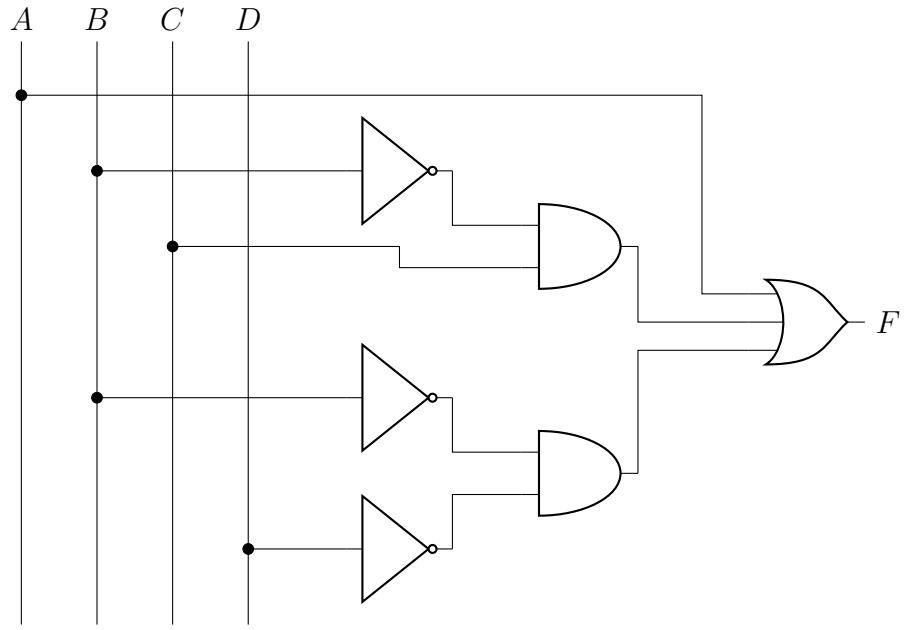

Figure 2: Circuit

```
import numpy as np

def incmatrix(genl1,genl2):
    m = len(genl1)
    n = len(genl2)
    M = None #to become the incidence matrix
    VT = np.zeros((n*m,1), int)  #dummy variable
```

```
#compute the bitwise xor matrix
M1 = bitxormatrix(genl1)
M2 = np.triu(bitxormatrix(genl2),1)

for i in range(m-1):
    for j in range(i+1, m):
        [r,c] = np.where(M2 == M1[i,j])
        for k in range(len(r)):
            VT[(i)*n + r[k]] = 1;
            VT[(i)*n + c[k]] = 1;
            VT[(j)*n + r[k]] = 1;
            VT[(j)*n + c[k]] = 1;

            if M is None:
                M = np.copy(VT)
            else:
                M = np.concatenate((M, VT), 1)

            VT = np.zeros((n*m,1), int)

return M
```

Promblem 2 : Design a 4-to-1 Multiplexer

1. Construct truth table.
2. Determine output function.
3. Draw the circuit.
4. Design a *Structural module* for this circuit (Using Verilog)

Promblem 3 : Adder Circuit

For each of the following circuit, Construct truth table, Determine the output function and Write Verilog code

1. Half Adder
2. Full Adder
3. Ripple Carry 4-bit Adder
4. Ripple Carry 16-bit Adder