Assignment 9

November 13, 2023

For each group: Simulate your designs on ModelSim. Create code coverage report, and waveform. Implement the content in section r 4 Regular Sequential Circuit, FPGA Prototyping by Verilog.

1. 4.3.1 Shift register (Free-running shift register - Universal shift register) (Group 1, 2, 3)
2. 4.3.2 Binary counter and variant (Free-running binary counter - Universal binary counter - Mod-m counter)(Group 4, 5, 6)
3. 4.4 Testbench for Sequential Circuit(Group 7, 8)
4. 4.5.1 LED time-multiplexing circuit (Time multiplexing with LED patterns)(Group 9, 10)
5. 4.5.1 LED time-multiplexing circuit (Time multiplexing with hexadecimal digits)(Group 11, 12)
6. 4.5.2 Stopwatch (Group 13, 14)
7. 4.5.3 FIFO Buffer (Group 15, 16)

The group leaders need to upload the report to Teams folder, the next lesson will be presented. In addition to delving into your topic, the team members also need to understand the others.