Assignment 3 : Structural Model

Ngo Van Canh

October 8, 2023

Problem 1 : Write testbench for all problems in Assignment 2

1. Problem 1

```
module Problem1_tb;
reg[0:4] I;
wire F;
// instantiate the design block
Problem1 p1(F, I[0], I[1], I[2], I[3]);
initial begin
    I=0;
    for(I=0; I<16; I=I+1) #5;
end

endmodule
```

Listing 1: Problem 1 testbench

2. 4-to-1 Multiplexer

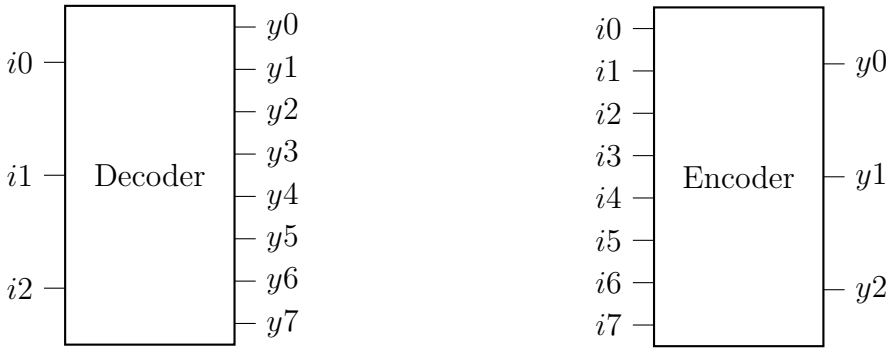
3. Hald Adder

4. Full Adder

5. 4-bit Ripple Carry Adder

Problem 2 : 8-to-3 Encoder and 3-to-8 Decoder

1. Construct truth table.
2. Determine output function.
3. Write Verilog code and testbench for that circuit.

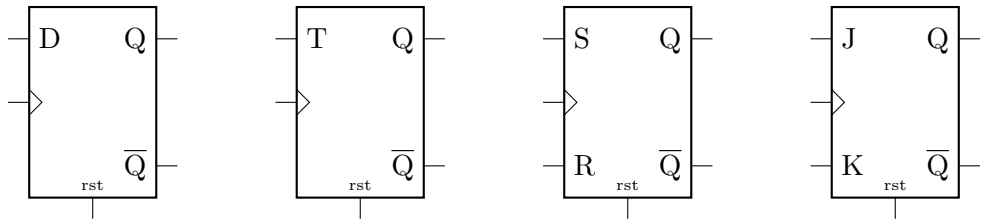


(a) 3-to-8 Decoder (b) 8-to-3 Encoder

Figure 1: Encoder and Decoder

Problem 3 : Flip-flops : D-FF, T-FF, JK-FF, SR-FF

1. Construct truth table.
2. Determine output function.
3. Write Verilog code and testbench for that circuit.



(a) D Flip-flop (b) T Flip-flop (c) SR Flip-flop (d) JK Flip-flop

Figure 2: Flip-flops

NOTE : Using structural model. Flip flops include reset signal.