Assignment 2 Solution

Ngo Van Canh

1 Oct 2023

Problem 1 :

$F(A, B, C, D) = \sum m(0, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15)$

	A	B	C	D	F
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	1
11	1	0	1	1	1
12	1	1	0	0	1
13	1	1	0	1	1
14	1	1	1	0	1
15	1	1	1	1	1

Table 1: Truth Table

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

(a) Layout

AB \ CD	00	01	11	10
00	1	0	1	1
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

(b) Prime implicant

Figure 1: Karnaugh-map

$\Rightarrow F = A + B'D' + B'C$

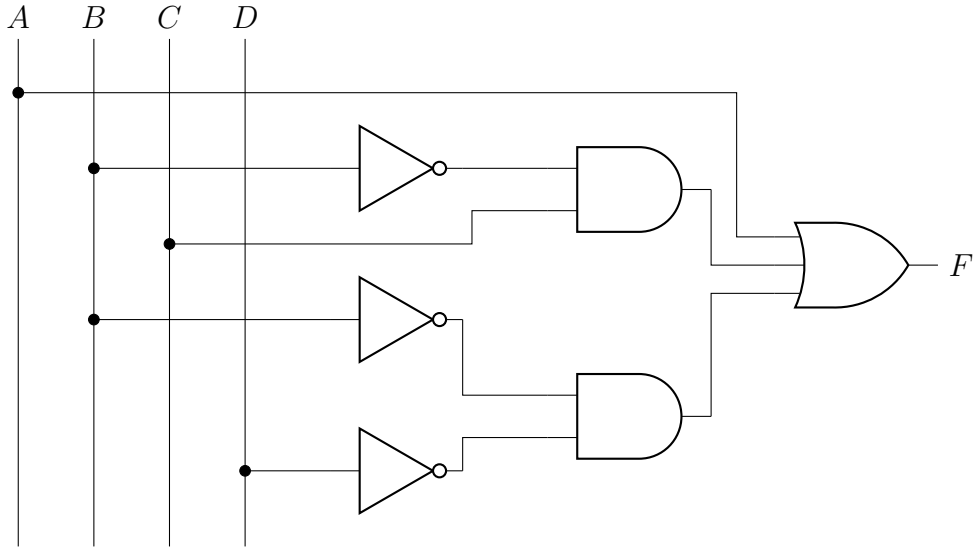

Figure 2: Circuit

```
1  module Problem1(F,A,B,C,D);
2  input A,B,C,D;
3  output F;
4  wire S1,S2,S3,S4;
5  not N1(S1,B);
6  not N2(S2,D);
7  and A1(S3,S1,C);
8  and A2(S4,S1,S2);
9  or O1(F,A,S3,S4);
10 endmodule
```

Listing 1: Verilog code for Problem 1

Problem 2 : Design a 4-to-1 Multiplexer

$s0$	$s1$	F
0	0	$i0$
0	1	$i1$
1	0	$i2$
1	1	$i3$

Table 2: Truth Table for a 4-to-1 Multiplexer

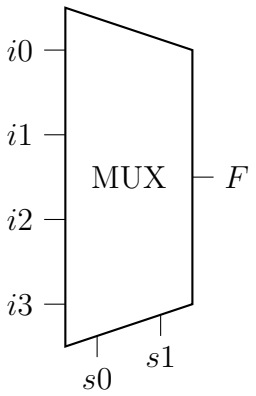

Figure 3: 4-to-1 Multiplexer

$$\Rightarrow F = s0's1'i0 + s0s1'i1 + s0's1i2 + s0s1i3$$

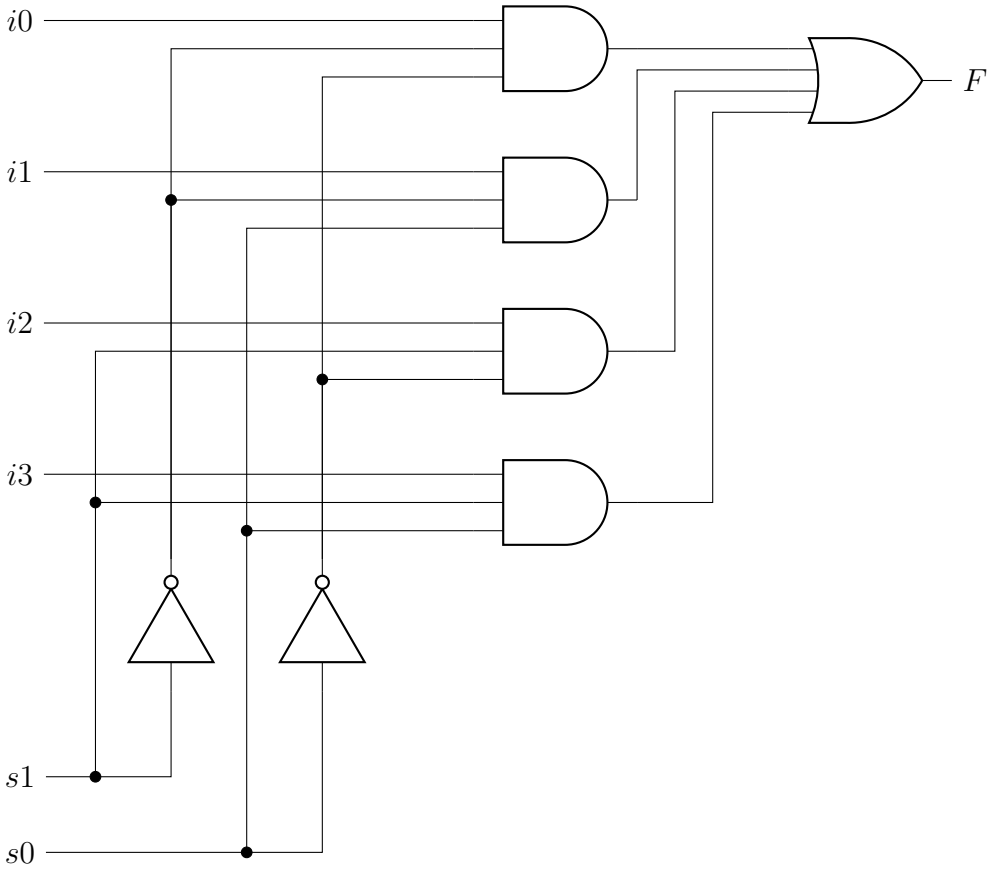

Figure 4: 4-to-1 Multiplexer Circuit

```
1  module mux4_to_1 (F, i0, i1, i2, i3, s1, s0);
2  output F;
3  input i0, i1, i2, i3, s1, s0;
4  wire s1n, s0n;
5  wire y0, y1, y2, y3;
6  not (s1n, s1);
7  not (s0n, s0);
8  and (y0, i0, s1n, s0n);
9  and (y1, i1, s1n, s0);
10 and (y2, i2, s1, s0n);
11 and (y3, i3, s1, s0);
12 or (F, y0, y1, y2, y3);
13 endmodule
```

Listing 2: Verilog code for 4-to-1 Multiplexer

Problem 3 : Adder Circuit

1.Half Adder

X	Y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 3: Truth Table for Half Adder

$$\Rightarrow \begin{cases} S = X'Y + XY' = X \oplus Y \\ C = XY \end{cases}$$

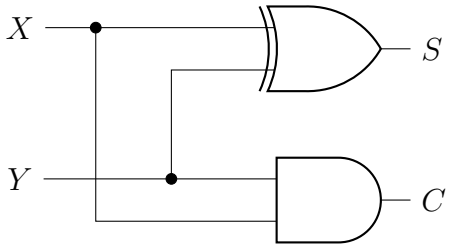

Figure 5: Half Adder Circuit

```
1 module half_adder (X, Y, S, C);
2 input X, Y;
3 output S, C;
4 xor Xor (S, X, Y);
5 and And (C, X, Y);
6 endmodule
```

Listing 3: Verilog code for Half Adder

2.Full Adder

X	Y	Ci	S	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 4: Truth Table for Full Adder

(a) $S = Ci \oplus X \oplus Y$ (b) $Co = XY + YCi + XCi$

Figure 6: Karnaugh-map Full Adder

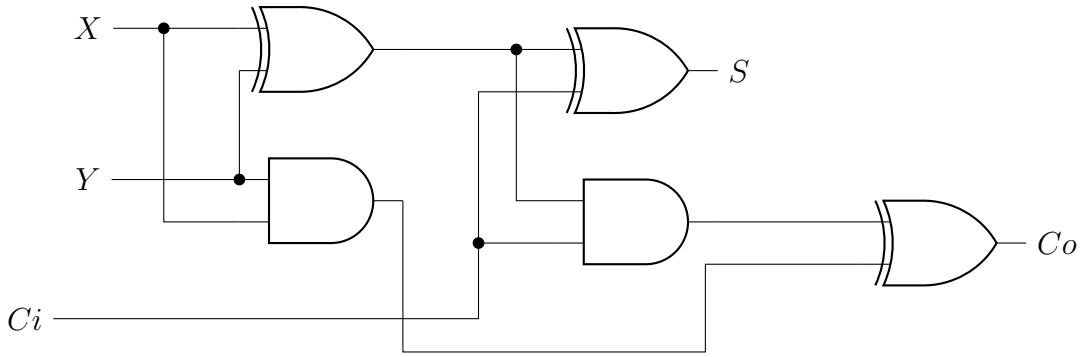

Figure 7: Full Adder Circuit

```
1  module full_adder (X, Y, Ci, S, Co);
2  input X, Y, Ci;
3  output S, Co;
4  wire w1, w2, w3
5  xor (w1, X, Y);
6  and (w1, X, Y);
7  xor (S,  w1, Ci);
8  and (w3, w1, Ci);
9  xor (Co, w3, w2);
10 endmodule
```

Listing 4: Verilog code for Full Adder

3.Ripple Carry 4-bit Adder

```
1  module Ripple_Carry_Adder(X, Y, Ci, S, Co);
2  output [3:0] S;
3  output Co;
4  input[3:0] X, Y;
5  input Ci;
6  wire w1, w2, w3;
7  full_adder fa0(S[0], w1, X[0], Y[0], Ci);
8  full_adder fa1(S[1], w2, X[1], Y[1], w1);
9  full_adder fa2(S[2], w3, X[2], Y[2], w2);
10 full_adder fa3(S[3], Co, X[3], Y[3], w3);
11 endmodule
```

Listing 5: Verilog code for Ripple Carry Adder

4.Ripple Carry 6-bit Adder

Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Etiam lobortis facilisis sem. Nullam nec mi et neque pharetra sollicitudin. Praesent imperdiet mi nec ante. Donec ullamcorper, felis non sodales commodo, lectus velit ultrices augue, a dignissim nibh lectus placerat pede. Vivamus nunc nunc, molestie ut, ultricies vel, semper in, velit. Ut porttitor. Praesent in sapien. Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Duis fringilla tristique neque. Sed interdum libero ut metus. Pellentesque placerat. Nam rutrum augue a leo. Morbi sed elit sit amet ante lobortis sollicitudin. Praesent blandit blandit mauris. Praesent lectus tellus, aliquet aliquam, luctus a, egestas a, turpis. Mauris lacinia lorem sit amet ipsum. Nunc quis urna dictum turpis accumsan semper. Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Etiam lobortis facilisis sem. Nullam nec mi et neque pharetra sollicitudin. Praesent imperdiet mi nec ante. Donec ullamcorper, felis non sodales commodo, lectus velit ultrices augue, a dignissim nibh lectus placerat pede. Vivamus nunc nunc, molestie ut, ultricies vel, semper in, velit. Ut porttitor. Praesent in sapien. Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Duis fringilla tristique neque. Sed interdum libero ut metus. Pellentesque placerat. Nam rutrum augue a leo. Morbi sed elit sit amet ante lobortis sollicitudin. Praesent blandit blandit mauris. Praesent lectus tellus, aliquet aliquam, luctus a, egestas a, turpis. Mauris lacinia lorem sit amet ipsum. Nunc quis urna dictum turpis accumsan semper. Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Etiam lobortis facilisis sem. Nullam nec mi et neque pharetra sollicitudin. Praesent imperdiet mi nec ante. Donec ullamcorper, felis non sodales commodo, lectus velit ultrices augue, a dignissim nibh lectus placerat pede. Vivamus nunc nunc, molestie ut, ultricies vel, semper in, velit. Ut porttitor. Praesent in sapien. Lorem ipsum dolor sit amet, consectetuer adipiscing elit. Duis fringilla tristique neque. Sed interdum libero ut metus. Pellentesque placerat. Nam rutrum augue a leo. Morbi sed elit sit amet ante lobortis sollicitudin. Praesent blandit blandit mauris. Praesent lectus tellus, aliquet aliquam, luctus a, egestas a, turpis. Mauris lacinia lorem sit amet ipsum. Nunc quis urna dictum turpis accumsan semper.