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NO EXERCISE SHEET TITLE SPECIFIED

Assignment 2

Problem 1

$F(A, B, C, D) = \sum m(0, 2, 3, 8, 9, 10, 11, 12, 13, 14, 15)$

1. Simplify F using Karnaugh Maps.

2. Construct truth table.

3. Draw the circuit.

4. Design a *Structural module* for this circuit (Using Verilog)

Promblem 2 : Design a 4-to-1 Multiplexer

1. Construct truth table.

2. Determine output function.

3. Draw the circuit.

4. Design a *Structural module* for this circuit (Using Verilog)

Promblem 3 : Adder Circuit

For each of the following circuit, Construct truth table, Determine the output function and Write Verilog code

1. Half Adder

2. Full Adder

3. Ripple Carry 4-bit Adder

4. Ripple Carry 16-bit Adder

Submitted by Student unknown *on* .