Assignment 4

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Problem 1 : 16-bit Carry Look Ahead Adder

Write code Verilog: Design code and testbench code
NOTE : A 16-bit Carry Look Ahead Adder can be formed by cascading four 4-bit Carry Look Ahead Adder

Problem 2 : 4-bit Ripple Carry Counter

Write Verilog code and testbench. Simulate your design.
NOTE : Using T - flipflop (structural model) you designed in Assignment 3.

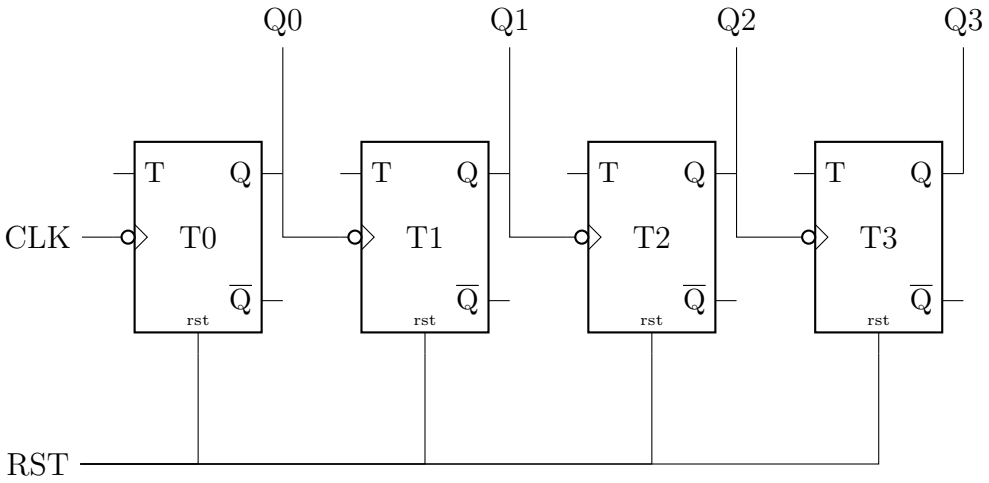


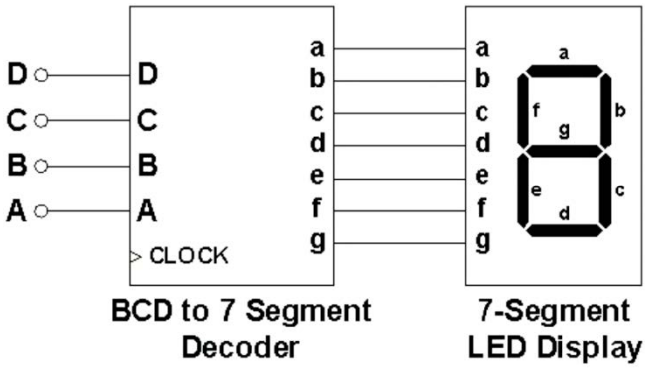
Figure 1: 4-bit Ripple Carry Counter

Problem 3 : 4-bit Gray Counter

Write code Verilog: Design code and simulation by testbench.
NOTE : Note: Using $display syntax and screenshot waveform.

Problem 4 : BCD to 7 Segment Display Decoder

Write code Verilog: Design code and simulation by testbench.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BCD to 7 Segment Decoder
7-Segment LED Display