A Novel High PSRR Bandgap Over a Wide Frequency Range

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Abstract

This paper describes a novel bandgap reference with high PSRR over a wide frequency range. The design utilizes an internally regulated supply voltage without high gain feedback loop. Thus improve PSRR even at high frequency. Additional transistors are added to further improve supply rejection and minimize the second order effect. The circuit is implemented in 0.25μm CMOS technology. It generates a reference voltage of 1.262V which has a voltage variation versus temperature of 0.1% from -20C to 90C. It has a PSRR of 85dB at 1kHz and still 64dB at 1MHz.

1. Introduction

Bandgap reference generators are widely used in precision analog design. They are required to be stabilized over process, supply voltage, and temperature variations, and also expected to be implemented with a simple process for economic reasons. Regarding modern SOC design, there is a growing trend of designing reference generators with a high power supply rejection ratio even at high frequency range to reject noise from high speed digital circuits.

Many papers can be found in bandgap reference design [3]-[6]. In such cases regulated supply voltage is often used to achieve a high PSRR. However, the design always trades off between power dissipation and silicon area. In the other hand it is the control loop in regulator that will degrades the high frequency PSRR because of the gain attenuation. In this paper a simple but efficient structure for better high frequency PSRR performance will be presented. It combines internally regulated supply voltage and bootstrapped techniques and achieves a PSRR of -64dB at 1MHz.

The paper is organized as follows: Section II discusses the basic operation of bandgap and the existing circuit topology for high PSRR design. In section III the proposed bandgap circuit is described. The simulation results will be presented in last section.

2. Existing High PSRR Techniques

In a bandgap circuit, the reference voltage is obtained by compensating the base-emitter voltage of bipolar transistor for its temperature dependence. As shown in Fig.1, a proportional-to-absolute-temperature (PTAT) current is generated by forcing node 1 to be at the same potential as node 2. This current can be written as:

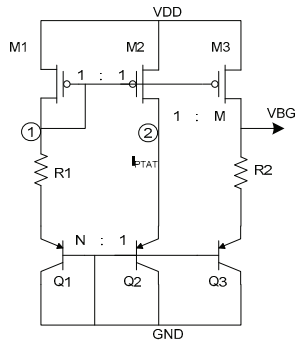

Figure 1. Bandgap core circuit

$$I_{PTAT} = \frac{kT}{q}\frac{1}{R1}\ln N \tag{1}$$

Thus the output reference voltage can be calculated as:

$$V_{BG} = V_{BE3} + M\frac{kT}{q}\frac{R2}{R1}\ln N \tag{2}$$

where N is the ratio of the emitter areas of bipolar transistors Q1 and Q2 and M is the geometric ratio of current mirror. At room temperature V_{BE} has a negative temperature coefficient of -2.0mv/ºC, whereas kT/q has positive temperature coefficient of about +0.086mv/ºC. By proper choice of R2/R1 and N, M value, temperature dependence of VBG can be compensated to be zero.

In many cases the power supply rejection can be improved by regulating the supply voltage of bandgap core circuit as presented in [4]. In the design an operational amplifier is configured as a regulator to generate a local supply, and greatly improve the low frequency PSRR. However, in applications silicon area and power dissipation is of concern this method runs in low efficiency. On the other hand, in order to meet the goals of requirements mentioned previously, an op amp-less bandgap reference is described in [5]. In this circuit an internal regulated supply is generated for bandgap core by using a high gain feedback loop. The higher of the loop gain, the higher supply rejection would the design be. However, with the loop gain reduces at high frequency, PSRR decreases also.

3. Proposed Structure

Our proposed structure starts with a simple V_T-referenced bias circuit [1]. As shown in Fig.2, the current mirror feedback loop forces M1 and M2 to operate at the same bias current, thus forcing node 1 and node 2 to be at the same potential. The supply voltage dependence of I_a can be calculated as follows:

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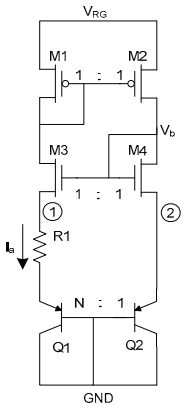

Figure 2: A simple V_T-referenced bias circuit

$$\frac{V_{RG}-V_b}{r_{o2}}+I_a\frac{g_{M2}}{g_{M1}}=\frac{V_b}{R_b}=I_b \tag{3}$$

$$R_a=R1+r_{be1} \qquad R_b=\frac{1}{g_{M4}}+r_{be2} \qquad g_{M1}=g_{M2} \tag{4}$$

$$I_a=G_{M3}V_b \qquad G_{M3}=\frac{g_{M3}}{1+g_{M3}R_a} \tag{5}$$

$$\frac{I_a}{V_{RG}}=\frac{G_{M3}R_b}{R_b+r_{o2}(1-G_{M3}R_b)} \tag{6}$$

where r_{o2} is output resistance of transistor M2, r_{be1} and r_{be2} is the emitter resistance of Q1 and Q2 respectively. From (6) it can easily be found that sensitivity of I_a to V_{RG} is inversely proportional to r_{o2} [2]. While in many cases cascoding is used to improve the value of r_{o2} but at the cost of consuming more voltage headroom and thus is not suitable for low voltage operation.

On the other hand, a voltage less sensitive to power supply is always desired as local supply voltage of bandgap core circuit for better PSRR. Such internally generated regulator can be implemented as shown in Fig.3. Cascoding is used here to improve the output impedance of current mirror. Only two overdrive voltages are consumed and thus the structure is well suited for low supply voltage applications. However, the error current produced by output resistance of M7 will be multiplied by g_m ratio from M9 to M12 and thus severely degrade the performance. By adding transistor M5 and M6 the performance can be drastically improved, as is our proposed structure also shown in Fig.3.

First, since the PTAT current I_a is first orderly determined by the emitter voltage difference of Q1 and Q2 and resistance value of R1, V_b is almost constant once transistor M4 is designed. The error current mentioned above will make drain source voltage difference between M1 and M2 so large that the design can be ruined. However, with M5 properly sized and sourced by a current mirrored from M1, V_{RG} can be fixed and thus minimize the second order effect.

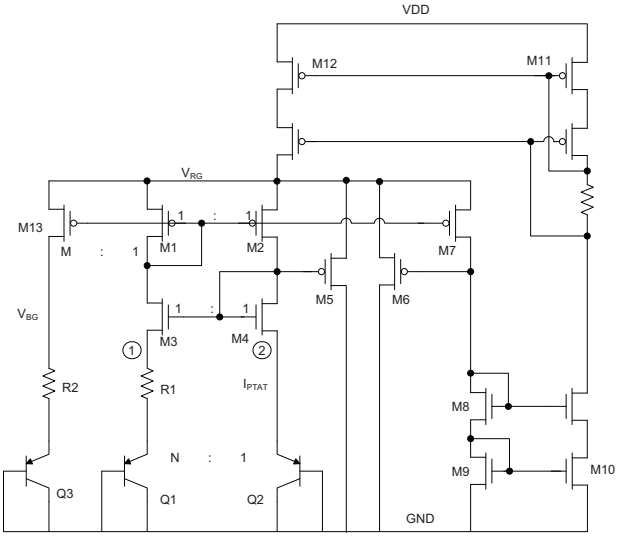

Figure 3: Proposed circuit structure

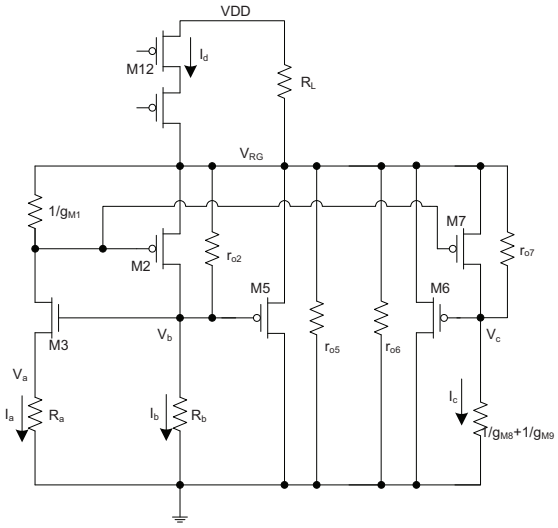

Figure 4: Simplified schematic of Fig.3 for ac analysis

Considering M6, we can draw a simplified schematic in Fig.4 for ac analysis. Neglecting VBG branch, we can write:

$$I_c=I_a\frac{g_{M7}}{g_{M1}}+\frac{V_{RG}-V_c}{r_{o7}}=\frac{g_{M8}g_{M9}V_c}{g_{M8}+g_{M9}} \tag{7}$$

For simplicity, assuming $g_{M1}=g_{M2}=g_{M5}=g_{M6}=g_{M7}$, $g_{M5}>>1/r_{o5}$, $g_{M6}>>1/r_{o6}$, current ratio of I_d to I_c is 5 and neglecting all error current produced by those cascode current mirrors:

$$I_d=5I_c \tag{8}$$

$$I_a+I_b+g_{M5}(V_{RG}-V_b)+g_{M6}(V_{RG}-V_c)+I_c=I_d+\frac{VDD-V_{RG}}{R_L} \tag{9}$$

Substitute (3), (7) and (8) to (9),

$$\frac{V_{RG}-V_b}{r_{o2}}+g_{M5}(V_{RG}-V_b)+g_{M6}(V_{RG}-V_c)-2I_a-\frac{4(V_{RG}-V_c)}{r_{o7}}=\frac{VDD-V_{RG}}{R_L} \quad (10)$$

Combining (10) with (3)-(7) and make assumption of $2g_{M5}>>(1/r_{o2}\ -4/r_{o7}+1/R_L)$ and $1/g_{M8}+1/g_{M9}<<\ r_{o7}$ & r_{o2}, we can get:

$$\frac{I_a}{VDD}\approx\frac{G_{M3}R_b}{g_{M5}R_L(R_b+2r_{o2}(1-G_{M3}R_b))} \quad (11)$$

Comparing results of (11) with (6), the PSRR is boosted to a fairly high value. From an intuitive perspective the follower characteristic of M5 will make V_c follow V_{RG}. Thus the error current produced by r_{o7} in (7) is zero. It can be viewed that r_{o7} is bootstrapped to infinite because no ac current flows when there is no voltage drop on this resistor. Similarly ro2 is bootstrapped by M5. As a result the sensitivity of V_{RG} to VDD is only decided by impedance ratio on this node. That is $V_{RG}/VDD\approx1/(2g_{M5}R_L)$. Combining with (6) we will get a result close to that listed in equation (11). The discrepancy is due to the current feedback loop formed by M1-M4.

Since no high gain feedback loop is engaged in our design, the stability is of little concern. The poles are all at high frequency which ensures a high PSRR over a wide frequency range. In higher frequency it is parasitic capacitance that will limit the performance.

The current consumed by the whole circuit is directly proportional to I_{PTAT} which is in turn determined by the value of R1. By careful design low power dissipation can easily be achieved. The major sources of error and noise contributors are similar to that of conventional bandgap voltage generators. The start-up issue can be solved by adding a temporary small current at beginning as conventional bandgap circuit does.

4. Simulation Results

The proposed bandgap voltage reference shown in Fig.3 has been simulated in HSPICE with TSMC 0.25um CMOS process.

According to the dc sweep simulation results shown in Fig.5 the circuit realizes a voltage reference of about 1.262V which has a voltage variation versus temperature of 0.1%. The simulated PSRR is -85dB at 1kHz and can still be -64dB at 1MHz as shown in Fig.6, which is 24dB better than that in [5]. The results imply a better high frequency PSRR performance as desired.

5. Conclusion

In this paper a novel bandgap voltage reference is proposed with a high PSRR even at high frequency. The inner regulated circuit provides a local supply voltage less sensitive to outer power rail for bandgap core. Bootstrap technique is used here to further improve PSRR. Simulation results show that the PSRR is -85dB at 1kHZ and still -64dB at 1MHz. The circuit can be realized in a digital CMOS process and thus can be widely used in SOC design to suppress noise from the high speed digital circuits on the chip.

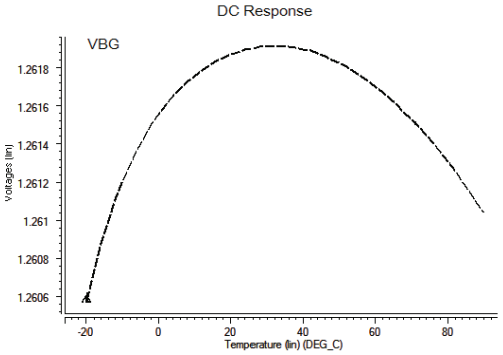

Figure 5. Reference Voltage versus Temperature

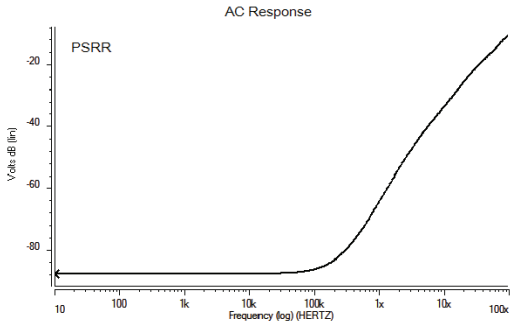

Figure 6. PSRR

Acknowledgments

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References

[1] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated circuits, Fourth Ed., New York: Wiley, 2001, ch4.

[2] B. Razavi, Design of Analog CMOS Integrated Circuits. New york, NY:2001, ch 11.

[3] G. Nicollini and D. Senderowicz, "A CMOS bandgap reference for differential signal processing," IEEE J. Solid-State Circuits, Jan. 1991.

[4] T. Brooks and A.L. Westwisk. "A low-Power Differential CMOS Bandgap Reference." ISSCC Dig.of Tech. Papers, pp.248-249, Feb. 1994.

[5] Khong-Meng Tham and Krishnaswamy Nagaraj, "A Low Supply Voltage High PSRR Voltage Reference in CMOS Process," IEEE J. Solid-State Circuits, May.1995.

[6] K. Lasanen, et. Al, " Design of a 1-V low power bandgap reference based on Resistive Subdivision", Proceedings of the 45th IEEE Midwest Symposium on Circuits and Systems, Tulsa, Oklahoma, USA, August2002