A Design of Ultra-Low Noise LDO using noise reduction network techniques

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***Abstract*— This paper presents an ultra-low noise low-dropout (LDO) regulators for powering RF applications. The proposed LDO employs two internal noise reduction network at the output of the bandgap reference (BGR), and between output and feedback resistors node (VFB in Fig. 1) of LDO to achieve ultra-low noise at interest frequencies. The 5-bits controlled resistor ladder is adopted to compensate the process, voltage, and temperature (PVT) variations. The output voltage level of LDO can be from 1.05 V to 2.6 V with trimming step of 50 mV. The highest output noise of the LDO is 64.52 nV/√Hz at 10 KHz. The proposed LDO is implemented in CMOS 55 nm technology with the die size of 480 µm x 330 µm.**

Keywords—Ultra-Low Noise; Bandgap Reference; Low-Dropout Regulator; VCO; PLL

I. INTRODUCTION

Noise is extremely important to designers of high-performance analog circuits, especially in high- speed clock, ADC, DAC, VCO, and PLL. A LDO can power these circuits. The key points to reducing noise are keeping the noise gain of LDO close to unity without compromising either AC performance or DC closed-loop gain and reducing the output noise of BGR. The average operating frequency of circuits is keeping increasing, that requires the synchronous circuits such as PLL and VCO should be able to operate at high frequency. For the VCO and PLL operation, the most important object that keeps circuit generating stable clock is the power supply. To maintain those aspects of a power supply, the precise and stable LDO output voltage is required in the power supply line. The proposed LDO is designed to provide the constant output voltage for VCO with high stability, ultra-low noise, wide bandwidth, and small size comparing to prior works [1-4].

II. BUILDING BLOCKS

The major sources of noise in LDO are the internal reference-voltage (BGR output) and the error-amplifier. Modern devices operate with internal bias currents of a few hundred nA or less to achieve quiescent currents of up to 15 µA. These small currents require bias resistors of up to 1 GΩ, resulting in noisier error-amplifier and reference-voltage circuits as compared to discrete implementations. Typical LDO uses a resistive divider to set the output voltage, so the noise gain is equal to the AC closed-loop gain, which as it turns out, is the same as the dc closed-loop gain.

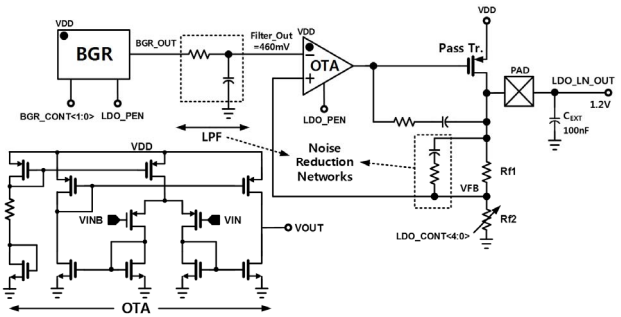


Fig. 1. Top Diagram of LN LDO with proposed Noise Reduction Networks.

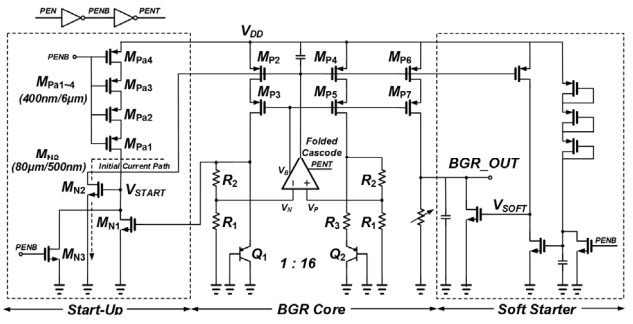


Fig. 2. Soft Starter BGR Structure.

This paper proposes two methods to reducing LDO noise. Filtering the soft starter reference voltage using RC-filter and reducing the noise gain of the error-amplifier using reduction simple RC-network as shown in Fig. 1. With the noise-reduction network, the AC gain is close to unity for much of the bandwidth, so the reference noise and error-amplifier noise are amplified to a lesser degree, resulting in reducing the noise. Also, with the RC-filter at the output of soft starter BGR, we can cancel the output noise of reference voltage. Fig. 2 shows the conventional architecture of BGR providing the reference voltage to LDO.

III. EXPERIMENTAL RESULTS

In this section, the post-layout simulation results will be shown. The proposed LDO is implemented in CMOS 55 nm technology. The active area of the LDO is 480 µm x 330 µm and the top layout is shown in Fig. 3. Fig. 4(a) shows the

transient result of LDO for different corner cases and Fig. 4(b) summarizes the Monte Carlo simulation of the proposed LDO. The slowest wakeup time is 1.9ms in SS corner. The output noise of the LDO is illustrated in Fig. 5 and corner case values are presented in Table I. The highest noise is 64.52 nV/√Hz in SS corner. Fig. 6 shows load & line regulations, temperature variations, and PSRR of proposed LDO at different corner cases.

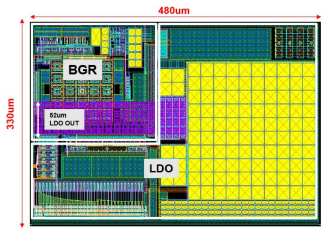
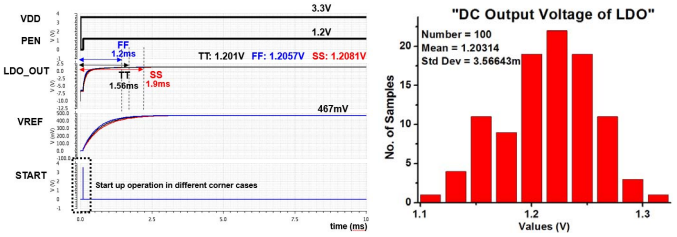


Fig. 3. Layout of Proposed LDO and BGR.



(a) (b)

Fig. 4. (a) Transient Results of LDO, and (b) its Monte Carlo Simulation.

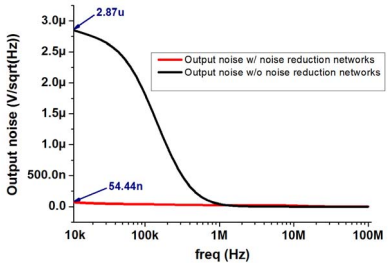


Fig. 5. Proposed LDO Output Noise Simulation.

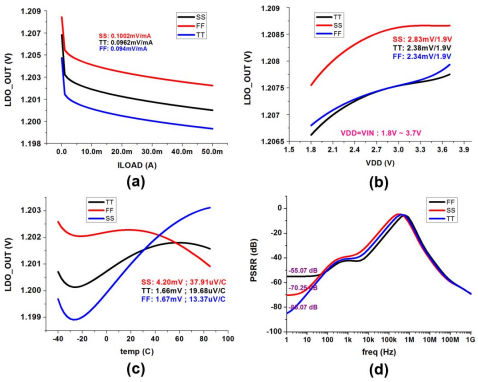


Fig. 6. (a) Load Regulation, (b) Line Regulation, (c) Temperature Variations, and (d) PSRR of LDO.

IV. Conclusion

This work proposes an ultra-low noise LDO using two methods which are noise reduction network for reducing gain of error-amplifier and RC-filter. The worst output noise performance of the LDO is 64.52 nV/√Hz at 10 KHz. The die size is 480 µm x 330 µm. While we obtaining low noise performance, stability is maintained at least 58.45 degrees in the worst case. The proposed LDO architecture can be applied to RF applications which require an ultra-low noise power supply. Table II, shows the performance comparison of this work with prior works.

Acknowledgment

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TABLE I. Output Noise (V/√Hz) Performance

Freq.	*FF/3.6V/-40°C*	*TT/3.3V/27°C*	*SS/3V/85°C*
10KHz	50.87E-9	54.44E-9	64.52E-9
50KHz	35.06E-9	45.41E-9	55.11E-9
200KHz	42.40E-9	55.91E-9	64.19E-9
1MHz	5.64E-9	5.06E-9	4.61E-9
10MHz	103.48E-12	82.8E-12	66.9E-12

TABLE II. Performance Comparison

	[1]	*[2]*	*[3]*	*[4]*	*This Work*
Process	0.25µm	0.35µm	0.13µm	0.18µm	**55nm**
VIN	-	3.6V	3V-4.5V	3V	**1.8-3.7V**
Max Load	100mA	100mA	150mA	100mA	**50mA**
Noise (V/√Hz)	130n (100Hz)	21.2µ (10KHz-100KHz)	100n (5KHz-400KHz)	56.4µ (1KHz-1MHz)	**<64.52n (10KHz-100MHz)**
PSRR	50	60	67	71.6	33
Die Area	0.21mm^2	0.26mm^2	0.166mm^2	-	0.158mm^2