PSRR Improvement Technique for Amplifiers with Miller Capacitor

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***Abstract*— A simple circuit technique is presented for improving poor midband power supply rejection ratio (PSRR) of single ended amplifiers that use Miller capacitance to set the location of the dominant pole. The principle of the technique is to create an additional parallel signal path from the power supply to the output, which cancels the dominating unity gain signal path through the output stage and Miller capacitor above the dominant pole frequency. Simulation results of a two-stage amplifier show that more than a 20dB improvement in the midband PSRR is obtainable as compared with an amplifier without the suggested circuit.**

I. Introduction

Constant demands for lower cost and smaller size, together with the low supply voltage requirements of modern IC processes, have forced analog designers to work in System-on-Chip (SoC) environment where noisy digital and dc-dc converter circuitry are integrated on the same die with sensitive analog blocks [1], [2]. Because in this environment the available dynamic range of analog blocks is already severely constrained by the low supply voltage and power consumption limits, good PSRR performance becomes essential in order not to degrade the available dynamic range any further [3], [4]. This is especially the case in applications, where differential signal processing is not applicable, such as in low voltage current and voltage reference cells, certain buffers and LDO regulators with on-chip frequency compensation capacitors.

One essential part of the above mentioned analog cells is the high gain operational amplifier. Due to fact the PSRR performance depends on the available differential gain, as shown by (1), where A_v is the differential gain and A_{dd} is the gain from the supply line to the output, the good low frequency PSRR that is needed e.g. in cell phone and audio applications requires either some kind of postregulation or more gain than is available from a simple high PSRR class A OTA structure [1], [4].

$$PSRR = \frac{A_v(s)}{A_{dd}(s)} \tag{1}$$

In a SoC environment things are further complicated by the extensive use of dc-dc converters that can have switching frequencies as high as 300kHz [1]. Attention therefore has to be paid, not only to the PSRR performance below the amplifier dominant pole p_1, but also to the midband ($p_1 < f < GBW$) PSRR performance, especially in regulator applications.

It is general knowledge that a simple two-stage Miller compensated (SMC) amplifier with an NMOS input stage suffers from poor midband PSRR [5]–[7]. Therefore in applications that drive predominantly capacitive loads a cascode or current buffer compensation is preferred, which virtually eliminates this problem [5], [6]. However cascode compensation is rarely used in high current applications due to possible poorly damped complex pole pair [8], [9]. Also the use of current buffer does not solve the PSRR problem of three-stage amplifiers that almost without exception use Miller Capacitor spanning second and third stages to set the dominant pole.

PSRR improvement techniques exist for Miller compensated amplifiers [10], [11]. However, these techniques use compensation networks that lie on a signal path, and may therefore degrade stability margins, or rely on a quiet DC bias, which is not always available in a single supply environment. Also they waste chip area by requiring an additional capacitor, which is as big as the main frequency compensating capacitor.

The purpose of this paper is to introduce a simple current mirror based PSRR improvement technique for two- and three stage amplifiers. The benefits of the suggested technique include smaller additional capacitor, better stability and suitability also for applications, which drive heavy resistive loads.

Section II discusses briefly, what is the reason behind the poor midband PSRR of Miller compensated amplifiers, how it can be improved by using a simple current mirror based circuit and how to apply it efficiently. Section III shows the topology of a two-stage amplifier used in simulations. Finally in sections IV and V simulation results are given and conclusions are drawn.

II. Suggested PSRR Improvement Technique

A better understanding of the PSRR problem and how it can be fixed can be obtained by looking at a simple Miller compensated amplifier shown in Fig. 1 (a). As discussed in several sources [12]–[14], the principal problem of Miller compensation is the fact that above the dominant pole frequency the Miller capacitor short circuits the gate and the drain of M_L together causing the stage enclosed by the compensation capacitor C_M to act like unity gain amplifier ($A_{dd} \approx 1$), which couples all the noise in the supply to the output. This behavior does not depend on the number of gain stages enclosed, but on the fact that the Miller capacitor acts

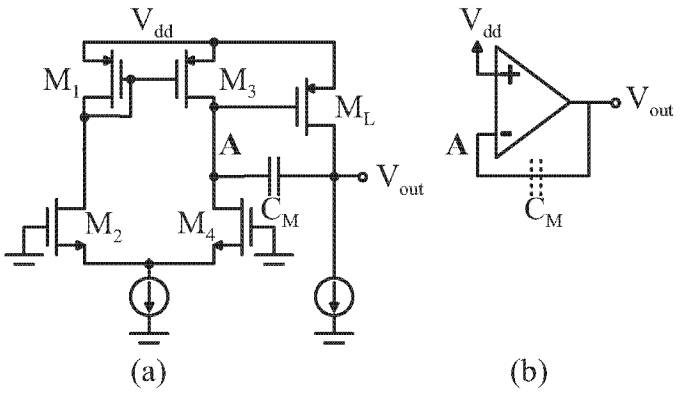

Fig. 1. Simple Miller compensated amplifier (a) and model of the output stage at midband frequencies (b).

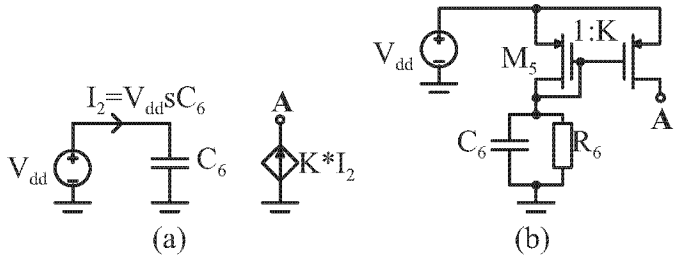

Fig. 2. Creating additional signal path by using an ideal current amplifier (a) or a current mirror (b).

as a short circuit at midband frequencies as shown in Fig. 1 (b). Therefore, if the second stage of a three-stage amplifier is a PMOS transistor, it will have exactly the same PSRR problems as its two-stage Miller compensated counterpart.

The PSRR of Miller compensated amplifiers could be improved if there were another signal path that would have gain of -1 at the frequency range of interest. According to the superposition principle this would cancel out the direct unity gain signal path through the output stage and thus considerably improve the midband PSRR.

One possibility for crating the additional gain is to use an ideal current amplifier of Fig. 2 (a) or its practical implementation (b) in parallel with the current mirror of Fig. 1 (a). The current through this amplifier to the node A is

$$I_A = V_{dd} K s C_6 \tag{2}$$

This current is integrated by the output stage, which at midband frequencies acts like an ideal integrator that sinks all the current entering node A. Thus the output voltage becomes

$$-V_{out} = \frac{I_A}{sC_M} \tag{3}$$

By combining the above equations we get

$$\frac{V_{out}}{V_{dd}} = -1 \tag{4}$$

as long as $C_M = C_6 K$.

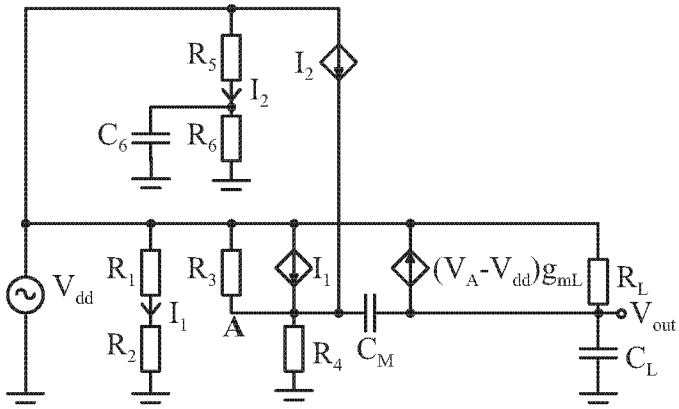

Fig. 3. Small signal model of the amplifier with the PSRR improvement circuitry.

A. Design Equations

The design equations were derived using the small signal model shown in Fig. 3, which included the PSRR circuit from Fig. 2 (b). Analysis of the small signal model with an assumption that $C_6 = C_M$ results in

$$A_{dd}(s) = \frac{1 + g_{mL}(g_4 - g_2 - g_6)R_L R_3||R_4 + a_1 s + a_2 s^2}{(1 + s/p_1)(1 + b_1 s + b_2 s^2)}, \tag{5}$$

where the poles p_1 and other terms are given as

$$a_1 = C_M R_3||R_4$$
$$a_2 = C_M^2(R_L + g_{mL}R_5 R_L)R_3||R_4$$
$$p_1 = 1/(C_M g_{mL} R_L R_3||R_4)$$
$$b_1 = (C_L + C_6 g_{mL} R_5)/g_{mL}$$
$$b_2 = C_6 C_L R_5/g_{mL}$$

Comparing (5) with the A_{dd} of SMC amplifier given in [12] shows two important differences. First, if the differential pair transistor output conductances are not well matched and the conductance g_6 is not small, the additional circuitry can actually degrade the low frequency PSRR performance. Second, a low frequency zero, which is responsible for the poor midband PSRR performance in the nominal case, is not present. Instead there are two high frequency zeroes, which should be made complex and pushed to as high frequencies as possible to maximally benefit from the discussed technique. This corresponds to the requirement

$$\frac{4(R_L + g_{mL}R_5 R_L)}{R_3||R4} > 1 \tag{6}$$

When designing a circuit, component parameters such as g_{mL}, R_L, C_L and C_M are usually set by requirements other than PSRR performance, so the only parameter that can be set freely when designing the PSRR circuitry is the value of the diode connected transistor $1/g_{m5}$. The impedance of this node affects the frequency of the complex zero pair, which in turn sets the frequency up to the point where the circuit maintains

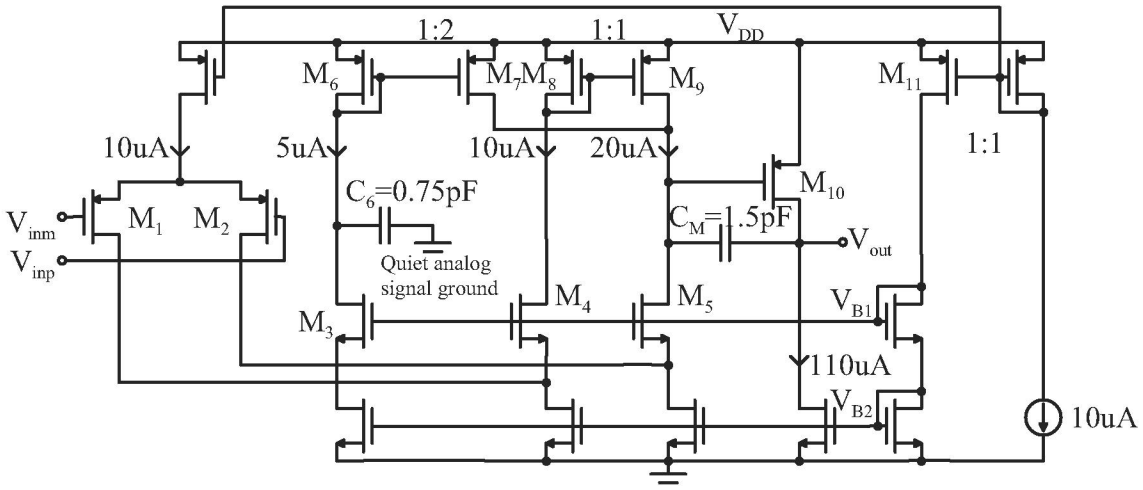

Fig. 4. Schematic of the simulated class A amplifier with the suggested PSRR improvement circuitry.

its DC PSRR performance. By knowing this desired frequency f, $R_5 = 1/g_{m5}$ can be chosen according to (7)

$$R_5 = \frac{1}{g_{mL}}\left(\frac{1}{4\pi^2 f^2 C_M^2 R_L R_3 || R_4} - 1\right) \qquad (7)$$

Note that the calculated value for R_5 can result in the third pole lying close to the second pole of the A_{dd} transfer function. However, the parallel path for the PSRR circuitry means that the third pole is not visible to the differential signal path and therefore it does not degrade the stability margins. In other words, high frequency pole locations don't need to be considered, which allows the presented technique to be used equally well in heavy resistive load applications, where the absolute second pole location varies considerably with the load current.

III. Amplifier Circuit

The class A amplifier used in the simulations is shown in Fig. 4. Transistors M_6 and M_7 together with C_6 implement the additional parallel path from the supply line. The gain in the mirror is used to effectively multiply the current through the capacitance C_6 in order to save space.

It must be emphasized that like cascode compensation, the presented technique relies on a quiet signal ground for C_6 [10]. However, unlike in the cascode compensation approach, DC value of this signal ground is not used to bias any transistors. This means that the quietness of V_{B1}, and therefore the output impedance of M_{11}, is of less importance here than in the cascode compensation approach.

The disadvantage of the added circuitry is that, because of the additional parallelling transistor M_7, it reduces DC gain by approximately 6dB and contributes to noise and offset of the amplifier. The efficiency of the discussed technique is however not jeopardized due mismatch as it relies on the current mirror and capacitor ratios, which are well controlled in practice.

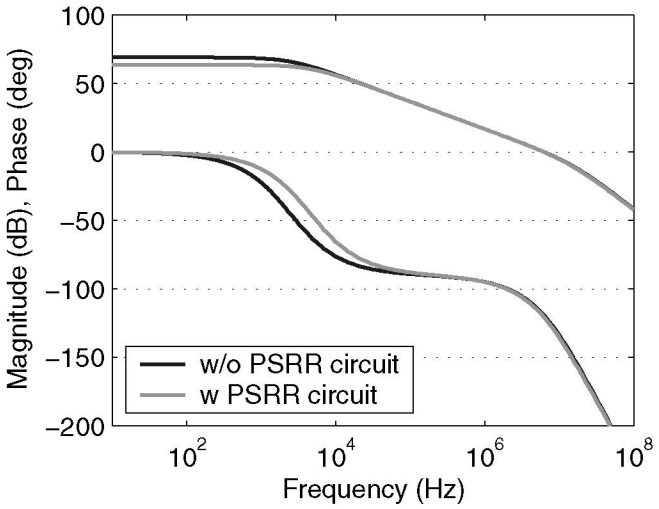

Fig. 5. Nominal frequency response (A_v) of the simulated amplifiers with 15pF capacitive load.

IV. Simulation Results

To verify the theoretical findings, the two-stage amplifier of Fig. 4 was simulated in 0.35μm CMOS process using a 3V supply voltage with and without the PSRR improvement circuitry.

The nominal signal path frequency response (A_v) is shown in Fig. 5. The corresponding phase margins and unity gain frequencies with and without the suggested circuitry were 60°@6.2MHz and 61°@6.2MHz respectively. The current mirror obviously isolated the large additional capacitance C_6 so that it did not degrade the stability margins.

Frequency responses from the supply line to the output node (A_{dd}) are given in Fig. 6. From the figure it is seen that A_{dd} with the PSRR improvement circuitry shows first order low pass characteristics up to the frequency of complex zeroes, which in this case was approximately 200kHz. This can also be seen from the closed loop plots for 1/PSRR given in Fig.

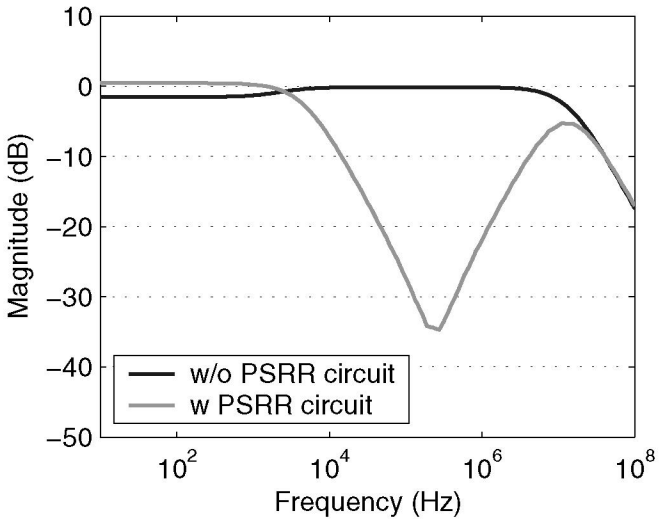

Fig. 6. Frequency responses from the supply line to the output (A_{dd}) of the simulated amplifiers.

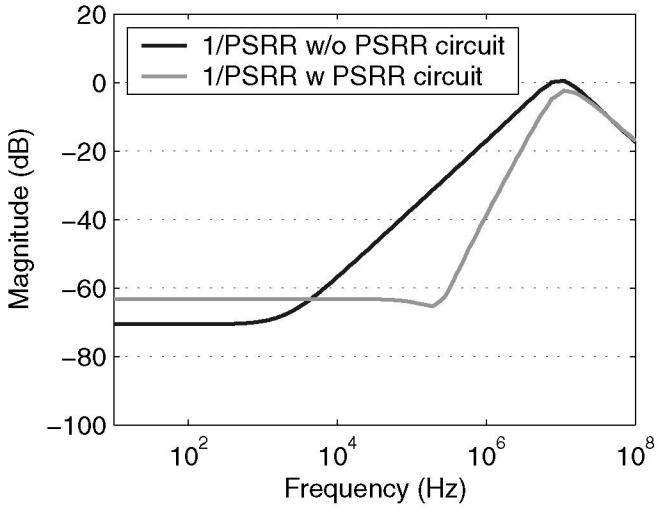

Fig. 7. 1/PSRR of the simulated amplifiers.

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The amplifier responses to a 100mV 100kHz signal present in the positive supply are given in Fig. 8. The resulting amplitudes at the output nodes with and without the suggested circuit were 62μV and 1.44mV respectively, which approximately correspond to the AC simulation results.

V. Discussion

The principle of the circuit technique introduced here for improving the poor midband PSRR of Miller compensated two- and three-stage amplifiers was to create an additional parallel signal path from the power supply to the output that cancelled the dominating unity gain signal path through the output stage.

Small signal analysis and simulations of a compact class A amplifier demonstrated that, by taking advantage of the current

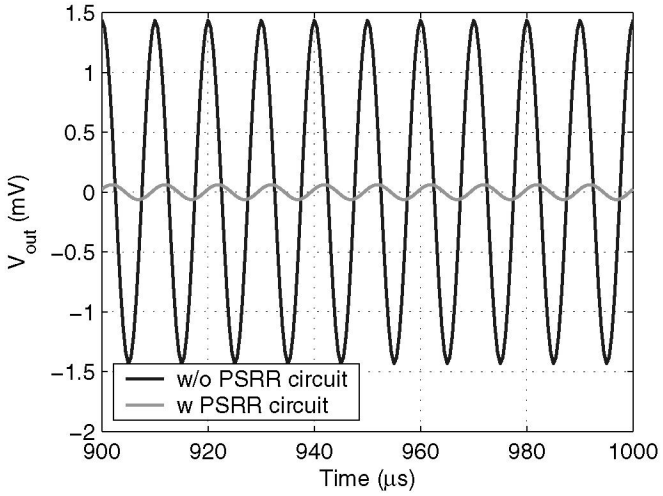

Fig. 8. Response at the output to a 100mV 100kHz signal riding on V_{DD}.

mirror current gain, a PSRR improvement of more than 20dB was easily obtained over a wide frequency range in an area efficient manner.

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