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A 3-A CMOS low-dropout regulator with adaptive Miller compensation

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Abstract A 3-A CMOS low-dropout regulator (LDO) is presented by utilizing adaptive Miller compensation (AMC) technique, which provides high stability, as well as fast line and load transient responses. The proposed LDO has been fabricated in a standard 0.5 μm CMOS technology, and the die area is small as 1330 μm × 1330 μm with the area-efficient waffle layout for power transistors. Both load and line regulation are less than $\pm 0.1\%$. And the output voltage can recover within 80 μs for full load changes. The power–supply rejection ratio (PSRR) at 20 KHz is −30 dB. Moreover, it is stable enough with a ceramic capacitor small to 2.2 μF, and the added series resistance is not needed.

Keywords Adaptive Miller compensation · Loop-gain stability · Low-dropout regulator · Waffle power transistors

1. Introduction

The phenomenal growth in portable, battery-operated devices and other complicated equipments which need high precision supply voltages has fueled the growth of the low-dropout regulator (LDO) due to its many advantages [1, 2]. With the rapid development of complicated system, the large output current and high precision output voltage are needed. However, output current varying with large range may lead to instability [3]. Moreover, the voltage gain should be increased by additional gain stages to get high precision output voltage. In that case, the bandwidth should be reduced to obtain enough phase margin. So, the precision of output voltage and transient response are tradeoffs with LDO stability. And when the loop gain increases, the classical LDO based on dominant-pole compensation may be unstable [1].

In this paper, a CMOS LDO is presented for solving the correlated tradeoffs on stability, precision and recovery speed. The circuit architecture is based on a three-stage amplifier. Both fast load transient response and high PSRR are achieved due to the fast and stable loop gain provided by the proposed LDO structure and adaptive Miller compensation (AMC) scheme, which makes the pole generated at the gate of power MOSFET push to a high frequency and generates a zero having frequency varying with the output current to compensate the nondominant pole. Hence, the frequency of zero changes to maintain the stability of the LDO despite the variation in the frequency of the low-frequency pole generated by the output resistance and capacitance.

The structure of the proposed method is presented in Section 2. In it, the analysis of stability will be discussed in detail. The correlated circuit is then introduced in Section 3. Finally, the experiment measurements and results will be presented in Section 4.

2. Proposed LDO structure with adaptive Miller compensation

For three-stage amplifier, nested Miller compensation is a good selection. A simple scheme of three-stage LDO with nested Miller compensation is shown in Fig. 1. However, there are some disadvantages with this structure. The gain-band width (GBW) of those LDOs are directly proportional to g_{mp} [4] which varies with the output current, so it is not suitable for large current design. In addition, the parasitical capacitance between source and gate cannot be neglected due

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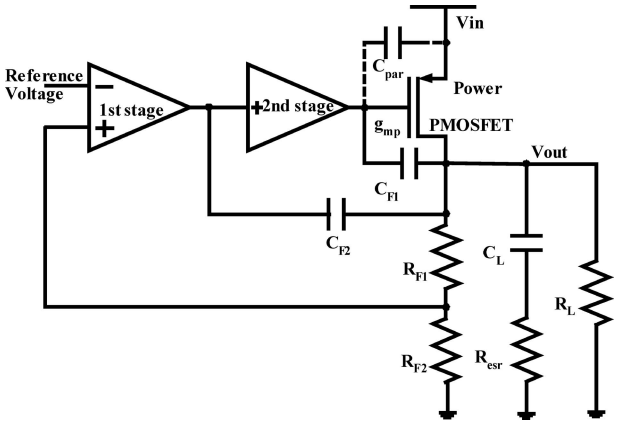

Fig. 1 Structure of LDO with nested Miller compensation

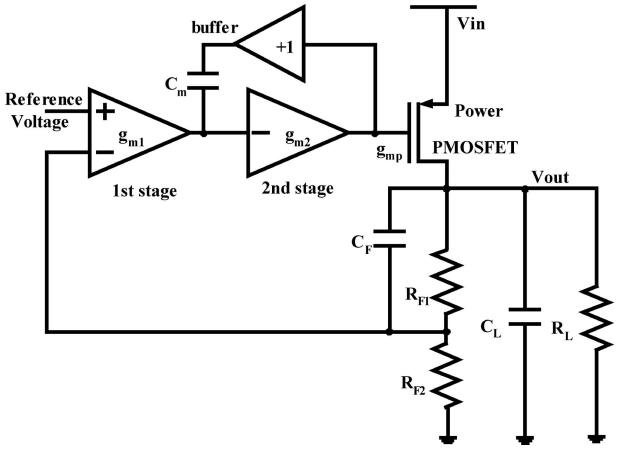

Fig. 2 Structure of the proposed LDO

to the large size of the power transistors, which obviously leads to the decrease of PSRR in high frequency. In this section, the LDO with novel AMC technique is discussed to solve above problems.

The structure of the proposed LDO with AMC and phase-lead compensation is shown in Fig. 2. In this structure, the output resistance of buffer varies with the output current, so that an adaptive zero can be introduced to cancel the pushed nondominant pole. By setting its value correctly, even in the worst case of stability, the LDO is stable enough due to this advanced frequency compensation.

2.1. Adaptive Miller compensation

The small signal model of the proposed LDO structure with AMC technique is shown in Fig. 3. In the figure, g_{mi}, R_{oi} and C_i are defined as transconductance, output resistance, and the lumped output parasitic capacitance of the ith gain stage, respectively. R_m is the equivalent output resistance of the buffer and C_m is the compensation capacitor. And g_{mp} is the transconductance of power transistors, R_o and C_L are the equivalent resistance and output capacitance of the output of

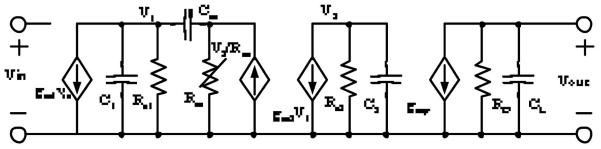

Fig. 3 Small signal model of AMC schematic

LDO. The value of R_m is a function of output current, which will be discussed in detail in Section 3.

With the analysis of [5], ignoring the high-frequency poles and zeros, the transfer function is given by the following equation:

$$H_1(s) = \frac{A_0(1 + s/z_m)}{(1 + s/p_1)(1 + s/p_2)} \tag{1}$$

where,

$$A_0 = g_{m1}R_{o1}g_{m2}R_{o2}g_{mp}R_o$$
$$p_1 = 1/R_oC_L$$
$$p_2 = 1/g_{m2}R_{o1}R_{o2}C_m$$
$$z_m = 1/R_mC_m$$

are the low-frequency open loop gain of the proposed scheme, the pole produced by output stage, and the pole and zero produced by AMC schematic.

At light load condition, p_1 is the dominant pole while p_2 is the second pole. In that case, the stability can be boosted by locating z_m near p_2. With the increase of output current, the resistance of R_m decrease, which will be discussed in Section 3. So that both p_1 and z_m move in parallel under a range of values for the output current. For a large current, p_2 is the dominant pole while p_1 is pushed to a high frequency. By using this technique, the GBW will not change too much.

It's clear that there are some ways to obtain enough phase margin from Eq. (1). One way is to decrease the open-loop gain A_0 by decreasing the transconductance or the output resistance of each gain stage. Another way is to increase the frequency of p_2 by decreasing g_{m2}, R_{o1} or R_{o2}. Obviously, it is a tradeoff between stability and precision, transient response etc.

The loop gain of proposed LDO is shown in Fig. 4. The parasitic capacitance at the output of the second stage is large due to the huge size of power transistors, so that it is advisable to locate z_m higher than p_2 at light load condition or p_1 at heavy load condition to decrease GBW, which can avoid instability introduced by the parasitic pole of power transistors.

2.2. Phase-lead compensation

If the output current is so large that z_m locates near the unit-gain frequency, this may lead to minor phase margin thus

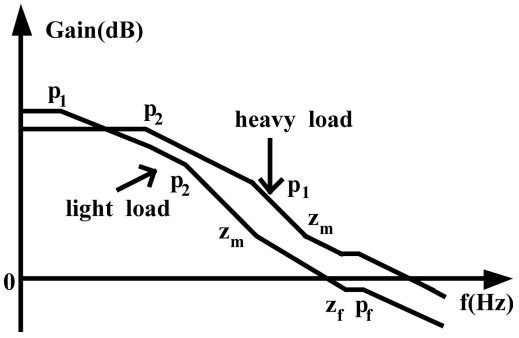

Fig. 4 Loop gain of proposed LDO (not in scale)

inferior stability. A first-order high-pass feedback network functioning as phase-lead compensation is introduced to optimize this condition. It comprises two feedback resistors R_{F1} and R_{F2}, and a capacitor C_F connected two ports of the top resistor R_{F1}, which is shown in Fig. 2. The transform function is given by

$$H_2(s) = \left(\frac{R_{F2}}{R_{F1}+R_{F2}}\right)\left[\frac{1+sC_{F1}R_{F1}}{1+sC_{F1}(R_{F1}//R_{F2})}\right] \tag{2}$$

From the above transfer function, it is shown that one pole (p_f) and one zero (z_f) are created, and p_f and z_f are, respectively, given by

$$p_f = \frac{1}{(R_{F1}//R_{F2})C_{F1}} \tag{3}$$

$$z_f = \frac{1}{R_{F1}C_{F1}}. \tag{4}$$

The zero frequency is lower than the pole frequency, and this zero, can be used to increase phase margin thus enhance the stability. In this design, the output voltage is optional from 1.8 V to 4.5 V, and the voltage reference divided from 1.2 V bandgap reference is 0.6 V. When the output voltage is 1.8 V, the ratio of R_{F1} to R_{F2} is 2:1, so that the frequency of p_f is about 1.5 times of z_f. The stability cannot be enhanced obviously unless the reference voltage becomes much smaller than output voltage. However, the stability can be optimized in any case by setting this zero frequency lower than GBW a little. This condition can be shown in Fig. 4. Moreover, the noise and PSRR performance can also be improved by utilizing this structure [6 , 7].

3. Circuit realization and layout consideration

The corresponding schematic diagram of Fig. 2 is illustrated in Fig. 5. The first gain stage is an operational transconductance amplifier (OTA), and the second gain stage is a simple common-source amplifier. To obtain enough phase margin, p_2 cannot be too low, one way to ensure that is to decrease g_{m2}, R_{o1} or R_{o2}, just as discussed in Section 2. This indicates that the drain-source current of M_6 and M_{11} should be large enough to maintain low output impedance. It's also very helpful to enhance the drive capability with large source or sink current of second stage. Furthermore, a large size of M_{10} is needed to increase the transconductance for higher frequency of p_2 and to provide large drive capability.

The buffer is made up of M_{12}–M_{15}, and the small-signal voltage gain is given by

$$Gain_{buffer} = \frac{g_{m15}}{g_{m14}}\frac{g_{m13}}{g_{m12}} \approx 1 \tag{5}$$

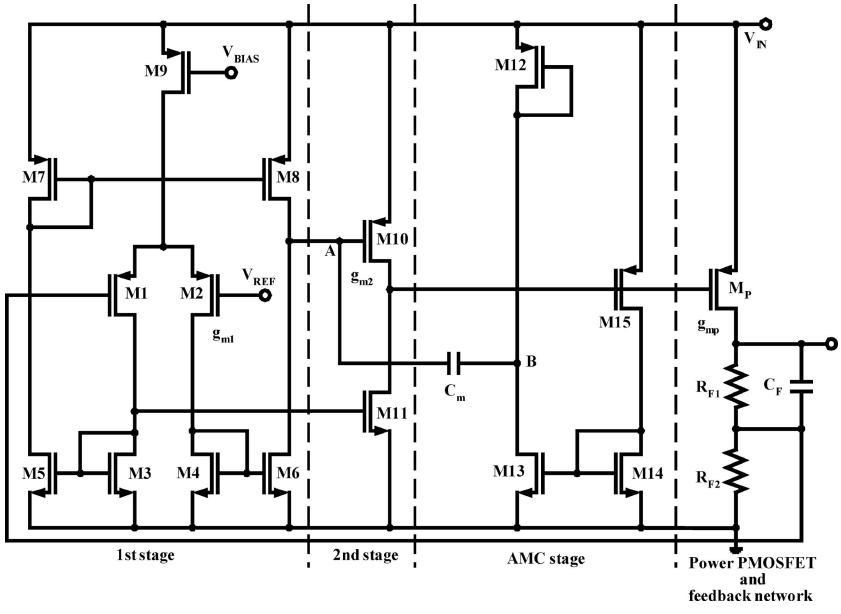

Fig. 5 Simple schematic of the proposed LDO

The output resistance of the buffer is:

$$R_m = \frac{1}{g_{m12}} = \frac{1}{\sqrt{2\mu_p C_{OX}\left(\frac{W}{L}\right)_{M12} k I_O}}. \quad (6)$$

Where k is the ratio factor of I_{D12} to I_O, and it equals approximately $\frac{(W/L)_{M12}}{(W/L)_{M_P}}$. So R_m is inversely proportional to $\sqrt{I_O}$, thus the zero frequency varies with I_O. Hence both p_1 and z_m move in parallel under a range of values for the output current. According the analysis of Section 2, an adaptive zero is generated for compensating the nondominant pole of the system, i.e., p_2 at light load while p_1 at heavy load. The ratio of M_{15} to power transistor M_P is set to be about 14000:1. When the load current is 1 mA, the simulated quiescent current of buffer is less than 0.2 μA, and the output resistance R_m is 800 KΩ. When the load current is 3 A, the quiescent current is about 400 μA while R_m is about 7 KΩ. So that the zero can vary more than 100 times to deal with the huge shift of p_1 due to different load conditions. Moreover, the GBW will not change too much and the parasitic poles are still out of GBW, and high stability is obtained.

Fast load transient response can be improved by high GBW and large drive capability with large current, however, GBW is a tradeoff with stability. In the proposed LDO, an artful method is introduced to enhance the transient response by biasing the load transistor M_{11} of second stage dynamically. It's clear that a negative feedback loop is generated through V_{out}, M_1, M_{11} and M_P, which can slow the recovery time thus speed up the transient response when load or supply voltage changes suddenly.

Power transistor M_P is also as the third gain stage of the proposed LDO, and this characteristic requires it could provide not only large output current but also enough gain. Furthermore, the dropout voltage is mainly decided by the size of the power transistor. It can be specified in terms of its equivalent on-resistance $R_{DS(on)}$ measured at a specified gate voltage V_{GS} and junction temperature [8], which is determined as follow

$$R_{DS(on)} \cong \frac{1}{\mu_n C_{OX}\frac{W}{L}(V_{GS} - V_{TH})} + R_P \quad (7)$$

where R_P is the sum of the resistance of the source and drain metallization and the bonding wire. The power transistor M_P of proposed LDO is made up of 21000 paralleling small transistors (the size of each is 13 μm/0.5 μm), which is large enough for gain and current requirements. The simulated on resistance ignoring R_P is about 50 mΩ.

In most cases, more than half of the chip area is devoted to the power transistors [9]. To save area and decrease parasitic capacitance, the waffle layout for power transistors is adopted, which is shown in Fig. 6. Due to fewer vias and contacts, the metal resistance is higher than that with

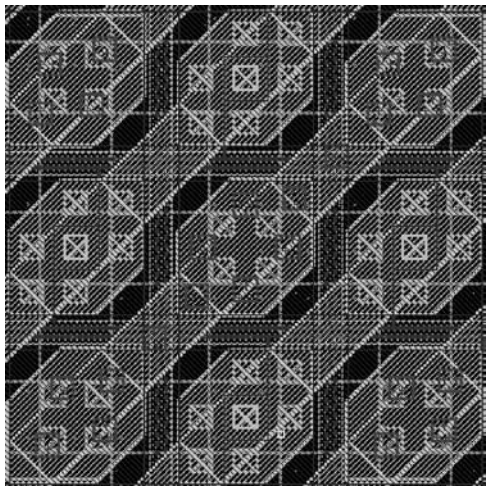

Fig. 6 Layout structure of power transistors

conventional rectangular layout. Because this chip is not mainly used in the battery-powered device, the requirement of dropout voltage is not too critical when it compares with the chip area. The experimental total on resistance is about 220 mΩ with three bonding wires for input or output pad, and this can meet applications well.

The simulated bold plots for different load conditions are shown in Fig. 7, and the phase margin at different load conditions is shown in Fig. 8. From the results, the phase margin of proposed LDO is more than 60 degrees at worst case and is absolutely stable in any time.

The PSRR is effectively improved due to the wide loop-gain bandwidth. And the required ESR of output capacitor is much smaller than classical LDO because it is not required to generate a low-frequency zero to compensate the nondominant pole. This also enhances the PSRR at high frequency [1].

4. Experiment results

The proposed LDO shown in Fig. 5 has been fabricated in a standard trinal-metal double-poly 0.5 μm CMOS technology, which has threshold voltage of about 0.85 V. It can be

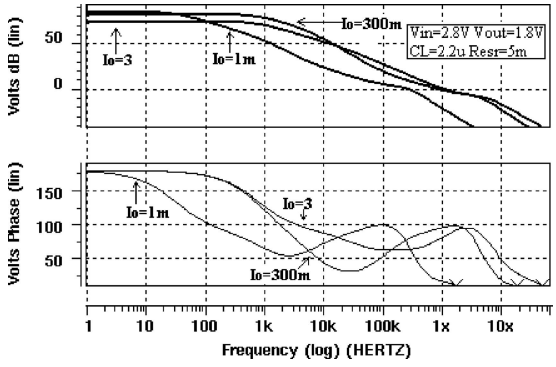

Fig. 7 Simulated bold plots for different load conditions

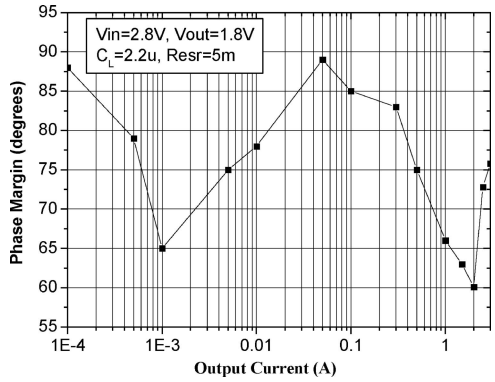

Fig. 8 Phase margin vs. output current

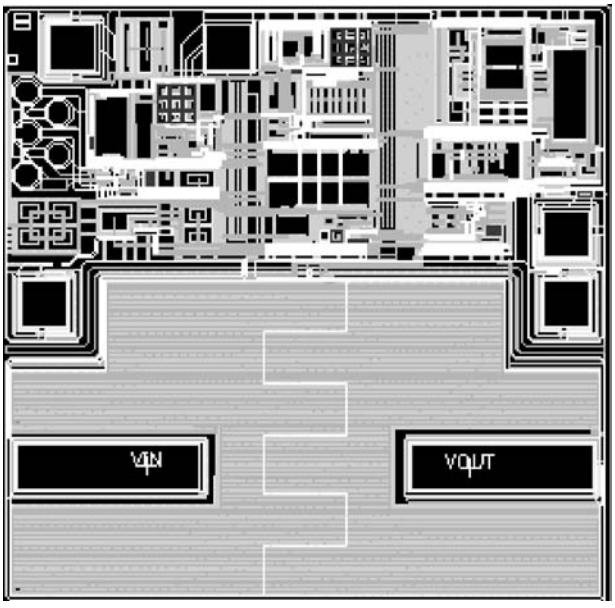

Fig. 9 Die plot

mainly used in PC add-in cards and post regulator of high-efficiency switching-mode power converters. The die plot of the proposed LDO is shown in Fig. 9, and die area is 1330 μm $\times$ 1330 μm. The quiescent current is 1 mA at no-load condition, and the maximum output current is as large as 3 A with a dropout voltage of 650 mV. Both load and line regulation are less than $\pm 0.1\%$.

The measured load transient response of the proposed LDO is shown in Fig. 10. Experiments results show that the proposed LDO can respond quickly within 2 μs and recover to the preset output voltage within 80 μs due to the fast loop-gain response provided by the AMC technique. Moreover, the fast response time is beneficial to reduce overshoot and undershoot, and a less than 200-mV deviation is recorded for the worst case scenario.

The measured line transient response is shown in Fig. 11. The LDO responds immediately and recovers the output voltage. Moreover, both overshoot and undershoot are less than 6 mV.

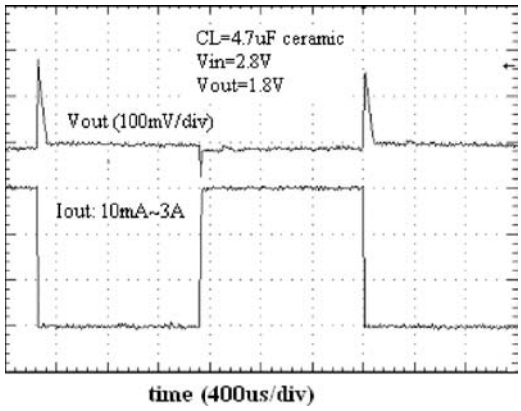

Fig. 10 Measured load transient response

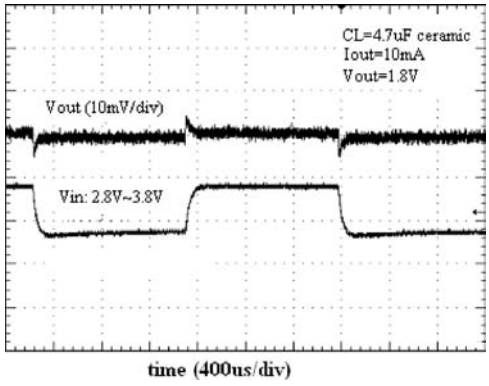

Fig. 11 Measured line transient response

In addition, the proposed LDO provides good performance on PSRR at high frequencies. As shown in Fig. 12, the LDO has at least -30 dB rejection ability at 20 KHz. This excellent performance is important for the LDO as a post regulator of high-efficiency switching-mode power converters [1].

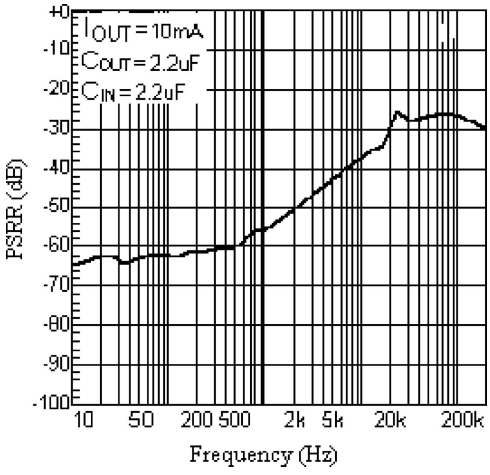

Fig. 12 Measured PSRR characteristic

5. Conclusion

A CMOS LDO, which has the output current large as 3 A, based on the architecture of three-stage amplifier is designed and fabricated using AMC technique. The fabricated IC proves to be stable for load current up to 3 A, output capacitor small to 2.2 μF with very low ESR value. Hence ceramic capacitors can be used without the series resistance required other regulators, so that the cost and circuit area can also be decreased consequently.

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