24.5 A 0.9V 0.35µm Adaptively Biased CMOS LDO Regulator with Fast Transient Response

Yat-Hei Lam, Wing-Hung Ki

Hong Kong University of Science and Technology, Kowloon, China

Portable applications often need multiple voltages controlled by a power management IC to power up many functional blocks [1]. A switching pre-regulator is usually followed by a low dropout (LDO) regulator to provide a regulated power source for noise-sensitive blocks. The LDO regulator has to be stable for all load conditions and frequency compensation is usually needed to stabilize the regulation loop [2, 3]. The output voltage droop due to rapid and large load changes could be minimized with a fast regulation loop, such that functional blocks powered by the same LDO regulator would have low crosstalk noise.

LDO regulators with fast load transient response were demonstrated in [4] and [5]. In [4], the regulator was implemented in an advanced 90nm CMOS process and the fast feedback loop used a small 600pF filter capacitor for stability. The fast response required a large quiescent current of 6mA to deliver an output current of 100mA and the $10\%_{P\text{-}P}$ output voltage variations were relatively large. In [5], the power PMOS pass transistor was driven by a dynamically biased super source-follower as a buffer for both stability and speed and the buffer had to operate at a voltage higher than is usually required by low-power digital circuits. The bias current of the error amplifier was fixed, and its speed and current consumption are difficult to be optimized simultaneously. The regulator also used a 10pF capacitor for compensation, which used silicon area.

A low-voltage fast transient-response LDO regulator using an inexpensive 0.35µm CMOS process is presented in this paper. It features a current-efficient adaptively biased regulation scheme using a low-voltage high-speed super current mirror and does not require a compensation capacitor (Fig. 24.5.1). It is stabilized by a low-cost low-ESR ceramic filter capacitor of 1µF. The adaptively biased error amplifier EA (M_{A1} to M_{A8}) drives a small transconductance cell, M_{A9}, to modulate the output current I_{OUT} through a transient-enhanced super current-mirror (SCM).

The PMOS differential input stage of the EA (M_{A1} and M_{A2}) is driven by NMOS level shifters (M_{A3} and M_{A4}). The level shifters allow the EA to function properly at a V_{DD} that is only 150mV higher than V_{OUT}. The PMOS differential pair and the NMOS active loads (M_{A5} and M_{A6}) give a ground-referenced voltage, V_{EA}, to drive M_{A9}. The bias currents of the level shifters and the differential pair are proportional to I_{OUT}. As I_{OUT} increases, the outputs of the level shifters V_{REF}' and V_{OUT}' decrease, which compensates for the increase of the source-gate voltages of M_{A1} and M_{A2}. Thus, the source node of the differential pair, V_S, remains constant as I_{OUT} varies, and M_{ADB} of the SCM that provides the bias current I_{ADB} to the EA will not be forced into the triode region at heavy loads. The current densities of M_{A5} and M_{A6} are designed to be half that of M_{A9} such that the adaptive-biasing loop has a gain <1 for stable and robust operation. The current sources I_{B1} through I_{B4} are essential to keep the LDO regulator active even when I_{OUT} is zero.

For loop stability, the frequency responses of the EA and the SCM should have low phase shifts at frequencies lower than the unity gain frequency. The gain bandwidth product GBW is $A_{OL}/(2\pi R_{OUT}C_{OUT})$, where A_{OL} and R_{OUT} are the low-frequency open-loop gain and output resistance of the regulator (including R_{LOAD}), respectively. With C_{OUT} = 1µF and A_{OL} = 50dB, the GBW with a full load of 50mA (R_{LOAD} = 18Ω for V_{OUT} = 0.9V) is a few MHz, while at light loads it could drop to a few tens of Hz. The large current gain of K = 1000 for the SCM allows the use of a small M_{A9} in minimizing the parasitic capacitance at V_{EA}. Due to adaptive biasing, the EA has low power consumption at light loads, and the non-dominant pole generated at V_{EA} tracks with the GBW and the regulator remains stable as I_{OUT} varies.

Figure 24.5.2 shows a conventional current mirror CM and the SCM. The CM achieves a high current gain by using a large transistor aspect ratio. Speed is limited by the large time constant of C_g/g_{mIN}, where g_{mIN} is the transconductance of the diode-connected input transistor M_{IN}, and C_g is the total equivalent gate capacitance of both M_{IN} and M_{OUT}. The proposed SCM utilizes a low-voltage transient-enhancing circuit that provides extra transient current to C_g to enhance the current mirroring speed. A very small on-chip compensation resistor, R_Z = 250Ω, is sufficient to stabilize the transient-enhancing circuit. In steady state, $V_G = V_{B2}$ and V_{BOOST} regulates M_{B1} such that $I_{BOOST} = I_{IN} = I_{OUT}/K$. If there is a rapid increase of I_{IN}, which would reduce the drain currents of M_{B5} and M_{B6} quickly, M_{B3} and M_{B4} react with a delay by design. The sudden mismatch in the drain currents of M_{B6} and M_{B4} pulls V_{BOOST} up to increase I_{BOOST}. The node voltage V_{B2} is then pulled down first followed by V_G due to the RC delay generated by R_Z and C_g. The voltage difference across R_Z is amplified by M_{B3} through M_{B6} and pulls V_{BOOST} further up to provide extra current such that $I_{BOOST} > I_{IN}$ to compensate for the delay and to stabilize the transient-enhancing loop. A similar mechanism applies to a rapid decrease of I_{IN}.

Figure 24.5.3 shows the frequency responses of the SCM and the CM for comparison. At a light load of I_{LOAD} = 1mA, the CM has a phase shift of 60° at 100kHz, but the SCM has the same phase shift at a much higher frequency of 2MHz. The minor gain peaking at 2.5MHz is caused by the <90° phase margin of the transient-enhancing loop. It occurs at a frequency much higher than the GBW of the regulation loop and the overall stability of the regulator is not affected. At a full load of I_{LOAD} = 50mA, both the bandwidths of the SCM and the CM are larger due to the increase in the bias currents. The CM has a phase shift of 60° at 2MHz, and the SCM has the same phase shift at 8MHz, which is high enough for the regulator to be stabilized with a 1µF filter capacitor.

Figure 24.5.4 shows the measured load transient response. The load current is switched between 0µA and 50mA with rise and fall times of 10ns. No overshoot is observed for the switching from 50mA to 0µA, as the regulation loop had a large bias current initially, giving a high unity gain frequency. For the switching from 0µA to 50mA, a minor undershoot occurs due to the low bias current at I_{OUT} = 0mA. However, the total output voltage variation is only 6.6mV ($0.73\%_{P\text{-}P}$) and is much smaller than those in [4] and [5].

Figure 24.5.5 shows the measured quiescent current I_Q versus I_{OUT}. At a high I_{LOAD}, I_Q increases linearly, demonstrating a working adaptive-biasing scheme. At no load, the EA and the SCM are kept active by a total bias current of only 4.04µA. Figure 24.5.6 tabulates all the important parameters of the proposed regulator in comparison with those of [4] and [5]. The die micrograph is shown in Fig. 24.5.7. The regulation loop occupies only 24% of the total active area.

References:

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[2] G. A. Rincon-Mora and P. E. Allen, "A Low-Voltage, Low Quiescent Current, Low Drop-out Regulator," *IEEE J. Solid-State Circuits*, pp. 36-44, Jan. 1998.

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[4] P. Hazucha, T. Karnik, B. A. Bloechel et al., "Area-Efficient Linear Regulator With Ultra-Fast Load Regulation," *IEEE J. Solid-State Circuits*, pp. 933-940, Apr. 2005.

[5] M. Al-Shyoukh, H. Lee and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation," *IEEE J. Solid-State Circuits*, pp. 1732-1742, Aug. 2007.

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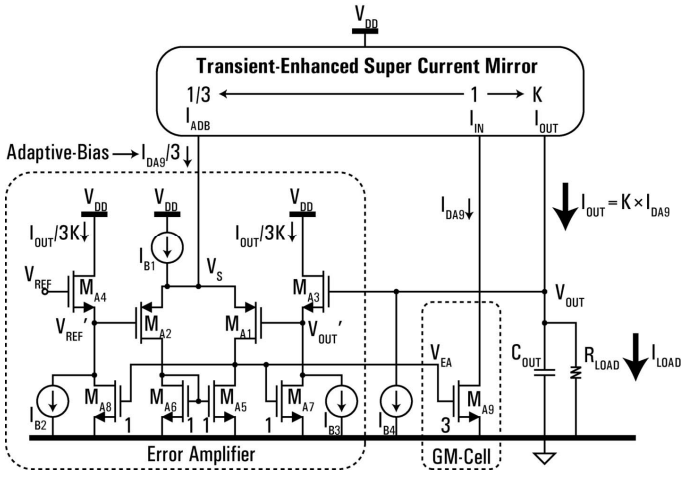

Figure 24.5.1: LDO regulator.

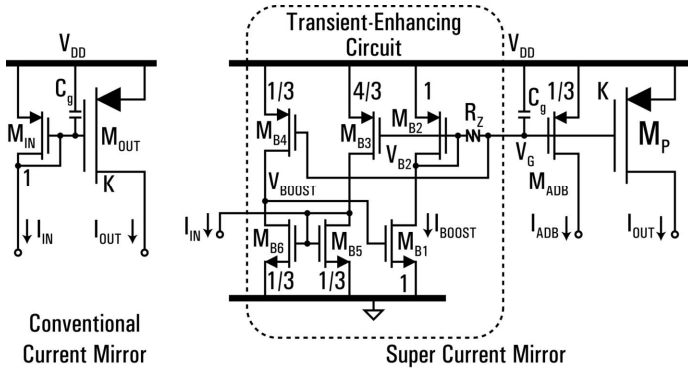

Figure 24.5.2: A conventional current mirror and the super current mirror with the low-voltage transient-enhancing circuit.

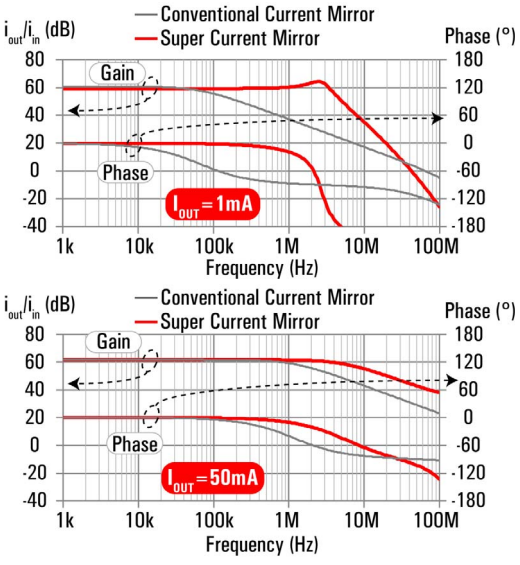

Figure 24.5.3: Frequency response of the super current mirror.

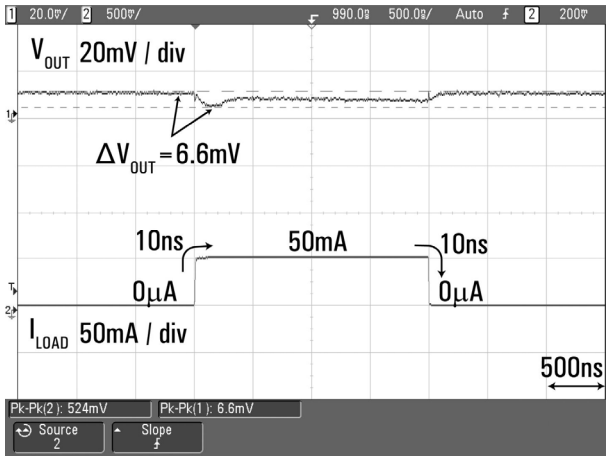

Figure 24.5.4: Measured load transient response.

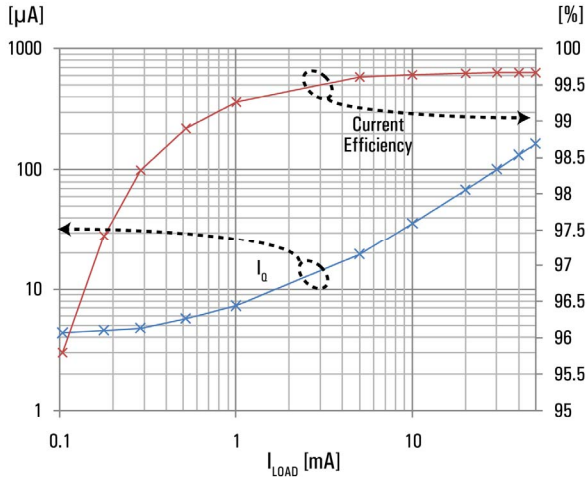

Figure 24.5.5: Measured I_Q versus I_{LOAD} and current efficiency (I_{LOAD}/I_Q) versus I_{LOAD}.

	Unit	[4]	[5]	This Work
Technology	µm	0.09	0.35	**0.35**
Active Area	mm²	0.008	0.264	**0.053**
Minimum V_{DD}	V	1.2	2	**1.05**
Nominal V_{OUT}	V	0.9	1.8	**0.9**
Dropout Voltage	mV	0.3	0.2	**0.15**
Maximum Load	mA	100	200	**50**
Line Regulation @ Maximum Load	mV/V	N. A.	2 (V_{IN}=2–5.5V)	**1.061 (V_{IN}=1.05–3.5V)**
Load Regulation	mV/mA	1	0.170	**0.0614 @ V_{DD}=1.05V 0.0176 @ V_{DD}=3.5V**
Compensation Capacitor	pF	No	10 (On-Chip)	**No**
Decoupling Capacitor	µF	0.0006 (on-chip)	1 (off-chip)	**1 (off-chip)**
I_Q	µA	6000	20 to 320	**4.04 to 164**
PSRR	dB	N. A.	>45 (0Hz to 20kHz)	**>50 (0Hz to 1MHz)**
Current Efficiency	%	94.3	99.8	**99.67**
$\Delta V_{OUT}/V_{OUT}$	V/V	0.09/0.9	0.054/1.8	**0.0066/0.9**
T_R #	µs	0.00054	0.27	**0.132**
FOM #	ns	0.032	0.027	**0.0106**

#Adopted from [4], $T_R=C_{OUT}\times\Delta V_{OUT}/I_{OUT(MAX)}$ and $FOM=T_R\times I_Q/I_{OUT(MAX)}$

Figure 24.5.6: Performance summary and comparison with previously published LDO regulators.

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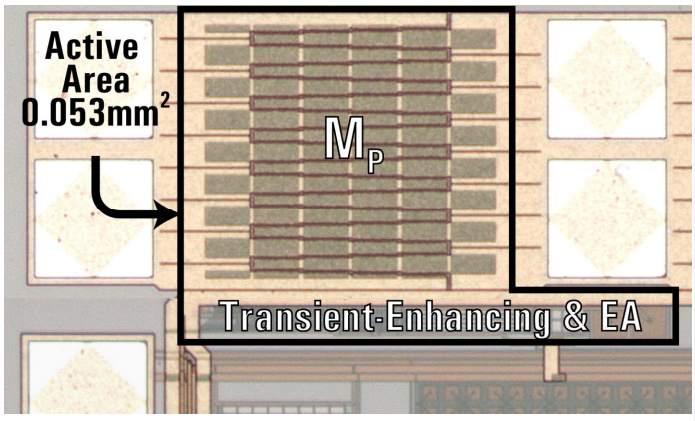

Figure 24.5.7: Die micrograph.

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