A Supply-Noise-Insensitive CMOS PLL With a Voltage Regulator Using DC–DC Capacitive Converter

Chang-Hyeon Lee, *Member, IEEE*, Kelly McClellan, *Member, IEEE*, and John Choma, Jr., *Fellow, IEEE*

***Abstract*—A 500-MHz supply-noise-insensitive CMOS phase-locked loop (PLL) with a voltage regulator using a capacitive dc–dc converter (VRCC) achieves a jitter level of 30-ps RMS for quiet supply, and 42-ps RMS for 600-mV supply noise, with a locking range of 110 to 850 MHz. The worst-case power supply noise rejection (PSNR) using the VRCC shows −45 dB in the mid-frequency band. The circuit is fabricated in a 0.35-μm 3.3-V standard digital CMOS process and occupies 2.3 mm^2. The power consumption at 3.3 V including buffer is 42 mW at 500 MHz.**

***Index Terms*—Clock generator, CMOS phase-locked loop, dc–dc capacitive converter, voltage regulator.**

I. Introduction

NUMEROUS papers have recently addressed the problems surrounding the design of a phase-locked loop (PLL) that is nominally insensitive to power supply noise [1]–[7]. The analog performance of a monolithic PLL suffers from noise almost unavoidably induced on power supply lines due to requisite switching of internal digital subcircuits. This supply-line noise appears as pulses having very steep rising and falling edges, and its effect is to change the frequency and phase of the signal produced by the voltage-controlled oscillator (VCO) in the PLL. The resultant phase error generates a transient impulse response that prevails until the PLL corrects the subject error to the extent that its bandwidth permits. Because the effects of switching-induced power supply noise dominate over those incurred by the routine jitter present on an otherwise quiet supply line [2], it is essential to maximize the power supply noise rejection (PSNR) of the VCO used to establish the frequency of the output clock in a PLL [5].

Several authors have addressed the issue of reducing PLL jitter caused by switching-induced power supply line noise. One technique adopts a source follower coupling approach [1], another exploits an active pMOS cascode configuration [4], and several others advocate the use of voltage regulators [5]–[7]. Unfortunately, these contributions still give rise to observable jitter in the transient response of a PLL because the maximum PSNR recorded in these publications is only −20 dB.

This paper proposes a voltage regulator using a dc–dc capacitive converter (VRCC) to achieve a PSNR in the range of −50 to −40 dB. The VRCC includes a wide bandwidth n-type cascode output stage. Two problems encountered in a cascode topology are diminished headroom and threshold voltage increases precipitated by body effect. A straightforward solution to these problems entails boosting gate voltage, but, unfortunately, boosting techniques using capacitive dc–dc converters introduce switching noise. In this work, minimal converter noise is achieved through both replica biasing of the output stage and the use of passive *RC* lowpass filters.

Other sources of noise, such as thermal noise and shot noise within the ring-type VCO, can be reduced by optimal scaling of transistors in each delay cell. Moreover, increased PLL bandwidths suppress the performance impact of these noise sources. However, since the switching-induced supply noise has a bandpass frequency domain characteristic, the bandwidth of the PLL must be optimized to ensure acceptable levels of overall noise performance. Accordingly, an analysis of the PLL phase noise response, inclusive of switching noise phenomena, is undertaken. The upshot of this analysis is that adequate supply noise desensitization at reasonable signal frequencies mandates only limited increases in PLL bandwidth, together with substantive suppression of the peak amplitudes of supply line noise.

Section II of this work overviews the deleterious effects of supply noise on PLL performance and describes the proposed supply-noise-insensitive phase-locked loop (SNI–PLL) architecture. Section III gives the circuit diagrams associated with this architecture, while Section IV presents the VRCC circuit implementation in silicon. Experimental results verifying the validity and propriety of the adopted design approach appear in Section V.

II. SNI–PLL Architecture

The degree to which the requisite VCO in a PLL is sensitive to power supply noise ultimately determines the achievable performance of a PLL-based clock generator. If the delay cells within the VCO insufficiently reject supply noise, the noise coupled to these cells results in frequency and phase errors than can produce several significantly distorted clock cycles. Since the PLL has a long time constant in comparison to the clock period, many clock cycles are required until the feedback implicit to the PLL is able to correct the frequency and phase errors of the VCO. In

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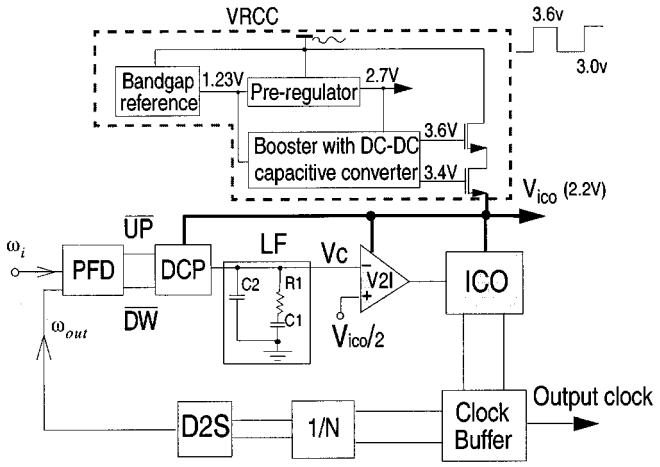

Fig. 1. Block diagram of the supply-noise-insensitive phase-locked loop (SNI–PLL) with voltage regulated capacitive converter (VRCC).

the architecture proposed herein, a differential signal flow path, which inherently possesses a low common-mode noise figure, is adopted to achieve the requisite robustness of power supply noise rejection.

Fig. 1 depicts the system level diagram of the SNI–PLL used in a 500-MHz clock generator.The radial frequency ω_i, which is 2π (50 MHz) in this application and serves as the reference frequency for the phase frequency detector (PFD), derives from a quartz oscillator that is not shown in the diagram. The feedback clock signal, of which the radial frequency is indicated as $\omega_{\rm out}$, is compared to the reference clock for phase and frequency differences. The result of this comparison is that the PFD generates pulse signals $\overline{UP}$ and $\overline{DW}$. These generated signals are applied to the differential charge pump (DCP), whose output port is terminated in a lowpass filter (LF) consisting of a resistance R_1 and two capacitances C_1 and C_2. In turn, the lowpass filter excites a transconductor, or voltage-to-current converter (V2I), whose output controls a current-controlled oscillator (ICO). The ICO is designed for a wide operating frequency range that extends nominally from 110 to 850 MHz. The frequency divider circuit comprised of the interconnection of the indicated clock buffer, a divider $(1/N)$, and a differential-to-single-ended converter (D2S) sets the feedback clock frequency to $1/N$ times the output clock frequency. In this design, $N = 10$.

A. PLL Dynamics

The driving point impedance, say, $Z_{lp}(s)$, of the LF shown in Fig. 1 is

$$Z_{lp}(s) = \frac{1}{s(C_1+C_2)}\left[\frac{1+sR_1C_1}{\frac{1+sR_1C_1C_2}{(C_1+C_2)}}\right]. \tag{1}$$

The loop gain $T(s)$ of the PLL follows as

$$\begin{aligned} T(s) &= \left(\frac{I_{cp}}{2\pi N}\right)\left(\frac{K_v}{s}\right)Z_{lp}(s) \\ &= \left(\frac{I_{cp}}{2\pi N}\right)\left[\frac{K_v}{s^2(C_1+C_2)}\right]\left[\frac{1+sR_1C_1}{\frac{1+sR_1C_1C_2}{C_1+C_2}}\right] \end{aligned} \tag{2}$$

where I_{cp} is the peak current of the charge pump and K_v, in units of radians/V-s, represents the combined gain of the VCO and transconductor. Observe a loop gain double pole at the s-plane origin, a left half plane zero at the frequency

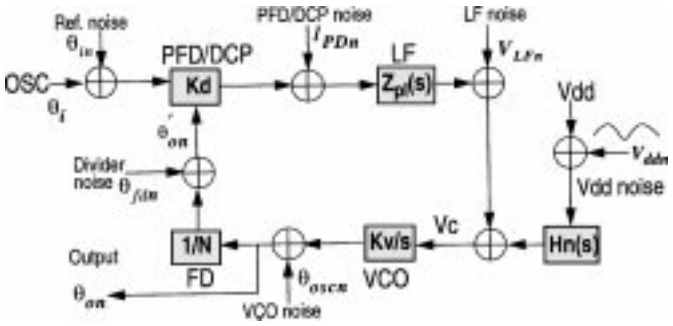

Fig. 2. Noise model of the PLL with all relevant noise sources incorporated.

$$\omega_z = \frac{1}{R_1C_1} \tag{3}$$

and a left half plane pole at the frequency

$$\omega_p = \frac{C_1+C_2}{R_1C_1C_2}. \tag{4}$$

To the extent that $C1 \gg C2$, then $\omega_p \gg \omega_z$ and the unity gain frequency ω_u of the loop gain function can be approximated as

$$\omega_u = \frac{K_vR_1I_{cp}}{2\pi N}. \tag{5}$$

Despite the third-order nature of the loop gain relationship, the corresponding closed loop is stable provided that $\omega_z < \omega_u < \omega_p$, for which $C1 \gg C2$ is a necessary condition. In view of the presumption of large ω_p, the characteristic polynomial $1+T(s)$ of the closed loop approximated as a second-order system provides an undamped natural frequency ω_n and damping factor ζ, given respectively by

$$\omega_n = \sqrt{\omega_u\omega_z} \tag{6}$$

and

$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_u}{\omega_z}}. \tag{7}$$

If the closed loop were to be designed for maximally flat frequency response, $\omega_u = 2\omega_z$, the natural frequency, therefore, is now identical to the closed loop bandwidth, of $\omega_n = \sqrt{2}\omega_z$.

B. PLL Noise Analysis

The PLL noise model, inclusive of supply noise phenomena, is shown in Fig. 2. In the locked condition, the output phase noise $\theta_{\rm on}$ of the loop is expressible conceptually as

$$\begin{aligned} \theta_{\rm on} = \frac{K_v}{s}\Bigg\{ Z_{lp}(s)\left[\frac{I_{cp}}{2\pi}\left(\theta_{\rm in} - \frac{\theta_{\rm on}}{N} - \theta_{\rm fdn}\right) + I_{\rm PDn}\right] \\ + V_{LFn} + H_n(s)V_{ddn}\Bigg\} + \theta_{\rm oscn} \end{aligned} \tag{8}$$

where

$\theta_{\rm in}$	output noise of the reference oscillator;
$\theta_{\rm oscn}$	output noise of the controlled oscillator;
$\theta_{\rm fdn}$	noise of the frequency divider (FD);

$I_{\rm PDn}$ noise attributed to the phase frequency detector and differential charge pump (PFD/DCP);
V_{ddn} voltage supply line noise;
$H_n(s)$ transfer function from the power line to the VCO control voltage.

It has been assumed in this analysis that all noise sources are uncorrelated. The resultant mean square output noise can be shown to be

$$\theta^2_{\rm on}(j\omega) = \left|\frac{\frac{T(j\omega)}{N}}{1+T(j\omega)}\right|^2 \cdot \left[\theta^2_{\rm in}(j\omega) + \theta^2_{\rm fdn}(j\omega) + \left(\frac{2\pi I_{\rm PDn}(j\omega)}{I_{cp}}\right)^2\right] + \frac{\theta^2_{\rm oscn}(j\omega)}{|1+T(j\omega)|^2} + \left|\frac{\frac{K_v}{j\omega}}{1+T(j\omega)}\right|^2 \cdot \left[V^2_{LFn}(j\omega) + |H_n(j\omega)|^2 V^2_{ddn}(jw)\right] \quad (9)$$

where $T(j\omega)$ derives from the loop gain $T(s)$, given by (2). Note in this expression that the frequency spectrum of the reference oscillator noise and the noise attributed to the PFD/DCP is that of a lowpass filter characteristic. On the other hand, the VCO and supply noise contributions follow highpass and bandpass frequency domain responses. In order to minimize the effects of the noise $\theta_{\rm oscn}$ of the VCO, the loop bandwidth must be as wide as possible. Within the loop bandwidth, the in-band noise contributed by the other loop components must therefore be minimized. However, the loop bandwidth should be less than the reference input frequency in order to enable a stable loop that suppresses the spurious frequencies generated by the reference leakage signal. Accordingly, optimal loop design necessarily entails a loop bandwidth tradeoff that achieves low in-band phase noise within the constraint of sufficiently low spurious frequency responses.

The multiorder time-domain equations relating the oscillator control voltage $V_c(t)$ to the net effective power line voltage $V_{dd}(t)$ are deduced from computer-based simulations of the VRCC. These equations comprise the basis for determining the transfer function $H_n(s) = V_c(s)/V_{dd}(S)$, the frequency domain locations of its concomitant poles and zeros, and the resultant contribution of power supply noise to the overall noise properties of the loop. The frequency spectrum of this supply noise, as shown in Fig. 3, has bandpass characteristics and, thus, both the low- and high-frequency noise components are attenuated. The suppression of mid-frequency noise requires a large PLL bandwidth, as well as suitable isolation between parasitic noise coupling and the signal path. The proposed VRCC achieves this requisite isolation with respect to both the control voltage of the loop filter and the power supply of the delay cells implicit to the VCO. By replacing the functional blocks of the PLL with idealized controlled sources, computer-based analyses prescribe that such isolation, as well as transient response and loop stability, are optimized to first order by selecting ω_u in (5) and ζ in (7) to be 1.1 and 1.5 MHz, respectively.

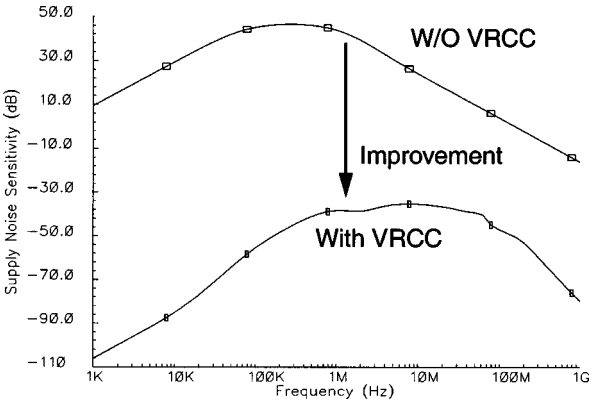

Fig. 3. Supply noise sensitivity of the SNI–PLL, with and without the VRCC.

III. PLL Blocks

The PLL proposed in this work is comprised fundamentally of a phase frequency detector (PFD), differential charge pump (DCP), voltage-to-current $(V$–$I)$ converter, replica bias cell, and a current-controlled oscillator (ICO).

A. PFD, DCP, and V–I Converter

A type-four PFD with D-type flip-flop and RS latch is incorporated in the design [8]. This detector monitors phase and frequency error between the reference clock and the feedback clock. The PFD generates $\overline{UP}$ and $\overline{DW}$ signals when the feedback clock lags or leads, respectively, the reference clock. To minimize peak-to-peak jitter, it is essential to minimize any dead zone between the generated signals producing a delay through the reset path in [12]. In the locked condition, this delay subcircuit generates a minimum pulse when both the reference and feedback clock pulses are in phase.

In the locked state, a mismatch between the $\overline{UP}$ and $\overline{DW}$ current source responses results in current leakage into the loop filter. This periodic effect conduces sideband frequency components at the output. When the $\overline{UP}$ and $\overline{DW}$ switches are in transition between on and off states, charge injection and clock feedthrough result in a control voltage error that perturbs the oscillation frequency and phase angle of the VCO. The charge pump shown in Fig. 4(a) prevents $\overline{UP}/\overline{DW}$ switching noise from coupling into the loop filter through the incorporation of constant voltage sources at the input stages. In contrast, conventional charge pumps are plagued with switching noise problems caused by charge sharing and clock feedthrough because $\overline{UP}$ and $\overline{DW}$ digital signals are applied directly to the lowpass filters [3]–[8]. The differential loop filters are replaced by a single-ended lowpass filter (LF) and a constant voltage reference. This replacement, which conserves silicon area, has the same benefits as differential filters because the single-ended LF and the voltage reference are connected to the same power supply rail and, therefore, both experience the same noise excitation.

Because the regulated supply voltage can be as low as 2.2 V, a V–I converter with a rail-to-rail differential input stage, as shown in Fig. 4(b), is required for sufficient common mode voltage. Transistors *M1* and *M2* establish a constant current

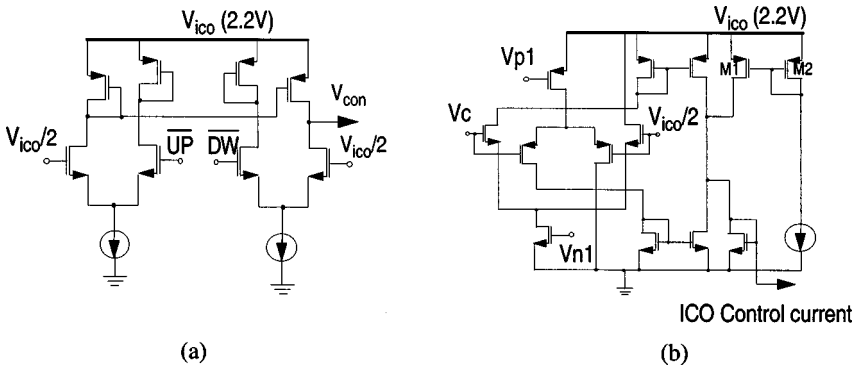

Fig. 4. (a) Schematic representation of the differential charge pump (DCP). (b) Schematic representation of the voltage to current converter (V2I).

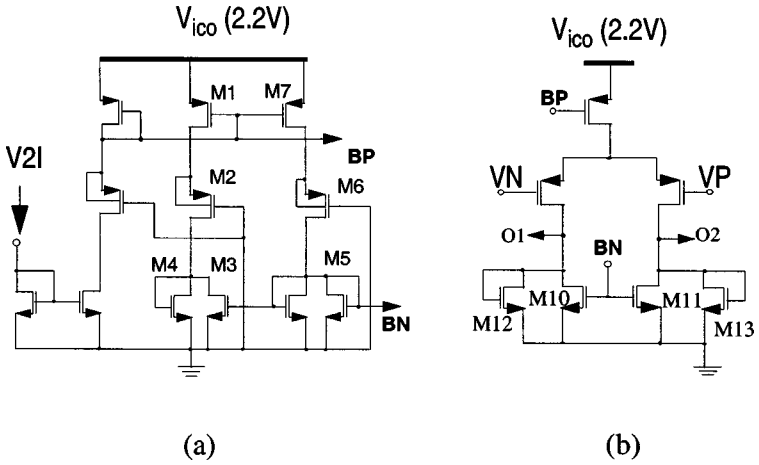

Fig. 5. (a) Schematic diagram of the replica bias subcircuit for the VCO. (b) Schematic representation of the delay cell for the VCO.

source for the center frequency when the difference voltage applied to the differential input stage of the V–I converter is zero. This current source sets the center frequency of the PLL output to the frequency tuning range. The operating frequency is determined by adding current to, or subtracting current from, the constant current, depending on the difference voltage detected at the input port of the differential input stage.

B. Replica Bias Circuit and ICO

Both the signal and control paths of the ICO must be differential if high rejection of supply and substrate noises is to be realized. It follows that the supply noise and the substrate noise are attenuated by the VRCC and the differential delay unit, respectively. In Fig. 5, variable resistances are implemented by the triode region biasing of transistor *M3* [2]. The value of this resistance is controlled by the replica bias circuit comprised of *M5–M7*, which produces the exact gate voltage commensurate with setting the output common mode voltage of the delay cell. The cell bias current controls the delay cell to determine the ICO operating frequency and the nMOS drain–source voltage required to prevent the nMOS loads from leaving their triode regions. This operating requirement derives from exploiting appropriate gate aspect transistor ratios in the diode connected current mirror and delay cell [8]. The output voltage swing is maintained constant by varying the active resistance of the loads in such a manner that the variation is inverse to the observed current change. If the loads were fixed passive resistors, the ICO delay cell would suffer progressively decreased gain from decreased bias, thereby giving rise potentially to an ICO with insufficient gain to sustain oscillation. Minimal jitter in each delay cell mandates a delay cell gain that is as small as possible within the constraint of satisfying the oscillation condition [11].

IV. Voltage Regulator

Fig. 6 abstracts the block diagram of the VRCC, in which is embedded a low-dropout preregulator (LDOPR), a capacitive charge pump (CCP), a clock generator (CG), several operational amplifiers (OPs), and nMOS cascode output transistors. The supply voltage perturbations are regulated by the noise rejection-enhanced LDOPR, which establishes a constant voltage for the charge pump, the clock generator, and the operational amplifiers (OP2). Since the OP2s are energized from a supply voltage that derives from the preregulator output, their responses are relatively immune to supply voltage changes on the main power bus. The slow response time precipitated by several capacitors within both loops in Fig. 6 renders good regulation difficult for boosted voltages. Accordingly, the LDOPR supplies 20 dB of supply noise attenuation for the clock generator, charge pump, and the two operational amplifiers labeled OP2.

An n-channel output stage boasts higher power supply noise rejection than does a p-type output stage [1]. Although both are connected in common-gate configuration, the nMOS provides a higher impedance, therefore better isolation to the supply than

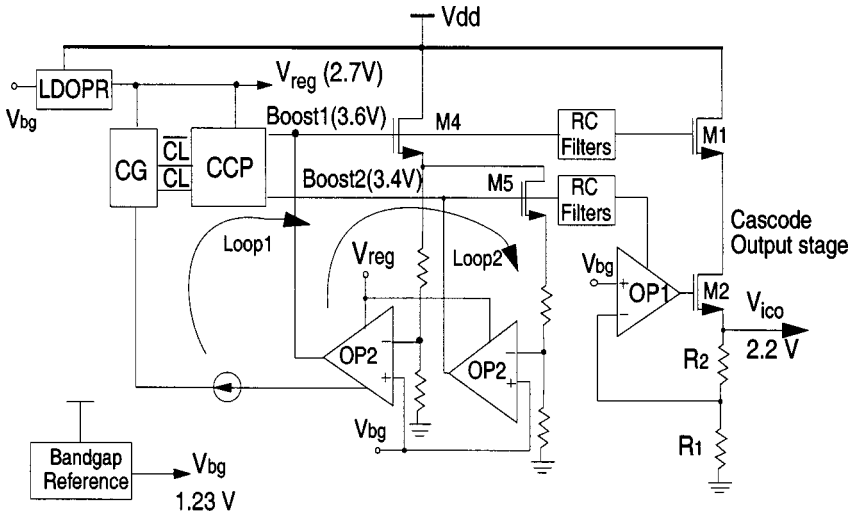

Fig. 6. A voltage regulator using a capacitive dc–dc converter.

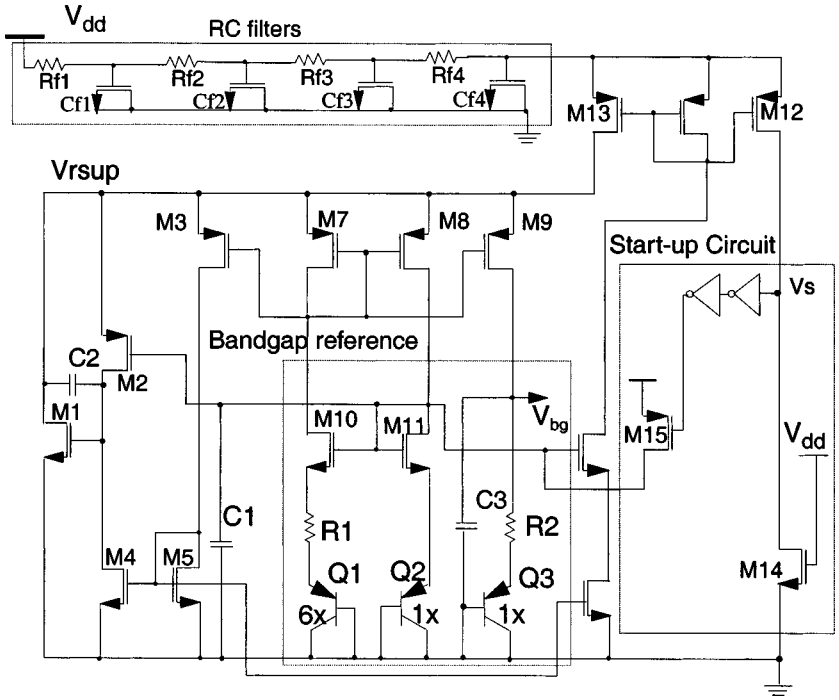

Fig. 7. Supply-noise-insensitive bandgap reference with *RC* lowpass filters.

pMOS. However, the body effect indigenous to the inherent n-well architecture of most CMOS digital processes increases the threshold voltage of the transistors utilized in the n-type output stage. This situation requires boosting the voltage levels of the output stage by several hundreds of millivolts in order to ensure sufficient voltage headroom for subsequent analog topologies.

A. Bandgap Reference

The *RC* passive filter comprised of the R_{f1}–R_{f4} and $C1$–$C4$ filter sections in Fig. 7 attenuate supply noise at frequencies larger than the response capability of the bandgap reference circuit. As such, these filter sections respond to the commonly encountered problem that most regulators are unable to reject high-frequency input noise because of limitations incurred by frequency rolloff of the loop. Input noise is therefore rejected over a large frequency interval by both the low-frequency rejection capability of the voltage regulator and the high-frequency rejection characteristics of the passive filter. The bandgap reference voltage for biasing the regulator and other subcircuits is insensitive to temperature and power supply voltage variations.

The voltage drop through the *RC* filters is minimized to preclude limiting the headroom of the bandgap reference. To this end, a 10-μA quiescent current yields a headroom in the range of 300–400 mV. An approximate voltage gain of 80 dB within the bandgap configuration, which derives from transistors *M1* and *M2*, ensures adequate supply noise attenuation with a self-regulated supply line $(V_{r\,\mathrm{sup}})$ at low frequencies.

The regulated supply line voltage of $V_{r\,\mathrm{sup}} = 2.3$ V delivers a bandgap output voltage of $V_{\mathrm{bg}} = 1.23$ V. Startup reliability is

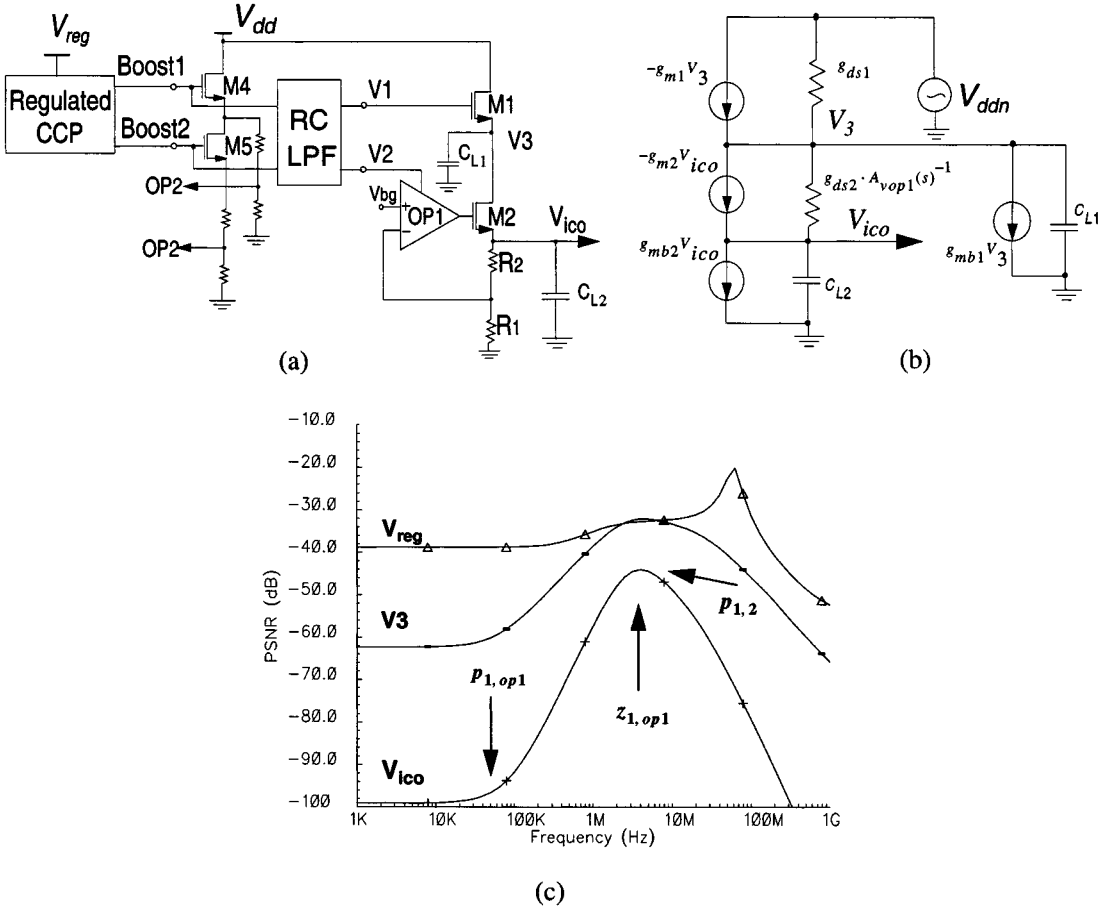

Fig. 8. (a) System level diagram of the proposed implementation of robust high-frequency power supply noise rejection. (b) Simplified small-signal model of the output stage. (c) Simulated frequency response of the noise rejection system.

ensured because the voltage V_{dd} always forces transistor *M14*, which has a small gate aspect ratio, to conduct. This conduction forces current through *M12*, which is biased in its triode regime. Biasing in the triode region constrains the source–drain voltage so that the drain output voltage of *M12* is sufficiently large to switch off M15 through the two inverters shown in Fig. 7. The high voltage gain of the two inverters subsequently enhances the startup of the bandgap reference circuit. The bipolar p-n-p transistors *(Q1–Q3)* shown in the diagram derive as parasitic elements implicit to the CMOS process.

B. Cascode Output Stage

The stacked n-channel transistors (*M1–M2*) in the diagram of Fig. 8(a) establish robust power supply noise rejection by boosting the impedance with OP1 to the power supply with the constant bias voltages V_1 and V_2. These voltages are Boost1 and Boost2 with high-frequency switching noise (produced by the capacitive charge pump) filtered out by an *RC* lowpass filter. On the other hand, the low-frequency noise spectra lying within the operational amplifier passband is attenuated by the negative feedback invoked around this amplifier. It is necessary to have a 200-mV voltage difference between the indicated Boost 1 and Boost 2 ports to prevent saturation of transistor *M2*. The resultant worst-case power supply noise rejection at 20 MHz is found to be −45 dB.

Fig. 8(b) is the small-signal equivalent circuit for estimating the PSNR of the network offered in Fig. 8(a). A first-order analysis of this model reveals a transfer function $V_{\rm ico}(s)/V_{ddn}(s)$, which can be interpreted as a measure of the power supply noise rejection with respect to the V_{dd} supply line, of

$$\frac{V_{\rm ico}(s)}{V_{ddn}(s)} \approx \left(\frac{1}{A_{\rm vop1}}\right)\left(\frac{g_{\rm ds2}}{g_{m1}-g_{mb1}}\right)\left(\frac{g_{\rm ds2}}{g_{m2}-g_{mb2}}\right) \cdot \left[\frac{\left(1+\frac{s}{P_{\rm 1op1}}\right)}{\left(1+\frac{s}{P_1}\right)\left(1+\frac{s}{P_2}\right)\left(1+\frac{s}{z_{\rm 1op1}}\right)}\right]. \quad (10)$$

In (10), $g_{\rm ds1}$, g_{m1}, and g_{mb1} respectively symbolize the small-signal drain–source conductance, forward transconductance, and bulk transconductance of transistor *M1*, $g_{\rm ds2}$, g_{m2}, and g_{mb2} are the counterpart parameters of transistor *M2*, $A_{\rm vop1}$ is the low-frequency voltage gain of operational amplifier OP1, $p_{\rm 1op1}$ and $z_{\rm 1op1}$ are the dominant pole and zero frequencies of OP1, and finally

$$P_1 = \frac{g_{m1}-g_{mb1}}{C_{L1}} \quad (11)$$

and

$$P_2 = \frac{g_{m2}-g_{mb2}}{C_{L2}}. \quad (12)$$

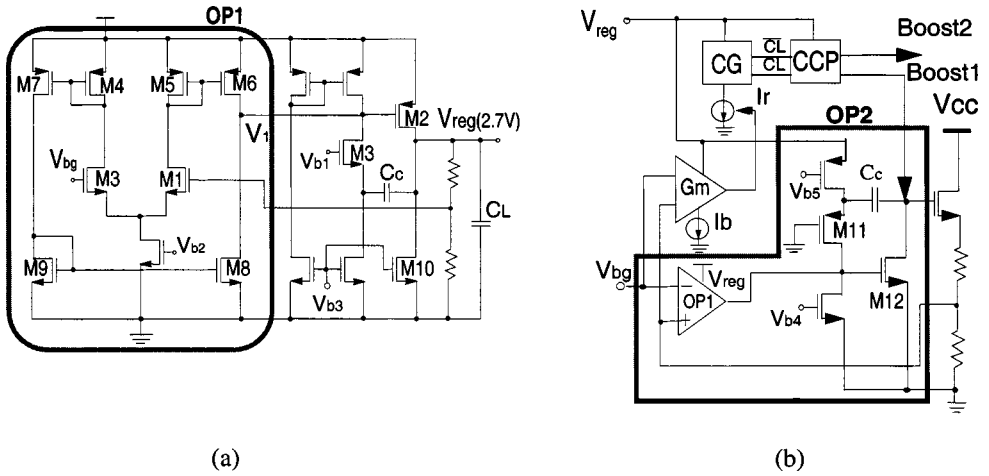

Fig. 9. (a) Schematic diagram of low dropout preregulator (LDOPR) with enhanced power supply noise rejection. (b) Schematic diagram of the operational amplifier (OP2) and transconductance stage with enhanced power supply noise rejection.

Fig. 8(c) displays the resultant PSNR frequency responses for the boosted voltages, the preregulator, and the clock generator. The observed peaking of the regulator response in the neighborhood of 70 MHz is caused by complex poles in the transfer function of the preregulator. This peaking can be reduced substantively by increased load capacitance.

C. LDO Preregulator (LDOPR) and Operational Amplifier

The power supply rejection ratio in conventional operational amplifiers is improved through use of the grounded gate cascode compensation technique, as shown in Fig. 9(a) [13]–[15]. Because the source terminal of transistor *M3* is a virtual ground at the left terminal of the compensation capacitance $C_{\rm c}$, the indicated voltage V_1 is insensitive to power supply noise. The displacement current $C_{\rm c}dv_{\rm reg}(t)/dt$ conducted by capacitor $C_{\rm c}$ flows into the source of *M3* and thence from the drain terminal of *M2*. In effect, this conduction path cancels the dynamic effects of the feed-forward path that arises from $C_{\rm c}$ in the absence of transistor *M3*.

If the drain–source channel conductances of transistors *M6, M7, M8,* and *M9* are nominally equivalent and if the forward transconductance of transistor *M2* is significantly larger than the channel conductance of *M2*, the positive supply rejection ratio (PSRR) can be shown to be

$$\mathrm{PSRR} \approx \frac{g_{m1}}{2g_{\rm ds8}} \tag{13}$$

where g_{m1} is the forward transconductance of *M1* and $g_{\rm ds8}$ is the drain–source channel conductance of *M8*. In the closed-loop configuration, the corresponding ripple, say, $V_{\rm or}$, in the regulated output voltage can be estimated in accordance with

$$V_{\rm or} \approx \frac{1}{f} \cdot \left(\frac{V_{ddr}}{\mathrm{PSRR}} + V_{\rm bgr} \right) \tag{14}$$

where f is the feedback factor associated with the two resistances appearing in the source lead of the output transistor, and V_{ddr} and $V_{\rm bgr}$, respectively, represent the ripple voltage on the voltage supply line and the bandgap reference output port.

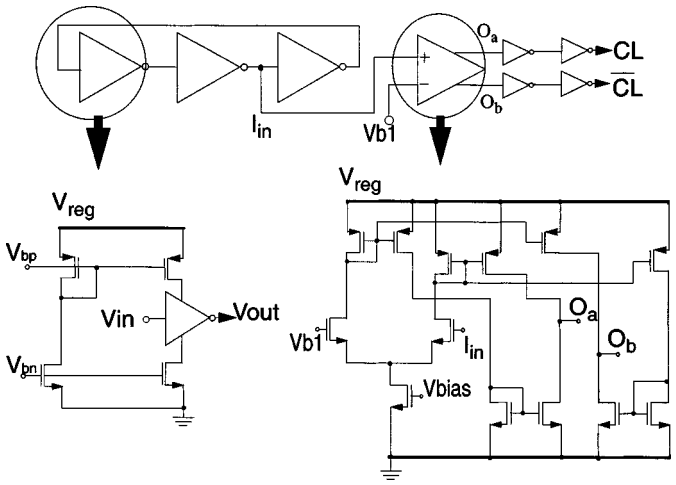

Fig. 10. (a) Schematic diagram of the inverter delay cell used in the clock generator (CG) circuit for purposes of voltage boosting. (b) Schematic diagram of the differential clock generator circuit.

The two most dominant poles of the circuit are widely spaced and set by the load capacitance $C_{\rm L}$ and the compensation capacitance $C_{\rm c}$. In order to reap the stability benefits of at least a 60° phase margin, the frequency $g_{m2}/C_{\rm L}$ of the second of these poles must be approximately 2.2 times larger than the frequency $g_{m1}/C_{\rm c}$ of the unity-gain bandwidth.

The operational amplifier in Fig. 9(b) also boasts operating efficiency with respect to dynamic power dissipation. This efficiency stems from an amplifier transconductance that is dependent on bias current. The operating frequency of the clock generator is determined by the static current I_r. This frequency varies from its maximum value at $I_r = I_b$ to its minimum value at $I_r = I_b/2$. It follows that the power dissipated by the capacitive charge pump is reduced by a factor of two.

D. Clock Generator

The clock generator consists of three inverters and a differential subcircuit having a regulated supply voltage, as is depicted in Fig. 10. The frequency range of the clock is 10–150 MHz for biasing currents of 1–5μA. The oscillation frequency sensitivity to clock supply is reduced by the preregulator. Since the

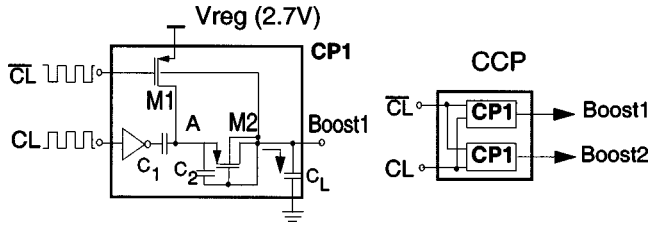

Fig. 11. Proposed capacitive charge pump circuit.

boosted output voltage is a function of the clock output swing, the preregulator voltage $V_{\rm reg}$ maintains constant output clock amplitude.

E. Voltage Booster

The booster generates an independent power supply voltage that is larger than that of the normal supply. Conventional voltage boost circuits use a transformer, which is heavy, expensive, and plagued by low conversion efficiency. The principle attributes of a charge pump dc–dc converter are small size and reasonably high conversion efficiency. However, capacitive voltage boost circuits suffer at least two drawbacks. First, the booster output voltage is unregulated and is a sensitive function of its input voltage. Second, the output voltage is temperature dependent.

Most of the currently utilized voltage boost circuits derive from a circuit proposed by Dickson [17]–[22]. Unfortunately, the Dickson circuit is not suitable for the low-voltage operation mandated by n-well CMOS processes that feature channel lengths smaller than 0.35 μm. Moreover, insufficient power supply rejection, power supply regulation, temperature sensitivity, and operating power efficiency plague the Dickson topology. A circumvention of these operating shortfalls requires that the input supply voltage be replaced by the preregulator output voltage to maintain constant clock swing at the booster pump. The performance of the proposed capacitive charge pump shown in Fig. 11 is optimized at an output voltage of 3.6 V, which is smaller than the nominal 4-V gate breakdown indigenous to the utilized 0.35-μm CMOS process. The multiplied clock voltage at Node "A" is not applied directly to the transistor gate; rather, it is applied to the drain, which is characterized by higher breakdown limits. Additional breakdown protection is provided by the exclusive use of pMOS transistors, whose breakdown voltages exceed those of nMOS devices in an n-well process.

Observe that the multiplied clock voltage at Node "A" can turn on transistor *M1*, thereby reversing source and drain and establishing a means of pumping charge back into the nominal power supply. This reversed pump charge, which degrades power efficiency, can be minimized by embedding a PN junction diode between Node "A" and the drain terminal of transistor *M1*. The engineering price paid for incorporating the diode is an approximate 800-mV reduction in voltage headroom.

Ignoring the 1-μA current that is used to bias OP1 as shown in Fig. 8(a), the capacitive charge pump establishes an output voltage $V_{\rm out}$ that can be approximated as

$$V_{\rm out} \approx \left(1 + \frac{C_1}{C_1 + C_2}\right) V_{\rm reg} - V_D \qquad (15)$$

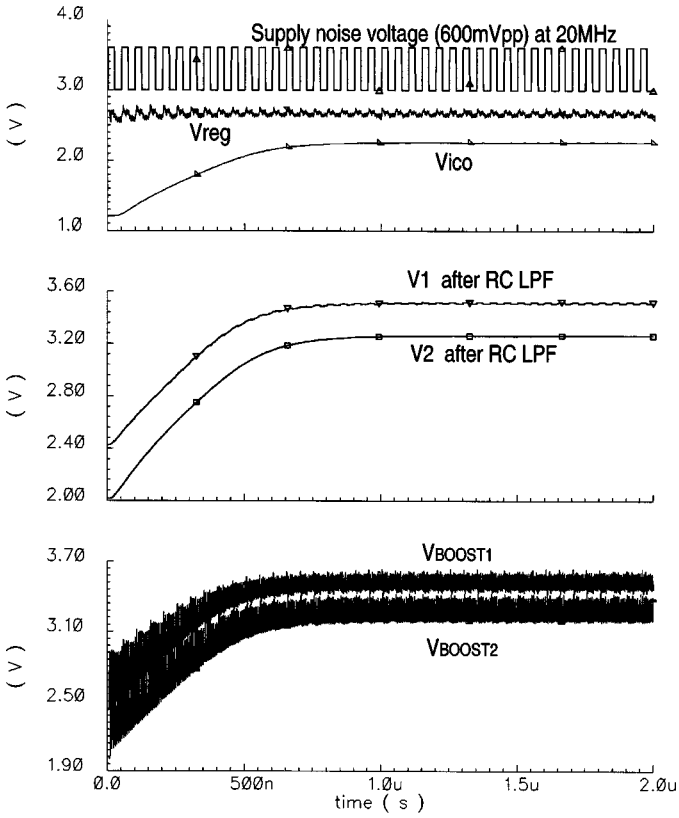

Fig. 12. Simulated transient response of the voltage regulated charge pump in the face of a parasitic square-wave signal superimposed on the power supply line.

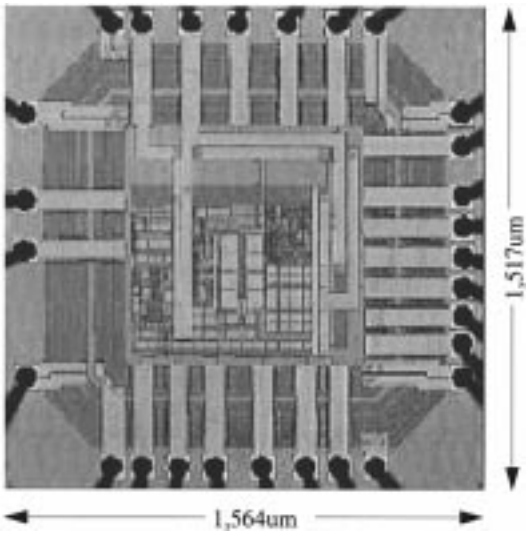

Fig. 13. Photomicrograph of the fabricated PLL chip.

where

- $V_{\rm reg}$ input supply voltage from the preregulator;
- C_1 clock coupling capacitance;
- C_2 parasitic capacitance;
- V_D forward turn on voltage of the diode-connected pMOS (M2).

To the extent that diode voltage V_D is nominally constant, (15) confirms that the change in output voltage with respect to fluc-

TABLE I
MEASURED PERFORMANCE SUMMARY OF THE FABRICATED PLL

PLL die area	*2.2 mm*^{2}(with buffer/ loop filters)
Power dissipation (Vdd=3.3)	*45 (mW)* at 500MHz (with buffer)
Static phase error	*< 60ps*
Lock in time (30MHz-50MHz jump)	*10.8us*
Bandwidth	*1.1MHz*
Phase Margin	*65* (deg.
VCO dc power supply sensitivity	*20* (ps/V)
Jitter1 (quiet supply)	*30ps* RMS (at 500MHz)
Jitter2 (600mV 20MHz square wave on the power supply)	*42ps* RMS (at 500MHz)
Operating frequency range	*110-850 (MHz)*
Device Technology	0.35um 3M/1P CMOS n-well

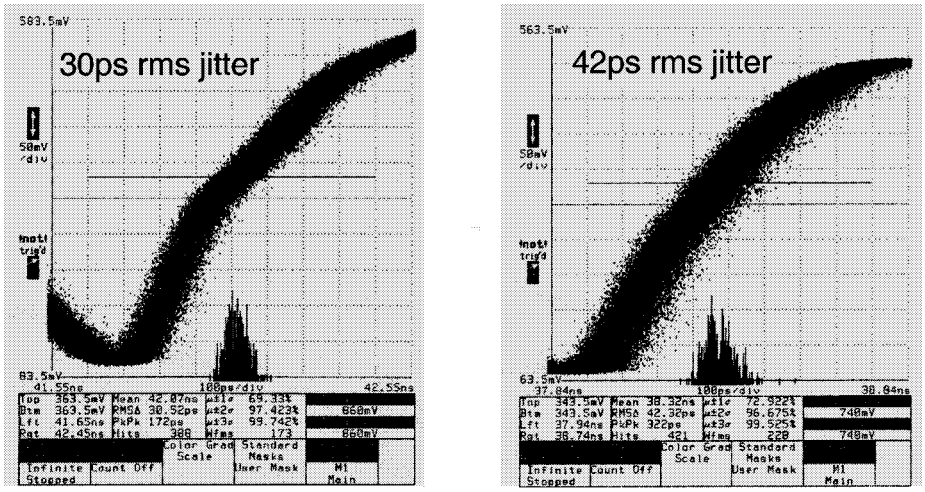

Fig. 14. (a) Measured jitter for the case of a quiet supply line. (b) Measured jitter for the case of a 600-mV 20-MHz, square wave incident with the power bus.

tuations in the power line voltage V_{dd} is as good as is the power supply noise regulation of the regulator voltage $V_{\rm reg}$.

Fig. 12 depicts a worst-case time-domain simulation wherein noise in the form of a 600-mV peak-to-peak 20-MHz square wave is superimposed on the 3.3 V power line voltage. The preregulator attenuates this supply voltage fluctuation to several tens of millivolts. The capacitive charge pump converts the noisy line voltage to a 3.6-V level at Boost 1 and a 3.4-V level at Boost 2, where it is understood that switching noise prevails at both of these boosted ports. These levels are prescribed by internal resistance ratios and by the bandgap reference voltage. The boosted voltage $V_{\rm ico}$ at the output of the *RC* filter is relatively "clean" in that the noise-induced variations about the nominal value of $V_{\rm ico}$ are under several microvolts.

Because the *RC* filter incurs minimal input-to-output voltage drop, the next cascode stage is biased the same as its predecessor. The output response of the filter, which is applied to the gate of the nMOS output transistor, sharply attenuates the high-frequency switching noise associated with the 100-MHz clock generator. The drain–gate capacitive path from the power supply to the nMOS output transistor gate is effectively blocked by the enhanced impedance provided by the stacked cascode transistors. As the output voltage of the charge pump increases to the regulated voltage, the operating frequency decreases in proportion to the control current I_r, which is diminished by the transconductance amplifier. Accordingly, power dissipation in the charge pump and clock generator is reduced.

V. SIMULATION AND MEASUREMENT RESULTS

The experimental prototype of the design proposal has been implemented in a 0.35-μm TSMC CMOS process. The SNI–PLL circuit, of which the photomicrograph is offered in Fig. 13, contains 580 transistors, 120 resistors, and 50 capacitors that collectively consume an area of 1564 $\times$1517 μm^2. The chip is packaged in a 44-pin leadless chip carrier. Table I summarizes the relevant performance indices of the PLL system.

Fig. 14 shows that the measured RMS cycle-to-cycle jitter is 30 ps ($\pm$ 86 ps peak-to-peak) with a quiet supply and 43-ps RMS ($\pm$ 161 ps peak-to-peak) in the presence of a 600-mV

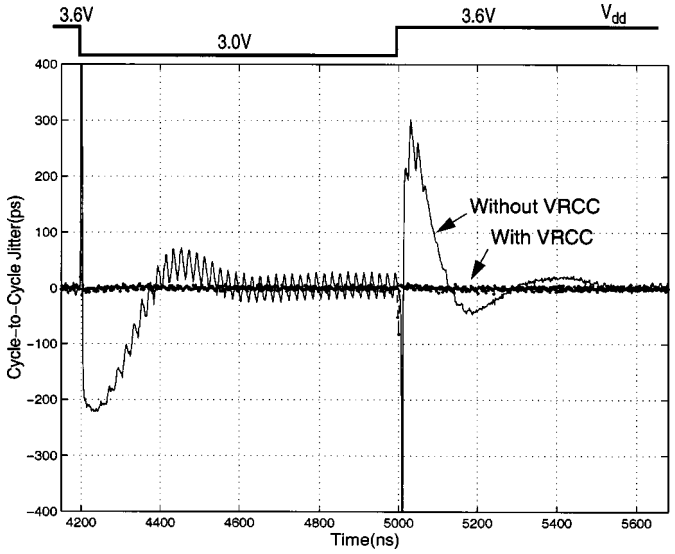

Fig. 15. Simulated jitter for the case of a 600-mV 20-MHz, 1 ns rise/fall time square wave incident with the power bus.

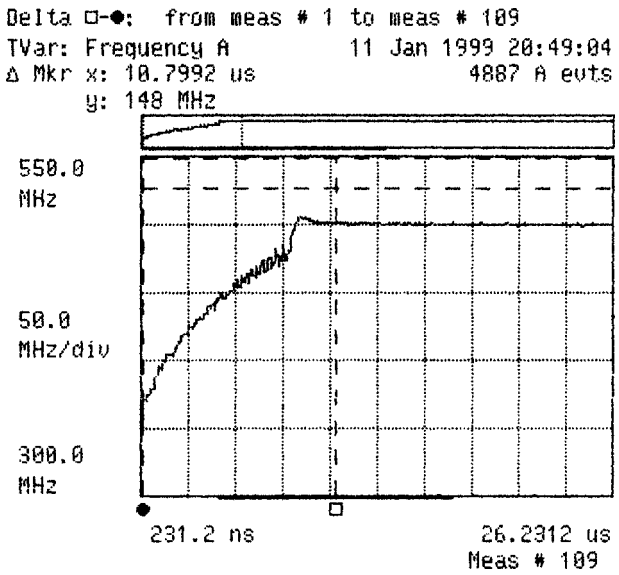

Fig. 16. Measured locking time of the fabricated PLL.

20-MHz square-wave supply noise. In contrast, the simulated cycle-to-cycle jitter due to a 600-mV step with 1-ns rise and fall times imposed on the supply line is $\pm$ 86 ps peak-to-peak with the VRCC and $\pm$ 230 ps peak-to-peak without the VRCC, as is depicted in Fig. 15. When the reference clock is switched from 30 to 50 MHz, the measured locking time is 10.8 μs, as shown in Fig. 16. The power consumption of the entire PLL system is 42 mW at 500 MHz. The PLL operates at an external reference frequency in the range of 110 to 850 MHz with a 49.8% duty cycle.

VI. Conclusion

The SNI–PLL described, analyzed, and designed in this work has been implemented monolithically in a 0.35-μm CMOS process with a total chip area of about 2.3 mm^2. All experimental results corroborate well with corresponding analytical disclosures. The subject chip includes a type-four phase frequency detector boasting small dead band, a charge pump with minimized switching noise, a voltage-to-current converter, lowpass filters, frequency divider circuitry, a voltage regulated dc–dc capacitive regulator, a current-controlled oscillator having reduced thermal noise, output buffers, and electrostatic device protection appended to each pin of the packaged chip. Seven separate power supplies, each with a separate ground pin, are used on chip to discourage coupling of digital switching noise into analog signal paths. The voltage regulated capacitive regulator achieves -45 dB of power supply noise rejection to ensure the delivery of noise insensitive power to analog cells that are constrained to operate in noisy environments.

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