A 6-μW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology

Jianping Guo, *Student Member, IEEE*, and Ka Nang Leung, *Senior Member, IEEE*

***Abstract*—An output-capacitorless low-dropout regulator (LDO) compensated by a single Miller capacitor is implemented in a commercial 90-nm CMOS technology. The proposed LDO makes use of the small transistors realized in nano-scale technology to achieve high stability, fast transient performance and small voltage spikes under rapid load-current changes without the need of an off-chip capacitor connected at the LDO output. Experimental result verifies that the proposed LDO is stable for a capacitive load from 0 to 50 pF (estimated equivalent parasitic capacitance from load circuits) and with load capability of 100 mA. Moreover, the gain-enhanced structure provides sufficient loop gain to improve line regulation to 3.78 mV/V and load regulation to 0.1 mV/mA, respectively. The embedded voltage-spike detection circuit enables pseudo Class-AB operation to drive the embedded power transistor promptly. The measured power consumption is only 6 μW under a 0.75-V supply. The maximum overshoot and undershoot under a 1.2-V supply are less than 66 mV for full load current changes within 100-ns edge time, and the recovery time is less than 5 μs.**

***Index Terms*—Capacitor-less, low-dropout regulator (LDO), nano-scale technology, transient response.**

I. Introduction

RECENT development of output-capacitorless low-dropout regulator (OCL-LDO) realizes on-chip, local voltage regulation [1] to enable more effective integrated power management for System-on-a-Chip (SoC). Parasitic effects such as bond-wire inductance and resistance due to the external connections with passive components existing in the classical non-OCL-LDO can all be eliminated. In addition, the chip area occupied by the I/O pads for connecting with external passive components is no longer required so that the function-to-area ratio of the SoC with integrated power management can be significantly improved. Due to these reasons, many OCL-LDOs were proposed [2]–[11]. In the prior works, loop stability and load-transient response of the OCL-LDOs are regarded as important design issues. Frequency-compensation approaches for enhancing the loop bandwidth, as well as the closed-loop stability, and dynamic-biasing methods for solving the serious slew-rate limit problem at the gate of the integrated power transistor are two key aspects currently under extensive investigation.

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The authors are currently with the Department of Electronic Engineering, Chinese University of Hong Kong, Shatin, Hong Kong SAR, China (e-mail: jpguo@ee.cuhk.edu.hk; knleung@ee.cuhk.edu.hk).

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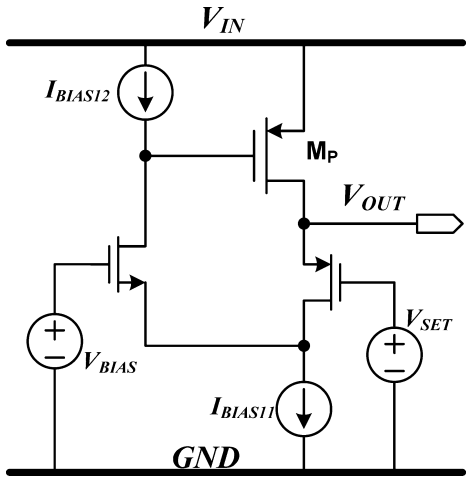

Fig. 1. Prior work: LDO structure based on FVF [3], [7], [10], [11].

With forecasting that more SoC will be implemented by ultra-small-scale technologies in the next decade, the impacts, either positive or negative, of the nano-scale technology on the OCL-LDO design cannot be overlooked anymore. Unfortunately, most of the foregoing OCL-LDO designs are not implemented in nano-scale technologies, except one fully-integrated 50-mA LDO design implemented in 90-nm CMOS technology reported in 2005 [3]. This design consumes a quiescent current (I_Q) of 6 mA and is stabilized by a 0.6-nF on-chip capacitor. The load regulation under voltage positioning is 90 mV/50 mA. The performance of this LDO design reveals that the design challenges of OCL-LDO in nano-scale technology are (1) enhancement of loop gain for better load regulation, (2) optimization of quiescent current for power saving, and (3) minimization of on-chip capacitance for chip-area reduction.

The recently reported OCL-LDO structures are based on a LDO reported in [3], [7], [10] and [11], as shown in Fig. 1. The core is a flipped voltage follower (FVF) [12]. The stability of this LDO structure has been proven stable under the absence of an off-chip capacitor. However, the large-signal response under the low- I_Q condition limits the transient response, and thus dynamic biasing was proposed in [7] and [11]. When the LDO is implemented in nano-scale technology, both the small-signal and large-signal responses are expected to be significantly improved due to the much smaller parasitic capacitance associated with nano-devices. However, the FVF-based LDO structure itself does not have a high loop gain due to its simple folded circuit structure, even though it is implemented in a submicron CMOS technology. As a result, the reported load regulation is not outstanding. It can be easily predicted that when

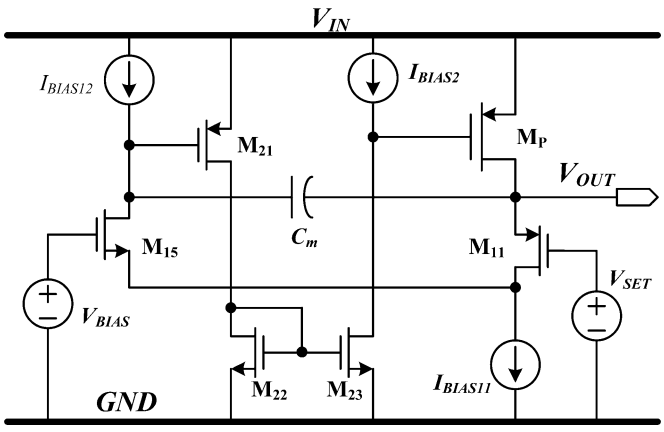

Fig. 2. Proposed OCL-LDO structure (core part, without slew-rate enhancement).

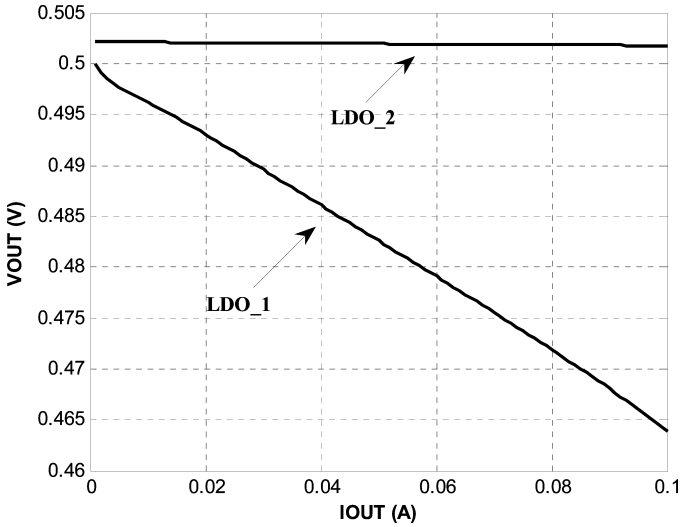

Fig. 3. Simulated load regulations of the LDOs shown in Fig. 1 (LDO_1) and Fig. 2 (LDO_2) designed in CMOS 90-nm technology and operated at $V_{\rm IN} = 0.75$ V.

the FVF-based LDO is implemented in nano-scale technology, the load regulation should be worse due to the more serious channel-length modulation in the nano-devices.

With regard to the above issues, an OCL-LDO, based on FVF and compensated by a single Miller capacitor, implemented in 90-nm CMOS technology is proposed in this paper. The proposed LDO makes use of the small transistors realized in nano-scale technology to achieve high stability, fast transient performance and small voltage spikes without the need of an off-chip capacitor connected at the LDO output. In Section II, the proposed OCL-LDO structure, implementation and principle of operation will be presented. Detailed measurement results will be reported in Section III. A comparison of the proposed design with the reported OCL-LDOs will be given in Section IV. The conclusion of this paper is given in Section V.

II. Proposed LDO Structure and Circuit Implementation

In this section, the structure and circuit implementation of proposed OCL-LDO will be presented. Performance improvement on regulation, stability and transient response will be addressed.

A. Proposed LDO Structure With Regulation Improvement

The proposed OCL-LDO structure is shown in Fig. 2, which originates from the FVF-based LDO structure. $\rm M_P$ is the power PMOSFET. The input voltage and output voltage are $V_{\rm IN}$ and $V_{\rm OUT}$, respectively, whereas $V_{\rm SET}$ is a control voltage generated by a voltage reference circuit and a V_{SG}-shifting circuit, which have been previously presented in [11]. Comparing with the structure shown in Fig. 1, an additional non-inverting gain stage, formed by $\rm M_{21}, M_{22}, M_{23}$ and $I_{\rm BIAS2}$, could boost the loop gain to improve both line and load regulations. Another important advantage of the added gain stage is that the dynamic range of the gate voltage of $\rm M_P$ in the proposed structure is also extended, which is just one saturation voltage of $\rm M_{23}$ above the ground. This enables a larger achievable V_{SG} of $\rm M_P$, so that the W/L aspect ratio of $\rm M_P$ can be smaller under the condition that the metal routing of $\rm M_P$ is sufficiently wide or thick to sustain the maximum output current with sufficiently low *IR* drop. A compensation capacitor, C_m, is inserted between $V_{\rm OUT}$ and the drain of $\rm M_{15}$ to stabilize the LDO. Detailed analysis of the loop stability will be given later in Part B of this section.

Circuit simulation is conducted to compare the load regulation of the LDO structures shown in Fig. 1 (denoted as LDO_1) and Fig. 2 (denoted as LDO_2). Both LDOs are simulated using the BSIM3v3 models provided by the foundry of UMC 90-nm CMOS technology. The sizes of $\rm M_P$ used in both LDOs are 1500 μm/0.08 μm.[1] The test conditions are $V_{\rm IN} = 0.75$ V and $I_{\rm OUT} = 1$ to 100 mA, where $I_{\rm OUT}$ is the load current. The results are consolidated and shown in Fig. 3. Obviously, the proposed OCL-LDO has better load regulation due to enhanced loop gain.

B. Frequency Compensation Strategy

The proposed LDO shown in Fig. 2 is suspected of closed-loop stability if no compensation strategy is applied, since there is no low-frequency dominant pole due to the small parasitic capacitance and drain resistance in the 90-nm technology. The poles at the output of the LDO, the gate of $\rm M_P$ and the input of the non-inverting gain stage are all not at very low frequency. To solve this problem, pole-splitting technique is adopted. A compensation capacitor, C_m, is inserted between $V_{\rm OUT}$ and the input of the added gain stage. Since the parasitic gate-to-drain capacitance of $\rm M_P (C_{gd})$ is very small in the 90-nm technology and the gain of $\rm M_P$ under different load current conditions is not large, the Miller effect of $C_{\rm gd}$ of $\rm M_P$ is negligible. Thus, the compensation topology, in fact, is not nested Miller compensation (NMC) [13]. The structure is similar to single Miller compensation reported in [14]. Fig. 4 shows the small-signal modelling of the proposed LDO, where R_{Oi} and C_{Pi} are the equivalent output resistance and lumped output parasitic capacitance of the i-th gain stage, respectively. $R_{\rm OUT}$ is the output resistance including the loading resistance, and $C_{\rm OUT}$ is the sum

[1]The drawn channel length is 80 nm which is the adjustment defined by the foundry and stated in the design rules.

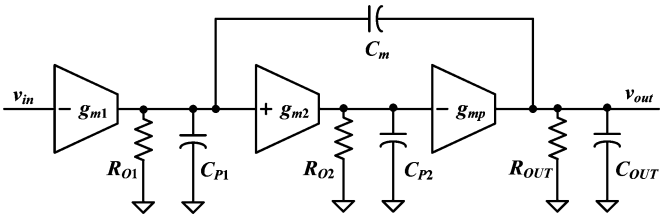

Fig. 4. Small-signal modelling of the proposed LDO.

of the parasitic capacitance from the LDO itself, power lines and load circuits. With the assumption of $g_{mp} \gg g_{m\mathrm{i}}, C_m \gg C_{p\mathrm{i}}$, and $C_{p2}R_{o2} \gg C_{\mathrm{OUT}}R_{\mathrm{OUT}}$ (C_{p2} is about 1.3 pF and R_{o2} is about 300 kΩ, their product is much larger than $C_{\mathrm{OUT}}R_{\mathrm{OUT}}$ since C_{OUT} is up to 50 pF and R_{OUT} is less than 500 Ω) which are all valid in this OCL-LDO design, the transfer function of the LDO modelling shown in Fig. 4 is given by

$$\begin{aligned} A_v(s) &= \frac{v_{\mathrm{out}}(s)}{v_{\mathrm{in}}(s)} \\ &\approx \frac{A_{\mathrm{dc}}\left(1 - s\dfrac{C_m}{g_{m2}R_{o2}g_{mp}} - s^2\dfrac{C_mC_{p2}}{g_{m2}g_{mp}}\right)}{\left(1+\dfrac{s}{p_{-3\mathrm{db}}}\right)\left(1+s\dfrac{C_{p2}}{g_{m2}g_{mp}R_{\mathrm{OUT}}}+s^2\dfrac{C_{p2}C_{\mathrm{OUT}}}{g_{m2}g_{mp}}\right)} \\ &\approx \frac{\left(1 - s\dfrac{C_m}{g_{m2}R_{o2}g_{mp}} - s^2\dfrac{C_mC_{p2}}{g_{m2}g_{mp}}\right)}{\dfrac{s}{\mathrm{GBW}}\left(1 + s\dfrac{C_{p2}}{g_{m2}g_{mp}R_{\mathrm{OUT}}} + s^2\dfrac{C_{p2}C_{\mathrm{OUT}}}{g_{m2}g_{mp}}\right)} \end{aligned} \quad (1)$$

where $A_{\mathrm{dc}} = g_{m1}g_{m2}g_{mp}R_{o1}R_{o2}R_{\mathrm{OUT}}$ is the low-frequency open-loop gain, $p_{-3\mathrm{dB}} = 1/(C_mR_{o1}g_{m2}g_{mp}R_{o2}R_{\mathrm{OUT}})$ is the dominant pole, and $\mathrm{GBW} = A_{\mathrm{dc}} \cdot p_{-3\mathrm{dB}} = g_{m1}/C_m$ is the gain-bandwidth product of the loop gain. There are two non-dominant poles and two zeros. It is highlighted here that C_m does control the GBW of the loop gain but it does not affect the location of the non-dominant poles. When the chosen C_m is small and g_{mp} is large, the zeros are located at high frequencies and are negligible. Thus, (1) can be simplified to

$$\begin{aligned} A_v(s) &= \frac{v_{\mathrm{in}}(s)}{v_{\mathrm{out}}(s)} \\ &\approx \frac{A_{\mathrm{dc}}}{\left(1+\dfrac{s}{p_{-3\mathrm{dB}}}\right)\left(1+s\dfrac{C_{p2}}{g_{m2}g_{mp}R_{\mathrm{OUT}}}+s^2\dfrac{C_{p2}C_{\mathrm{OUT}}}{g_{m2}g_{mp}}\right)}. \end{aligned} \quad (2)$$

To avoid frequency peaking due to complex poles, the relationship shown below should be met:

$$C_{\mathrm{OUT}} \le \frac{C_{p2}}{4g_{m2}g_{mp}R_{\mathrm{OUT}}^2}. \quad (3)$$

With an approximation of $R_{\mathrm{OUT}} \approx 1/(\lambda I_{\mathrm{OUT}})$, (3) can be rewritten as

$$C_{\mathrm{OUT}} \le \frac{\lambda^2 I_{\mathrm{OUT}}^2 C_{p2}}{4g_{m2}\sqrt{2\mu_pC_{\mathrm{OX}}(W/L)_{M_P}I_{\mathrm{OUT}}[1+\lambda(V_{\mathrm{IN}}-V_{\mathrm{OUT}})]}}. \quad (4)$$

Based on the above condition, (2) can be further simplified to

$$A_v(s) = \frac{v_{\mathrm{out}}(s)}{v_{\mathrm{in}}(s)} = \frac{A_{\mathrm{dc}}}{\left(1+\dfrac{s}{p_{-3\mathrm{dB}}}\right)\left(1+\dfrac{s}{p_2}\right)\left(1+\dfrac{s}{p_3}\right)} \quad (5)$$

where

$$p_2 = \frac{1}{2C_{\mathrm{OUT}}R_{\mathrm{OUT}}} - \sqrt{\frac{1}{4C_{\mathrm{OUT}}^2R_{\mathrm{OUT}}^2} - \frac{g_{m2}g_{mp}}{C_{p2}C_{\mathrm{OUT}}}} \quad (6)$$

$$p_3 = \frac{1}{2C_{\mathrm{OUT}}R_{\mathrm{OUT}}} + \sqrt{\frac{1}{4C_{\mathrm{OUT}}^2R_{\mathrm{OUT}}^2} - \frac{g_{m2}g_{mp}}{C_{p2}C_{\mathrm{OUT}}}} \quad (7)$$

To make the LDO stable, p_2 and p_3 should satisfy the condition: $\mathrm{GBW} \le (1/2)p_2 \le (1/4)p_3$ [15]. In this design, a condition of $p_2 \ge 10$ GBW is set to maintain high stability.

The relationship between C_{OUT}, V_{IN} and I_{OUT} can be found from (4). It indicates that a smaller C_{OUT} is needed for a smaller I_{OUT} or a higher V_{IN}. Thus, the condition stated in (4) actually specifies the maximal restriction of C_{OUT} to maintain stability. Since a larger I_{OUT} is needed for a larger C_{OUT} or V_{IN}, the minimal requirement of I_{OUT} can be found from (4) and is given by

$$I_{\mathrm{OUT}} \ge \sqrt[3]{\frac{32g_{m2}^2C_{\mathrm{OUT}}^2\mu_pC_{\mathrm{OX}}(W/L)_{M_P}[1+\lambda(V_{\mathrm{IN}}-V_{\mathrm{OUT}})]}{\lambda^4C_{p2}^2}}. \quad (8)$$

Similar to the LDOs compensated by NMC or some advanced compensation methods [2], [5], [6], (8) reveals that there is a minimum load current requirement to maintain the overall stability of the proposed LDO design. However, since the leakage current of 90-nm CMOS technology is significant and is up to several milliamperes in some designs [3], the proposed LDO is always stable in these applications. The reduction of the minimal load current requirement is not performed in this design although some methods reported in [5], [6], and [9] can lessen this problem.

The simulated loop gains of the proposed LDO at different V_{IN} and I_{OUT} are shown in Fig. 5. The highest low-frequency loop gain is 75 dB, whereas the lowest value is 50 dB. The phase margins in all conditions are more than 80°. Both the sufficient loop gain and large phase margin show that the proposed LDO has good voltage regulation and high closed-loop stability.

C. Circuit Implementation With Slew-Rate Enhancement

The error amplifier in Fig. 2, formed by M_{11}, M_{15}, I_{BIAS11}, I_{BIAS12}, M_{21}, M_{22}, M_{23}, and I_{BIAS2}, features a Class-A output stage to drive the gate capacitance of M_{P} (C_g, which is equivalent to C_{p2} in Fig. 4). The charging current of C_g is defined by I_{BIAS2}, whereas the discharging current of C_g is from M_{23}. When V_{OUT} drops due to rapid increase of the load current, the source terminal of M_{11} senses the changes and then propagates to the gate of M_{21} via M_{15}. The voltage change at the gate of M_{21} is between $\{V_{\mathrm{IN}} - \min[V_{(I\_\mathrm{BIAS12})}]\}$ and $(V_{\mathrm{BIAS}} - V_{\mathrm{GS15}} + V_{\mathrm{DS15(sat)}})$, where $\min[V_{(I\_\mathrm{BIAS12})}]$ is the minimum operational voltage of I_{BIAS12}. As a result, the discharging current from M_{23} is not small and this enhances

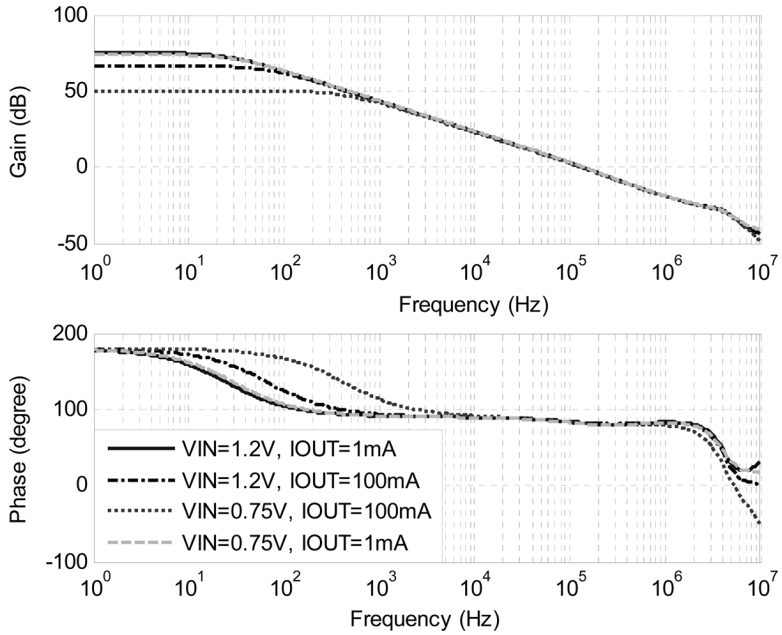

Fig. 5. Simulated Bode plots of proposed LDO with different $V_{\rm IN}$ and $I_{\rm OUT}$ ($C_{\rm OUT} = 10$ pF).

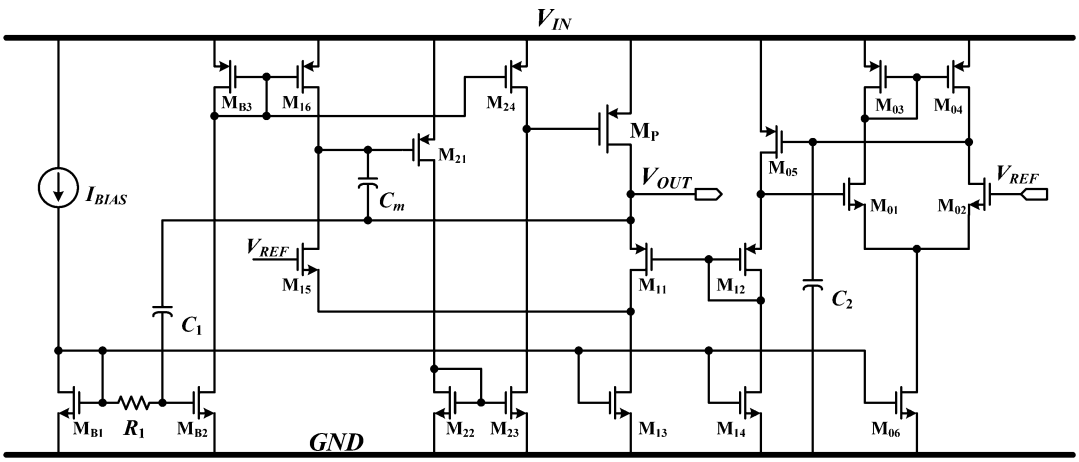

Fig. 6. Full schematic of the proposed LDO (with slew-rate enhancement).

the discharge of C_g. However, when an overshoot of $V_{\rm OUT}$ happens, the static charging current provided by $I_{\rm BIAS2}$ is not sufficiently large to charge C_g in the low quiescent-current LDO design. In that case, a direct voltage-spike detection technique is adopted to suppress this large overshoot. The detailed operation will be introduced using the full schematic of the proposed LDO.

The complete schematic of the proposed LDO is shown in Fig. 6. The error amplifier is formed by a common-gate differential pair consisting of $\rm M_{11}$–$\rm M_{16}$ and a non-inverting gain stage consisting of $\rm M_{21}$–$\rm M_{24}$, whereas the function of the non-inverting gain stage is to enhance the loop gain and increase the signal swing at the gate of $\rm M_P$. The aforementioned voltage-spike detection circuit is formed by $\rm M_{B1}, M_{B2}, \mathit{R}_1$ and C_1 [11]. C_1 is used to detect the output voltage spikes, and the detected changes of $V_{\rm OUT}$ activate the dynamic-biasing circuit to improve the slew rate at the gate of $\rm M_P$. For example, when $V_{\rm OUT}$ increases suddenly, C_1 couples the effect to the gate of $\rm M_{B2}$ and hence the gate voltage of $\rm M_{B2}$ is increased to make the drain current of $\rm M_{B2}$ increase simultaneously. As a result, more charging current from $\rm M_{24}$ to C_g helps to suppress the output voltage spike. With the added output-detection high-pass network, consisting of R_1 and C_1, the error amplifier features a pseudo Class-AB output stage, which improves the slew rate effectively and thus improves the transient performance. Comparing with the spike-detection circuit in [11], only one pair of *RC* is needed and so the chip area for another pair of *RC* component can be saved.

The simulated load transient results of the LDO shown in Fig. 1 (LDO_1), the proposed LDO without voltage-spike detection circuit shown in Fig. 2 (LDO_2) and the proposed LDO with voltage-spike detection circuit (denoted as LDO_proposed) are given in Fig. 7. Under a 0.75-V supply, when the output current switches between 1 mA and 100 mA within 100-ns edge time (i.e., the rise and fall times taken for the change of $I_{\rm OUT}$), the overshoots of LDO_proposed, LDO_2 and LDO_1 are 97 mV, 242 mV, and 230 mV, respectively. The overshoots of the last

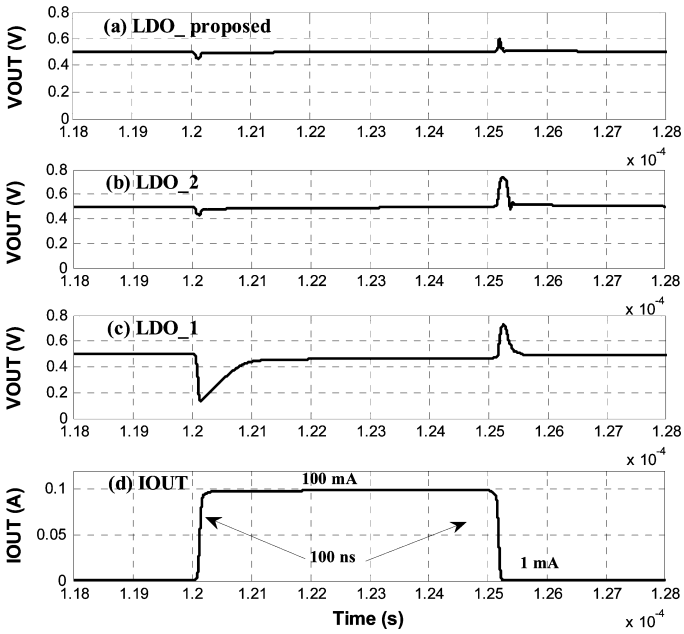

Fig. 7. Simulated load transient responses of different LDO topologies. (a) $V_{\rm OUT}$ of LDO_proposed. (b) $V_{\rm OUT}$ of LDO_2. (c) $V_{\rm OUT}$ of LDO_1. (d) $I_{\rm OUT}$.

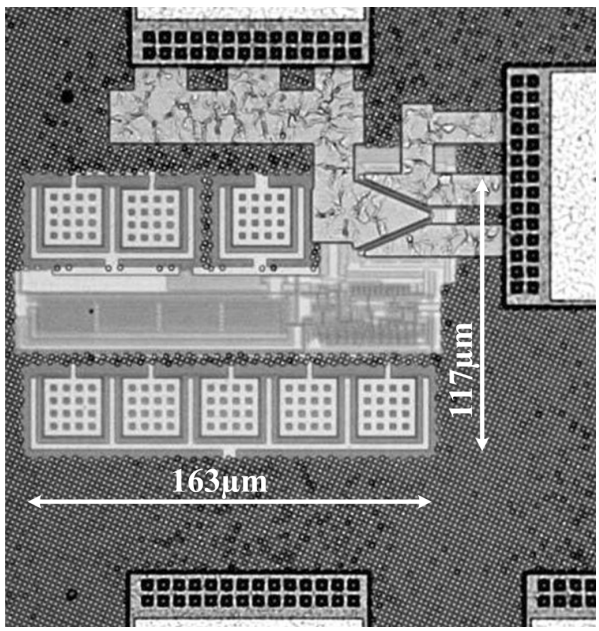

Fig. 8. Microphotograph of the proposed LDO.

two cases are close to the supply, and they are larger at a higher supply. Moreover, the simulated undershoots of LDO_proposed, LDO_2 and LDO_1 are 54 mV, 65 mV, and 359 mV, respectively. The output voltage spike is much reduced due to the enhanced loop-gain structure with a pseudo Class-AB output stage of the error amplifier. In other words, the proposed LDO shown in Fig. 6 has much improved steady-state and transient accuracies.

III. Experimental Results

The proposed LDO has been realized in UMC 90-nm CMOS technology. The chip microphotograph is shown in Fig. 8. It occupies 0.019 mm^2 (163 μm $\times$ 117 μm) of the chip area. The input supply range is 0.75–1.2 V, and the dropout voltage is 200 mV at 100 mA of $I_{\rm OUT}$. The quiescent current is only 8 μA. The minimal output voltage can be down to 0.5 V, which can meet the requirements of some ultra-low-voltage advanced circuits [16].

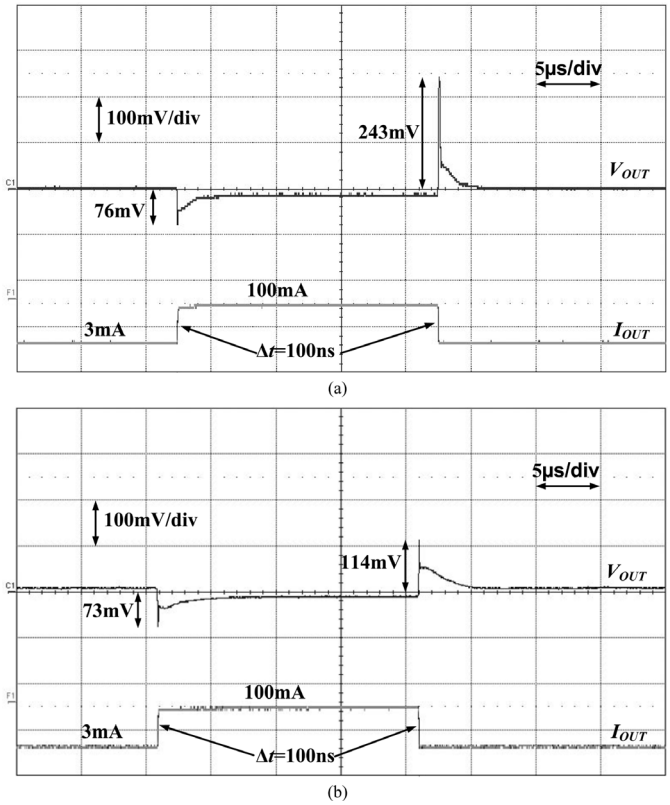

Fig. 9. Measured load transient response at $V_{\rm IN} = 0.75$ V, $V_{\rm OUT} = 0.5$ V, $C_{\rm OUT} = 50$ pF and 100-ns edge time (a) without slew-rate enhancement and (b) with slew-rate enhancement.

The proposed LDO is stable in full input supply range with equivalent capacitive load of no more than 50 pF and $I_{\rm OUT}$ of larger than 3 mA. Load transient measurements have been done to prove the stability and the improved transient performance of the proposed LDO structure. The measured load transient waveforms under different supply voltages and edge times are shown in Figs. 9 –11. Both the LDOs (with and without the voltage-spike detection circuit, i.e., the slew-rate enhancement circuit) have been measured. As shown in Fig. 9, when the output current is switched between 3 mA and 100 mA within 100 ns, the overshoot of $V_{\rm OUT}$ with the slew-rate enhancement is about 114 mV, while it is about 243 mV (nearly reach the supply rail of 0.75 V) when without the slew-rate enhancement circuit. In Fig. 10, the measurement condition is changed to $V_{\rm IN} = 1.2$ V. The overshoot for the case with slew-rate enhancement is only 66 mV, while the overshoot for the case without slew-rate enhancement is about 413 mV. The reduction of the overshoot by the slew-rate enhancement circuit is over 6 times. As shown in Fig. 11, both the overshoot and undershoot are within 30 mV when the load current changes with 1 μs edge time. The voltage spikes are much smaller when the load current change is slower.

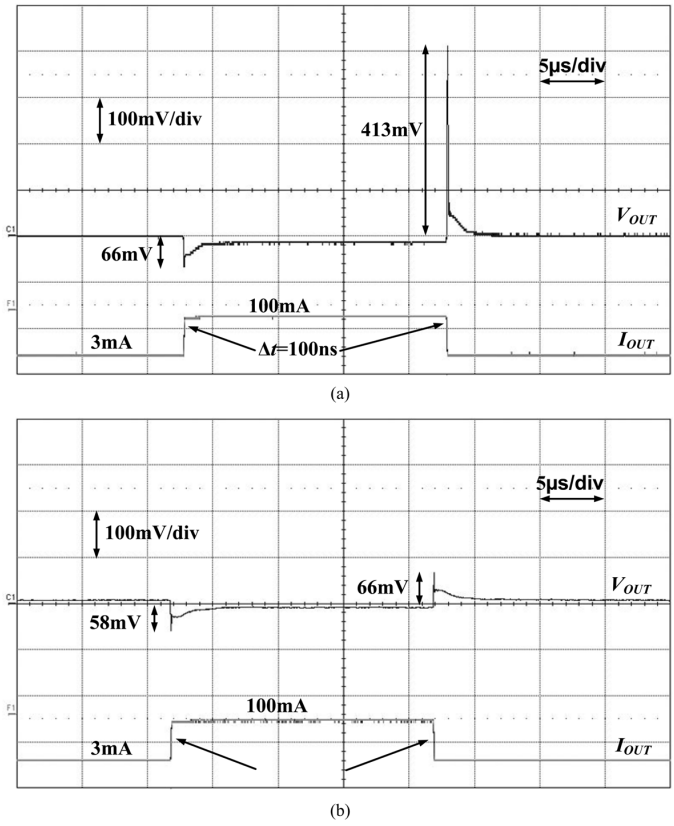

Fig. 10. Measured load transient response at $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 0.5$ V, $C_{\rm OUT} = 50$ pF and 100 ns edge time (a) without slew-rate enhancement and (b) with slew-rate enhancement.

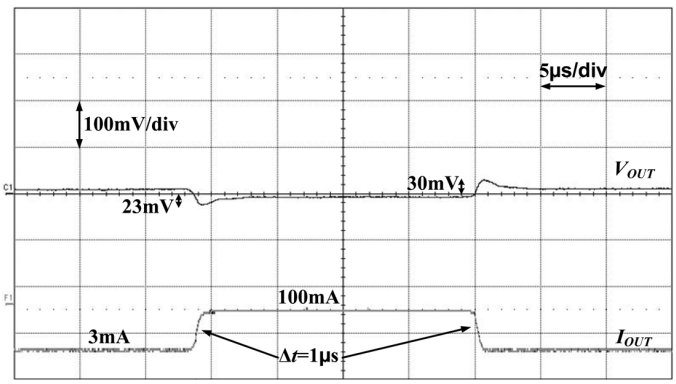

Fig. 11. Measured load transient response at $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 0.5$ V, $C_{\rm OUT} = 50$ pF and 1 μs edge time.

From Section II-B and (8), the minimal load current requirement is a function of the input voltage and the equivalent load capacitance of the LDO. It is verified experimentally that the minimal load current can be reduced when $V_{\rm IN}$ and $C_{\rm OUT}$ are smaller. Table I summarizes the measurement results of the minimal load current requirement under different supply voltages and output capacitances when $V_{\rm OUT}$ is set to 0.5 V. It shows the minimal load current is 1 mA for $V_{\rm IN} = 0.75$ to 1.2 V when $C_{\rm OUT} = 10$ pF. The corresponding transient response is shown in Fig. 12 (top: full view; bottom: zoom-in view). This measured result verifies the foregoing analysis that the minimal load current can be smaller when $C_{\rm OUT}$ is smaller. When $C_{\rm OUT}$ is increased to 50 pF, the minimal load current is 1.5 mA with $V_{\rm IN} = 0.75$ V. This transient response is shown in Fig. 13 (top: full view; bottom: zoom-in view). This measured result verifies that the minimal load current can be smaller when $V_{\rm IN}$ is smaller. Finally, when $V_{\rm IN} = 1.2$ V and $C_{\rm OUT} = 50$ pF, it becomes 3 mA, which have been verified in Figs. 10 and 11.

TABLE I
MEASURED MINIMAL LOAD CURRENT REQUIREMENT UNDER DIFFERENT $V_{\rm IN}$ AND $C_{\rm OUT}$

	C_{OUT} = 10 pF	C_{OUT} = 50 pF
V_{IN} = 0.75 V	I_{OUT} (min) = 1 mA	I_{OUT} (min) = 1.5 mA
V_{IN} = 1.2 V	I_{OUT} (min) = 1 mA	I_{OUT} (min) = 3 mA

Fig. 14 shows the line transient response. The voltage spikes are within 40 mV when supply voltage changes between 0.78 V and 1.2 V within 10 μs.

In addition of the transient measurements, both the dc and ac measurements are also performed. The measured line and load regulations are shown in Figs. 15 and 16, respectively. From the results, it shows that $V_{\rm OUT}$ varies 1.7 mV and 3 mV, respectively, when $V_{\rm IN}$ changes from 0.75 V to 1.2 V for $I_{\rm OUT} = 1$ mA and $I_{\rm OUT} = 100$ mA. When $V_{\rm IN} = 0.8$ V, $V_{\rm OUT}$ varies about 10 mV when load current changes from 1 mA to 100 mA. Fig. 17 shows the relationship between the dropout voltage and the load current at $V_{\rm REF} = 1$ V. Finally, power-supply ripple rejection (PSRR) against different load currents is shown in Fig. 18. The proposed LDO can achieve about -44-dB PSRR at 1-kHz when $I_{\rm OUT} = 100$ mA.

IV. PERFORMANCE COMPARISON

Performance comparison between the proposed OCL-LDO and some selected recently-published OCL-LDOs is shown in Table II. Due to the implementation in the 90-nm CMOS technology, the proposed LDO has the smallest chip area. More importantly, the proposed LDO does not need a large on-chip output capacitor as in [3], and thus the proposed LDO shows more suitable for high-density SoC applications. Moreover, the proposed LDO can operate in an ultra-low-voltage supply of 0.75 V, and it achieves the lowest quiescent current of 8 μA among other designs. Both the line and load regulations are good as well. The measured transient performance shown in Section III reflects the design has good small-signal and large-signal responses under a low quiescent-current level.

When comparing the load transient performance, both the output voltage variation $(\Delta V_{\rm OUT})$ and the edge time taken for the change of the output current (Δt) relate to each other closely. In general LDO design with an output capacitor, when the load current change is faster than the loop response of a LDO, the output capacitor will be charged or discharged until the LDO can respond the change. In that case, the voltage spike is directly related to the output capacitance. However, in OCL-LDO design, there is no output capacitor. The equivalent lumped capacitance at the output of an OCL-LDO is a few tens

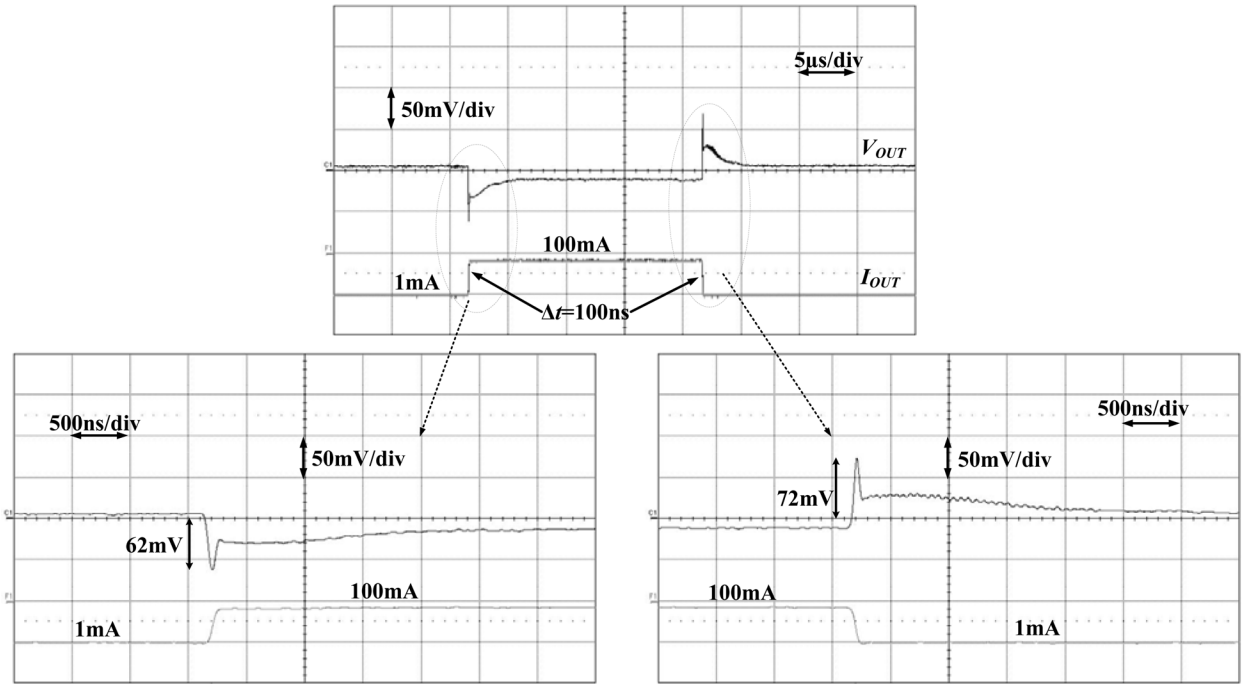

Fig. 12. Measured load transient response at $V_{\rm IN} = 1.2$ V, $V_{\rm OUT} = 0.5$ V, $C_{\rm OUT} = 10$ pF and 100 ns edge time.

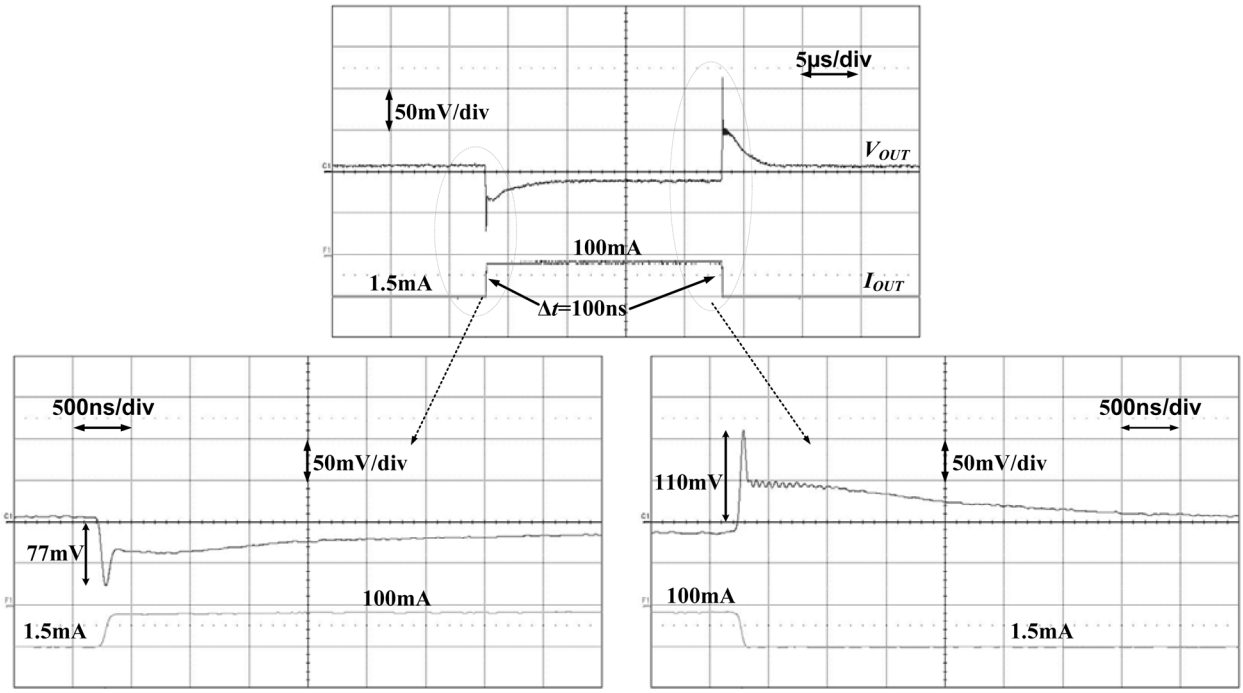

Fig. 13. Measured load transient response when $V_{\rm IN} = 0.75$ V, $V_{\rm OUT} = 0.5$ V, $C_{\rm OUT} = 50$ pF and 100 ns edge time.

of pF and is not helpful to the transient response. In fact, the equivalent output capacitance is a big problem to the OCL-LDO stability [2], [4]–[11]. As a result, the figure of merit (FOM) proposed in [3], which includes the dependence of the output capacitance, is not suitable for the comparison of different OCL-LDOs. In addition, the edge time is another key factor affecting the response speed of an OCL-LDO. This effect can be proved by the experimental results shown in Figs. 10 and 11. Based on these considerations, a new FOM for comparison of different OCL-LDOs, which takes $\Delta V_{\rm OUT}$, $\Delta I_{\rm OUT}$, I_Q, and Δt into account, is proposed in this section. It is given by

$$\text{FOM} = K\left(\frac{\Delta V_{\rm OUT}\cdot I_Q}{\Delta I_{\rm OUT}}\right)$$

where K is edge-time ratio which is defined by

$$K = \frac{\Delta t \text{ used in the measurement}}{\text{the smallest } \Delta t \text{ among the designs for comparison}}.$$

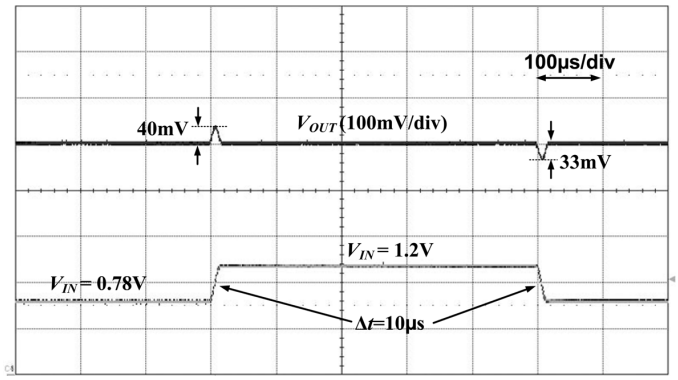

Fig. 14. Measured line transient waveform when $V_{\rm OUT} = 0.5$ V, $I_{\rm OUT} = 1$ mA and $C_{\rm OUT} = 10$ pF.

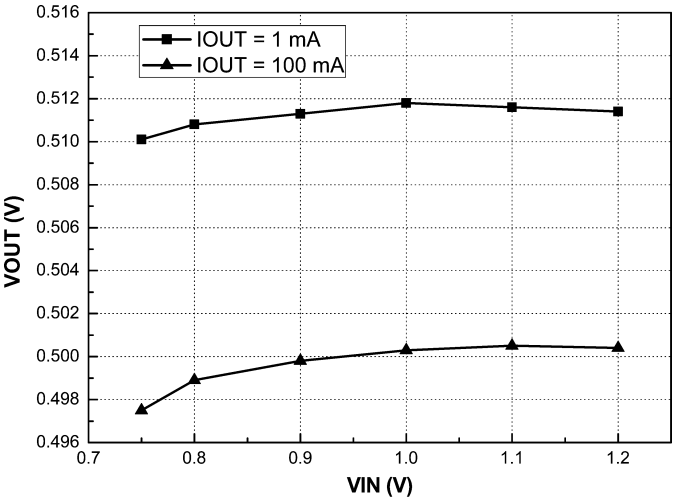

Fig. 15. Measured line regulation for $I_{\rm OUT} = 1$ mA and $I_{\rm OUT} = 100$ mA when $V_{\rm REF} = 0.5$ V (no external $C_{\rm OUT}$ is added).

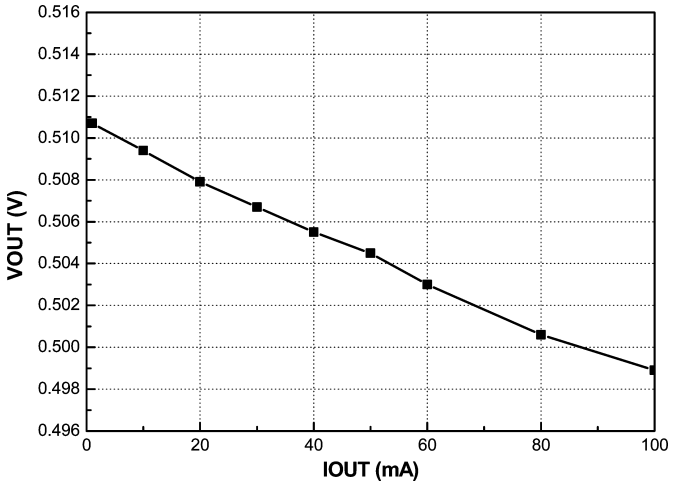

Fig. 16. Measured load regulation when $V_{\rm IN} = 0.8$ V, $V_{\rm REF} = 0.5$ V (no external $C_{\rm OUT}$ is added).

It is noted that the unit of this FOM is volts. The K-factor does include a mutual comparison of the edge time used in the measurement of the OCL-LDOs. Since the edge time used in [3] is the smallest in the comparison, it becomes the reference of other designs and its K-factor equals to 1. A smaller FOM of an OCL-LDO design implies that the transient response of this design is better. From Table II, it shows that the proposed LDO has the smallest FOM.

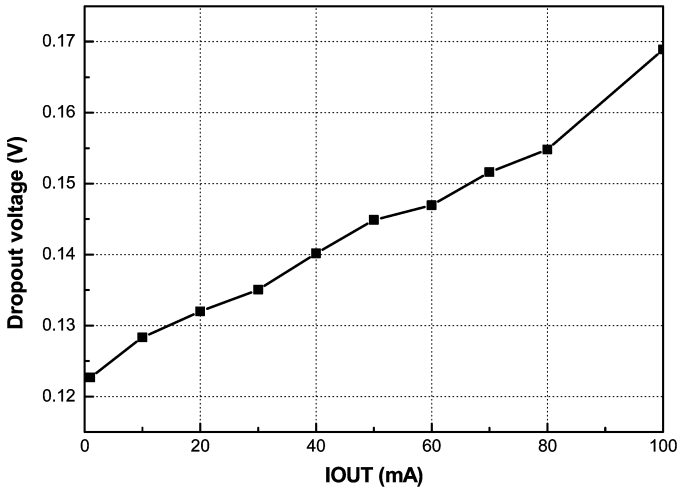

Fig. 17. Measured dropout voltage versus $I_{\rm OUT}$ when $V_{\rm REF} = 1$ V (no external $C_{\rm OUT}$ is added).

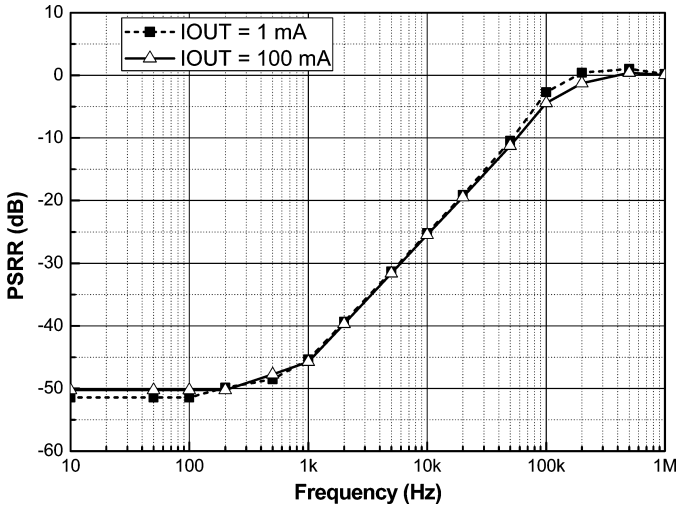

Fig. 18. Measured PSRR versus frequency for $I_{\rm OUT} = 1$ mA and $I_{\rm OUT} = 100$ mA when $V_{\rm OUT} = V_{\rm REF} = 0.5$ V, $V_{\rm IN} = 1$ V and $C_{\rm OUT} = 10$ pF.

V. Conclusion

In this paper, a 0.75-V output-capacitorless LDO implemented in 90-nm CMOS technology is presented. Closed-loop stability under output-capacitorless condition is maintained by a single Miller capacitor. Even though the quiescent current is as low as 8 μA, the voltage spike generated during transient change of the load current is small due to the proposed pseudo Class-AB error amplifier. Both line and load regulations are also improved due to the added non-inverting gain stage. Moreover, the required on-chip capacitor is small, and so the chip area of this design is much smaller than one published design implemented in 90-nm CMOS technology. The achieved specifications of the proposed LDO (i.e., 100-mA load capability

TABLE II
PERFORMANCE COMPARISON WITH RECENT PUBLISHED OCL-LDOS

	[2]	[3]	[4]	[8]	[9]	[11]	**This work**
Year	2003	2005	2006	2007	2008	2010	**2010**
Technology (μm)	0.6	0.09	0.18	0.35	0.35	0.35	**0.09**
Chip area (mm^2)	0.307	0.098	0.122	0.120	0.342	0.155	**0.019**
V_{IN} (V)	1.5 – 4.5	1.2	0.65 – 0.95	3 - 4.2	3 – 5	0.95 – 1.4	**0.75 – 1.2**
V_{OUT} (V)	1.3	0.9	0.5	2.8	2.8	0.7 – 1.2	**0.5 – 1**
I_Q (μA)	38	6000	12.72	65	170	43	**8**
I_{OUT} (max) (mA)	100	50	50	50	100	100	**100**
Dropout voltage (mV)	200	300	150	200	200	200	**200**
Line regulation (mV/V)	±0.25%	N/A	~ 30	~ 23	3.3	N/A	**3.78**
Load regulation (mV/mA)		1.8	~ 0.19	~ 0.56	0.02	~ 0.4	**0.1**
On-chip capacitance (pF)	~ 12	600	N/A	23	6.5	6	**7**
ΔV_{OUT} (mV)	~ 120	90	300	~90	~ 80	~ 70	**114**
ΔI_{OUT} (mA)	90	50	50	50	~ 100	99	**97**
Edge time Δt (μs)	0.5	0.0001	~ 4	1	5	1	**0.1**
Edge time ratio K	5000	**1**	40000	10000	50000	10000	**1000**
$\text{FOM} = K\left(\frac{\Delta V_{OUT} \cdot I_Q}{\Delta I_{OUT}}\right)$ (V)	0.253	0.011	3.053	1.170	6.800	0.304	**0.009**

and 0.5-V minimal output) are suitable for modern low-voltage mixed-signal SoC applications.

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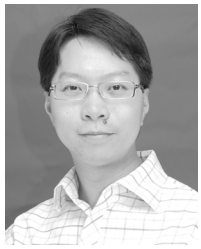
Jianping Guo (S'09) received the B.Sc. and M.Sc. degrees in electronic engineering from Xidian University, Xi'an, China, in 2003 and 2006, respectively. He is currently working toward the Ph.D. degree in The Chinese University of Hong Kong (CUHK), Hong Kong, China.

From 2004 to 2007, he worked in Xi'an Deheng Microelectronic Inc. as an IC designer, focusing on the design of low dropout regulator, switching DC-DC converter and PWM controller IC. His current research interest includes power management integrated circuits and their applications in wireless and biomedical systems.



Ka Nang Leung (S'02–M'03–SM'08) received the B.Eng., M.Phil., and Ph.D. degrees, all in electrical and electronic engineering, from The Hong Kong University of Science and Technology. His Ph.D. research area was power-management integrated circuits in CMOS technology.

He joined the Department of Electronic Engineering, The Chinese University of Hong Kong, in September 2005 as an Assistant Professor. He was a Visiting Assistant Professor in the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology. His current research interests include power-management integrated circuits for wireless telecommunication, biomedical filter design and CMOS image sensor.

Prof. Leung received a Best Teaching Assistant Award from the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, in 1996. In 2007, he received the Department Exemplary Teaching Award from The Chinese University of Hong Kong. He received the 2003 Young Scientist Award of the Hong Kong Institution of Science. He is a technical paper reviewer of several IEEE journals and international conferences.