High PSR Low Drop-Out Regulator With Feed-Forward Ripple Cancellation Technique

Mohamed El-Nozahi, *Student Member, IEEE*, Ahmed Amer, *Student Member, IEEE*, Joselyn Torres, *Student Member, IEEE*, Kamran Entesari, *Member, IEEE*, and Edgar Sánchez-Sinencio, *Fellow, IEEE*

***Abstract*—A low drop-out (LDO) regulator with a feed-forward ripple cancellation (FFRC) technique is proposed in this paper. The FFRC-LDO achieves a high power-supply rejection (PSR) over a wide frequency range. Complete analysis and design steps of the FFRC-LDO are presented in this paper. Kelvin connection is also used to increase the gain–bandwidth of the LDO allowing for faster transient performance. The LDO is implemented in 0.13 μm CMOS technology and achieves a PSR better than −56 dB up to 10 MHz for load currents up to 25 mA. Load regulation of 1.2 mV for a 25 mA step is measured, and the whole LDO consumes a quiescent current of 50 μA with a bandgap reference circuit included. To our knowledge, this is the first LDO that achieves such a high PSR up to 10 MHz.**

***Index Terms*—CMOS, DC-DC converters, feed-forward ripple cancellation, low drop-out regulator, power-supply rejection.**

I. Introduction

THERE is a great interest in efficient power management ICs. An important building block in power management is the low drop-out (LDO) linear regulator which often follows a DC-DC switching converter, as shown in Fig. 1. It is used to regulate the supplies ripples to provide a clean voltage source for the noise-sensitive analog/RF blocks. Designing a stable LDO for a wide range of load conditions, while achieving high power-supply rejection (PSR), low drop-out voltage, and low quiescent current, is the main target using state-of-the-art CMOS technologies [1]–[4].

Recently, there has been an increasing demand to integrate the whole power management system into a single system-on-chip (SoC) solution. Hence, operating frequencies of switching converters are increasing to allow higher level of integration [5]. This trend increases the frequency of output ripples and therefore the subsequent LDO regulator should provide high PSR up to switching frequencies. Conventional LDOs have poor PSR at high frequencies (above 300 kHz) especially the ones implemented using sub-250 nm technologies. The main reasons for poor PSR are summarized as follows: 1) Finite output conductance of the pass transistor, 2) low DC gain of sub-250 nm technologies which requires complex gain stages to achieve better regulation, and 3) finite bandwidth of the feedback path.

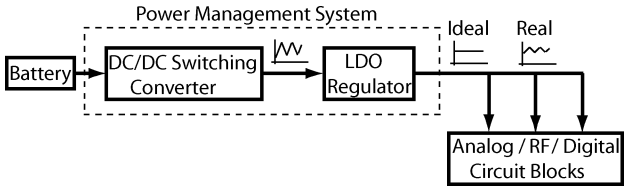

Fig. 1. Block diagram of typical power management system.

Researchers have contributed to improve power-supply rejection techniques. Some of those techniques are: i) Using simple *RC* filtering at the output of the LDO [6]; ii) Cascading two regulators [6]; iii) Cascading another transistor with the pMOS pass transistor along with *RC* filtering, using special technologies such as drain-extended FET devices, and/or charge-pump techniques to bias the gate of one of the transistors [7]–[9]. Simple *RC* filtering reduces the voltage ripple at the input of the LDO. However, this technique increases the drop-out voltage in LDO regulators that supply high current due to the high voltage drop across the resistance. Using an nMOS or pMOS transistor to cascade with the pMOS pass transistor can achieve high power-supply rejection over a wide frequency range. This technique increases the area and leads to a high drop-out voltage [7]. Charge pump techniques increase complexity and lead to higher power consumption because a clock is necessary along with *RC* filtering to remove clock ripples [9]. In summary, the main idea behind all previously proposed techniques is to provide more isolation between the input and output along the high-current signal path. Hence, the area consumption and drop-out voltage are large, which is not suitable for low-voltage technologies. In addition, these techniques provide high PSR at low frequencies, but are unable to provide sufficient PSR (better than −50 dB) at frequencies up to several MHz.

To overcome the drawbacks of previously reported PSR LDO regulators, we introduce a high PSR low voltage LDO regulator based on a feed-forward ripple cancellation (FFRC) approach [10]. The proposed LDO topology preserves traditional loop dynamics structure, while providing high PSR over a wide frequency range. In addition, it enables the design for high supply currents and low quiescent current consumption. The paper is organized as follows: Section II discusses main PSR limitation sources in conventional LDOs. Section III presents the proposed FFRC-LDO. The stability analysis using a single bond-wire and a Kelvin connection are presented in Section IV (To our knowledge, this analysis is not presented before for LDO regulators).

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The authors are with the Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843 USA (e-mail: melnozahi@ieee.org; ahmed.amer@ieee.org; jotorres@tamu.edu; kentesar@ece.tamu.edu; e.sanchez@ieee.org; sanchez@ece.tamu.edu).

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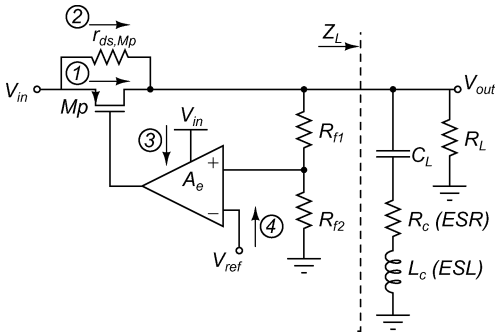

Fig. 2. Input to output ripple paths in conventional LDOs.

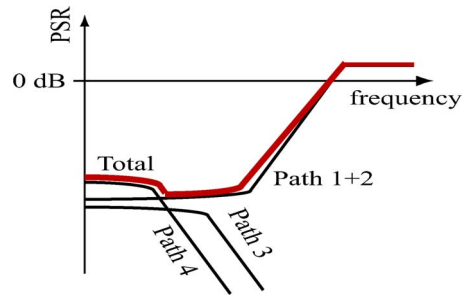

Fig. 3. Total PSR of LDO and PSR due to each path in Fig. 2.

Section V demonstrates the circuit implementation. Measurement results are shown in Section VI, and conclusions are provided in Section VII.

II. PSR of Conventional LDOs

In this section, fundamental limitations for PSR improvement of conventional LDOs at high frequencies are investigated. It is shown that PSR at high frequencies is mainly limited by the dominant pole of the error amplifier and equivalent self inductance (ESL) and resistance (ESR) of the off-chip capacitor.

The finite PSR of the conventional LDO is due to several paths between the input and output of the LDO. Fig. 2 shows various paths that could couple input ripples to the output of the LDO. Path 1 is the main path regulated by the LDO loop. Path 2 is caused by the finite conductance of the MOS pass transistor, M_p, and it is more significant for technologies with lower feature sizes. Path 3 is as a result of the finite power-supply rejection ratio (PSRR) of the error amplifier, and finally path 4 is due to the finite PSR of the bandgap circuit.

The LDO transfer function due to paths 1 and 2 is given by

$$\left.\frac{V_{\rm out}}{V_{\rm in}}(s)\right|_{1,2} = \frac{1+g_{m,Mp}\cdot r_{ds,Mp}}{1+\dfrac{r_{ds,Mp}}{Z_L(s)}+\dfrac{r_{ds,Mp}}{R_{f1}+R_{f2}}+\dfrac{g_{m,Mp}r_{ds,Mp}A_{eo}R_{f2}}{(R_{f1}+R_{f2})\left(1+\frac{s}{\omega_e}\right)}}. \quad (1)$$

where $g_{m,Mp}$ and $r_{ds,Mp}$ are the transconductance and channel resistance of the pass transistor, M_p. Z_L is the total load impedance (without feedback resistances R_{f1} and R_{f2}) that appear at node $V_{\rm out}$, and A_{eo} and ω_e are the DC gain and dominant pole of the error amplifier, respectively. Equation (1) shows that PSR depends on the feedback gain $(A_{eo}(R_{f2}/(R_{f1}+R_{f2})))$ at lower frequencies. For sub-250 nm technologies, increasing A_{eo} is challenging for conventional LDO designs.

As the frequency increases, the dominant pole of the error amplifier reduces the feedback gain; therefore, the PSR due to paths 1 and 2 starts to degrade. Without considering ESL and ESR of the off-chip capacitor, $(V_{\rm out}/V_{\rm in})|_{1,2}$ starts to decrease at higher frequencies because the off-chip capacitor shorts ripples to ground. However, due to ESL and ESR this effect does not happen at high frequencies, and the off-chip capacitor represents an open circuit. In this case, ripples at the output may get amplified at high frequencies. The upper and lower limits of PSR across the entire frequency spectrum due to paths 1 and 2 are given by

$$\left.\frac{V_{\rm out}}{V_{\rm in}}(s=0)\right|_{1,2\ \rm lower} \approx \frac{1}{A_{eo}\frac{R_{f2}}{R_{f1}+R_{f2}}},$$
$$\left.\frac{V_{\rm out}}{V_{\rm in}}(s=\infty)\right|_{1,2\ \rm upper} \approx g_{m,Mp}\frac{R_L\cdot r_{ds,Mp}}{R_L+r_{ds,Mp}}. \quad (2)$$

For paths 3 and 4, the transfer function is given by

$$\left.\frac{V_{\rm out}}{V_{\rm in}}(s)\right|_{3,4} = \frac{g_{m,Mp}Z_{\rm tot}(s)\dfrac{A_{eo}}{1+\frac{s}{\omega_e}}}{1+\dfrac{g_{m,Mp}Z_{\rm tot}(s)A_{eo}R_{f2}}{(R_{f1}+R_{f2})\left(1+\frac{s}{\omega_e}\right)}}(\mathrm{PSRR}_e+\mathrm{PSR}_{\rm BG}),$$
$$Z_{\rm tot}(s) = Z_L(s)//r_{ds,Mp}//(R_{f1}+R_{f2}) \quad (3)$$

where PSRR_e is the power-supply rejection ratio of the error amplifier, and $\mathrm{PSR}_{\rm BG}$ is the power-supply rejection of the bandgap circuit. Equation (3) shows that the finite PSR due to paths 3 and 4 is an amplified quantity of PSRR_e and $\mathrm{PSR}_{\rm BG}$. The amplification is given by the ratio of feedback resistances as $1+(R_{f1}/R_{f2})$. At higher frequencies due to the dominant pole of error amplifier, $(V_{\rm out}/V_{\rm in})|_{3,4}$ goes to zero, and hence, ripples leaking through the error amplifier and bandgap do not appear at the output.

In summary, all four paths affect the PSR at low frequencies and only paths 1 and 2 affect the PSR at high frequencies. Fig. 3 demonstrates the effect of each path on the overall PSR of the conventional LDO. Several techniques could be applied to reduce the PSR at lower frequencies by decreasing PSRR_e, $\mathrm{PSR}_{\rm BG}$ and increasing gain of error amplifier. However at higher frequencies, the dominant pole of the error amplifier degrades the PSR of the LDO, and the off-chip capacitor is considered as an open circuit because of its ESL. None of the previously presented techniques have solved this problem satisfactorily. Usually, the PSR of LDO starts to degrade around 10–100 kHz [9]. A proposed solution for achieving high PSR at higher frequencies is demonstrated in the next section.

III. Proposed Feed-Forward Ripple Cancellation LDO

The PSR at low frequencies can be enhanced by increasing the feedback gain of the LDO. However at high frequencies, the PSR is mainly due to paths 1 and 2 in Fig. 2, and is limited by the dominant pole of the feedback loop. To achieve higher PSR

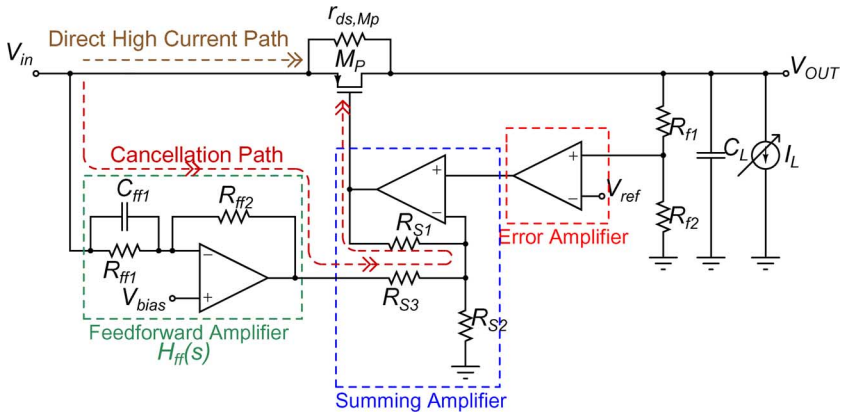

Fig. 4. Block-level representation of the feed-forward ripple cancellation LDO.

at both DC and high frequencies, ripples generated in paths 1 and 2 should be removed. The basic idea of the proposed LDO is demonstrated below. Its sensitivity to process–temperature (PT) variations is also discussed.

A. Basic Idea

To eliminate input ripples from appearing at the output, a zero transfer gain is necessary from the input to the output in Fig. 2. In the ideal case (without considering $r_{ds,Mp}$), this is achieved by implementing a feed-forward path that replicates same input ripples at the gate of the pass transistor. Hence, the gate-overdrive voltage is independent of input ripples, and as a result no ripple appears across the load. In the actual case (with $r_{ds,Mp}$), part of the ripples leak through the finite output resistance of M_p, and should be removed. This is done by increasing the ripple amplitude appearing at the gate of M_p to cancel ripples that leak through $r_{ds,Mp}$ by an amount of $(g_{m,Mp} + g_{ds,Mp})/g_{m,Mp}$.

Fig. 4 presents a simplified block-level description of the proposed FFRC-LDO. Supply ripples, appearing at the source of pass transistor M_p, are reproduced at the gate of M_p using the feed-forward path. The generated ripples at the gate are higher in magnitude than input ripples to cancel additional ripples appearing at the output due to $r_{ds,Mp}$ (path 2 in Fig. 2). The feed-forward path is implemented using a feed-forward amplifier and a summing amplifier. The summing amplifier is used to merge the feedback regulating loop with feed-forward path at the gate of the transistor M_p.

Optimum value of the feed-forward gain is obtained with the help of a mathematical model of the FFRC-LDO, as shown in Fig. 5. Without the feed-forward path, $H_{\rm ff}(s)$, the mathematical model is similar to a conventional LDO. The transfer gain of the system $H_{\rm ff}(s)$ yields

$$\frac{V_{\rm out}}{V_{\rm in}}(s) = \frac{1 + g_{m,Mp}\cdot r_{ds,Mp}\cdot\left[1 - H_{\rm ff}(s)\dfrac{A_{so}}{1+\frac{s}{\omega_s}}\right]}{1+\dfrac{r_{ds,Mp}}{Z_L(s)}+\dfrac{r_{ds,Mp}}{R_{f1}+R_{f2}}+\dfrac{g_{m,Mp}\cdot r_{ds,Mp}\cdot A_{eo}R_{f2}}{(R_{f1}+R_{f2})\left(1+\frac{s}{\omega_e}\right)}} \quad (4)$$

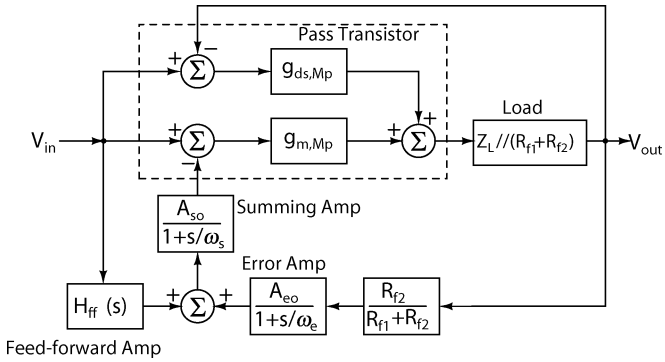

Fig. 5. Mathematical model of the FFRC-LDO.

where A_{so} and ω_s are the DC gain and dominant pole of the summing amplifier, respectively. To remove the ripples at the output, (4) is set to be zero. The optimum value for the feed-forward amplifier is then given by

$$H_{\rm ff}(s)|_{\rm opt} = \frac{1+\frac{s}{\omega_s}}{A_{so}}\cdot\left(1+\frac{1}{g_{m,Mp}r_{ds,Mp}}\right) = \frac{1+\frac{s}{\omega_s}}{A_{so}}\cdot\left(\frac{g_{m,Mp}+g_{ds,Mp}}{g_{m,Mp}}\right). \quad (5)$$

Equation (5) demonstrates that the optimum feed-forward gain has to contain a zero in its transfer function. The zero cancels the effect of the pole existing at the gate of the pass transistor to extend the frequency range of the ripple rejection. Hence, this cancellation technique is limited by internal poles of the summing and feed-forward amplifiers. The zero is implemented using the capacitor $C_{\rm ff1}$ in Fig. 4.

The simulated PSR of the LDO with and without FFRC technique is demonstrated in Fig. 6. Using the conventional architecture, the achieved PSR is less than 60 dB and it starts to degrade around 330 kHz. This frequency is located at the dominant pole of the error amplifier. Using the FFRC-LDO the PSR at DC is enhanced by 20 dB. Besides, the additional zero increases the frequency at which the PSR starts to increase to 9 MHz. This simulation shows the effectiveness of the FFRC-LDO to enhance the PSR at both DC and high frequencies. The PSR

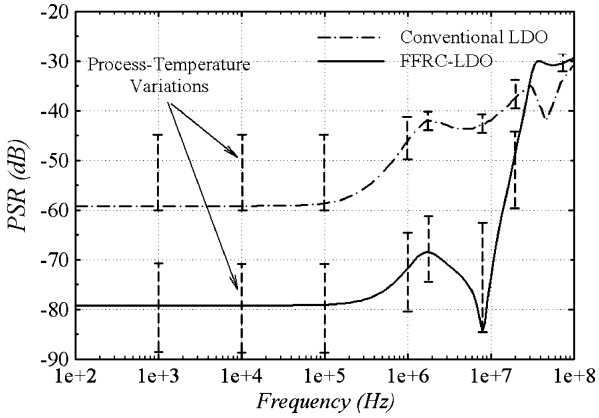

Fig. 6. PSR schematic simulations of conventional and FFRC-LDO ($R_L = 40\ \Omega$). The effect of PT variations are also demonstrated.

starts initially to increase around 330 kHz, which is the bandwidth of the error amplifier. Then around 1 MHz, the introduced zero stops the increase in the PSR. Due to the self-resonance frequency of the off-chip capacitor and finite non-dominate poles of the feed-forward and summing amplifiers, the PSR starts to degrade again at high frequencies. The main advantage of this FFRC approach is achieving a high PSR for a wide frequency range, without the need to increase the loop bandwidth and hence the quiescent power consumption. Moreover, this approach preserves the same low drop-out voltage of a conventional regulator, since supply rejection does not occur on the high-current signal path. The gain of the feed-forward and summing amplifiers is based on the ratio of resistors to reduce its dependency to process-temperature (PT) variations. Fig. 6 shows the simulated variations of PSR of the FFRC-LDO for a temperature ranging from -40 to 125 °C, and across process corners. Simulations over PT variations indicate that the LDO achieves comparable performance to that measured in the lab, making the LDO robust for high-performance power management ICs.

The variation of the PSR versus the load current is shown in Fig. 7. As depicted, the PSR has its best value for a current of 5 mA at low frequencies. As the current increases, PSR is degraded due to the dependency of the DC gain of $M_p(g_{m,Mp} \cdot r_{ds,Mp})$ on the output current. For small currents, the transistor M_p is biased in deep saturation with a DC gain of 20 dB. As the current increases, the transistor operating point moves near the linear region, and therefore, the DC gain is reduced to 14 dB at a load current of 25 mA. This example shows that $H_{\rm ff}(s)$ has to be configurable if the LDO is designed to cover a wide range of currents.

The biasing voltage of the summing amplifier, $V_{\rm bias}$ in Fig. 4 has to be adjusted such that the output DC voltage of the summing amplifier is higher than zero. There is a minimum value for $V_{\rm bias}$ for proper operation of the FFRC-LDO. $V_{\rm bias}|_{\rm min}$ is given by

$$V_{\rm bias}|_{\rm min} = V_{\rm in}|_{\rm max} \cdot \frac{R_{\rm ff2}}{R_{\rm ff1} + R_{\rm ff2}}. \tag{6}$$

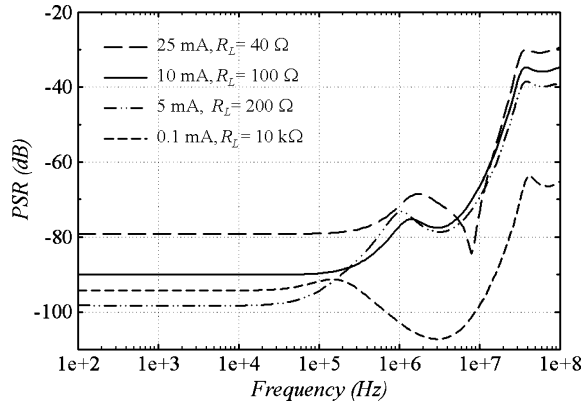

Fig. 7. PSR schematic simulations of FFRC-LDO for various load conditions ($R_L = 40, 100, 200, 10\,000\ \Omega$).

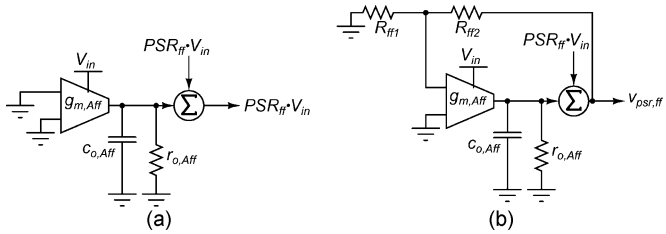

Fig. 8. Modeling of finite PSR of feed-forward amplifier (a) without feedback connection, and (b) with feedback connection.

As high PSR is only required when the output is stabilized, this system biases the positive terminal of the feed-forward amplifier directly from the output, i.e., $V_{\rm bias} = V_{\rm out}$. The maximum input voltage that can be applied in this case is 2 V for an output voltage of 1 V and $R_{\rm ff2}/R_{\rm ff1} = 1$. Connecting the output directly to $V_{\rm bias}$ requires no additional voltage reference circuit. However, in a different design, another reference voltage can be added if the output voltage of the LDO is not high enough to satisfy the condition in (6).

B. Effect of Finite PSRR of Summing and Feed-Forward Amplifiers

The effect of finite PSRR of summing and feed-forward amplifiers is studied in this section. It will be demonstrated that the PSR performance of these two amplifiers do not affect the PSR of the LDO significantly.

1) Feed-Forward Amplifier: The finite PSR of an amplifier can be modeled as an additive voltage at its output as shown in the equivalent model in Fig. 8(a). With the help of the equivalent model in Fig. 8(b), the output voltage, $v_{\rm psr,ff}$, that appears due to the finite PSR of the amplifier is given by

$$\frac{v_{\rm psr,ff}}{V_{\rm in}} = {\rm PSR}_{\rm ff} \cdot \frac{R_{\rm ff1} + R_{\rm ff2}}{G_{\rm ff} \cdot R_{\rm ff1}} \tag{7}$$

where ${\rm PSR}_{\rm ff}$ is the power-supply rejection of the feed-forward amplifier without the feedback connection, and $G_{\rm ff}$ is the open-loop gain of the feed-forward amplifier. In our design, ${\rm PSR}_{\rm ff} = 3$ dB and loop gain $(R_{\rm ff1} + R_{\rm ff2})/(G_{\rm ff} \cdot R_{\rm ff1})$ is 38 dB. Hence, $v_{\rm psr,ff}/V_{\rm in} = -35$ dB. The voltage $v_{\rm psr,ff}$ can be modeled as an additive at the output of the amplifier in Fig. 5.

Considering only the effect of $v_{\mathrm{psr,ff}}$, on the supply rejection of the LDO, the output PSR of the whole LDO, $\mathrm{PSR}_{vout,\mathrm{ff}}$, due to the feed-forward amplifier is given by

$$\mathrm{PSR}_{vout,\mathrm{ff}} \approx \mathrm{PSR}_{\mathrm{ff}} \cdot \frac{R_{\mathrm{ff1}} + R_{\mathrm{ff2}}}{G_{\mathrm{ff}} \cdot R_{\mathrm{ff1}}} \cdot \frac{1 + \frac{s}{\omega_e}}{A_{eo}\dfrac{R_{f2}}{R_{f1} + R_{f2}}}. \quad (8)$$

Equation (8) shows that the poor PSR of the feed-forward amplifier is attenuated by feedback resistances and the gain of error amplifier. Combining all these effects, $\mathrm{PSR}_{vout,\mathrm{ff}}$ is about 93 dB in the designed FFRC LDO. Equation (8) also demonstrates that $\mathrm{PSR}_{vout,\mathrm{ff}}$ starts to degrade beyond the bandwidth of the error amplifier, and hence it is important to maximize the bandwidth. In this design, a small capacitive load (summing amplifier) exists at the output of the error amplifier, leading to a bandwidth of 330 kHz. Beyond this value, the contribution of $\mathrm{PSR}_{vout,\mathrm{ff}}$ to the total PSR is higher, but its value is still not significant.

2) Summing Amplifier: Similar to the feed-forward amplifier, the PSR of the summing amplifier is reduced through its loop gain. This effect is also modeled as an additive voltage, $v_{\mathrm{psr,ff}}$, at the output of the amplifier that is given by

$$\frac{v_{\mathrm{psr,ss}}}{V_{\mathrm{in}}} = \mathrm{PSR}_{ss} \cdot \frac{R_{s2}//R_{s3} + R_{s1}}{G_{ss} \cdot R_{s2}//R_{s3}}. \quad (9)$$

where PSR_{ss} is the power supply rejection of the summing amplifier without the feedback connection, and G_{ss} is the gain of the summing amplifier without the feedback connection. The output PSR of the whole LDO, $\mathrm{PSR}_{\mathrm{vout,ss}}$, due to the finite PSR of the summing amplifier is given by

$$\mathrm{PSR}_{vout,ss} \approx -\mathrm{PSR}_{ss} \cdot \frac{R_{s2}//R_{s3} + R_{s1}}{G_{ss} \cdot R_{s2}//R_{s3}} \cdot \frac{1 + \frac{s}{\omega_e}}{A_{eo}\dfrac{R_{f2}}{R_{f1} + R_{f2}}} \cdot \frac{1 + \frac{s}{\omega_s}}{A_{so}}. \quad (10)$$

Equation (10) shows that the finite PSR of the summing amplifier is attenuated by its loop gain, error amplifier gain, and the summing amplifier gain. Simulations show a $\mathrm{PSR}_{vout,ss}$ higher than 95 dB is achievable.

In summary, the above analysis showed that the finite PSR of the feed-forward and summing amplifier can be neglected in the analysis as stated earlier in this section.

IV. Stability Analysis

In this section, the design of a stable LDO is demonstrated. Ideally, the feed-forward path does not affect the stability of the LDO because it does not exist in the feedback loop. However in this implementation, the node V_{bias} of feed-forward amplifier is connected to V_{out} to remove the need for another reference voltage. Hence, the feed-forward path appears in the feedback, but still it does not affect the stability as demonstrated in this section. The effect of packaging is considered to highlight the importance of considering the inductance of the bond wire. Two cases are considered: 1) a single bond-wire and 2) a Kelvin connection (two bond-wires).

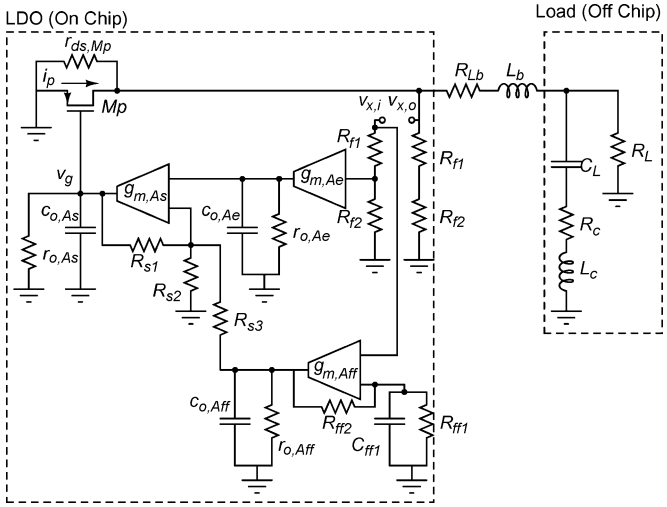

Fig. 9. Open-loop equivalent circuit with single bond wire connection.

A. Single Bond-Wire

Fig. 9 shows the open-loop circuit diagram of the proposed LDO when a single bond wire is used to interface with the external components. The equivalent series inductance (ESL) and resistance (ESR) of the off-chip capacitor is also considered in the analysis.

The open-loop gain of the LDO is given by

$$\begin{aligned}\frac{v_{x,o}}{v_{x,i}} &= \frac{v_g}{v_{x,i}} \cdot \frac{i_p}{v_g} \cdot \frac{v_{x,o}}{i_p} \\ &= -\frac{g_{m,Mp}}{\left(1 + \dfrac{sc_{o,As}\left(1 + \dfrac{R_{s1}}{R_{s2}//R_{s3}}\right)}{g_{m,As}}\right)} \cdot (A_{\mathrm{fb}} - A_{\mathrm{ff}}) \cdot \frac{v_{x,o}}{i_p}\end{aligned}$$

$$A_{\mathrm{fb}} = \frac{R_{f2} g_{m,Ae} r_{o,Ae}\left(1 + \dfrac{R_{s1}}{R_{s2}//R_{s3}}\right)}{(R_{f1} + R_{f2})(1 + s r_{o,Ae} c_{o,Ae})}$$

$$A_{\mathrm{ff}} = \frac{R_{s1}\left(1 + \dfrac{R_{\mathrm{ff2}}}{R_{\mathrm{ff1}}}\right)(1 + sC_{\mathrm{ff1}}(R_{\mathrm{ff1}}//R_{\mathrm{ff2}}))}{R_{s3}} \quad (11)$$

where $v_{x,o}$, $v_{x,i}$, v_g, and i_p are as shown in Fig. 9, $g_{m,Ae}$, $g_{m,As}$, and $g_{m,Mp}$ are the effective transconductance of error amplifier, summing amplifier, and pass transistor, respectively, and $r_{o,Ae}$ and $c_{o,Ae}$ are the total resistance and capacitance at the output of error amplifier. Also, $r_{o,As}$ and $c_{o,As}$ are the total resistance and capacitance at the output of summing amplifier. A_{fb} is the gain of the error amplifier, and A_{ff} is the additional term due to connecting V_{bias} of the feed-forward amplifier to V_{out}. A_{ff} does not affect the stability of the LDO because it is much smaller than A_{fb}, and the loop bandwidth is determined by the output pole. In this analysis the output impedance of the feed-forward amplifier is neglected because it is much smaller than R_{s3}. Fig. 10 shows stability simulation results of the LDO when V_{bias} is connected to V_{out} and when it is connected to a constant reference voltage. As depicted, the feed-forward path does not affect the stability of LDO even if V_{bias} is connected to V_{out}.

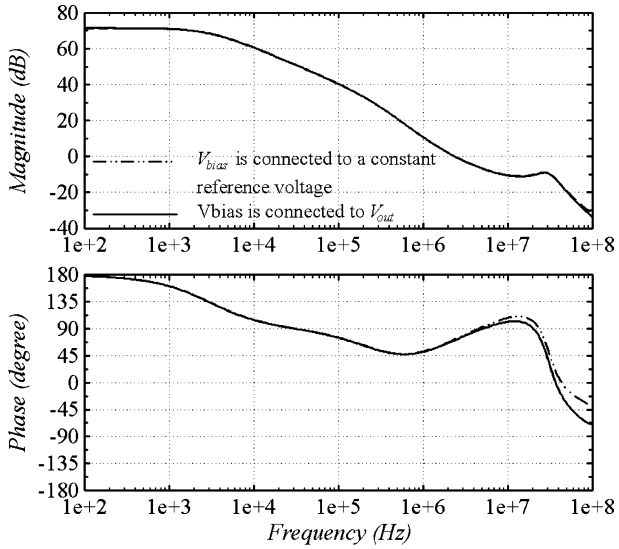

Fig. 10. Schematic simulations of the open-loop gain and phase frequency responses when $V_{\rm bias}$ is connected to $V_{\rm out}$ or to a constant reference voltage. ($L_b = 0$ nH, $C_L = 4$ μF, $L_c = 0.4$ nH, $R_c = 30$ mΩ, $R_L = 40$ Ω, $R_{\rm tot} = 14$ Ω).

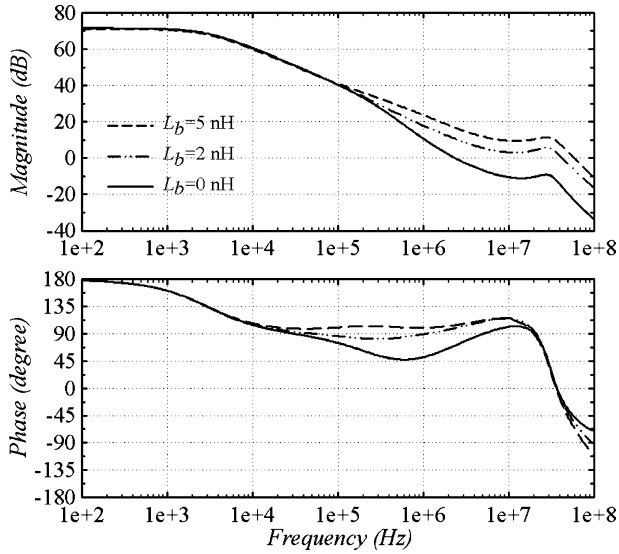

Fig. 11. Schematic simulations of the open-loop gain and phase frequency responses for different values of L_b using single bond-wire. ($C_L = 4$ μF, $L_c = 0.4$ nH, $R_{Lb} = 40$ mΩ per 1 nH, $R_c = 30$ mΩ, $R_L = 40$ Ω, $R_{\rm tot} = 14$ Ω).

The term $v_{x,o}/i_p$ in (11) is the one that is different in single bond wire case and Kelvin connection case. For the single bond wire case, $(v_{x,o}/i_p)|_{\rm single}$ is given by

$$\left.\frac{v_{x,o}}{i_p}\right|_{\rm single} \approx R_{\rm tot}\cdot\frac{1+\dfrac{s}{Q_{z,s}\omega_{oz,s}}+\dfrac{s^2}{\omega_{oz,s}^2}}{\left(1+\dfrac{s}{\omega_{pL1}}\right)\left(1+\dfrac{s}{\omega_{pL2}}\right)}$$

$$\approx R_{\rm tot}\cdot\frac{1+\dfrac{s}{Q_{z,s}\omega_{oz,s}}+\dfrac{s^2}{\omega_{oz,s}^2}}{\left(1+\dfrac{s}{\omega_{pL1}}\right)},$$

$$Q_{z,s} = \frac{\sqrt{(L_b+L_c)C_L}}{\left(\dfrac{L_b}{R_L}+C_L(R_c+R_{Lb})\right)},$$

$$\omega_{oz,s} = \frac{1}{\sqrt{(L_b+L_c)C_L}},$$

$$\omega_{pL1} = \frac{1}{C_L R_{\rm tot}},$$

$$\omega_{pL2} = \frac{R_{\rm tot}}{L_c + L_b\dfrac{R_{\rm tot}}{r_{ds,Mp}//(R_{f1}+R_{f2})}}$$

$$R_{\rm tot} = R_L//r_{ds,Mp}//(R_{f1}+R_{f2}) \qquad (12)$$

where R_{Lb} is the series resistance of the bond-wire. Equations (11) and (12) show that the open-loop transfer function consists of four poles and two zeros. ω_{pL1} is the dominant pole of the loop. ω_{pL2} can be neglected because it appears at very high frequency (GHz range). The other two poles in (11) are the first two non-dominant poles. If L_b and L_c are neglected, only one real zero $(1/C_L R_c)$ appears and it is used to cancel the first non-dominant pole ($1/r_{o,Ae}c_{o,Ae}$ in this case). However in the practical case, L_b and L_c have values of at least 2 and 0.4 nH, respectively. These finite values produce two zeros. Increasing the value of L_b reduces the value at which these two zeros appear. The simulated frequency response for different values of L_b, while $L_c = 0.4$ nH, is shown in Fig. 11. In this simulation, it is assumed that the series resistance of the bonding wire is 40 mΩ for each 1 nH. Fig. 11 shows that increasing L_b beyond a specific value may lead to an instability of the LDO.

The main reason for the instability is that higher values of L_b reduce the value of $\omega_{oz,s}$, and hence, the two zeros move towards the DC frequency. Fig. 12 shows zero locations of (12) for different values of L_b. For $L_b = 0$, the first zero cancels the first non-dominant pole by adjusting the value of R_c, and the second zero appears above the gain-crossover frequency. As L_b increases, two zeros start to move towards DC, and as a result, the gain-crossover frequency is located at higher frequencies. This situation lead to instability of the LDO because the higher non-dominant poles change the phase abruptly at higher frequencies (Fig. 11). To solve this problem, the dominant pole should be decreased to a lower frequency to guarantee the second zero is located after the gain-crossover frequency. As a result, increasing L_b requires reducing the gain-bandwidth product (GBW), and hence the speed of the LDO, when the zero (due to ESR) is used to compensate any non-dominate pole. This example shows the location of zeros is very sensitive to L_b, and it may affect the functionality of LDO.

In summary, the disadvantage of using a single bond-wire can be summarized as follows: 1) zeros are sensitive to the value of L_b, 2) the loop bandwidth has to be decreased, hence lowering the speed, and 3) there is a voltage drop across the bond-wire due to its series resistance which affects the load regulation. Kelvin connection solves these issues.

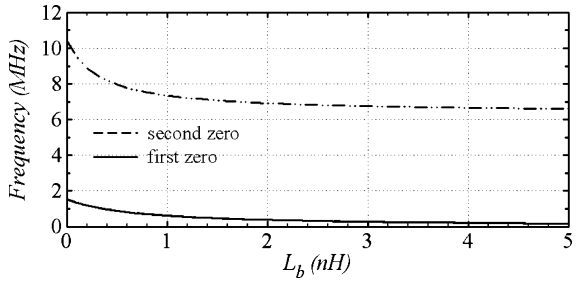

Fig. 12. Zero locations of $(v_{x,o}/i_p)|_{\text{single}}$ for different values of L_b. ($C_L = 4\ \mu$F, $L_c = 0.4$ nH, $R_{Lb} = 40$ mΩ per 1 nH, $R_c = 30$ mΩ, $R_L = 40\ \Omega$, $R_{\text{tot}} = 14\ \Omega$).

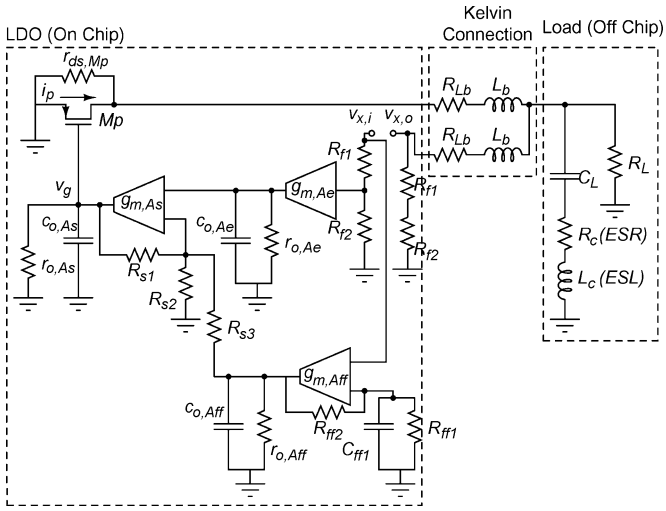

Fig. 13. Open-loop equivalent circuit with a Kelvin connection.

B. Kelvin Connection

To remove the dependency of the two zeros in (12) to L_b, a Kelvin connection is used as an interface with the external load (Fig. 13). The Kelvin connection relies on closing the loop using two bond wires that are connected to the same pin of the package. In this case, $(v_{x,o}/i_p)|_{\text{kelvin}}$ is given by

$$\left.\frac{v_{x,o}}{i_p}\right|_{\text{kelvin}} \approx R_{\text{tot}} \cdot \frac{1 + \dfrac{s}{Q_{z,k}\omega_{oz,k}} + \dfrac{s^2}{\omega_{oz,k}^2}}{\left(1 + \dfrac{s}{\omega_{pL1}}\right)\left(1 + \dfrac{s}{\omega_{pL2}}\right)},$$

$$Q_{z,k} = \sqrt{\frac{L_c}{C_L}} \cdot \frac{1}{R_c},$$

$$\omega_{oz,k} = \frac{1}{\sqrt{L_c C_L}}. \tag{13}$$

Equation (13) shows that the zeros in $(v_{x,o}/i_p)|_{\text{kelvin}}$ do not depend on L_b, and hence a more robust design can be implemented. The zero produced using the ESR of off-chip capacitor, R_c, can be used to compensate the first non-dominant pole, as a result allowing for a larger GBW product. Fig. 14 shows the simulated open-loop gain of the proposed LDO using a Kelvin connection for different values of L_b. As depicted, the magnitude response does not change significantly with L_b when compared to a single bond-wire case. Hence, the design of a more stable LDO system is feasible using the Kelvin connection.

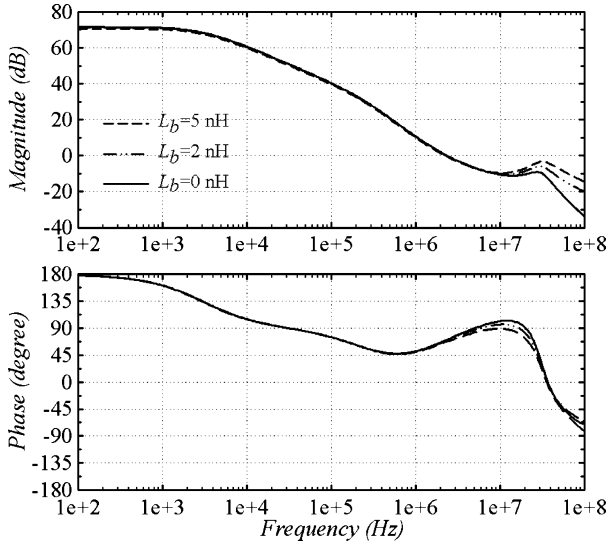

Fig. 14. Schematic simulations of the open-loop gain and phase frequency responses for different values of L_b using Kelvin connection. ($C_L = 4\ \mu$F, $L_c = 0.4$ nH, $R_{Lb} = 40$ mΩ per 1 nH, $R_c = 30$ mΩ, $R_L = 40\ \Omega$, $R_{\text{tot}} = 14\ \Omega$).

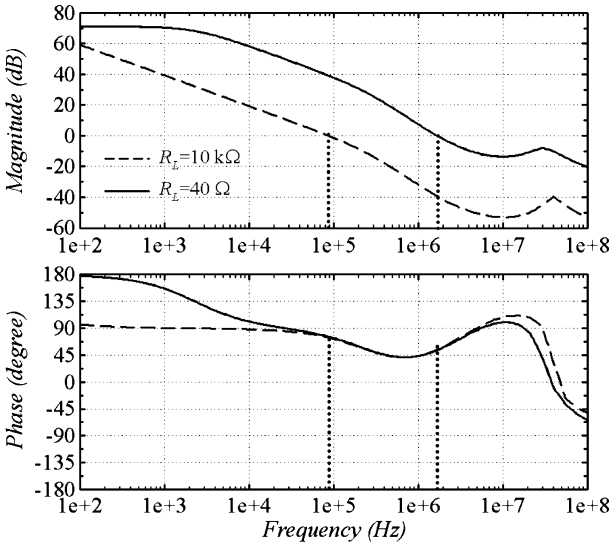

Fig. 15. Simulation of the open-loop gain and phase responses versus frequency of the LDO schematic using Kelvin connection for ($R_L = 40\ \Omega$ and 10 KΩ). ($L_b = 2$ nH $C_L = 4\ \mu$F, $L_c = 0.4$ nH, $R_{Lb} = 40$ mΩ per 1 nH, $R_c = 30$ mΩ, $R_{\text{tot}} = 14\ \Omega$).

The simulated open-loop transfer function of the LDO schematic using a Kelvin connection is shown in Fig. 15. For heavy load condition ($R_L = 40\ \Omega$), the LDO achieves a phase margin of 53° with a GBW of 1.65 MHz. The first non-dominant pole is due to the error amplifier $(1/(r_{o,Ae} \cdot c_{o,Ae}))$ and appears at 330 kHz. This pole is compensated using the real zero produced by ESR of the capacitor. The pole at the gate of the pass transistor appears at a much higher frequency because of the small output resistance of summing amplifier and the use

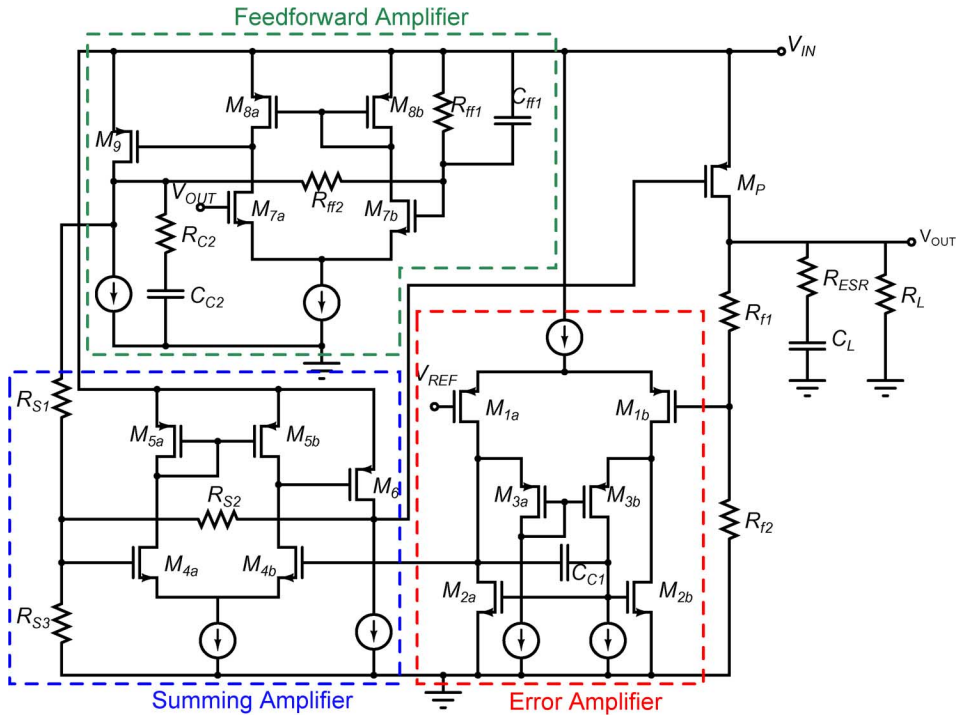

Fig. 16. Transistor-level implementation of the FFRC-LDO.

of smaller technology that reduces the node capacitance. For the light load condition ($R_L = 10\,\mathrm{k}\Omega$) a GBW of 90 kHz with a phase margin of 74° is obtained (Fig. 15). An important observation in Fig. 15 is the complex poles that result in peaking after the unity gain frequency. In case of a single wire, this peaking crosses 0 dB leading to instability. However using the Kelvin connection, the peaking amplitude has been reduced. The peaking beyond the unity gain frequency increases with L_b because of the substrate coupling through the n-well enclosing the high resistivity poly resistors. The n-well is connected to the output voltage at the drain of the pass transistor. Increasing L_b increases the amount of substrate coupling, and therefore the peaking increases. Similar situation happens for the single bond-wire case.

The transient performance in this case is better than the single bond-wire case because one can design for a stable LDO with higher loop bandwidth. In addition, the extra inductor does not affect the transient load/line regulation because it does not appear along the high current variation path. Finally, an additional advantage of the Kelvin connection is better load regulation compared to the single bond-wire case because the output voltage is sensed after the voltage drop across the bond-wire resistance.

V. Circuit Implementation

The complete transistor-level implementation of the FFRC-LDO is shown in Fig. 16. The error amplifier utilizes current sources with improved output impedance as active loads [12]. This implementation boosts the output impedance of the amplifier through the feedback loop formed by transistors M_{3a} and M_{2a}. The resultant gain is higher than 55 dB. In addition, PSRR_e exceeds 90 dB at DC to guarantee that the output PSR

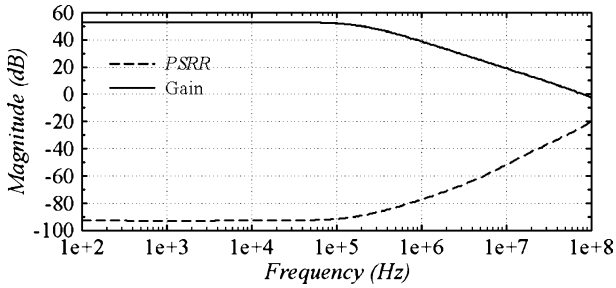

Fig. 17. Schematic level simulations of the gain and PSRR_e of the error amplifier.

of the LDO is not limited by error amplifier as defined in (3). The capacitor, C_{c1}, is added to stabilize the internal feedback loop of the error amplifier. The gain and PSRR_e schematic level simulations of the stand-alone error amplifier are shown in Fig. 17. The error amplifier achieves a 3 dB bandwidth of 180 kHz, and consumes a current of 12 μA. This simulation shows that the PSR of the LDO does not depend on the bandwidth of the error amplifier when the FFRC technique is used. Process, voltage and temperature (PVT) variations showed a variation in the gain and PSRR_e less than 5 dB.

The error amplifier has a limited output swing. This limited swing could be problematic for conventional LDOs when the error amplifier drives the pass transistor to accommodate a wide range of load currents. However in the presented LDO, the summing amplifier drives the gate of the pass transistor. The summing amplifier is implemented using a two stage amplifier configuration with resistive feedback, as shown in Fig. 16. A wide output swing is achieved from the second stage of this amplifier. The pass transistor gate capacitance is used to create the dominant pole of the amplifier, and hence, no additional capacitor is

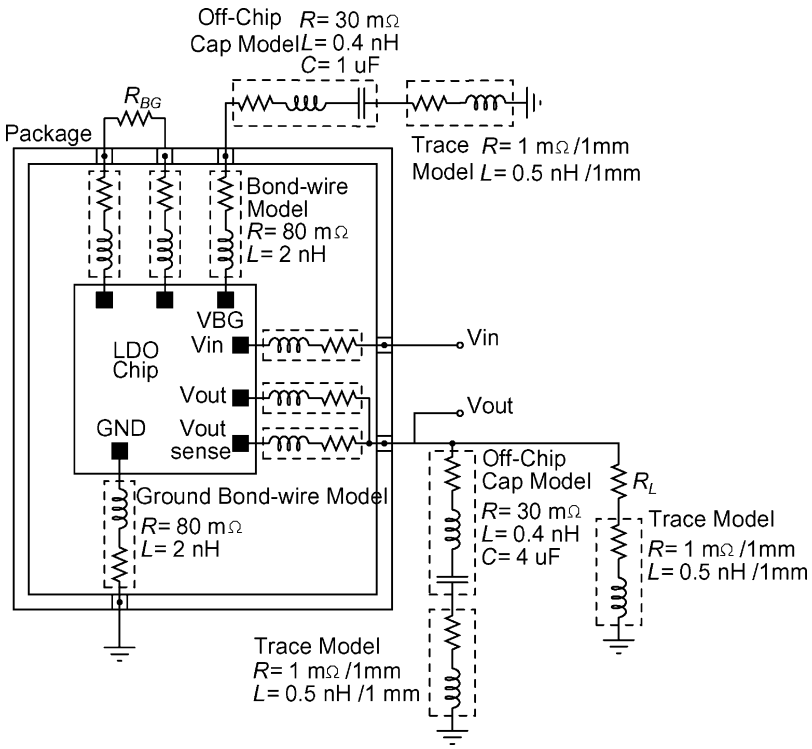

Fig. 18. Simulation setup of the FFRC LDO including the model of trace and off-chip capacitor parasitic models.

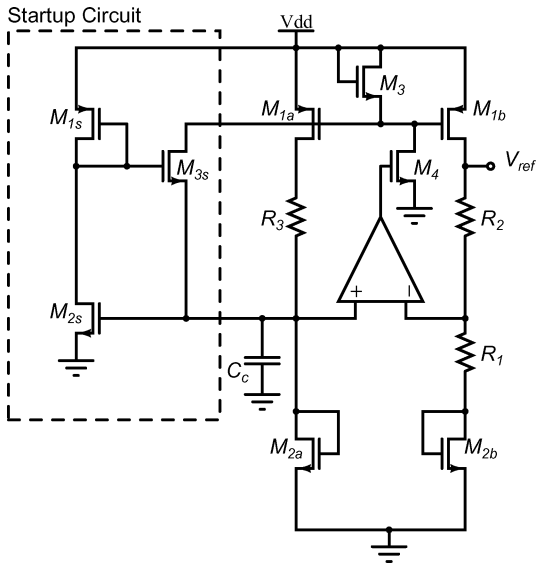

Fig. 19. Transistor-level implementation of the bandgap circuit.

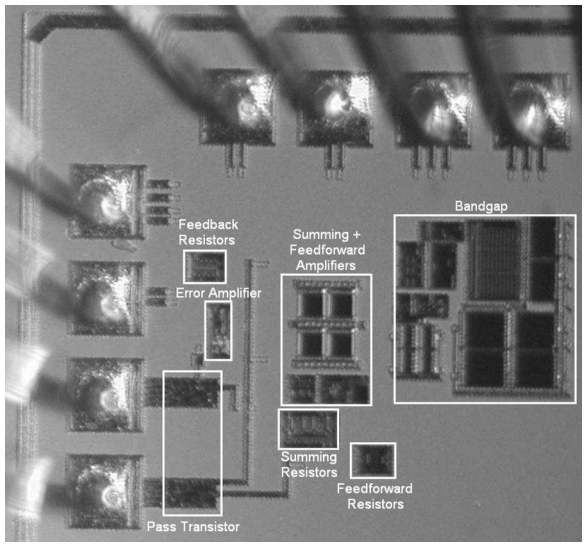

Fig. 20. Chip micrograph of the fabricated LDO with a total active area of 0.049 mm^2 including the bandgap circuitry.

required to stabilize the amplifier. Without summing feedback resistances (R_{s1}–R_{s3}), the output pole exists at 500 kHz, and the internal non-dominant pole is at 28 MHz resulting in an amplifier phase margin of 45°. With the summing feedback resistances, the amplifier has a pole at 28 MHz, which is much higher than the GBW of the complete LDO. Therefore, the two stage topology does not affect the stability of LDO. As explained in Section III-B, the PSRR of the summing amplifier is not critical in this design because the PSRR is attenuated by the gain of the error amplifier. The feed-forward amplifier is also implemented using a two-stage amplifier with resistive feedback. The capacitor C_{c2} and resistor R_{c2} are used to stabilize the amplifier. In this design, each of the summing and feed-forward amplifiers consumes a current of 13 μA. The total on-chip capacitance that is used to compensate the amplifiers is less than 5 pF.

The pass transistor is implemented using a pMOS device with minimum channel length and 2.4 mm width. Interdigitized and common centroid layout techniques are used to achieve high matching between the various resistors and transistors. Kelvin connection is utilized to connect the LDO to the package to reduce the dependency on the bonding inductance. Two off-chip

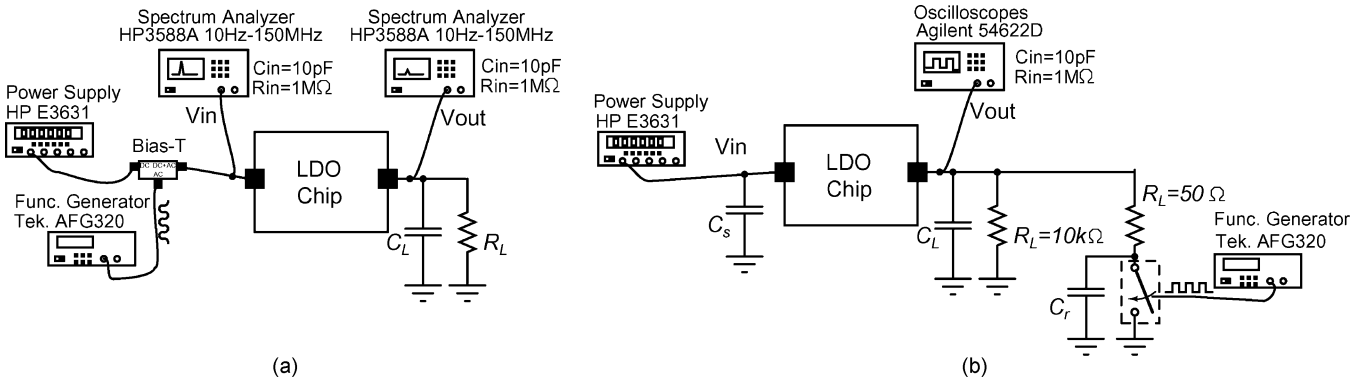

Fig. 21. Measurement setup for (a) PSR and (b) load transient measurements.

capacitors, each 2 μF, are used as the capacitive load of the LDO. During the design phase, the parasitic inductances, capacitances and resistances of the printed circuit board are also modeled to achieve simulations close to the measured performance as demonstrated in Fig. 18. The inductance and resistance of the traces are assumed to be 0.5 nH and 1 mΩ per 1 mm, respectively. Without modeling these effects, the simulated PSR at high frequencies is not close to the one measured.

Bandgap voltage reference is used to generate the reference voltage of the LDO. Fig. 19 shows the implemented bandgap reference voltage circuit based on the architecture in [13]. The basic idea of this circuit is to replicate ripples at the gate of the current mirror (M_{1a} and M_{1b}), such that the output voltage is free from ripples. This is achieved through the transistors M_3 and M_4 [13]. The startup circuit is sized such that ripples leaking through the transistors do not affect the overall PSR of the bandgap circuit. An off-chip resistor is used for R_1 to adjust the required output voltage. The bandgap operates for a supply ranging from 1.15 to 1.8 V. The reference voltage, $V_{\rm ref}$, is selected to be 0.5 V. This value is scaled to 1 V through the feedback resistors, R_{f1} and R_{f2}. The bandgap circuit consumes a total current of 8 μA.

VI. Experimental Results

The LDO is fabricated using 0.13 μm CMOS technology provided through UMC. The chip is encapsulated in a Quad Flat No (QFN) leads package, and the chip micrograph is shown in Fig. 20. The total active area of LDO is 0.1 mm^2 including the bandgap circuitry. The bandgap circuit occupies around 50% of the total area. Two off-chip capacitors, each 2 μF, are used to stabilize the LDO. The off-chip load capacitor has an ESL and ESR of 400 pH and 30 mΩ, respectively. However, the effective ESL and ESR are higher due to the trace parasitics.

The total quiescent current of the LDO is 50 μA at an input of 1.15 V, where 8 μA is consumed by the bandgap circuitry. The LDO operates for an input voltage ranging from 1.15 V to 1.8 V and the output voltage is 1 V. This shows a measured drop-out voltage of 0.15 V. The quiescent current depends on the input voltage and load current due to the DC path formed by summing and feed-forward resistances. At 1.8 V, the quiescent current increases by 6 μA. It is important to note, that the biasing current of the second stage of summing and feed-forward amplifier should account for such current variations.

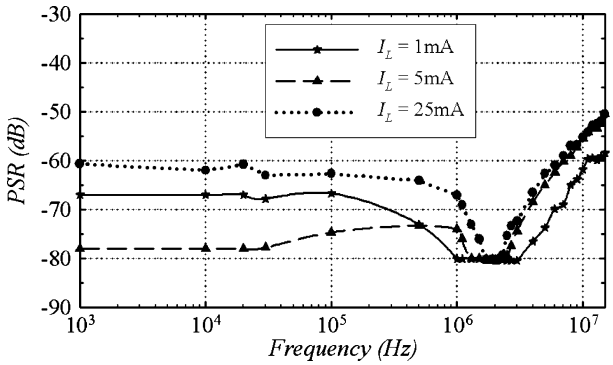

Fig. 22. Measured PSR for different load conditions (drop-out voltage = 0.15 V).

The PSR measurement setup is shown Fig. 21(a). The HP3588A spectrum analyzer with a high input impedance ($R_{\rm in}$ = 1 MΩ) is used to measure the signal level at the input and output of the LDO. The PSR is measured by sweeping the frequency of an input sine wave across the band of interest. The sine wave at the input of LDO is adjusted to 0.1 V at each measurement point, and the DC input is adjusted such that the minimum input signal, including DC and 0.1 V ripples, is 1.15 V. The measured PSR for different load currents is shown in Fig. 22 for a drop-out voltage of 0.15 V and input ripples of 0.1 V. The LDO achieves a worst PSR of $-$56 dB at 10 MHz for a load current of 25 mA. For frequencies above 4 MHz, the PSR starts to increase due to internal poles of the feed-forward and summing amplifiers, and the self resonance frequency of off-chip capacitor. The PSR at a load current of 25 mA is worse than that at 5 mA because the pass transistor is operating near the triode region. In this case, the output conductance of the pass transistor is decreased, hence increases the PSR. Increasing the drop-out voltage moves the operating point towards saturation, and a better PSR is achievable, as demonstrated in Fig. 23. For a conventional LDO with comparable performance at MHz frequencies, the open-loop gain and bandwidth should be increased, simultaneously. This increase comes at the cost of higher quiescent current as in [11], which is not the case using the FFRC technique.

The load transient response is measured using the setup shown in Fig. 21(b). A switch that is controlled by a clock, is used to switch the load current from the minimum to maximum

TABLE I
PERFORMANCE SUMMARY OF THE PROPOSED FFRC-LDO AND COMPARISON WITH THE EXISTING WORK

	Tech. (μm)	Active Area (mm^2)	V_{in} (V)	V_{out} (V)	Drop-out Voltage (V)	Max. Load (mA)	Quiescent Current (μA)	PSR (dB)	Trans. Load Regulation (mV/mA)	$\Delta V_{out}/V_{out}$ (mV/V)	Approach
[8]	0.13	0.166	3	2.8	0.2	150	100*	-57 @ 100 kHz -40 @ 1 MHz N.A. @ 10 MHz	0.133	19.3/2.8	Two pass transistors
[9]	0.6	N.A.	>1.8	1.2	0.6	5	70**	-70 @ 100 kHz -40 @ 1 MHz -27 @ 10 MHz	34.2	766/1.2	Two pass transistors
[11]	0.35	0.053***	>1.05	0.9	>0.15	50	80 @ 25 mA 160 @ 50 mA	-50 @ 100 kHz -50 @ 1 MHz N.A. @ 10 MHz	0.0614	6.6/0.9	Extend loop bandwidth
This Work	0.13	0.049***	>1.15	1	>0.15	25	50****	-60 @ 100 kHz -67 @ 1 MHz -56 @ 10 MHz	0.048	26/1	FFRC

* Quiescent current for no-load condition. For full load the expected quiescent current is higher.
** Error amplifier and voltage reference only. *** Without the bandgap circuit.
**** Overall quiescent current including amplifiers and bandgap voltage reference.

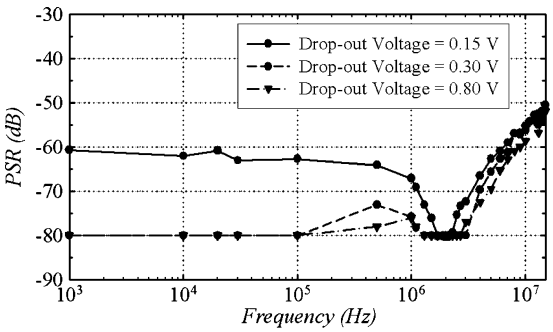

Fig. 23. Measured PSR for different drop-out voltage ($I_L = 25$ mA).

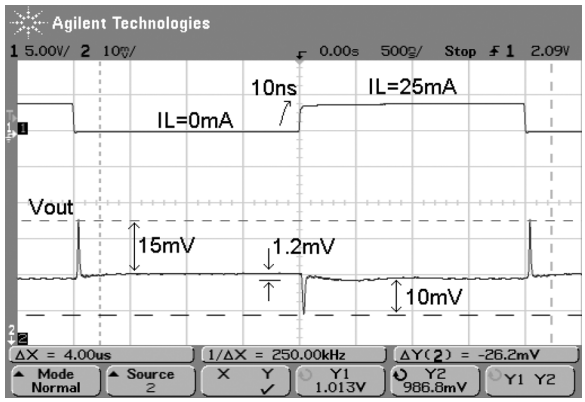

Fig. 24. Measured load transient response for a load current step of 25 mA.

load current. Capacitor C_r is added to control the rise time of the load current. Capacitor C_s is added to guarantee a clean ground at the input of the LDO. Also, this capacitor shorts any inductive effect due to the measurement cables. Fig. 24 shows the measurement of the load transient response. A maximum overshoot of 15 mV is achieved for a 25 mA load current step with rise and fall times of 10 ns. The FFRC technique does not degrade the load transient response, when compared to [9], because the high-current path does not include any additional device for isolation other than the main pass transistor. Finally, the line transient response measurement for an input that varies from 1.15 to 1.8 V shows a maximum variation at the output of 1 mV as shown in Fig. 25. A performance summary for the proposed FFRC-LDO and other existing architectures, which target high PSR LDOs, is summarized in Table I.

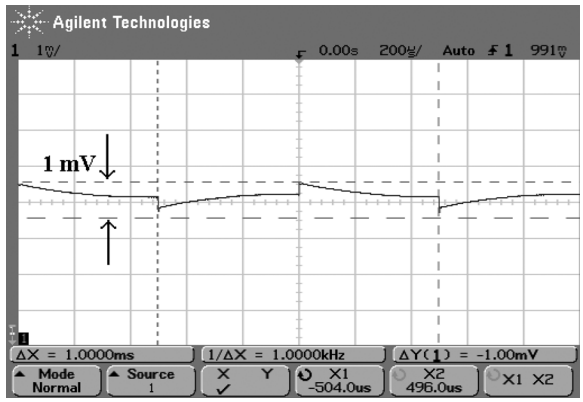

Fig. 25. Measured line transient response for an input step from 1.15 to 1.8 V and a load current 25 mA.

VII. Conclusion

An LDO with a feed-forward ripple cancellation (FFRC) technique was proposed. The proposed topology provides a robust design when the process, temperature and bonding inductance variations are considered. The FFRC can be extended to any existing LDO architecture to yield a high PSR for a wide range of frequencies. A fabricated prototype of the FFRC-LDO achieved a power-supply rejection (PSR) better than -56 dB up to 10 MHz. To our knowledge, this is the first LDO that achieves this high PSR up to 10 MHz. A complete analysis of PSR for the FFRC and the conventional LDO were presented. In addition, it was shown that Kelvin connection at the output helps to increase the GBW of the LDO without affecting the stability at heavy loads. The LDO was implemented in 0.13 μm CMOS technology and occupies an area of 0.049 mm^2. Measurements showed a load regulation of 1.2 mV for a 25 mA step current, and the whole LDO consumed a quiescent current of 50 μA with a bandgap reference circuit included.

Acknowledgment

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Mohamed El-Nozahi (S'00) received the B.Sc. and M.Sc. degrees, both in electrical engineering, from Ain Shams University, Cairo, Egypt, in 2000 and 2004, respectively. Since 2006, he has been with Texas A&M University, College Station, where he is working towards the Ph.D. degree.

From 2000 to 2004, he was a Teaching and Research Assistant with the Electronics and Communications Engineering Department, Ain Shams University. In summer 2007, he was a Design Intern with Texas Instrument Incorporated, Dallas, TX. In summer 2009, he was a Design Intern with Qualcomm Incorporated, San Diego, CA. His research interests include transceivers system and circuit design at millimeter-wave frequencies and power management ICs.

Mr. El-Nozahi was a co-recipient of the 2009 Semiconductor Research Corporation (SRC) Design Challenge Award, and a recipient of TI Excellence Fellowship from 2006 to 2009.

Ahmed Amer (S'05) received the B.Sc. degree in electronics and communications (*magna sum laude*) and the M.Sc. degree in electronic engineering, both from Ain Shams University, Cairo, Egypt, in 2002 and 2006, respectively. He is currently pursuing the Ph.D. degree at Texas A&M University.

From 2002 to 2006, he was a Teaching and Research Assistant in the Electronics and Communications Engineering Department at Ain Shams University. From 2004 to 2006, he was an RFIC Design Engineer in SysDSoft Inc., Cairo, Egypt. During the summers of 2008 and 2009, he was an intern in the medical group at Texas Instruments, Dallas, TX. His research interests include power management electronics, biomedical electronics and wideband/multiband RF receivers design.

Mr. Amer was a co-recipient of the 2009 Semiconductor Research Corporation (SRC) Design Challenge Award. He also received Fouraker/Ebensberger Fellowship in 2007, and Texas Instruments Excellence Fellowship in 2008 and 2009.

Joselyn Torres (S'09) was born in Mayaguez, Puerto Rico. He received the B.S. degree from the University of Puerto Rico, Mayaguez, in 2004, and the M.S. degree from University of Michigan, Ann Arbor, in 2006. Since 2006, he has been working toward the Ph.D. degree in electrical engineering at Texas A&M University, College Station.

He has interned in IBM and Texas Instruments several times. His current research interests are in low-dropout voltage regulators, dc-dc switching converters, and class D amplifiers.

Kamran Entesari (S'03–M'06) received the B.S. degree in electrical engineering from Sharif University of Technology, Tehran, Iran, in 1995, the M.S. degree in electrical engineering from Tehran Polytechnic University, Tehran, Iran, in 1999, and the Ph.D. degree from the University of Michigan, Ann Arbor, in 2005.

In 2006, he joined the Department of Electrical and Computer Engineering at Texas A&M University where he is currently an Assistant Professor. His research interests include design of radio frequency/microwave/millimeter-wave integrated circuits and systems, RF MEMS, related front-end analog electronic circuits, and medical electronics.

Dr. Entesari was a co-recipient of the 2009 Semiconductor Research Corporation (SRC) Design Challenge Award for his work on dual-band millimeter-wave receivers on silicon.

Edgar Sánchez-Sinencio (F'92) was born in Mexico City, Mexico. He received the degree in communications and electronic engineering (Professional degree) from the National Polytechnic Institute of Mexico, Mexico City, the M.S.E.E. degree from Stanford University, Stanford, CA, and the Ph.D. degree from the University of Illinois at Champaign-Urbana, in 1966, 1970, and 1973, respectively.

He is currently the TI J. Kilby Chair Professor and Director of the Analog and Mixed-Signal Center at Texas A&M University. His research work has more than 2410 citations according to the Thomson Reuters Scientific Citation Index. He has graduated 42 M.Sc. and 31 Ph.D. students. He is a coauthor of six books on different topics, such as RF circuits, low-voltage low-power analog circuits, and neural networks. His present interests are in the area of power management, RF communication circuits, analog and medical electronics circuit design. His website is http://amesp02.tamu.edu/~sanchez/.

Prof. Sánchez-Sinencio is the former Editor-in-Chief of IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II. In November 1995, he was awarded an Honoris Causa Doctorate by the National Institute for Astrophysics, Optics and Electronics, Mexico. This degree was the first honorary degree awarded for microelectronic circuit design contributions. He was a co-recipient of the 1995 Guillemin–Cauer Award for his work on cellular networks. He was also a co-recipient of the 1997 Darlington Award for his work on high-frequency filters. He received the IEEE Circuits and Systems (CAS) Society Golden Jubilee Medal in 1999. He also received the prestigious IEEE CAS Society 2008 Technical Achievement Award. He was the IEEE CAS Society's Representative to the Solid-State Circuits Society (2000–2002). He was a member of the IEEE Solid-State Circuits Society Fellow Award Committee from 2002 to 2004. He is a former IEEE CAS Vice President–Publications.