A 3.6-μW Sub-1V Fast-Transient-Response Output-Capacitor-Free LDO Regulator in 0.13-μm CMOS Technology

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Abstract

A sub-1V output capacitor-free CMOS low-dropout regulator, which can realize fast transient behavior with low power dissipation, is presented in this paper. The proposed LDO regulator utilizes class AB operational amplifier to increase the slew rate at the gate of power PMOS transistor during transient state. An extra slew rate enhancement circuit is adopted to deliver extra current when the output voltage increases suddenly with automatic shut-off property. The proposed LDO regulator has been designed and simulated in a standard 0.13-μm CMOS process. The LDO regulator can deliver 100mA load current at 0.9V input voltage with 200mV dropout voltage. The output voltage is able to recover within 1.6μs at 4μA quiescent current, when the output current steps from 50μA to 100mA.

1. Introduction

Output capacitor-free low-dropout (LDO) regulators are widely used in hand-held products powered by Li-battery such as cellular phones and personal digital assistants due to their low-noise characteristics and relatively simple structures. Minimizing quiescent current and dropout voltage to prolong the battery cycle with good regulation and fast response is the main issue of the output capacitor-less LDO regulator design [1].

There are several reported approaches to improve the transient responses without increasing the quiescent current at light load. Q-Reduction presented in [2] increases the bandwidth and phase margin. Slew rate enhancement circuit proposed in [3] and push–pull technique used in [4] boost the slew rate during transient state. Adaptive biasing [5] and dynamic bias-current boosting employed in [6]–[8] improve both the slew rate and bandwidth. Generally, the transient response of the output capacitor-free LDO is dominated by the slew rate at the gate of power PMOS transistor (SR_G) limit [7].

In this work, a sub-1V fast transient response output capacitor-free LDO regulator with low power dissipation is proposed. The structure of proposed LDO and circuit design are shown in Section 2. Simulation results and conclusions are given in Sections 3 and 4, respectively.

2. Proposed fast transient response LDO regulator

The proposed LDO regulator shown in Figure 1 utilizes class AB operational amplifier to increase SR_G for transient-response improvement. Two flipped voltage follower cells composed by M_{03}-M_{08} act as level shifters for M_{01} and M_{02}. M_{11}-M_{13} is the output stage of class AB operational amplifier. C_M is the Miller capacitor forming the feedback loop. The slew rate enhancement circuit composed of M_{A1}-M_{A5} increases SR_G by delivering extra current to push up the gate voltage of power PMOS transistor (M_P) when output voltage increases suddenly. In steady state, M_{A1}-M_{A4} force M_{A5} into cutoff region.

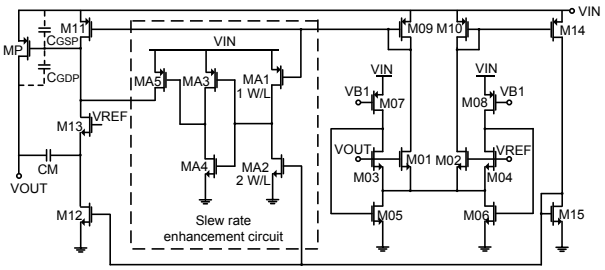

Figure 1. Proposed fast transient response LDO regulator

2.1 Stability of proposed LDO regulator

The small-signal transfer function of the open-loop gain of the proposed LDO regulator shown in Fig. 2 can be obtained by analyzing its equivalent small-signal circuit.

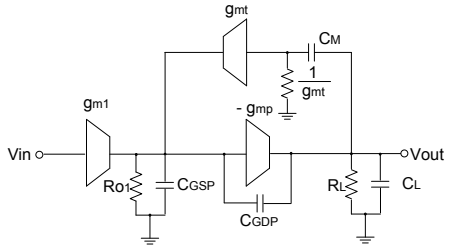

Figure 2. Small-signal model of the LDO regulator

The small-signal transfer function of the open-loop gain of the proposed LDO regulator can then be expressed by a third-order expression which is given by

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$$\frac{V_{out}}{V_{in}} = \frac{A_{dc}\left(1+\frac{s}{\omega_3}\right)\left(1+\frac{s}{\omega_4}\right)}{\left(1+\frac{s}{\omega_d}\right)\left(1+\frac{s}{\omega_1}+\frac{s^2}{\omega_1\,\omega_2}\right)} \quad (1)$$

$$A_{dc} = g_{m1}\, g_{mp}\, R_{o1}\, R_L \quad (2)$$

$$\omega_d = \frac{1}{g_{mp}\, R_{o1}\, R_L\, (C_M + C_{GDP})} \quad (3)$$

$$\omega_1 = \frac{g_{mp}\,(C_M + C_{GDP})}{(C_{GSP} + C_{GDP})\,(C_M + C_L + C_{GDP})} \approx \frac{g_{mp}}{C_L} \propto \sqrt{I_{OUT}} \quad (4)$$

$$\omega_2 = \frac{g_{mt}\,(C_M + C_L + C_{GDP})}{C_M\, C_L} \approx \frac{g_{mt}}{C_M} \quad (5)$$

$$\omega_3 = -\frac{g_{mp}}{C_{GDP}} \quad (6)$$

$$\omega_4 = \frac{g_{mt}}{C_M} \quad (7)$$

A_{dc} is the low-frequency gain. ω_d is the dominant pole. g_{m1} and R_{o1} are the transconductance and output resistance of the operational amplifier, C_L is the output capacitor, g_{mp} is transconductance of M_P, R_L is the overall output resistance, C_{GSP} and C_{GDP} are the gate source capacitance and gate drain capacitance of M_P, respectively.

ω_0 is another important frequency factor, which represents the gain-bandwidth product and is given by

$$\omega_0 = A_{dc}\ \omega_d = \frac{g_{m1}}{C_M + C_{GDP}} \quad (8)$$

Because ω_2 and ω_4 are beyond the gain-bandwidth product and they are almost equal, for simplification, we assume that ω_2 is compensated by ω_4. After neglecting the high frequency right half plane zero ω_3, ω_1 which depends on g_{mp} and C_L should be larger than two times of ω_0 in order to keep the phase margin above 60°. The phase margin would be reduced when M_P delivers low current since ω_1 is proportion to $\sqrt{I_{OUT}}$ but ω_0 keeps constant. Gain-bandwidth product should be well designed by adjusting the value of C_M to obtain enough phase margin at low output current.

2.2 Transient response of proposed LDO regulator

The transient response of output capacitor-free LDO regulator is dominated by SR_G which is reciprocal proportion to the total capacitor at the gate of M_P. In conventional design, C_M between the gate and the drain of M_P degrades SR_G. In proposed LDO regulator, C_M is not connected to the gate of M_P, but to the drain of M_{12}. The voltage at the drain of M_{12} approximately keeps constant from load variation. Hence, C_M in proposed LDO improves the stability of LDO regulator without transient performance degradation. When M_P delivers large output current, M_{13} which is biased by reference voltage would be forced into liner region. The equivalent resistance seen from the gate of M_P to the ground would reduce but it is still much larger than the drain-source resistance of M_{11} and M_{12}. Hence, the R_{o1} is still equal to the drain-source resistance of M_{11}.

The proposed LDO regulator utilizes class AB operational amplifier to realize high slew rate and low quiescent current simultaneously [9]. In the steady state, the gate source voltages of M_{01}-M_{04} are equal and all transistors carry equal quiescent currents set by M_{07} and M_{08}. However, when output voltage (V_{OUT}) decreases, the gate source voltage of M_{01} and M_{03} is kept approximately constant by flipped voltage follower. Accordingly, the gate source voltage of M_{02} and M_{04} increases by V_{OUT} variation during transient state. The differential voltage between M_{01} and M_{02} generates current variations that follow the MOS square law. Most importantly, the maximum output current of M_{02}, and therefore the maximum output current of M_{12}, are no longer limited by the constant current source as conventional operational amplifier, but determined by the current driving capability of M_{05} and M_{06}. Therefore, the current through M_{02} increases drastically and then M_{12} pulls the gate voltage of M_P down momentarily. Hence, SR_G improves dramatically compared with conventional LDO which is constrained by the constant current source, the settling time of LDO regulator reduces greatly and the spike is suppressed.

Similarly, when V_{OUT} abruptly increases, M_{01} and M_{11} deliver large current to push the gate voltage of M_P up immediately. However, the large V_{OUT} forces M_{01} into liner region, hence, the current through M_{11} is limited. To boost SR_G when V_{OUT} abruptly increases, M_{A1}-M_{A5} is utilized. M_{A1} and M_{A2} act as complementary current comparator while M_{A3} and M_{A4} compose an inverter. In steady state, both M_{11} and M_{12} work in saturation region and carry equal current. Since the equivalent W/L aspect ratio of M_{A1} is smaller than that of M_{A2}, M_{A1} works in saturation region while M_{A2} is forced into deep liner region. The gate voltage of M_{A5} is biased to be close to V_{IN}, and therefore M_{A5} is cut off. When V_{OUT} abruptly increases, the current though M_{A1} rises dramatically, the gate voltage of M_{A5} is pulled down to near GND by M_{A3} and M_{A4} immediately. Since the gate source voltage of M_{A5} is approximate equal to the input voltage, M_{A5} delivers large current to push up the gate voltage of M_P during slewing time. The operation is automatically shut down when V_{OUT} approximately returns to the steady state. Compared with conventional SRE circuit [3], the response time of proposed SRE circuit is reduced because the complementary current comparator is adopted.

3. Simulation results

The sub-1V capacitor-free LDO regulator has been simulated in a standard 0.13-μm CMOS. The LDO regulator can provide a 100-mA output current at 0.7 V output voltage, from a supply ranging from 0.9 to 1.2V (the maximum voltage allowed in the 0.13-μm standard CMOS process). The simulated quiescent current of the proposed LDO regulator is 4μA at 0.9V input voltage.

Load and line transient behavior is simulated here to

evaluate the transient performance of LDO regulator. Fig. 3 shows the simulated load-transient responses without output capacitor and with a 100 pF output capacitor (It is used to model the output-parasitic capacitance from the metal lines). The output current is switched between 50uA and 100mA with rise and fall time of 1μS at 0.9V input voltage, 0.7V output voltage and 4μA quiescent current. The undershoot, overshoot and the recovery time of the LDO regulator are about 150 mV, 80 mV and 1.6us, respectively.

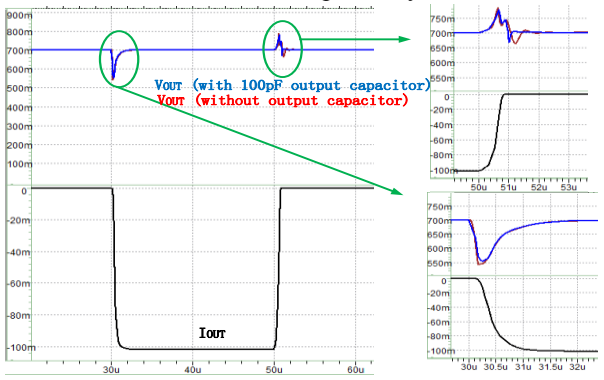

Figure 3. Simulated load transient responses of the proposed LDO regulator

Figure 4 shows the line transient responses under full load (100mA). V_{IN} is changed from 0.9V to 1.2V in 1µS. Both without output capacitor and with a 100 pF output capacitor cases are simulated and the results are almost the same. The proposed LDO recovers from the positive and negative supply changes in 1.4 and 1.2µS with 40mV overshoot and 35mV undershoot, respectively. The simulation results above confirm that the proposed LDO regulator concurrently realizes low-power operation and fast transient response with good stability.

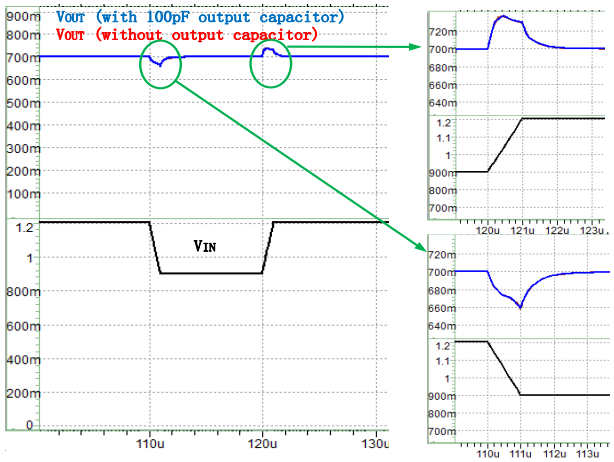

Figure 4. Simulated line transient responses of the proposed LDO regulator

A performance comparison with recent published capacitor-less or capacitor-free LDO regulators is given in Table 1. A figure of merit shown in equation 9 used in [10] is adopted here to evaluate different current efficient designs for improving transient response effect. A lower FOM implies a better transient performance.

$$FOM = T_{settle} * I_Q/I_{load(max)} \quad (9)$$

Table 1 Performance comparison

	[6]	[7]	This work
Year	2011	2010	2012
Technology (µm)	0.13	0.35	0.13
Minimum input voltage (V)	0.9	0.95	0.9
Dropout voltage (mV)	100	200	200
Quiescent current (µA)	1.3	43	4
Output current (mA)	50	100	100
Settling time (µs)	28	~3	1.6
FOM (ns)	0.728	1.29	0.064

4. Conclusion

A sub-1V low power fast transient response output capacitor-free LDO regulator in 0.13µm CMOS technology is presented in the paper. With the joint efforts of class AB amplifier and slew rate enhancement circuit as well as the compensation method, both line and load-transient responses are improved greatly while maintaining low quiescent current. The output voltage is able to recover within 1.6µs with output current switched from 50uA to 100mA at 4µA quiescent current. Simulation results have verified the functions of the proposed regulator.

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