

# High PSRR Class AB Power Amplifier

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**Abstract**—A simple class AB power amplifier topology for wide supply range is presented, which combines feedback type class AB biasing with low voltage gain boosting. The amplifier uses Miller compensation with nulling resistor, but avoids typical poor midband power supply noise attenuation of Miller compensated amplifiers by creating a cancelling signal path from the power supply to the output, using limited gain boosting amplifier bandwidth and bias network. The amplifier achieves 10.6MHz unity gain frequency with phase margin of 51° when driving 20pF||10kΩ load and has approximately 63dB positive power supply noise attenuation at 100kHz frequency, while drawing 298μA from 3V supply.

## I. INTRODUCTION

Constant demand for lower cost and smaller size, together with the low supply voltage requirements of modern IC processes have forced analogue designers to work in a System-on-Chip (SoC) environment where noisy digital and dc-dc converter circuitry are integrated on a same die with sensitive analog blocks such as amplifiers [1], [2]. Because in this environment the available dynamic range of the analog blocks is already severely constrained by the the low supply voltage and power consumption limits [3], *PSRR* performance becomes an important design issue in order not to degrade the available dynamic range of the system any further [4].

The problem of insufficient *PSRR* is often solved by applying differential signal processing or by subregulating the power supply. However in applications such as linear regulators, headphone amplifiers and certain buffers, the heavy resistive load is ground referenced and therefore differential signal processing is not easily applicable and additional voltage drop caused by subregulation is not desired. Therefore in these applications the *PSRR* performance issue has to be solved by topological means.

Improving *PSRR* performance by topological means is not straightforward, because the class AB amplifiers that are required for driving heavy resistive loads normally don't have the asymmetry that is naturally present in the class A amplifiers. In the single supply environment the topological asymmetry, which also leads to asymmetrical *PSRR*, is however desired. This is because normally only the positive rail of the amplifier is connected to a noisy supply, while the lower rail of the amplifier is connected to a common reference node. Another topological problem is related to the frequently used Miller compensation. As explained e.g. in [5], above the dominating pole frequency the Miller capacitor acts as a short circuit, which creates an unity gain signal path from the power

supply to the output. This unnecessarily degrades the midband positive supply  $PSRR_{dd}$  due to fact it depends on the ratio of the signal path gain  $A_v(s)$  and the parasitic power supply gain  $A_{dd}(s)$ .

This paper introduces a high gain, high  $PSRR_{dd}$  power amplifier topology, which achieves excellent bias current stability and is also suitable for low voltage applications. The suggested *PSRR* improvement technique is based on creating a parallel signal path from the power supply to the output by using limited gain boosting amplifier bandwidth and bias network. The additional signal path creates needed asymmetry to the class AB amplifier and cancels the unity gain signal path through the output stage above dominant pole frequency. Because all the components are already part of the amplifier topology the suggested technique does not require any additional components, which is a considerable advantage over existing *PSRR* improvement techniques [6], [7].

In section II structures of the amplifier and the constant-gm bias source are shown and operation of each sub-block is explained. In section III the circuit technique to improve gain boosted amplifier *PSRR* is introduced through small signal analysis and finally in sections IV and V measurement results are shown with conclusions.

## II. AMPLIFIER TOPOLOGY

In addition to limited midband *PSRR*, typical problems in designing a Miller compensated class AB amplifier for wide supply range are: how to stabilize the quiescent current consumption despite the large mirroring ratios and different  $V_{DS}$  voltages appearing in the design and how to obtain high DC gain despite impact ionization effects.

The suggested Miller compensated amplifier that solves the above mentioned problems is based on an amplifier described in [8] and is shown in Fig. 1. It is basically a gain boosted folded cascode amplifier, which uses feedback type class AB circuit in controlling the output stage transistor quiescent and minimum currents.

In the following the operation of each essential transistor and circuit block is explained, except the *PSRR* improvement circuit, which is examined in detail in section III.

$M4HV$  is a high voltage transistor that is used for two purposes. First it equalizes the  $V_{DS}$  voltages of the lower split cascode, which helps to reduce systematic offset. Second, it protects the transistor  $M15$  from impact ionization, which starts to degenerate DC gain above 3V supply.

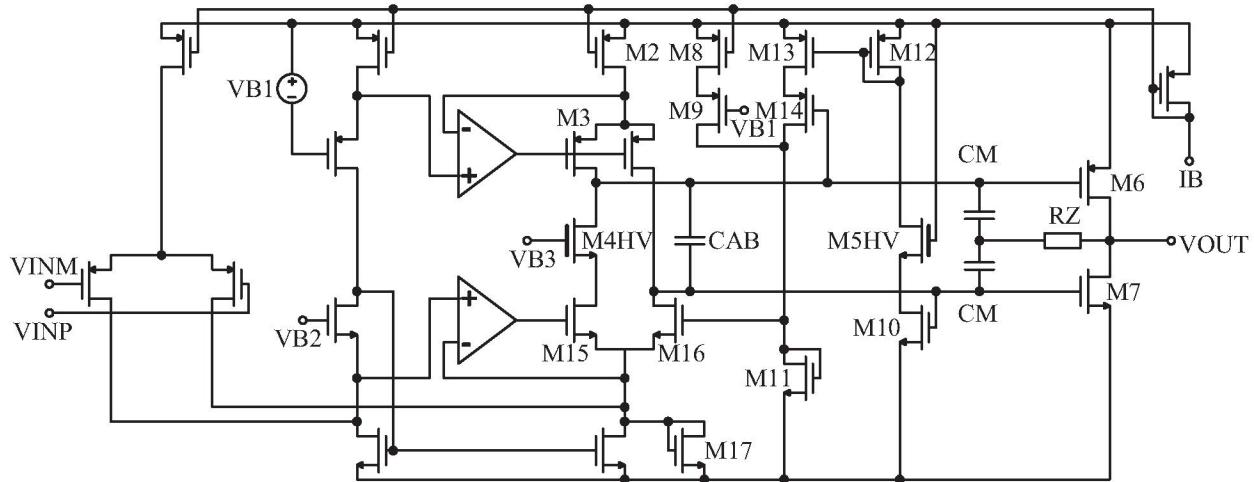


Fig. 1. Schematic of the amplifier.

The improved class AB control circuit includes transistors  $M5HV$  and  $M8-M11$ . The purpose of the transistor  $M5HV$  is two fold. First it makes the measuring transistor  $V_{DS10}$  to match better the output stage transistor  $V_{DS7}$  therefore improving the current measurement accuracy as the supply voltage is varied. Second it drives the measuring transistor  $M10$  into triode region when  $NMOS$  output stage transistor is driving heavy resistive loads thus limiting the amount of current wasted in the class AB control loop. Transistors  $M8$  and  $M9$  further help to stabilize the output stage bias current by creating a supply dependent change of  $V_{GS11}$ , which matches the supply dependent change of bias voltage  $VB2$  thus keeping the current in the class AB control loop constant.

#### A. Gain Boosting Amplifiers

Amplifier topology of Fig. 1 allows easy connection of current input gain boosting amplifiers, shown in Fig. 2, to the split cascode transistors  $M15$  (and  $M3$ ). This is possible, because ideally the gain boosting amplifier maintains the gate of  $M15$  at the same potential as  $VB2$ , which in turn is tracked by the fast feedback class AB control circuit.

Potential problem with the suggested configuration is the operation under large negative inputs that can temporally drive the split cascode transistors  $M15$  and  $M16$  into cut off region. If the cascode transistors are driven deeply into cut off region the  $M15$  gate voltage starts to drift towards lower supply rail causing delays that lead to severe nonlinear overshoot in the step response. This behavior is prevented by adding a minimum size transistor  $M17$  and a voltage clamp with intentional offset that shown in Fig. 3. The voltage clamp creates a temporary feedback path that keeps the  $M15$  gate voltage approximately constant during slew rate limited operation.

### B. Constant- $gm$ Bias Source

In order to have good quiescent current stability and *PSRR* performance the bias current for the amplifier should be as stable as possible [9]. In this work this was achieved by using

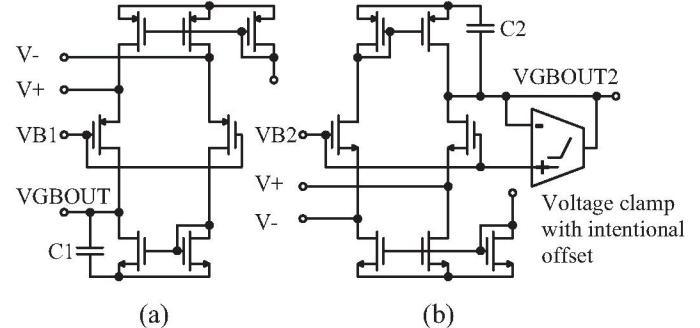


Fig. 2. The PMOS side (a) and NMOS side (b) gain boosting amplifiers.

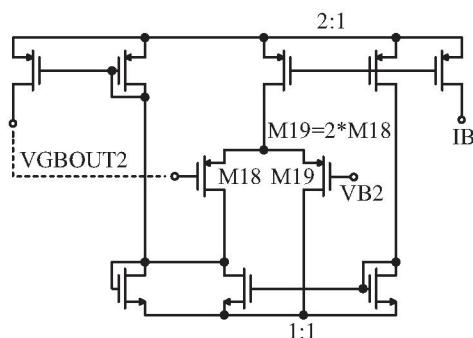


Fig. 3. Voltage clamp of the lower gain boosting amplifier.

a slightly modified constant-gm bias source described in [10] and shown in Fig. 4.

Inclusion of the capacitor  $C2$  to the bias circuit stabilizes the feedback loop through the start up circuitry during power up transient. In addition to stabilizing the start up feedback loop the capacitor  $C2$  forms a first order low pass filter with  $M20$  from the power supply to the gate of  $M21$ . This reduces interaction between the core and the start up feedback loops by reducing the likelihood of false activation of the start up circuit during normal operation in a noisy environment.

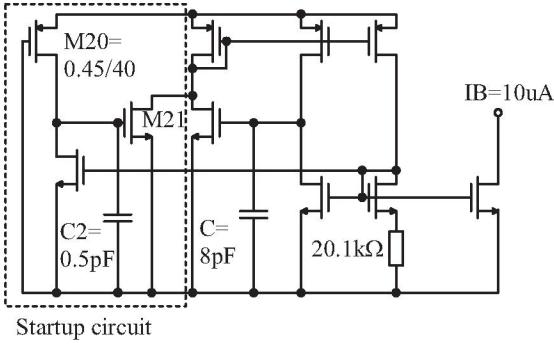


Fig. 4. Constant-gm bias source.

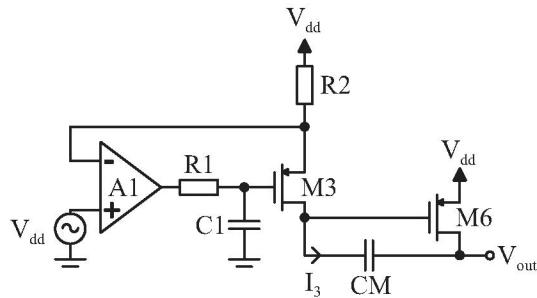


Fig. 5. Half circuit for calculation of  $A_{dd}$ .

### III. PSRR IMPROVEMENT TECHNIQUE

The suggested *PSRR* improvement technique suppresses one of the parasitic power supply gains above the dominant pole frequency. This is done by creating an additional parallel signal path from the power supply to the output, by using limited gain boosting amplifier bandwidth and bias network, which cancels the unity gain signal path through the Miller capacitor and the output stage. The needed asymmetry is obtained by applying transconductance-output impedance matching, to be explained next, only to the PMOS side.

The mechanism how the inverting unity gain signal path can be created is most easily understood by performing an intuitive analysis of the positive power supply gain  $A_{dd}$  half circuit shown in Fig. 5.

Solving the transfer function  $I_3(s)/V_{dd}(s)$  from Fig. 5 gives

$$\frac{I_3(s)}{V_{dd}(s)} = \frac{\frac{(1+R_1C_1)s}{R_2A_1}}{1 + \frac{R_1C_1s}{A_1}} \quad (1)$$

At midband frequencies (1) is further simplified to

$$\frac{I_3(s)}{V_{dd}(s)} = \frac{R_1C_1s}{R_2A_1} \quad (2)$$

Combining (2) with an approximate output stage transfer function

$$\frac{V_{out}(s)}{I_3(s)} = \frac{-1}{C_M s} \quad (3)$$

results gain of -1 as long as

$$C_M = \frac{R_1C_1}{R_2A_1} = \frac{C_1}{R_2g_{m1}} \quad (4)$$

, where  $g_{m1}$  is the gain boosting amplifier input stage transconductance. In other words, the presented technique relies on accurate matching of transistor output impedance and transconductance and the two capacitors in order to be effective. Complete analysis of Fig. 5 with the output stage reveals that the above choice, which sets the additional signal path gain to -1, creates two complex high frequency zeroes, which appear approximately at

$$z_1, z_2 = \sqrt{\frac{g_{m1}R_1R_2 - R_3}{C_1C_M R_1R_2R_3}} \quad (5)$$

Equation (5) is useful in design, because the zero locations indicate the frequency up to where the amplifier maintains its DC power supply rejection performance.

### IV. MEASUREMENT RESULTS

The amplifier was manufactured in a high voltage  $0.35\mu\text{m}$  CMOS process. The amplifier was measured using supply voltages ranging from 2.7V to 5V. Typical amplifier performance at 3V supply and with typical 20pF||10kΩ load is summarized in Table I.

Measured frequency and 1/PSRR responses are given in Figs. 6 and 7 respectively. PSRR performance was constant over the measured temperature range of -40 to +85°C and over supply range from 2.7V to 5V. Typical 1/PSRR<sub>dd</sub> at 100kHz frequency was loop gain +23dB.

Large signal step response is given in Fig. 8. It shows no nonlinear overshoot, which proofs that the voltage clamp concept discussed in section II was working properly.

### V. DISCUSSION

A power efficient high gain class AB power amplifier topology with excellent quiescent current stability and midband PSRR<sub>dd</sub> was described. Amplifier used feedback type class AB circuit to control the quiescent and the minimum currents of the output stage transistors and was compensated using SMCNR, but avoided normal problems such as poor midband PSRR and quiescent current supply dependence associated with this simple amplifier topology.

TABLE I  
PERFORMANCE SUMMARY

Quiescent current consumption	$298\mu\text{A}$
Maximum capacitive load	>100pF
Maximum output current (1V from rails)	109mA
Quiescent current variation with supply	1.3 %/V
DC gain	>106dB
Line regulation	80.4dB
Unity gain frequency	10.6MHz
Phase margin	51°
Slew rate min.	$5.8\text{V}/\mu\text{s}$

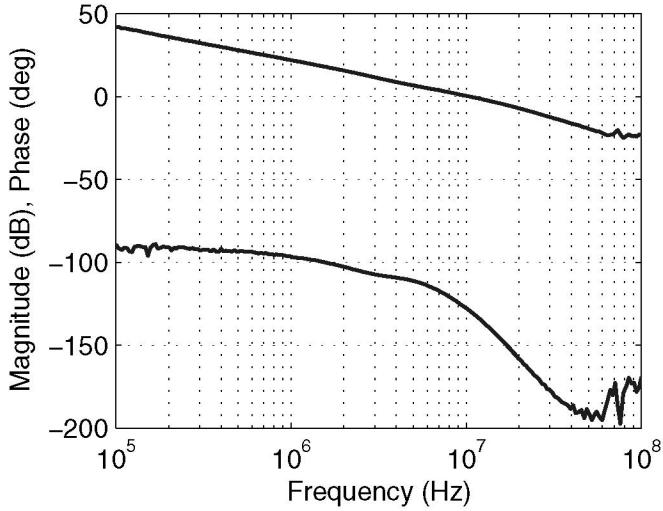


Fig. 6. Amplifier frequency response with  $20\text{pF}||10\text{k}\Omega$  load.

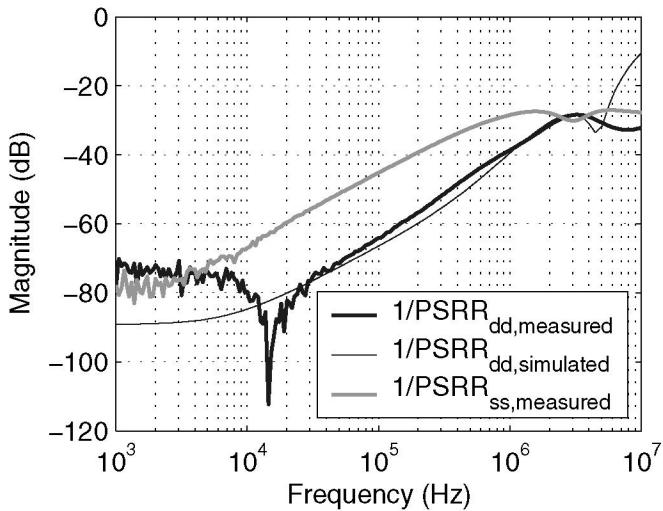


Fig. 7. Simulated and Measured 1/PSRR.

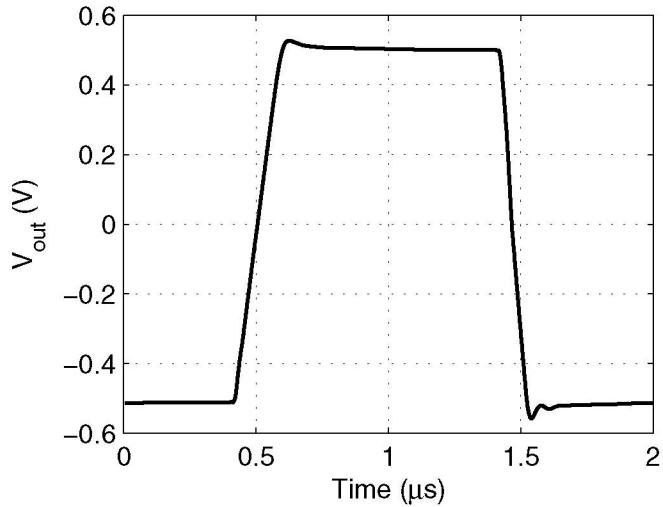


Fig. 8. Large signal step response with  $20\text{pF}||10\text{k}\Omega$  load.

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