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Mikko Loikkanen

DESIGN AND COMPENSATION OF HIGH PERFORMANCE CLASS AB AMPLIFIERS

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MIKKO LOIKKANEN

DESIGN AND COMPENSATION OF HIGH PERFORMANCE CLASS AB AMPLIFIERS

Academic dissertation to be presented with the assent of the Faculty of Technology of the University of Oulu for public defence in OP-sali (Auditorium L10), Linnanmaa, on 12 May 2010, at 12 noon

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Abstract

Class A and class AB operational amplifiers are an essential part of a mixed- signal chip, where they are used as active filter sub-blocks, compensators, reference current generators and voltage buffers, to name just a few of many applications. For analog circuits such as operational amplifiers a mixed-signal chip is a very unfriendly operating environment, where the power supply is often corrupted by high current switching circuits. In addition, power supply voltages for analog blocks are shrinking, because of the deployment of new battery technologies and fine line length integrated circuit processes, which can reduce the amplifier dynamic range a problem requiring supply insensitive low voltage compatible amplifier topologies and other analog blocks.

The aims of this thesis were to further develop the low voltage compatible class AB amplifier topologies published earlier by other authors, to improve their bandwidth efficiency by means of re-examining two- and three-stage amplifier compensation techniques and to find solutions for enhancing the high frequency power supply noise rejection performance of class A and class AB amplifiers without degrading their signal path stability.

The class AB amplifier cores presented here improve the amplifier’s power supply noise insensitivity at high frequencies and increase bandwidth efficiency when compared to the commonly used two-stage Miller compensated amplifier, enabling the construction of better buffers and more power-efficient and reliable low voltage mixed signal chips.

Keywords: amplifiers, analog circuits, CMOS analog integrated circuits, compensation, feedback amplifiers, operational amplifiers, power supply rejection ratio

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Abbreviations and symbols

ADC	Analog to digital converter
AhujaR	Cascode compensated amplifier with a separation resistor
CMRR	Common-mode rejection ratio
FOM	Figure of merit
KCL	Kirchhoff's current law
LDO	Low dropout linear regulator
LHP	Left half plane
NMC	Nested Miller Compensation
NMC+HBW	Nested Miller Compensated amplifier with a wide bandwidth stage
OpAmp	Operational amplifier
PSRR	Power supply rejection ratio
RHP	Right half plane
SAhuja	Strange cascode compensated amplifier
SMC	Simple Miller compensation
SMC+FF	Simple Miller Compensation with feedforward stage
SMC+HBW	Simple Miller Compensated amplifier with a high bandwidth stage
SMCNR	Simple Miller Compensation with nulling resistor
SMCR	Simple Miller Compensated amplifier with a separation resistor
SR	Slew rate
SSMC	Strange Simple Miller Compensated amplifier

γ	Body-effect coefficient
μ_o	Surface mobility of the channel
ω_{-3dB}	Closed loop -3dB bandwidth
ω_d	Damped natural frequency, true oscillation frequency
ω_{eq}	Equivalent second pole
ω_n	Undamped natural frequency
ω_t	Feedback loop unity-gain frequency
ϕ_F	Fermi potential
θ	Phase
ζ	Damping factor
$\zeta_{HF-pole}$	Three-stage amplifier high frequency pole damping factor

A_{cm}	Amplifier common-mode gain
A_{DC}	Gain stage/amplifier DC gain

$A_{dd,ss}$	Frequency dependent small signal gain from the positive/negative power supply to the amplifier output
A_v	Amplifier differential small signal gain
C_{ox}	Gate oxide capacitance per unit area
g_m	Small signal transconductance
GBW	Gain-bandwidth product
GBW_i	Innermost compensation loop gain bandwidth product
I_D	Transistor DC drain current
K	Separation factor
K_i	Inner compensation loop separation factor
L	Transistor channel length
n	Weak inversion slope factor
p_1	First pole
p_2	Second pole
p_3	Third pole
p_{eq}	Equivalent second pole
PM	Phase margin
R_{ds}	Transistor output resistance
V_{eff}	Effective gate-to-source voltage of a MOS transistor
$V_{th,0}$	Zero bias threshold voltage
V_{th}	Threshold voltage
V_t	Thermal voltage
V_X	Node x DC voltage
V_x	Node x total voltage
v_x	Node x small signal voltage
W	Transistor channel width
z_1	First zero
z_2	Second zero

List of original articles

I Loikkanen M & Kostamovaara J (2006) Low voltage CMOS power amplifier with rail-to-rail input and output. Analog Integrated Circuits and Signal Processing 46(1): 183–192.

II Loikkanen M & Kostamovaara J (2003) Active nested miller compensation. Proceedings of the European Conference on Circuit Theory and Design 1: 62–65.

III Loikkanen M & Kostamovaara J (2004) Improving capacitive drive capability of miller compensated amplifier. Proceedings of the 22th Norchip Conference: 257–260.

IV Loikkanen M & and Kostamovaara J (2005) Improving capacitive drive capability of two-stage op amps with current buffer. Proceedings of the European Conference on Circuit Theory and Design 1: 99–102.

V Loikkanen M & Kostamovaara J (2006) PSRR improvement technique for amplifiers with miller capacitor. Proceedings of the International Symposium on Circuits and Systems: 1394–1397.

VI Loikkanen M, Bognár G & Kostamovaara J (2006) PSRR improvement technique for single supply class AB power amplifiers. Electronics Letters 42(25): 1435–1436.

VII Loikkanen M & Kostamovaara J (2006) High PSRR class AB power amplifier. Proceedings of the 24th Norchip Conference: 71–74.

VIII Loikkanen M, Keränen P & Kostamovaara J (2008) Single supply high PSRR class AB amplifier. Electronics Letters 44(2): 70–71.

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1 Introduction

1.1 Motivation and aim of the research

Although the use of amplifiers has not changed dramatically since the term 'operational amplifier' was introduced in the 1940's, the surroundings in which amplifiers function have. Single supply operational amplifiers are part of a complex system on a modern mixed-signal chip, where they commonly serve as reference voltage and sampling buffers, pre-regulators and filters/compensators, e.g. in switching voltage/current regulators, and also as low dropout linear regulators (LDO) when the permitted output capacitor is not large enough for standard regulator structures.

The operating environment for an amplifier on a mixed-signal chip is a hostile one. Fine line length processes often require supply voltage down-regulation, which increases interaction between the different parts of the chip through a common supply-, even when down regulation is not needed, the supply voltage may still be corrupted by high current switching circuits, which can cause the battery voltage to droop by several hundred millivolts in less than ten microseconds. Yet another problem concerns the future low voltage battery technologies, which under worst-case conditions require portable circuits to work at supply voltage levels down to 2.3V, in some cases preventing the use of certain well established class AB amplifier topologies [1, 2].

The aim of this thesis was to develop two- and three-stage low voltage compatible class AB amplifier topologies for mixed-signal environments, topologies which are capable of driving variable capacitive and resistive loads in a power efficient manner. Particular attention was to be paid to power supply noise attenuation at high frequencies, because it is easier in practise to solve power supply noise problems by controlling the disturbances at the beginning of the reference chain than later, at the system level.

As design complexity increases markedly when moving from the well-known two-stage class A folded cascode designs to three-stage class AB amplifiers, the emphasis here is on circuit topologies that have simple operation principles. This, together with the approximate transfer functions given in this thesis and in the original articles, gives the designer an insight into circuit operation that allow fine tuning of the design even in cases where hand calculations do not compare favorably with the actual simulations.

1.2 Thesis organization

The thesis is organized as follows. First, Chapter 2 reviews the amplifier input and output stages and compensation techniques which are frequently encountered in practise. The emphasis is on two-stage amplifier design techniques, although part of thesis deals with three-stage amplifiers, mainly because the latter are still rare in practical usage. The given transfer functions are by no means meant to be exact. Their only purpose is to be able show the limitations of each compensation technique discussed and the measures which can be taken to improve amplifier stability.

Chapter 3 summarizes the original papers included in the thesis and presents some unpublished experimental results which were not available at the time of the publications. Finally, the work carried here is compared with with published amplifier realizations in Chapter 4 and the thesis is summarized in Chapter 5.

2 Amplifier design techniques and building blocks

All amplifiers, whether of the two-stage class A or three-stage class AB type, are composed of relatively simple subblocks which implement a certain analog function such as level shift or differential to single-ended conversion. Chapter 2 reviews some of the most frequently encountered amplifier building blocks, starting from class A rail-to-rail input and class AB output stages and ending with amplifier frequency compensation and high frequency power supply rejection ratio (PSRR) improvement networks.

2.1 Input stages

Since the input stage of an amplifier is the stage that connects directly to the application environment, the limits defined by the application serve in many cases as specifications for the input stage, as common-mode disturbances, random noise or input stage induced distortion cannot longer be corrected in the subsequent stages.

Besides setting the ultimate noise limits for the amplifier, the input stage also determines the range of common-mode input signals that it can handle. As an operational amplifier is typically used in a closed-loop configuration, except for the lowest supply voltages, amplifiers other than those intended as buffers do not necessarily require rail-to-rail input stages as the maximum voltage swing in these cases is limited by the amplifier output stage, as seen from the Fig. 1 [3]. Nevertheless, almost all modern stand-alone amplifiers in practice contain a rail-to-rail input stage to ease application development, which makes the design of good rail-to-rail input stage an important subject [4]. The perfect input stage is yet to be discovered, but many techniques that come close to this have been published.

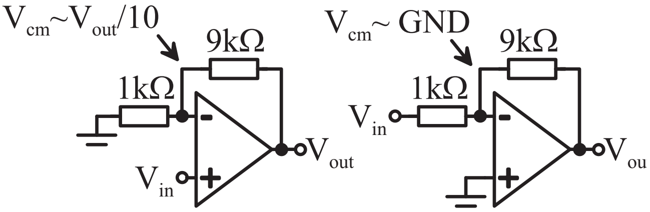


Fig. 1. Examples of operational amplifier configurations, which do not necessarily require rail-to-rail input stage.

2.1.1 NMOS||PMOS input stage

The most popular way of achieving full rail-to-rail input swing is based on a complementary NMOS||PMOS input stage as shown in Fig. 2 [5–7]. The advantage of this approach that it is easily applicable to any CMOS process, but it also has serious drawbacks, such as offset variation as a function of common-mode voltage, non suitability to low voltage amplifiers where $V_{supply} < V_{GS,NMOS} + V_{GS,PMOS} + 2V_{DS,sat}$. and non-constant total input pair transconductance without added control circuitry [3]. In addition, the input stage requires a special summing circuit, which makes the complete stage quite complex and limits its usability in amplifiers that necessitate input stage feed-forward compensation techniques.

The problems entailed in non-constant total input stage transconductance can be solved by controlling the currents that flow in the NMOS and PMOS differential pairs so that the sum of the transconductances remains constant irrespective of the common-mode input voltage.

$$g_{m,NMOS} + g_{m,PMOS} = constant \tag{1}$$

The transconductance in weak-inversion MOS transistor is directly proportional to the current, as shown:

$$g_m = \frac{I_D}{2nV_t}, \tag{2}$$

where I_D is the drain current, n is the weak-inversion slope factor and V_t is the thermal voltage. The sum of transconductances can thus be kept constant by keeping the sum of the input pair currents constant [8].

$$I_{D,NMOS} + I_{D,PMOS} = constant \tag{3}$$

Implementation of (3) is relatively simple [4, 7], as shown in Fig. 2. In this circuit $M1$

serves as a common-mode voltage measuring transistor, which divides the constant bias current I_1 between the two input stage differential pairs.

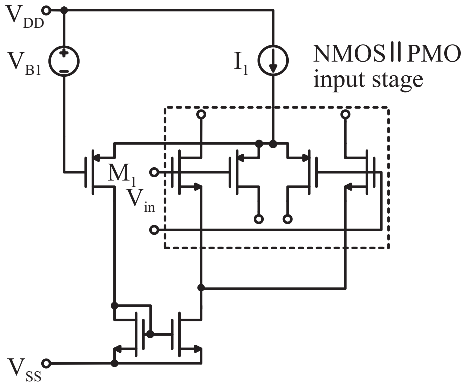


Fig. 2. A weak inversion NMOS||PMOS rail-to-rail input stage.

Accurate control of total input pair transconductance is not as easy to achieve in strong as in weak inversion, because the input pair operation regime changes from strong to weak inversion when the transistors are close to cutoff. Sufficiently stable input pair transconductance can be obtained, however, by controlling the input pair currents in a square root fashion (4), e.g. by means of a translinear loop [8], current switches [9] or a minimum selector circuit [4].

$$\sqrt{I_{D,NMOS}} + \sqrt{I_{D,PMOS}} = constant \tag{4}$$

Equation (4) can also be written in a different form using the dependence of MOS transconductance on V_{eff}, as shown by (5).

$$V_{GS,NMOS} + V_{GS,PMOS} = constant \tag{5}$$

A constant total g_m can then be obtained in strong inversion by regulating the sum of the gate-to-source voltages to a constant value.

The circuit realization of a constant rail-to-rail input stage of the form (5) is very elegant [6], as shown in Fig. 3. Here $M1$ and $M2$ implement an electronic zener diode/voltage clamp, which keeps the sum of the gate to source voltages and the input stage transconductances approximately constant despite the varying common-mode input voltage.

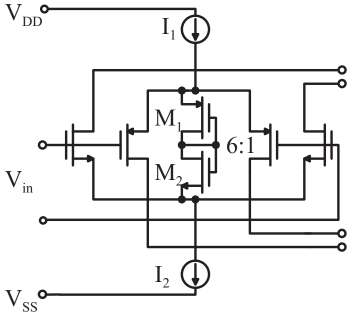


Fig. 3. Electronic zener based rail-to-rail input stage operating in strong inversion.

2.1.2 Charge pump input stage

Stabilization of the input stage transconductance facilitates amplifier frequency compensation by fixing the unity gain frequency, but it does not invalidate the fact that without trimming the input pair offset variation as a function of the input common-mode voltage will cause additional distortion and limit the common-mode rejection performance of the amplifier [9]. Many authors have therefore suggested alternative rail-to-rail input approaches which are based on a single input pair, allowing either an extended or a full rail-to-rail input common-mode range. Three such rail-to-rail input approaches will be discussed next: the charge pump approach, the bulk debiasing approach and the resistive level shifting approach.

The charge pump approach, shown in Fig. 4, is based on a low noise, low ripple charge pump which generates a high voltage supply rail for the input pair that exceeds the nominal supply by approximately 1V. This approach has been shown to allow a high dynamic range and excellent linearity in audio applications [10], but it requires a charge pump, a high frequency clock and possibly an additional subregulator [4] which all increase the silicon area required and increase the quiescent current consumption. Also, if the used process does not have high voltage transistors readily available, the higher voltage supply may violate the maximum allowed voltage limits of the process, which will restrict the general applicability of this technique.

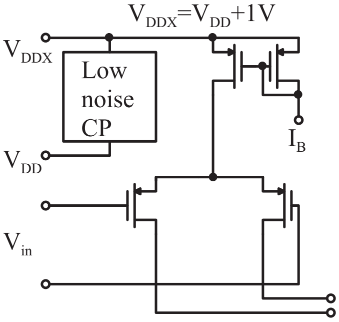

$V_{DDX}=V_{DD}$+1V
V_{DDX}
Low noise CP
V_{DD}
I_B
V_{in}

Fig. 4. A rail-to-rail input stage employing a low noise charge pump.

2.1.3 *Input stage with biased bulk terminal*

Another way of increasing the common-mode input range of an amplifier is to lower the PMOS differential pair threshold voltage by biasing the bulk terminal using either voltage or current [4, 11, 12] as shown in Fig. 5.

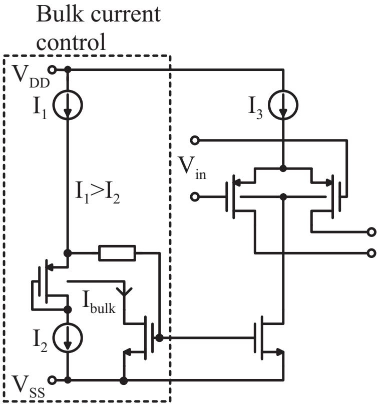

Bulk current control
V_{DD}
I_1
I_3
V_{in}
$I_1>I_2$
I_{bulk}
I_2
V_{SS}

Fig. 5. A rail-to-rail input stage using an input pair with biased bulk terminals.

The bulk biasing technique is based on the fact that, just as the transistor threshold voltage V_{th}, given by (6), can be numerically increased by biasing the bulk terminal above the source potential, it can also be lowered by about 100-200 mV by biasing the bulk terminal below the source potential [12, 13], as seen from

$$V_{th} = V_{th,0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}), \tag{6}$$

where ϕ_F is the Fermi potential, γ is the body-effect coefficient and $V_{th,0}$ is the PMOS zero bias threshold voltage [12, 14].

The bulk biasing technique can help to increase the input common-mode range, but it has the potential drawback of activating the parasitic PNP transistor, a problem requiring either bulk-source Schottky diode protection [15] or additional control circuitry, as shown in Fig. 5. In addition, without careful design, bulk debiasing can have the unwanted effects of lowering the transistor output impedance and adding low frequency pole-zero doublets to the amplifier frequency response [12]. Together with a low threshold voltage input pair, which may be biased in weak inversion to obtain almost zero V_{GS} it, can nevertheless be a useful technique that allows almost full rail-to-rail input swing [11, 16].

It should be noted that this technique has been successfully applied not only to amplifier input stages, but also to LDOs [15] and digital circuits [17], where the main motivation has been to increase the maximum output current/speed of the circuit.

2.1.4 Input stage with resistive level shifter

Last rail-to-rail input technique to be discussed is the resistive level shifter, or common-mode adapter approach [18–20]. The basic principle is to use common-mode feedback to keep the common-mode voltage level in the amplifier *PMOS* input stage sufficiently low by means of a resistive level shift network, as shown in Fig. 6.

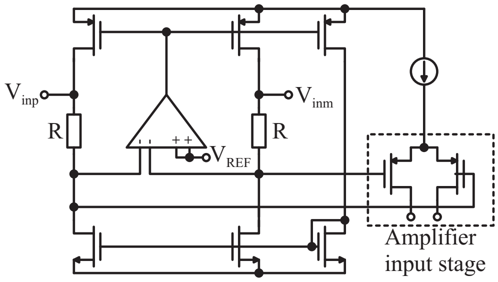


Fig. 6. A resistive level shifter connected in front of the amplifier PMOS input stage.

The main benefits of this technique are its low voltage compatibility and simple design, as the level shifting network can be designed independently of the main amplifier. There are also some serious drawbacks associated with this technique, however. These include added noise, reduced input impedance and possible stability and linearity problems, as discussed in detail in [18] and [I]. Therefore, although applicable to closed loop tracking systems, for example, this technique is not well suited for general operational amplifier cells.

2.2 Class AB output stages

The amplifier output stage is an important part of an operational amplifier, as it is the stage that delivers the input signal to the load. In a well-designed two or three-stage operational amplifier it is also the stage which consumes most of the amplifier biasing current and ultimately sets limits on linearity of the amplifier and its maximum tolerated capacitive load.

When the operating environment of an amplifier requires it to drive low ohmic resistive loads, high current source loads or large capacitive loads, the output stage must be able to source and sink currents that greatly exceed its biasing current. In practise this requires some kind of common drain-based class AB output stage, as shown conceptually in Fig. 7, at least in a low voltage environment, in order not to degrade the available dynamic range any further [21].

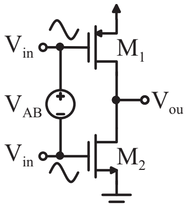


Fig. 7. A conceptual common drain stage-based class AB output stage.

A good class AB output stage should be as linear as possible at low and high frequencies and in addition have most, if not all, of the following properties:

1. It should control the quiescent and minimum currents in the output stage transistor accurately, independent of the supply voltage.
2. It should have a high maximum current to quiescent current ratio.
3. It should not degrade the signal path DC gain.
4. It should not degrade amplifier stability at any current level.
5. It should be low voltage compatible.

6. It should be simple and should not markedly increase the silicon area of the amplifier.

There are basically four approaches that fulfil the above requirements. One is to use super-source followers connected in a cross-coupled quad fashion [22, 23]. Another popular approach is to drive one or both output transistors from a low impedance point and possibly use a feedback circuit to control the quiescent current in the output stage [24–27]. A third common choice is to use a local class AB feedback loop, which typically also includes some sort of hard nonlinearity that allows accurate control of the quiescent and minimum currents in the output stage transistors [9, 28]. The last and probably most popular choice is based on the use of translinear loops, which utilize the fact that the sum of the gate-to-source voltages between two parallel branches is constant when the two branches are connected together [5, 10, 29–33]. In addition, it is possible in three-stage amplifiers to implement a modest class AB output stage without minimum current control by using a main high-gain signal path in parallel with a lower-gain feed-forward signal path [34, 35].

2.2.1 Basic class AB operation

The basic mechanism by which class AB control sets the quiescent current accurately without interacting with the signal path can be understood by comparing the second and third class AB control techniques mentioned above, as depicted in Figs. 8 and 9. In both cases the input signal drives the output stage transistors $M1$ and $M2$ in phase, but whether the class AB control cancels a differential or a common-mode signal depends on the particular implementation.

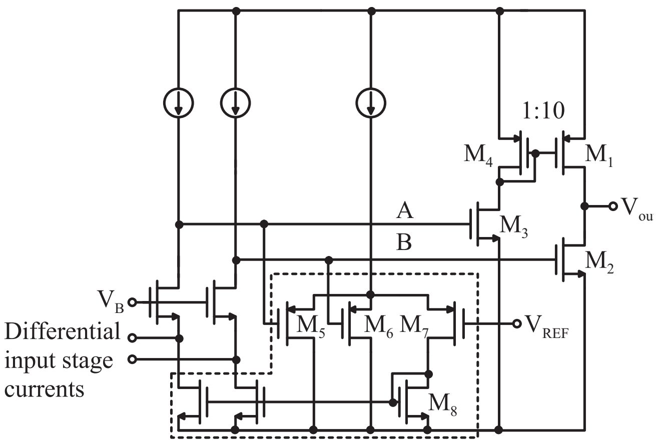

1:10
M4
M1
A
M3
Vou
B
M2
VB
Differential input stage currents
M5
M6
M7
VREF
M8

Fig. 8. Class AB output stage of with differential input.

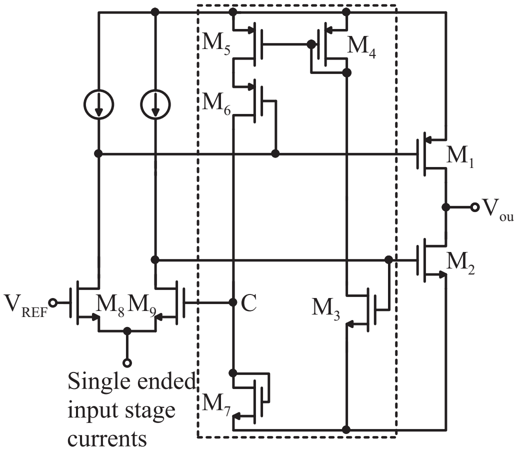

M5
M4
M6
M1
Vou
M2
VREF
M8
M9
C
M3
Single ended input stage currents
M7

Fig. 9. Class AB output stage of with single ended input.

The input to the class AB circuit in Fig. 8 is differential and the PMOS output stage class AB control signal is inverted once, so that the class AB control closely resembles a simple common-mode feedback circuit which cancels the differential input signal and controls the common-mode voltage level of M2. The signal path through the PMOS current mirror (M1 and M3) ensures that the class AB control circuit drives the output stage in a differential fashion. As the node voltages A and B are fixed to the reference voltage V_{REF}, the drain currents I_{D2} and I_{D3} are well controlled and therefore the quiescent current in the output stage is also set accurately, as the global feedback requires I_{D1} to be equal to I_{D2}.

The class AB operation of Fig. 9 is similar to the previous case, only this time the input signal drives the output stage in phase. Therefore the class AB circuit must be able to reject the common-mode input signals generated by the current measuring transistors $M3$ and $M6$ and typically generate a differential control signal for the output stage transistors.

Low common mode gain can be verified in the class AB control loop of Fig. 9 by analyzing the loop on the superposition principle. At a quiescent operation point the gate voltages of $M5$ and $M6$ are equal, so that M5 operates in a linear region and the two transistors therefore operate approximately as a single transistor of length $L5 + L6$ [36]. Assuming that the gate of $M6$ is connected to a small signal ground, we can write the voltage gain formula by inspection as

$$\frac{v_c}{v_{gs2}} \approx \frac{g_{m3}}{2g_{m7}}, \tag{7}$$

where it is assumed that $L4 = L5 = L6$.

The gain from the $M1$ gate to the summing node can similarly be written by inspection, only in this case $M5$ functions as a source degeneration resistor with a value of

$$r_{ds5} = \frac{1}{\mu_o C_{ox} \frac{W_5}{L_5} V_{eff5}} \tag{8}$$

Therefore, with the help of a source-degenerated common source stage effective g_m, the voltage gain can be written as

$$\frac{v_c}{v_{gs1}} \approx \frac{-g_{m6}}{1 + g_{m6} r_{ds5}} \frac{1}{g_{m7}} \approx \frac{-g_{m6}}{2g_{m7}} \tag{9}$$

Thus as long as the NMOS and PMOS transistors are properly rationed, the common-mode input signal is accurately canceled out by the class AB circuit.

2.2.2 Amplifier stability with class AB output stages

Driving resistive or high current loads using class AB output stages requires more careful evaluation of the amplifier stability than when the load is predominantly capacitive. There are two primary reasons for this. One is that the output stage transconductance and voltage gain varies markedly with the load current, and the other is that it is possible in some class AB topologies for the control loop itself to start to limit the amplifier bandwidth when one output stage transistor is driven hard [8].

A necessary requirement for the amplifier signal path to be stable in a global sense is that the amplifier should have enough phase and gain margin at every possible operating point [37]. In practical terms this means that the amplifier must be stable at every possible output current level and not only at quiescent operation points, which is normally ensured by connecting the compensation network symmetrically around the class AB output stage, as shown in Fig. 10. This is the case at least when Miller compensation or its derivatives are used, but it is not absolutely necessary with cascade-compensated amplifiers, as a compensated signal path exists even if one of the output stage transistors is driven hard [38].

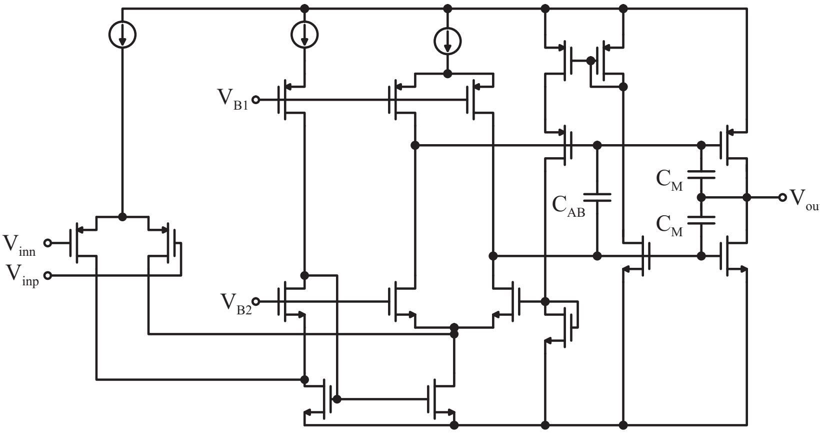


Fig. 10. A simplified class AB amplifier with class AB loop compensation capacitor.

In addition to signal path stability, class AB loop stability must also be considered. When the class AB loop is short and contains only one high impedance node, which is often the case with two-stage amplifiers, it is easy to stabilize the loop by applying dominant pole compensation. Typically, when the amplifier is Miller-compensated there is no need for the dedicated compensation capacitor C_{AB} of Fig. 10, because Miller capacitors themselves will act as ground-connected capacitors for the class AB circuit. With other compensation techniques, however, an additional compensation capacitor may be required.

When the class AB loop requires compensation, the best way to achieve this is to include the capacitor C_{AB}, as shown in Fig. 10, as in most cases this does not significantly affect the signal path bandwidth or the stability margins. The reason for this is that the input signal drives the output transistor gates in phase, so that ideally there is no AC signal across C_{AB} and it is bootstrapped out. Other compensation possibilities include reduction of the class AB loop gain by means of transistor splitting [IV], the addition of feed-forward paths to the loop [39] and the creation of additional replica bias branches [I], which basically exchange bias current accuracy for control loop stability.

2.3 Amplifier frequency compensation

Two- and three-stage amplifier frequency compensation is discussed extensively in numerous text books and scientific articles [39–45]. This chapter summarizes the basic time and frequency domain relationships and reviews some of the frequency compensation techniques that are commonly used in general class AB amplifiers driving variable heavy capacitive and resistive loads.

2.3.1 Basic time and frequency domain relationships

Although approximate amplifier transfer functions show how each design variable modifies the amplifier pole and zero locations, it is still useful to be able to relate AC simulation results such as the gain-bandwidth product (GBW), phase margin (PM) and unity gain frequency (ω_t) quickly to closed-loop parameters such as the damping factor (ζ), undamped natural frequency (ω_n) and closed-loop -3dB bandwidth (ω_{-3dB}), which determine the closed-loop amplifier response in the time domain.

The open-loop unity-gain frequency of an amplifier, also called the gain transition frequency or gain cross-over frequency, is typically estimated using the gain-bandwidth product [41]

$$\omega_t \approx GBW = p_1 A_{DC}, \tag{10}$$

where p_1 is the dominant pole of the amplifier and A_{DC} is the gain at DC.

A very simple relationship exists between an ideal two-pole amplifier gain-bandwidth product, the second pole of the amplifier (p_2) and the phase margin:

$$PM = \arctan(\frac{p_2}{\omega_t}) \approx \arctan(\frac{p_2}{GBW}) \Leftrightarrow \tan(PM) \approx \frac{p_2}{GBW}, \tag{11}$$

where the ratio between p_2 and GBW is sometimes called the separation factor (K), because it tells the designer how far above the gain-bandwidth product the second pole must be located for a certain phase margin [41].

An approximate relationship between the damping factor of a closed-loop system and the undamped natural frequency, which determines the step response of the amplifier in the time domain, can be obtained using the simulated phase margin, unity gain frequency and gain-bandwidth product. Strictly speaking the following applies only to pure second-order systems [46], but in practise the results are close enough to be used with more realistic amplifier and control systems as well, provided they have a dominant, well-damped complex pair of poles.

Using the gain-bandwidth product and phase margin, the undamped natural frequency and closed-loop pole damping factor, as defined in Fig. 11, can be estimated as [41, 46]

$$\omega_n \approx \sqrt{\tan(PM) GBW \omega_t} \approx \sqrt{\tan(PM)}\omega_t \tag{12}$$

$$\zeta = \frac{1}{2}\sqrt{\frac{p_2}{GBW}} \approx \frac{1}{2}\sqrt{\tan(PM)} \approx \frac{PM}{100}, \ (30^\circ < PM < 65^\circ) \tag{13}$$

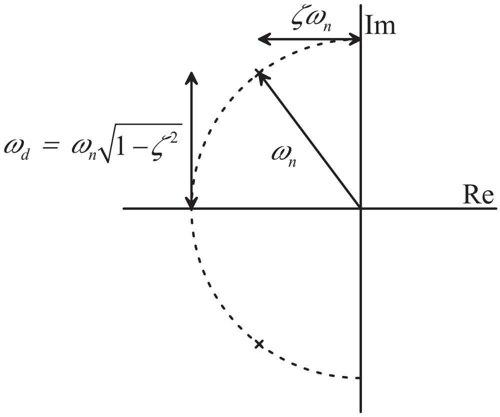


Fig. 11. Undamped natural frequency (ω_n), true oscillation frequency (ω_d) and damping factor (ζ) of a second-order system.

Approximating the resulting closed-loop bandwidth with a line results a very simple relationship between the damping factor, undamped natural frequency and closed-loop -3dB bandwidth [47]:

$$\omega_{-3dB} \approx (1.85 - 1.196\zeta)\omega_n, \ (0.3 < \zeta < 0.8) \tag{14}$$

The result is striking, because it tells us that the resulting -3dB closed-loop bandwidth for a 65 degree phase margin is approximately 1.56 times the open loop gain-bandwidth product when the amplifier is connected in a unity gain configuration.

In the time domain, the step response rise time and overshoot are dependent on the damping factor and undamped natural frequency. The 0% to 90% step response rise time of a linear system is normally estimated simply as [37]

$$t_{rise} \approx \frac{2\pi}{3\omega_{-3dB}} = \frac{1}{3f_{-3dB}}, \tag{15}$$

while the percentage step response overshoot may be given approximately as [41, 46]

$$\%\ \text{overshoot} = \exp^{\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}} \times 100\% \approx 75 - PM, (30^\circ < PM < 75^\circ) \tag{16}$$

The above relationship applies only to small input signals, where the amplifier is not limited by its slew rate (*SR*). It is well known that a limited amplifier slew rate makes the step response sluggish [48], but it is not so well known that it also effectively increases system damping the longer limited the slew rate period lasts. Combining the relationships and damping estimates introduced above with the results given in [49], the step response overshoot of an amplifier with limited slew rate can be formulated as

$$\%\ \text{overshoot, SR-limited} \approx \frac{SR}{GBW} \exp^{\frac{-\pi\zeta}{\sqrt{1-\zeta^2}}} \times 100\%, \tag{17}$$

where *GBW* and *SR* are given in radians and volts/second respectively. The damping effect is clearly seen in Fig. 12, which shows the large-signal step response of a two-stage amplifier with and without slew rate limitation.

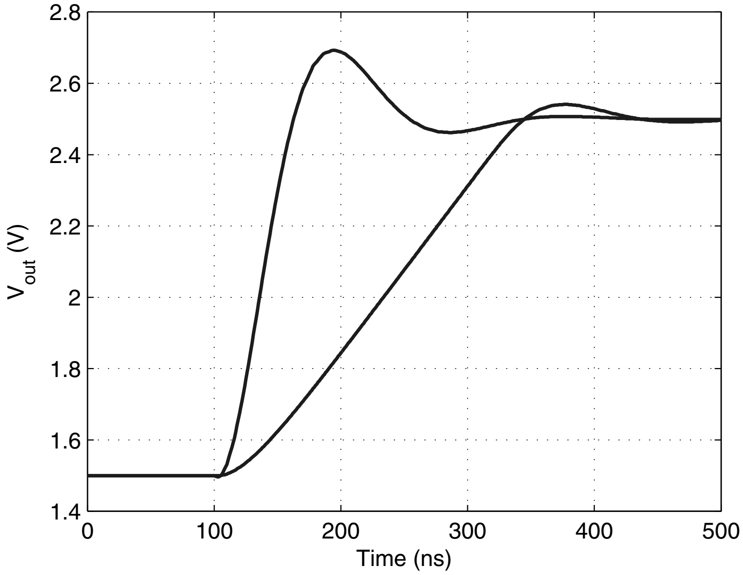


Fig. 12. Two-stage amplifier overshoot with and without slew rate limitation: PM=45°, SR=5V/μs, GBW=38 Mrad/s.

The above results also apply approximately to three-stage amplifiers with a complex pair of high frequency poles if the innermost compensation loop that determines the location of the high frequency poles is well damped. The problem with Bode diagrams, however, is that the damping of the high frequency poles is not easily seen from AC simulations, which can result in excessive step response ringing even though the phase margin seems to be sufficient. There is an approximate technique, however, which can be used to check high frequency pole pair damping in a three-stage amplifier.

According to Nilsson [50], the phase line tangent depends directly on the complex pole pair damping factor, so that the latter can be estimated for a three-stage amplifier by looking at tangent at the 180° phase change point, as shown in Fig. 13 and by calculating the damping factor estimate from

$$\zeta_{HF-pole} \approx 132 \frac{log(f_2/f_1)}{|\theta(f_2) - \theta(f_1)|} \tag{18}$$

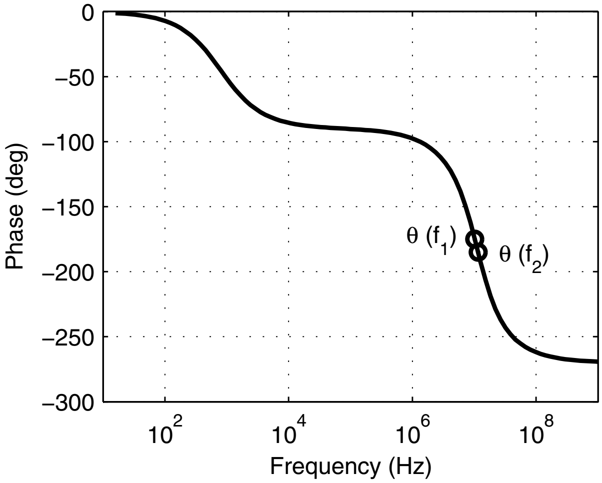


Fig. 13. Estimating the high frequency complex pole pair damping factor from an open loop phase plot.

2.3.2 Miller compensation

Simple Miller compensation (SMC), as shown in Fig. 14, is a well-known amplifier compensation technique which is still used extensively in general operational amplifiers. It also serves as a landmark for comparing two-stage amplifier compensation techniques.

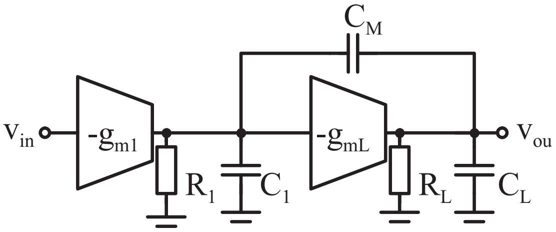


Fig. 14. Small-signal model of a two-stage Miller-compensated amplifier.

Assuming that the load capacitance (C_L) is much larger than the compensating Miller capacitance C_M, and that the last stage gain $g_{mL}R_L >> 1$, the small signal model for SMC results in the well-known approximate two-pole transfer function (19).

$$A(s) = \frac{g_{m1}g_{mL}R_1R_L(1 - s\frac{C_M}{g_{mL}})}{(1 + sC_M g_{mL}R_1R_L)(1 + s\frac{C_L}{g_{mL}})} \tag{19}$$

The resulting transfer function has a right half plane (RHP) zero and a band-limiting second pole, which due to current budget constraints is typically located close to the amplifier GBW.

Using (10) and (19) we obtain the well-known approximation for a SMC amplifier GBW

$$GBW = \frac{g_{m1}}{C_M} \tag{20}$$

As seen in (19) and (20), the location of the RHP zero in an SMC amplifier relative to the gain-bandwidth product depends on the ratio g_{mL}/g_{m1}. In addition, the second pole can be thought to be formed by the high frequency output impedance $1/g_{mL}$ of the amplifier and the load capacitance C_L. Therefore, for fixed phase margin, bandwidth and load capacitance, the only way to improve amplifier stability is to increase the output stage transconductance g_{mL}.

When an SMC amplifier is resistively loaded the output stage gain drops and the output stage time constant must be replaced with $(1/g_{mL}||R_L)C_L$, which results in a modified transfer function

$$A(s) = \frac{g_{m1}g_{mL}R_1R_L(1 - s\frac{C_M}{g_{mL}})}{(1 + sC_M(g_{mL}R_1R_L + 1))(1 + sC_L(1/g_{mL}||R_L))} \tag{21}$$

As the Miller effect depends on the output stage gain, the amplifier gain-bandwidth with small ohmic resistive loads is no longer accurately set by the input stage transconductance and Miller capacitance, as can be seen from

$$GBW \approx \frac{g_{m1}g_{mL}R_L}{C_M(g_{mL}R_L + 1)} = \frac{g_{m1}g_{mL}(1/g_{mL}||R_L)}{C_M}, \tag{22}$$

which is smaller than in the nominal case and directly proportional to g_{mL} and R_L when $g_{mL}R_L < 1$. As the second pole is also located at higher frequencies due to the parallel connection of R_L and $1/g_{mL}$, SMC amplifier stability is always improved when the load resistance is reduced or the output stage transconductance is increased.

In conclusion, SMC behaves well with varying resistive loads, and, due to the Miller effect, it is not sensitive to a large output stage gate-to-source capacitance (C_1 in Fig.

14). Also, it does not have low frequency pole-zero doublets, which would affect its settling behavior. It does have a relatively low frequency second pole and an RHP zero, however, both of which depend on the output stage transconductance and limit the amplifier bandwidth, especially when the load capacitance is large and the current budget is limited.

2.3.3 Miller compensation with a nulling resistor

Miller compensation with a nulling resistor (SMCNR) is in practise probably the most widespread and most frequently used compensation technique. A small-signal SMCNR model is presented in Fig. 15, from which it can be seen that the only difference relative to the basic SMC approach is the inclusion of the nulling resistor R_Z, the physical function of which is to reduce the non-inverted forward current through C_M at high frequencies, as this is responsible for the formation of the RHP zero. Analysis of the small-signal model in Fig. 15 while assuming a low ohmic resistive load results in

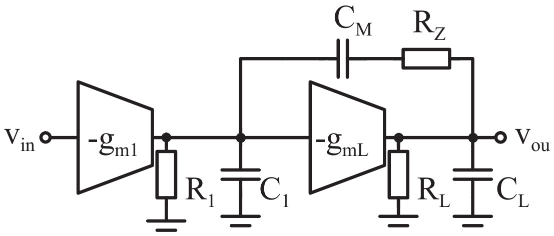


Fig. 15. Small-signal model of a Miller-compensated amplifier with a nulling resistor.

$$A(s) = \frac{g_{m1} g_{mL} R_1 R_L (1 + sC_M(R_Z - 1/g_{mL}))}{(1 + sC_M(R_1 g_{mL} R_L + 1))(1 + sC_L(1/g_{mL}||R_L))(1 + sC_1 R_Z)} \tag{23}$$

Comparing (23) with (21), we see that the inclusion of R_Z adds a third pole and relocates the zero, but it does not affect the location of the band-limiting pole. However, due to the fact that the zero can be located in the left half plane (LHP) by choosing $R_Z > 1/g_{mL}$, the stability is better than in the SMC case.

Thanks to this improved stability, SMCNR is well suited for driving variable and heavy resistive and capacitive loads. It is also simple and intuitive and does not increase current consumption in the amplifier. One practical limitation with resistive loads, however, is that accurate pole-zero cancelation is not feasible, because the output stage transconductance and the location of the second pole vary with the load current. Also, an LHP zero located before the second pole can result in a poor phase margin, which must be accounted for in the design phase. Yet another thing to consider is the required ratio C_M/C_1. Looking at the zero location and the highest frequency pole of (23) it can be seen that in order to apply the SMCNR technique effectively, C_M has to be made roughly 5-10 times larger than the parasitic output stage gate-to-source capacitance. Otherwise the LHP zero and the third pole will be located close to each other and SMCNR will have no advantage over SMC.

2.3.4 Miller compensation with a feed-forward stage

An alternative way to generate a LHP zero is to use a feed-forward stage in parallel with the main Miller-compensated amplifier, as presented in Fig. 16 [43, 51]. Although Miller compensation with a feed-forward stage (SMC+FF) is far less common than the SMCNR approach, one of its extensions to be discussed shortly demonstrates an important principle which has been applied in a different manner in this thesis.

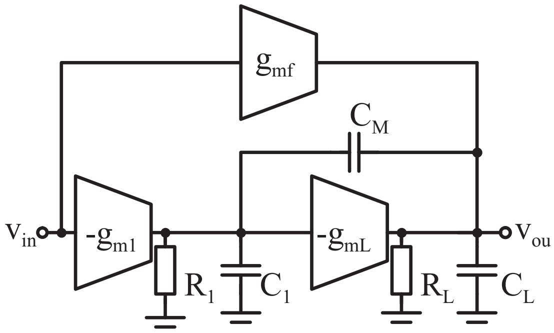


Fig. 16. Small-signal model of a Miller-compensated amplifier with a feed-forward stage.

When the amplifier is driving predominantly capacitive loads, the SMC+FF transfer function becomes [43]

$$A(s) = \frac{g_{m1}g_{mL}R_1R_L(1+s\frac{C_M(g_{mf}-g_{m1})}{g_{m1}g_{mL}})}{(1+sC_Mg_{mL}R_1R_L)(1+s\frac{C_L}{g_{mL}})} \tag{24}$$

Comparison of (24) with (19) shows that the SMC+FF amplifier has exactly the same poles as a normal SMC amplifier but in addition it also has an LHP zero as long as $g_{mF} > g_{m1}$.

Although the principle of the SMC+FF technique is simple, there are two major drawbacks associated with this compensation approach. First, the inclusion of a feed-forward transconductance stage complicates the design of the rail-to-rail input stage, and second, when the capacitive load in the amplifier is large, a large g_{mf} is needed to achieve a low frequency LHP zero which is costly in terms of current consumption.

The problem of the large g_{mf} required can be avoided if we replace the single transconductance element with a current mirror operational amplifier, which does not add low frequency poles to the transfer function [51]. To see the effect of the added amplifier, let us describe the $OpAmp||SMC$ connection above the dominant pole frequency, when C_M appears as a short-circuit, using the small-signal model of Fig. 17, where g_{mf} now represents the feed-forward amplifier output stage and A_F represents the total current gain in the input stage current mirror.

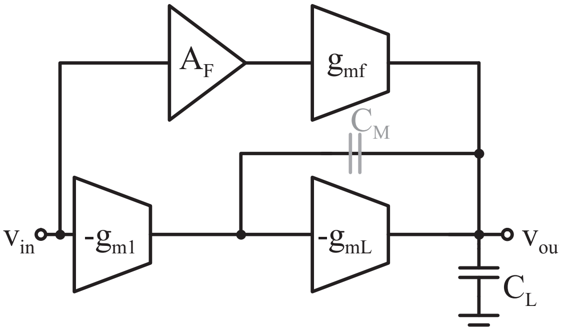


Fig. 17. Small-signal model of a Miller-compensated amplifier in parallel with a current mirror operational amplifier above the dominant pole frequency.

After a few lines of algebra the SMC+FF-amplifier transfer function above the dominant pole frequency becomes

$$A(s) \approx \frac{\frac{g_{m1}}{C_M}\left(1 - \frac{sC_M}{g_{mL}}\right)}{s\left(1 + \frac{s}{p2}\right)} + \frac{\frac{A_F g_{mf}}{g_{mL}}}{1 + \frac{s}{p2}} = \frac{\frac{g_{m1}}{C_M}\left(1 - \frac{sC_M}{g_{mL}}\right) + \frac{sA_F g_{mf}}{g_{mL}}}{s\left(1 + \frac{s}{p2}\right)}, \tag{25}$$

from where the LHP zero can readily be solved

$$z_1 = \frac{g_{m1} g_{mL}}{C_M (A_F g_{mf} - g_{m1})}, \tag{26}$$

which indicates that the added gain A_F relaxes the feed-forward stage transconductance requirement by virtue of the added gain.

The result is obvious if we look at the bode plots of the SMC amplifier and current mirror operational amplifier shown in Fig. 18, above the dominant pole frequency, when the Miller capacitor acts as a short-circuit. The current mirror operational amplifier frequency response simply takes over the total response as the SMC branch gain drops below the paralleling amplifier gain.

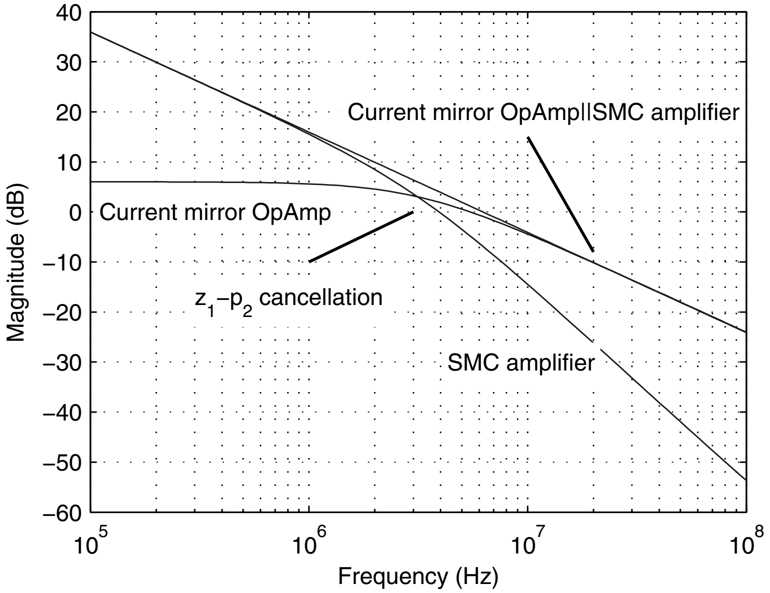


Fig. 18. Illustration of the frequency response of a current mirror operational amplifier in parallel with an SMC amplifier above the dominant pole.

The effective multiplication of g_m seen above is an important result which will be made use of extensively in the next section and has been used in the publications included in this thesis. This can be summarized as

If we can add voltage gain in front of a transconductance block without adding low frequency poles to the transfer function, we can effectively multiply the transconductance of the stage by the added voltage gain.

Finally it should be noted that the SMCNR and SMC+FF techniques can also be combined to achieve an even lower frequency left half plane zero. This approach is sometimes used in three-stage amplifiers [52, 53], but it is not really useful in two-stage amplifiers because the same effect can be obtained simply by increasing R_Z and topologically g_{mf} is not readily available as it is in three-stage class A amplifiers.

2.3.5 Miller compensation with a current buffer

As discussed in section 2.3.2, the bandwidth of an SMC amplifier is ultimately limited by the load-dependent second pole. Adding a LHP zero, e.g. by using a feed-forward stage, helps, but only marginally. With predominantly capacitive loads a popular alternative to the above-mentioned compensation techniques is to use the transconductance multiplication principle in a local feedback loop around the output stage as a means of modifying the location of the band-limiting pole. When the additional high frequency gain is implemented using a current buffer, this technique is normally called cascode compensation, or Miller compensation with a current buffer [54, 55]. In the small-signal model capacitor C_M is either added intentionally or represents a parasitic gate-to-drain capacitance of the output stage transistor, while $1/g_{mF}$ represents the input impedance of the cascode transistor/current mirror, which are typically used as current buffers.

Assuming that $C_F > C_1 + C_M$, we can derive a transfer function (27) for the current buffer compensated amplifier of Fig. 19, which is reasonably accurate except for the smallest resistive loads.

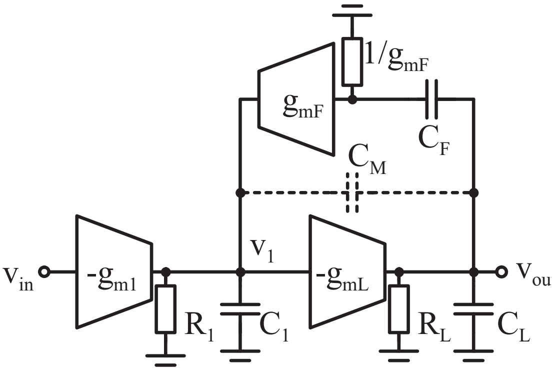


Fig. 19. Small-signal model of a Miller-compensated amplifier with a current buffer, showing explicitly the current buffer input impedance $1/g_{mF}$.

$$A(s) = \frac{g_{m1} g_{mL} R_1 R_L (1 + s\frac{C_F}{g_{mF}})(1 - s\frac{C_M}{g_{mL}})}{(1 + s C_F g_{mL} R_1 R_L)(1 + s\frac{C_L(C_1+C_M)}{g_{mL} C_F} + s^2 \frac{C_L C_1}{g_{mL} g_{mF}})} \tag{27}$$

The numerator of this transfer function has two, normally widely separated, zeros, of which the LHP zero is typically dominant and relatively fixed. The other, a higher frequency RHP zero, is that of a normal SMC amplifier. The poles of (27) can be either real or complex. If they are real we can rewrite (27) as

$$A(s) = \frac{g_{m1} g_{mL} R_1 R_L (1 + s\frac{C_F}{g_{mF}})(1 - s\frac{C_M}{g_{mL}})}{(1 + s C_F g_{mL} R_1 R_L)(1 + s\frac{C_L(C_1+C_M)}{g_{mL} C_F})(1 + s\frac{C_1 C_F}{g_{mF}(C_1+C_M)})} \tag{28}$$

Comparison of the second pole of (28) with the corresponding SMC pole shows that it is located at a higher frequency if $C_F > C_1 + C_M$, as is usually the case. The gain term $C_F/(C_1 + C_M)$ represents the high frequency voltage gain of an ideal compensation network with a current buffer at mid-band frequencies, as can readily be seen in Fig. 20. It is this added gain in the local feedback loop which reduces the high frequency output impedance of the amplifier and thus pushes the bandlimiting second pole to higher frequencies.

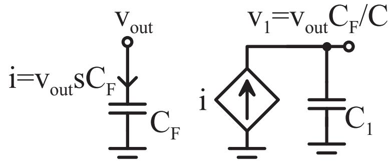


Fig. 20. Small signal model ($1/g_{mF} = 0$) for a simplified current buffer loop above the dominant pole frequencies, for visualizing the high frequency voltage gain in the compensation network.

Based on the above discussion the current buffer approach may prove intriguing. There are several problems with resistive loads, however. The first is related to the implementation of class AB control. In practice, when there are no large Miller capacitors it is difficult to implement stable feedback-type class AB control without affecting the signal path, as discussed in [IV]. Another more serious problem is damping of the high frequency poles and possible digital noise rectification in the cascode transistor.

In practice, when the output stage transconductance increases with the load current, a poorly damped complex pole pair will result, manifested as peaking in the amplifier frequency response. Using (27), an approximate formula can be derived for the high frequency pole pair damping factor:

$$\zeta_{HF-pole} = \frac{C_1 + C_M}{2C_F}\sqrt{\frac{C_L g_{mF}}{C_1 g_{mL}}} \tag{29}$$

Equation (29) shows that there are basically three ways to damp a possibly complex pole pair. One is to reduce the current buffer input resistance by increasing g_{mF}. This is not easy in practice if a cascode is used as a current buffer. The second choice is to add a small C_M across the output stage, as in [56]. This is often done in practise as it guarantees better damping of the complex poles, although the benefits of the current buffer approach over SMC are reduced at the same time. The last choice is to increase the load capacitance. This may not be possible in a general amplifier application but is a very useful property when compensating for instance low dropout regulators [57].

2.3.6 Nested Miller compensation

Like SMC, nested Miller compensation (NMC), as shown in Fig. 21, serves as a landmark for three-stage amplifiers. Despite the large bandwidth reduction associated with it, NMC and its variations are still used extensively in general operational amplifiers due to their insensitivity to parasitic capacitances, robustness to output stage small-signal parameter variations, good linearity in audio applications and the possibility for implementing stable feedback-type class AB control [4, 39, 41, 53, 58].

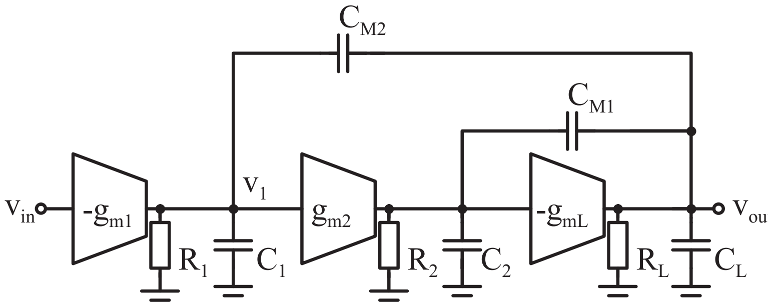


Fig. 21. Small-signal model of a nested Miller-compensated amplifier.

A transfer function for a resistively loaded NMC amplifier can be derived from Fig. 21 in the form

$$A(s) = \frac{g_{m1}g_{m2}g_{mL}R_1R_2R_L(1 - s\frac{C_{M1}}{g_{mL}} - s^2\frac{C_{M1}C_{M2}}{g_{m2}g_{mL}})}{(1 + sC_{M2}g_{m2}g_{mL}R_1R_2R_L)(1 + s\frac{C_{M1}}{g_{m2}g_{mL}(1/g_{mL}||R_L)} + s^2\frac{C_{M1}C_L}{g_{m2}g_{mL}})} \qquad (30)$$

This function has two zeros, of which the RHP zero is at lower frequencies, as can easily be seen with the help of a quadratic formula. In this sense NMC and SMC amplifiers are very similar. It comes as no surprise, therefore, that similar techniques are also used to reduce the effects of the RHP zero [41, 43, 53].

The denominator of (30), on the other hand, shows clear differences from the corresponding SMC transfer function denominator. First, due to added gain in the local feedback loop, the NMC amplifier GBW is well defined by the ratio g_{m1}/C_{M2} even with heavy resistive loads. NMC transfer function also has two high frequency poles, which can either be real or complex conjugates.

The high frequency poles deserve a closer look, as it is eventually these poles that limit the bandwidth of an NMC amplifier. Physically, the high frequency poles can be assumed to arise when the innermost resistively loaded two-stage Miller-compensated amplifier, formed by g_{m2} and g_{mL}, is connected in a unity gain configuration by the outermost compensation capacitor C_{M2}, as shown in Fig. 22.

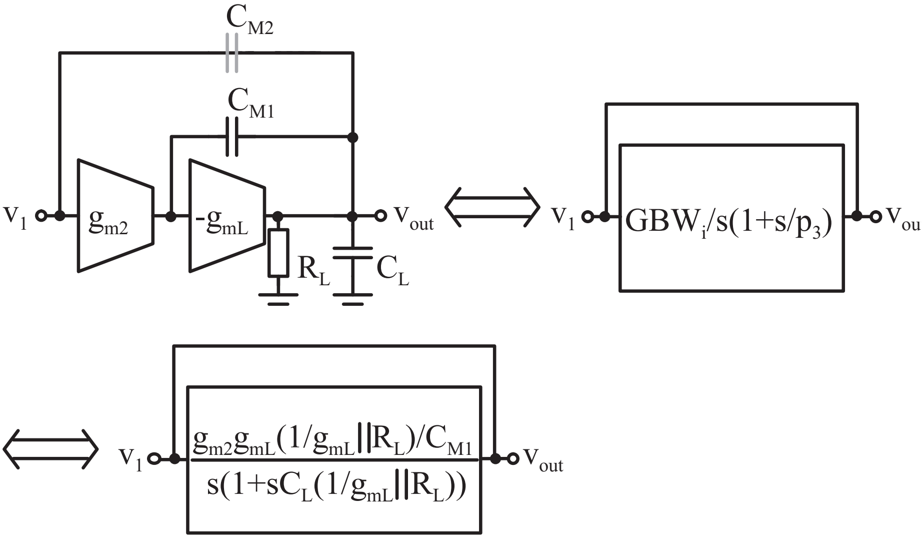


Fig. 22. Small-signal model for determining the high frequency poles of a resistively loaded NMC amplifier.

As stated in [41], the innermost compensation loop must have a sufficient phase margin for the complete amplifier to be stable and behave well. The amplifier bandwidth and load range are typically known in the design phase from the transient specifications, for instance. Therefore the GBW of the amplifier is known, and the only question is how to size the inner amplifier gain-bandwidth product (GBW_i) under the worst-case loading conditions in order to ensure good overall phase margin and transient behavior.

A good starting point for the design work is to have the innermost loop phase margin better than 63°, which corresponds to an inner amplifier p_3/GBW_i ratio of two (Note that the second pole of the inner amplifier is actually the third pole of the complete amplifier). Now, assuming no zeros and a pair of complex conjugate poles, the equation for the phase margin becomes [41]

$$tan(PM) = \frac{1 - \frac{GBW^2}{2GBW_i^2}}{\frac{GBW}{GBW_i}}, \tag{31}$$

and thus the requirement for the GBW_i/GBW ratio for a predetermined overall phase margin can be formulated as

$$\frac{GBW_i}{GBW} = \frac{\tan(PM)}{2}[1 + \sqrt{1 + \frac{2}{\tan^2(PM)}}], \tag{32}$$

which for an overall phase margin better than 60° is approximately

$$\frac{GBW_i}{GBW} = \tan(PM) \tag{33}$$

Interpretation of (33) leads to a very important conclusion that will also form the closing statement of this section. As long as the stability of the innermost compensation loop is taken care of, GBW_i can be thought to represent an equivalent second pole of the amplifier [41]. In other words, when the innermost amplifier compensation loop is well stabilized, the overall three-stage amplifier can be approximately represented as

$$A(s) = \frac{GBW}{s(1 + \frac{s}{GBW_i})}, \tag{34}$$

which reduces the complex three-stage amplifier compensation task to a much simpler one.

2.4 Amplifier power supply noise rejection ratio

Bandwidth efficiency is probably the most important figure of merit for stand-alone amplifiers, but in many applications where the amplifier is only a part of a larger system, e.g. a bandgap reference or an oscillator buffer on a mixed-signal chip, an equally important criterion is the amplifier's ability to reject power supply noise. This is especially the case when the analogue supply is corrupted by high current class AB stages, when the amplifier is connected directly to a battery voltage that can droop several hundred millivolts in couple of microseconds, or when it must share the same supply or ground pin with noisy switching circuits.

Problems can exist even when the disturbances caused by the switching circuits are small. One example of such a situation is shown in Fig. 23, where precision analogue blocks share the same internal low drop regulator output as the switch driver of a boost DC/DC converter due to system-level design constraints. As the driver draws large current spikes from the LDO output, the output voltage droops slightly. The LDO interprets this as a small error voltage at its input and tries to correct it, which results in a constant supply ripple of a few millivolts at a relatively low frequency, as seen in Fig. 24. In this sense it is vital that the analogue blocks should be able to attenuate any supply disturbances over wide range of frequencies and not only with DC.

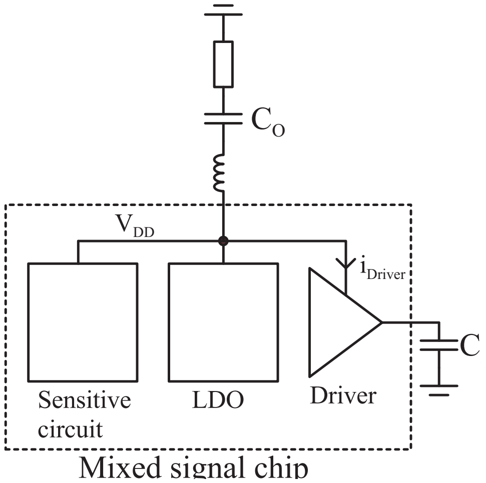


Fig. 23. Conceptual system block diagram, where poor high frequency PSRR of analog blocks can cause problems.

The purpose of this section is to point out quickly the differences between class A and class AB amplifiers from the point of view of supply noise rejection performance with DC and above the dominant pole and to introduce a few simple circuit techniques that can be used to improve the PSRR$_{dd}$ of amplifiers in single supply applications.

The following discussion ignores substrate noise issues, not because there are no substrate noise problems in practice, but because such matters are often tackled through system and layout design or by simply increasing the bandwidth of the amplifier, for example, so that it settles well before the next substrate disturbance occurs.

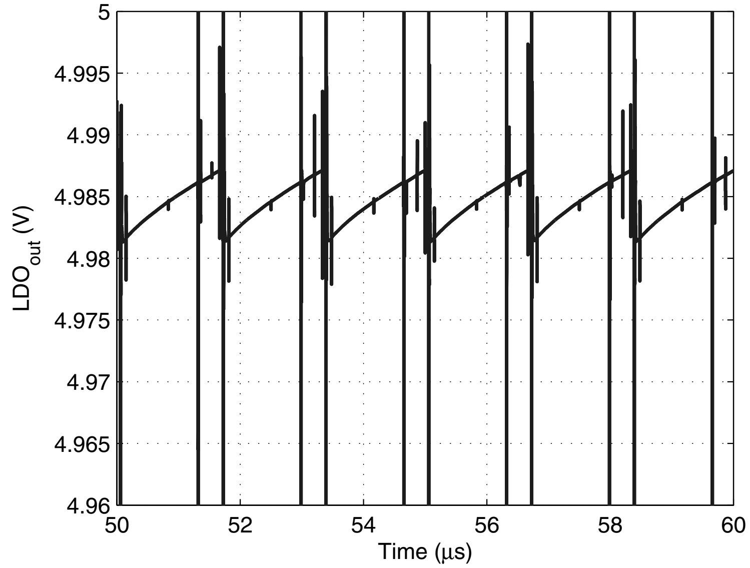


Fig. 24. Simulated commercial LDO output voltage with a switching load, showing a constant supply ripple of a few millivolts at a relatively low 625kHz switching frequency.

2.4.1 PSRR basics

The ability of an amplifier to overcome small power supply disturbances is described by its power supply rejection ratio (PSRR), or more often 1/PSRR. PSRR is defined as

$$PSRR_{dd,ss}(s) = A_v(s)/A_{dd,ss}(s), \tag{35}$$

where $A_{dd,ss}$ is the frequency-dependent gain from a positive/negative supply to the amplifier output and A_v is the differential small-signal gain [42].

PSRR$_{dd}$ and PSRR$_{ss}$ are not independent. In fact it can be shown that they are linked to each other and to the common-mode rejection ratio, as shown in

$$A_{cm}(s) + A_{dd}(s) + A_{ss}(s) \approx 1, \tag{36}$$

where $A_{cm}(s)$ is the common-mode gain from the amplifier input to the output [59]. The importance of this equation for the designer is that it shows that without a clean reference potential, PSRR$_{ss}$ and PSRR$_{dd}$ cannot be optimized at the same time.

Maximizing PSRR$_{dd}$ is normally not a problem for single supply class A amplifiers, because the lower supply rail is connected to the common, hopefully clean, reference potential by default and the circuit configuration can be often chosen so that PSRR$_{dd}$ is close to an optimum value. PSRR$_{dd}$ can be a problem, however, for symmetrical class AB amplifiers, especially above the dominant pole frequency, as will be discussed later.

2.4.2 PSRR of class A amplifiers

Analysis of PSRR with a pencil and paper is normally tedious, because of the multi-input nature of the PSRR problem. In order to simplify things and to show the essential differences in PSRR behavior between class A and class AB amplifiers, it is assumed in the following that the current sources shown are ideal and there is no mismatch in the differential pair or in the current mirrors. These assumptions lead to a situation where:

1. The input differential pair or current summing branches do not contribute to PSRR
2. Voltage gain from the supply to the internal node A of Fig. 25 is zero from V_{ss} and unity from V_{dd}
3. $A_{dd,ss}$ can be accurately determined from one or two injection points with the help of a voltage divider rule [59, 60].

To further simplify things, we will analyze only the gains $A_{dd,ss}$, because the differential gain that appears in (35) is well known.

Using the simplifying assumptions presented here, we can analyze the simple class A amplifier in Fig. 25. At DC the gain A_{ss} is formed by a simple voltage divider between the output resistances of $M5$, $M6$ and the load resistance R_L, as shown in

$$A_{ss}(DC) \approx \frac{R_{ds6}||R_L}{R_{ds5} + R_{ds6}||R_L} \tag{37}$$

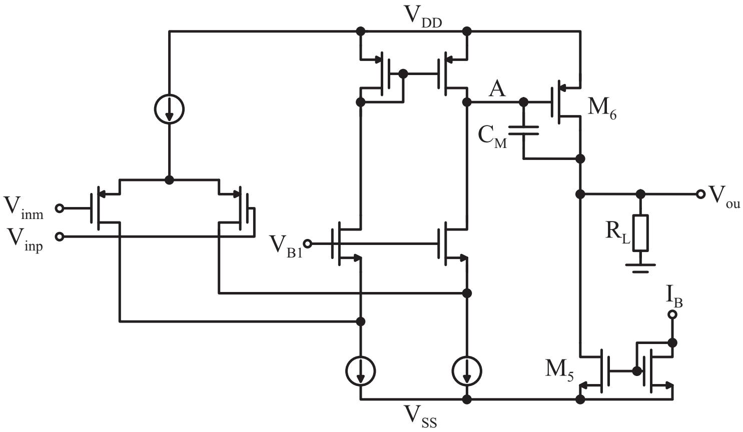


Fig. 25. Simple class A amplifier for determining $A_{dd,ss}$.

Above p_1 the compensating capacitor in Fig. 25 can be considered to be a short circuit. Therefore at mid-band frequencies A_{ss} becomes

$$A_{ss}(\omega > p_1) \approx \frac{1/g_{m6}||R_L}{R_{ds5} + 1/g_{m6}||R_L} \approx \frac{1}{R_{ds5}g_{m6}} \tag{38}$$

Thus from DC to *GBW*, the PSRR$_{ss}$ of a class A amplifier will be equal to or somewhat better than the available loop gain at that frequency.

Let us next consider the gain A_{dd} for the same class A amplifier. At DC the positive supply noise appears at the gate and the source of $M6$, so that the current through $M6$ is not modulated by the supply noise, and again A_{dd} is obtained using a simple voltage divider rule as

$$A_{dd}(DC) \approx \frac{R_{ds5}||R_L}{R_{ds6} + R_{ds5}||R_L}, \tag{39}$$

which is similar to (37).

After a frequency of p_1 the compensating capacitor again acts as a short circuit, and therefore A_{dd} at these frequencies becomes

$$A_{dd}(\omega > p_1) \approx \frac{R_{ds5}||R_L}{R_{ds5}||R_L + 1/g_{m6}} \approx 1 \tag{40}$$

Thus at mid-band frequencies the output stage acts like a unity gain amplifier and conducts all the supply noise from the supply to the output. Therefore PSRR$_{dd}$ at these frequencies can only be as good as the available loop gain [42].

2.4.3 PSRR of class AB amplifiers

Using the simplifying assumptions of subsection 2.4.1, simple estimates of $\mathrm{PSRR}_{dd,ss}$ for class AB amplifiers can be derived using Fig. 26. Monticelli-type class AB control [30] is used here as an example, but the general conclusions apply to most symmetrical class AB stages.

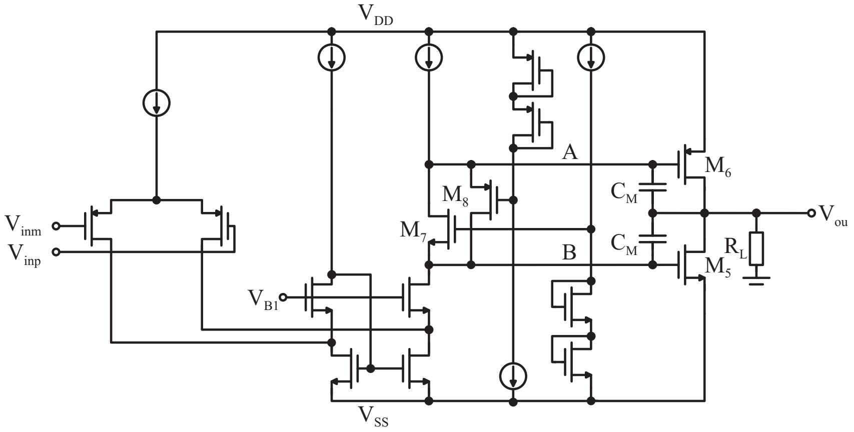


Fig. 26. Simple class AB amplifier for determining positive and negative power supply gain.

The DC model that allows us to derive expressions for $A_{dd,ss}$ is shown Fig. 27. The major difference relative to the class A amplifier case is that class AB amplifiers have two injection points that are important when calculating $\mathrm{PSRR}_{dd,ss}$, one through the output stage transistor output resistance and one through the class AB circuit itself.

The role of a class AB circuit in conducting the supply noise to the internal nodes is intuitively understood if we look at how a class AB circuit references the gates of the output transistors. From Fig. 26 it is easy to see that the M6 gate of the PMOS output stage transistor is referenced to the positive supply, whereas M5 is referenced to V_{ss}, which is also reflected in the DC model of Fig. 27.

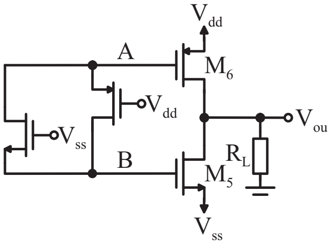


Fig. 27. A simple low frequency class AB amplifier model for calculating positive and negative power supply gain.

Using the model of Fig. 27, assuming equal output stage transconductances and marking the source follower gain as x, A_{ss} for a class AB amplifier becomes

$$A_{ss}(DC) \approx (1-x)g_{m5}R_{ds5}||R_{ds6}||R_L + \frac{R_{ds6}||R_L}{R_{ds5}+R_{ds6}||R_L} \tag{41}$$

As the class AB circuit in this example is symmetrical, (41) can be used to write an estimate for A_{dd}, which results in

$$A_{dd}(DC) \approx (1-x)g_{m5}R_{ds5}||R_{ds6}||R_L + \frac{R_{ds5}||R_L}{R_{ds6}+R_{ds5}||R_L} \tag{42}$$

If we compare (41) and (42) with the corresponding class A amplifier equations, we see that the greatest difference is the contribution of the class AB circuit to PSRR.

Above the dominant pole frequency the Miller capacitors act as short-circuits, which allows a modification to be made to the power supply gain model of Fig. 27. The result is shown in Fig. 28, where the capacitors of Fig. 26 have been replaced with a wire.

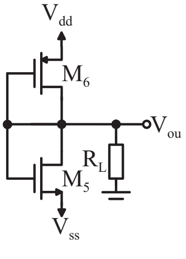


Fig. 28. Midband class AB amplifier small signal model for determining $A_{dd,ss}$.

Using the simplified mid-band PSRR model and assuming equal Miller capacitors, A_{ss} and A_{dd} at mid-band frequencies can be derived as

$$A_{ss}(\omega > p_1) \approx \frac{1/g_{m6}||R_{ds6}||R_L}{1/g_{m5} + 1/g_{m6}||R_{ds6}||R_L} + \frac{1/g_{m6}||R_{ds6}||R_L}{R_{ds5} + 1/g_{m6}||R_{ds6}||R_L} \approx 1/2 \tag{43}$$

and

$$A_{dd}(\omega > p_1) \approx \frac{1/g_{m5}||R_{ds5}||R_L}{1/g_{m6} + 1/g_{m5}||R_{ds5}||R_L} + \frac{1/g_{m5}||R_{ds5}||R_L}{R_{ds6} + 1/g_{m5}||R_{ds5}||R_L} \approx 1/2 \tag{44}$$

As the first term is dominant in both (44) and (43), it may be concluded that the greatest problem with symmetrical class AB amplifiers is that their symmetry unnecessarily degrades the mid-band PSRR performance in single supply applications. This behavior can be avoided by connecting a PSRR boosting capacitor from the positive supply to point B in Fig. 26, for example, which is similar to what was done in [61], or else by using cascode compensation [38] or the techniques discussed in [VI] or [VIII].

Finally it should be mentioned that the above models involve very crude approximations, which can lead to somewhat optimistic low frequency PSRR estimates even if mismatch is not taken into account, as seen in Table 1, which compares hand-calculated values with AC simulations. This is due to the fact that the input differential pair, current summing stage and bias branches also contribute in practise to the overall PSRR, which can be a problem, e.g. when using class A amplifiers with current buffer compensation [59], but can also be an advantage, as in [VI].

Table 1. Comparison of simulated Class A and AB amplifier power supply gains with hand calculations.

Power supply gain	Hand calculations	Simulations
Class A A_{dd} (DC/midband)	0.436/0.974	0.435/0.953
Class A A_{ss} (DC/midband)	0.437/0.021	0.437/0.028
Class AB A_{dd} (DC/midband)	1.416/0.560	1.279/0.540
Class AB A_{ss} (DC/midband)	0.400/0.440	0.457/0.455

3 Contributions

The following sections provide a brief summary of the original publications included in this thesis together with some unpublished measurement results and circuit schematics that were not available at the time of the publications. The papers are intended to reflect the main focus of the thesis, which is to improve low voltage compatible two- and three-stage class A and AB amplifiers bandwidth efficiency and high frequency PSRR.

3.1 Paper I

Paper [I] describes a low voltage compatible, adaptively biased amplifier with rail-to-rail input and output stages for driving varying heavy capacitive and resistive loads.

The rail-to-rail input stage of the amplifier is based on the simplified resistive level shift network of Section 2.1.4, as shown in Fig. 29. The adaptive biasing principle is based on the use of a first-order high pass filter and supply-independent adaptive biasing current block, which boosts the amplifier bandwidth for large, high frequency input signals. Adaptive biasing block is designed to be fast, so it can be considered as memoryless nonlinearity, which allows amplifier large signal bandwidth to be estimated with the help of describing functions.

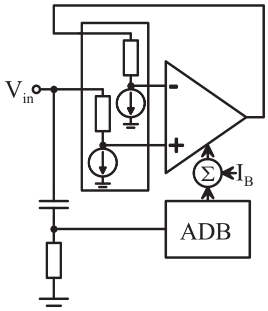


Fig. 29. Amplifier topology of paper [I].

The compensation approach used here, which is based on two-stage Miller compensation and a high bandwidth stage in front of the output stage (SMC+HBW), is depicted in Fig. 30. Being enclosed by the Miller capacitor, the high bandwidth stage effectively multiplies the output stage transconductance by the high bandwidth stage voltage gain, as discussed in Section 2.3.4, and this boosts the stability of the amplifier with heavy capacitive loads, because the second pole of the amplifier moves to

$$p_2 = \frac{A_2 g_{mL}}{C_L}, \tag{45}$$

where A_2 is the high bandwidth stage gain.

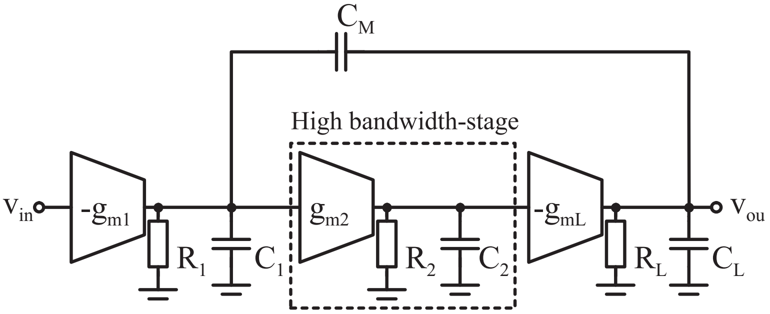


Fig. 30. Small-signal model of the simple Miller-compensated amplifier with a high bandwidth low gain stage (SMC+HBW) used in paper [I].

Although the output stage transconductance boosting was applied to a two-stage amplifier in the paper, it can also easily be applied to three-stage amplifiers. A three-stage nested Miller-compensated class AB amplifier with a high bandwidth stage (NMC+HBW) designed in $0.5\mu m$ CMOS technology is shown in Fig. 31.

The first stage of the amplifier is a simple folded cascode stage with two diode-connected transistors, M16 and M17, which clamp the cascode transistor source voltages during long SR-limited operation. The second stage is formed by the transistors M1-M4, while M5-M9 create a high bandwidth stage in which M9 is responsible for controlling the voltage gain. M12-M15 put up a single-ended feedback-type class AB control loop, which controls the output stage quiescent and minimum currents.

The measured NMC+HBW amplifier frequencies and step responses are shown in Figs. 32 and 33, respectively. Because the output stage is not symmetrical, the step response shows more peaking when the NMOS output stage is required to sink large currents, which is a typical form of behavior also for many commonly used commercial amplifiers. The measured performance of the SMC+HBW and NMC+HBW amplifiers is summarized in Table 2.

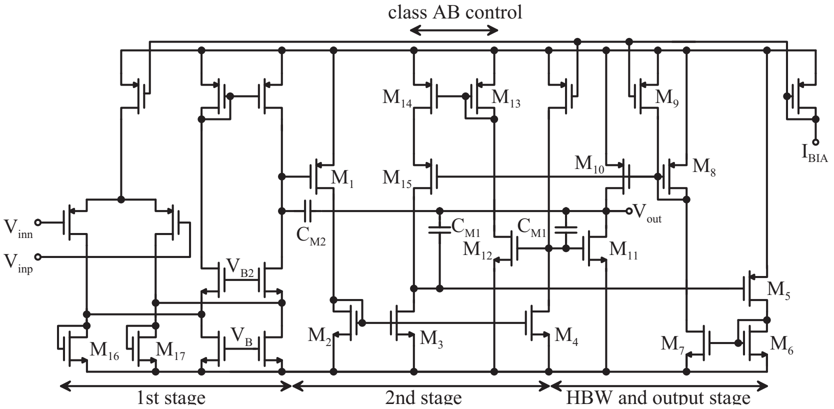

class AB control
M_{14}
M_{13}
M_9
I_{BIA}
M_1
M_{15}
M_{10}
M_8
V_{out}
C_{M2}
C_{M1}
C_{M1}
M_{12}
M_{11}
V_{inn}
V_{inp}
V_{B2}
M_5
M_2
M_3
M_4
M_7
M_6
M_{16}
M_{17}
V_B
1st stage
2nd stage
HBW and output stage

Fig. 31. Schematic diagram of the three-stage NMC+HBW amplifier used for measurements.

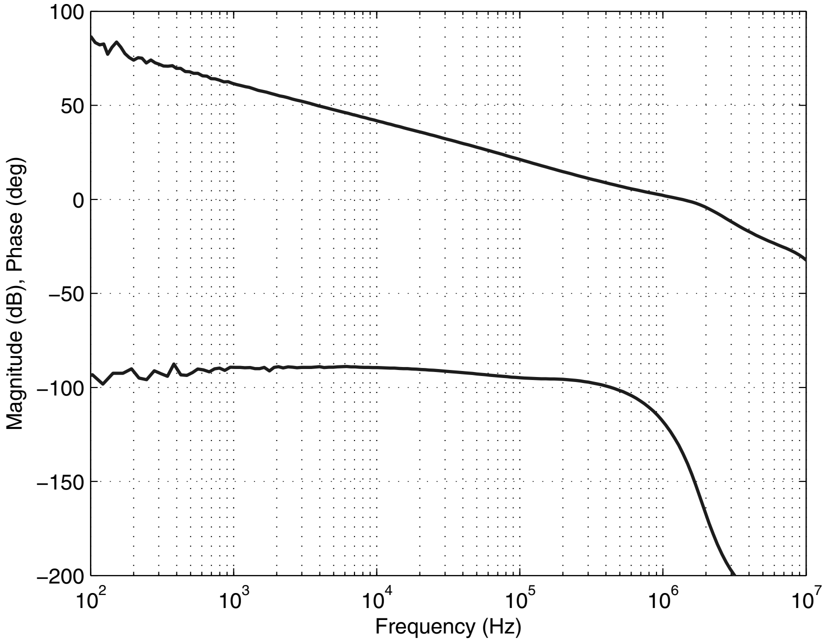


Fig. 32. Frequency response of NMC+HBW amplifier with 100 pF||10 kΩ load.

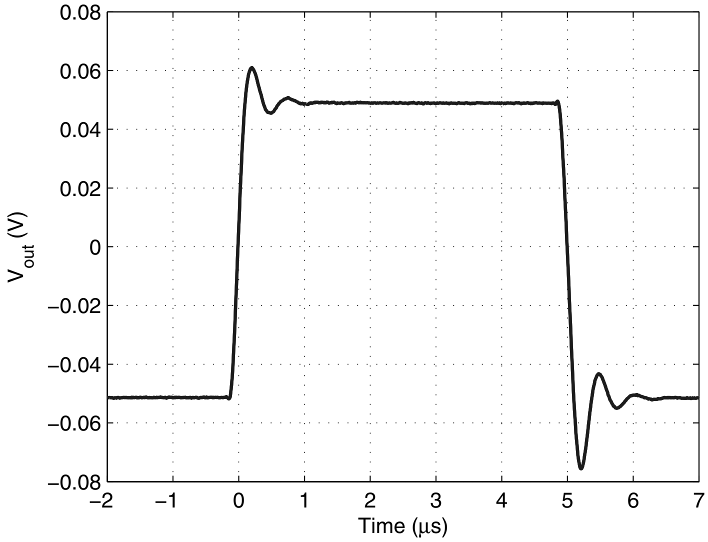


Fig. 33. Small-signal unity gain step response of an NMC+HBW amplifier with a 50 pF||10 kΩ load.

Table 2. SMC+HBW and NMC+HBW amplifier measurement results.

Measured variable	SMC+HBW	NMC+HBW
V_{DD} (V)	1.5	3.3
I_Q (μA)	2400	101
C_L (pF)	1000	50
GBW (MHz)	5.7	1.1
PM (°)	61	59
SR_{min} (V/μs)	3	0.68
FOM_S (MHz×pF/mW)	1580	166
FOM_L (V/μs×pF/mW)	833	103

3.2 Paper II

One very popular and power-efficient two-stage amplifier compensation strategy which is still being actively discussed [44, 62, 63] and reinvented on a regular basis in the literature is based on the use of a cascode transistor as a current buffer. This paper [II] analyzes a three-stage version of this compensation technique, a small-signal model of which is shown in Fig. 34.

The small-signal analysis shows that applications which predominantly drive capacitive loads can greatly benefit from this compensation technique, as it extends the bandwidth of the innermost compensation loop, in which stability is required for the complete amplifier to be stable, as discussed in Section 2.3.

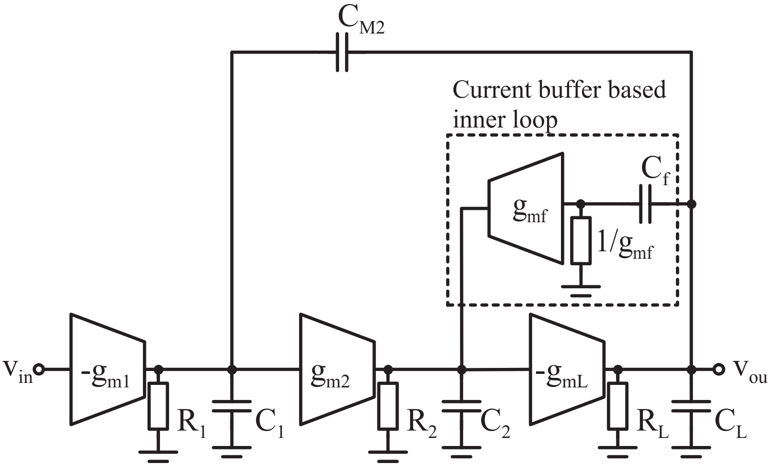
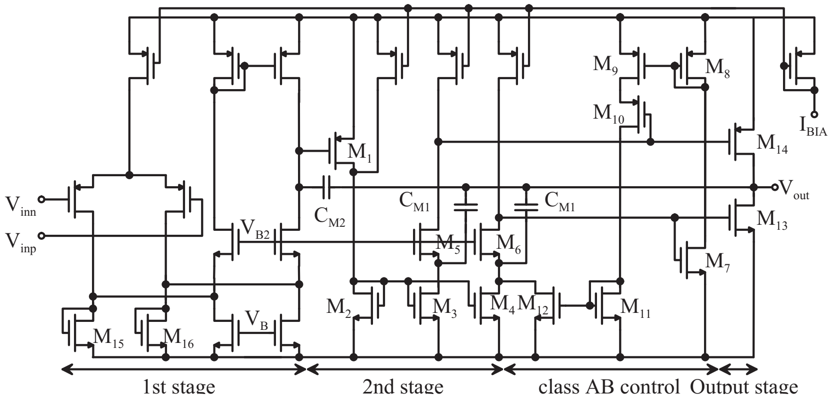


Fig. 34. Small-signal model of the three-stage nested Miller-compensated amplifier with current buffer (FBNMC) analysed in paper [II].

Three-stage amplifier compensation using a current buffer, also known as active feedback nested Miller compensation (FBNMC) in [II], allows good bandwidth efficiency, as demonstrated in the paper using a quite impractical class A amplifier core. A more practical measured but unpublished class AB implementation of an FBNMC amplifier designed in $0.5\mu m$ CMOS technology is shown in Fig. 35. Class AB implementation of the FBNMC concept ensures that the conditional instability which can arise due to a limited SR in the output stage with heavy capacitive loads is not a problem in this case. For comparison purposes, the design targets for this amplifier were the same as for the NMC+HBW amplifier.

Like that of the NMC+HBW amplifier, the first stage of the FBNMC amplifier in Fig. 35 is a simple folded cascode stage with two diode-connected transistors, M15 and M16, which clamp the cascode transistor source voltages during long SR-limited operation. The cascoded second stage is formed by the transistors M1-M6, where the cascode transistors M5 and M6 act as current buffers for the innermost compensation loop. M7-M12 create a single-ended feedback-type class AB control loop similar to [VIII] which controls the quiescent and minimum currents in the output stage of the amplifier. The single ended class AB control, which is less linear than the differential implementation, was used in the thesis in order to verify the stability of the single ended class AB loop with resistive loads. It is, however, easy to modify the control loop to be fully differential by simply copying transistors M9 and M10 and connecting them to the source of M5.

The measured FBNMC amplifier frequency and the transient responses are shown in Fig. 36 and Fig. 37, respectively. Because of the symmetrical compensation network, the step response is also symmetrical and behaves well. Other performance data measured for the three-stage amplifier are summarized in Table 3.



V_{inn}
V_{inp}
V_{B2}
V_B
M_{15}
M_{16}
M_1
M_2
M_3
M_4
M_5
M_6
M_7
M_8
M_9
M_{10}
M_{11}
M_{12}
M_{13}
M_{14}
C_{M2}
C_{M1}
C_{M1}
V_{out}
I_{BIA}
1st stage
2nd stage
class AB control
Output stage

Fig. 35. Schematic diagram of the measured three-stage FBNMC amplifier.

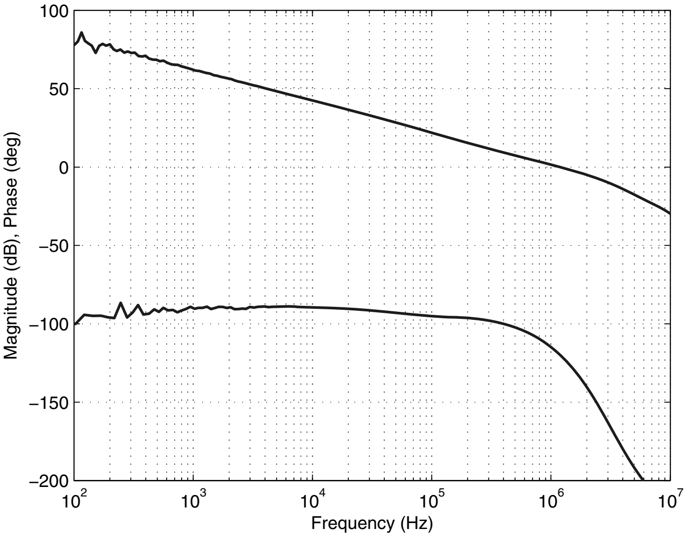


Fig. 36. Frequency response of the FBNMC amplifier with a 100 pF||10 kΩ load.

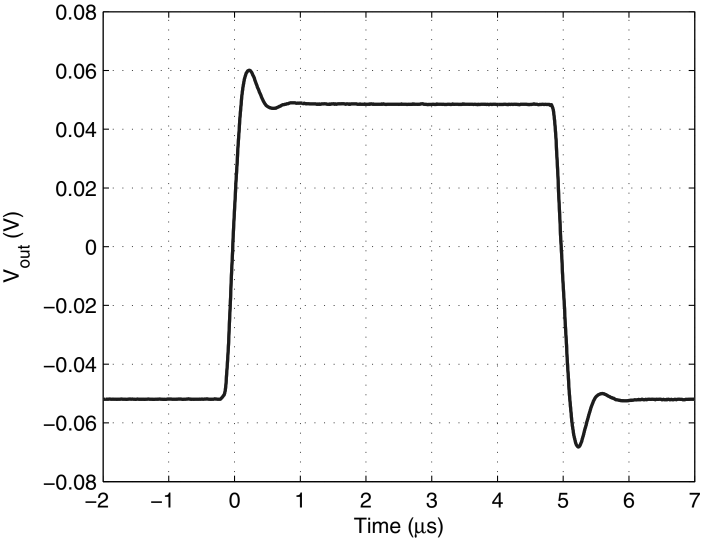


Fig. 37. Small-signal transient response of the FBNMC amplifier with a 50 pF||10 kΩ load.

Table 3. FBNMC amplifier measurement results.

Measured variable	*FBNMC*
V_{DD} (V)	3.3
I_Q (μA)	120
C_L (pF)	50
GBW (MHz)	1.1
PM (°)	63
SR_{min} (V/μs)	0.72
FOM_S (MHz×pF/mW)	138
FOM_L (V/μs×pF/mW)	90

3.3 Papers III and IV

With large capacitive loads, the operational stability of an amplifier is jeopardized if no protective measures are taken. To ensure stability and good settling behavior, a standard industrial technique is to isolate the feedback node from the large capacitive load with a resistor (R_S), as shown in Fig. 38, which reduces loading effects of the capacitive load at high frequencies [64–66].

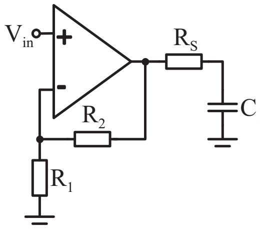


Fig. 38. Standard industrial operational amplifier configuration for driving large capacitive loads.

Papers [III] and [IV] examine the standard isolation or separation resistor approach used in industry when applied to Miller-compensated (SMCR) and cascade-compensated amplifiers (AhujaR), and an alternative separation resistor approach, called strange simple Miller compensation (SSMC) or strange Ahuja compensation (SAhuja).

The difference between the two techniques lies in how the internal compensation capacitance is connected to the large load capacitor, as depicted in Fig. 39.

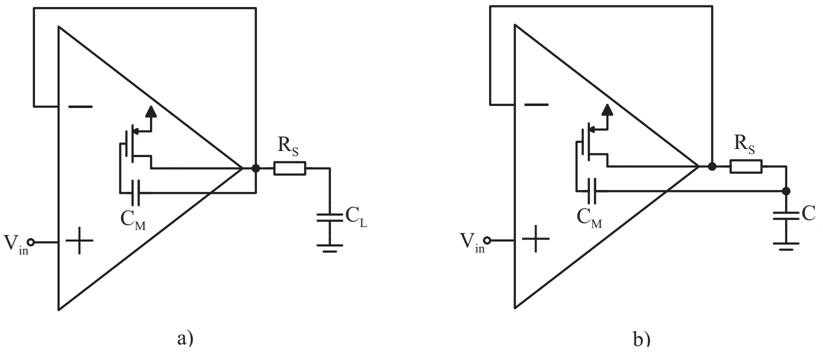


Fig. 39. Schematic circuit diagram showing explicitly how an on-chip Miller capacitor C_M is connected in SMCR a) and SSMC b) amplifiers.

It is shown in the papers using small-signal analysis and simulations that the standard industrial approach suffers from inaccurate pole-zero cancelation, which unnecessarily degrades the stability margins and bandwidth, and that this limitation affects both SMC and cascode-compensated amplifiers. The small-signal analysis and simulation results quoted in the papers were verified using the amplifier presented in [VIII]. The measurement results, as shown in Table 4 and Figs. 40 and 41, support the analysis and demonstrate that the alternative separation resistor technique introduced here indeed has advantages over the standard industrial technique in terms of bandwidth and stability. The simulated pole-zero cancelation, however, is not as perfect as in simulations, probably due to underestimated parasitic PCB capacitances. It should also be noted that in noisy environments use of SSMC technique requires careful consideration as in this technique the high frequency noise can couple directly to the output node.

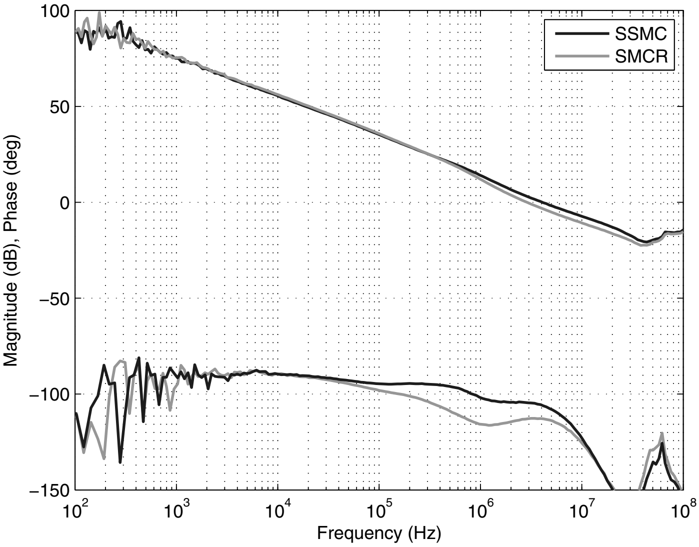


Fig. 40. Frequency responses of SSMC and SMCR amplifiers with a 50 pF||1 MΩ load and a 400 Ω isolation resistor.

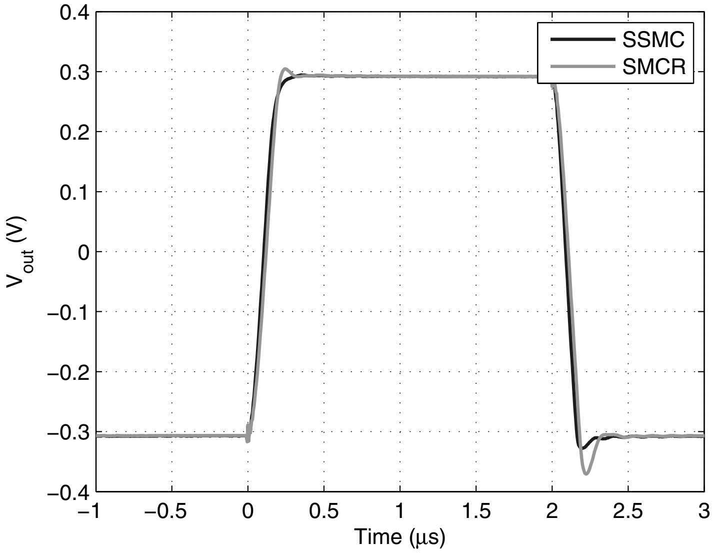


Fig. 41. Large-signal transient responses of SSMC and SMCR amplifiers with a 50 pF||1 MΩ load and a 400 Ω isolation resistor.

Table 4. SMCR and SSMC amplifier measurement results with a 400 Ω isolation resistor.

Measured variable	*SMCR*	*SSMC*
V_{DD} (V)	3.3	3.3
I_Q (μA)	165	165
C_L (pF)	50	50
GBW (MHz)	3.9	5.1
PM (°)	53	66
SR_{min} (V/μs)	3.7	3.7
FOM_S (MHz×pF/mW)	358	468
FOM_L (V/μs×pF/mW)	340	340

3.4 Papers V-VIII

As discussed in Section 2.4 and shown in Fig. 42, the basic problem of Miller compensation above the dominant pole frequency from the point of view of power supply noise rejection performance is the existence of the unity gain signal path from the positive power supply to the amplifier output. To tackle this problem, papers [V], [VI], [VII] and [VIII] describe three circuit techniques and their practical class A and AB amplifier realizations that can be used to improve the nominally poor high frequency PSRR_{dd} of Miller-compensated amplifiers.

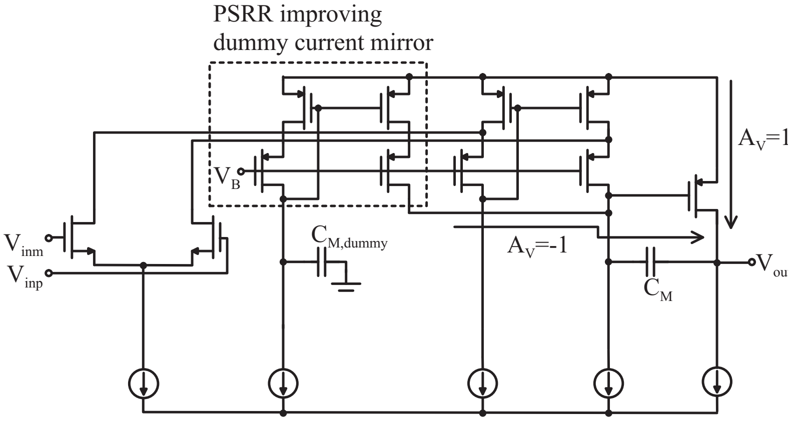


Fig. 42. A simple high PSRR Class A supply pre-regulator, showing explicitly the unity gain path through the output stage and the canceling signal path through the dummy current mirror.

The first two circuit techniques are based on creating an additional signal path from the positive supply to the amplifier output which approximately cancels out the unity gain signal path through the output stage, thus improving the PSRR_{dd} of the Miller-compensated amplifier above the dominant pole frequency. In [V] the additional signal path from the supply is created with a dummy current mirror, as shown in Fig. 42, whereas in [VI] it is created using gain boosting amplifiers inherent to the amplifier topology.

Paper [VII] supplements paper [VI] by presenting a modified version of a supply disturbance-insensitive constant-gm bias current generator [4] and voltage clamps, which were omitted from the original article.

The last paper [VIII] introduces yet another PSRR_{dd} improvement technique, based on a single-ended, ground-referenced, class AB control loop. It is shown by means of small-signal analysis that an asymmetric class AB feedback loop attenuates positive supply disturbances very effectively, allowing an improvement of up to 40dB in the mid-band PSRR_{dd} as compared with standard symmetrical class AB structures. The price to pay, however, is an asymmetric step response and possible class AB loop instability, due to the fact that the quiescent and minimum currents in the NMOS output stage transistor are effectively controlled through the global feedback path across the amplifier, which has more delay than the short local feedback loop that controls the PMOS output stage transistor.

The measured performance of the two high PSRR amplifiers manufactured in a 0.5μm CMOS process is summarized in Table 5. The results, which are plotted in the accompanying articles, show an improvement of more than 20dB over the basic structures.

Table 5. Measurements of the performance of the high PSRR amplifiers discussed in [VI] and in [VIII].

Measured variable	Amplifier in [VI]	Amplifier in [VIII]
V_{DD} (V)	2.7	3.3
I_Q (μA)	298	165
C_L (pF)	20	20
GBW (MHz)	10.6	5.4
PM (°)	51	61
SR_{min} (V/μs)	5.8	3.7
FOM_S (MHz×pF/mW)	261	198
FOM_L (V/μs×pF/mW)	143	135

4 Discussion

Although the first general purpose amplifier was introduced by Swarzel Jr. in 1941 [67], operational amplifiers are still topics of active research in universities and companies around the world, although the research field has nowadays become highly diversified.

Much of the research has focused on improving the bandwidth efficiency of two and three-stage amplifiers [39–41, 43, 52, 68–70] and amplifier architectures [4, 9, 11, 71]. This has resulted in new high DC gain rail-to-rail input and output amplifier topologies which support low voltage battery chemistry, are simpler and more structural than their predecessors and have improved rail-to-rail input and output stages. Another aspect of the research has been to improve other secondary amplifier performance parameters such as PSRR, CMRR, offset drift and high voltage performance [4, 72].

The first two articles, [I] and [II], and the additional data given in Chapter 3 of this thesis presented two practical implementations of bandwidth-efficient low voltage compatible class AB amplifiers and a theoretical analysis of the compensation techniques used. These techniques are not completely new and the theoretical work partly overlaps with other published results. The transconductance boosting principle, for example, is essentially the same as the one used by [73], but it is applied in a more general way in this thesis to create a true class AB amplifier with large positive and negative maximum currents. The second three-stage amplifier compensation technique is also well known from two-stage amplifiers [44, 54, 55, 74–77] and has been used without any rigorous theoretical analysis in three-stage and four-stage amplifiers [78, 79] and analysed and improved by other authors around the same time as paper [II] was published [80].

Most of the multi-stage amplifier compensation techniques published to date have been demonstrated using class A amplifiers [43, 51, 52, 69, 70, 81], whereas the goal in this thesis was to investigate compensation techniques that could be easily applied to class AB amplifiers with a rail-to-rail output stage, as has been done by Prof. Huijsing's group, for instance [39, 40]. If we compare the small-signal figures of merit obtained for a three-stage amplifier ($\approx 150\, MHz * pF/mW$) with the those published for state-of-the-art low voltage class A amplifiers, which range from 600 up to 9500 [43, 69, 80], the results seem no more than moderate, but if we compare the two and three-stage amplifier measurement results with the class AB implementations of SMC, NMC or multipath nested Miller-compensated amplifiers presented in [9] and [40], or with state-of-the-art industrial class AB amplifiers, which are often implemented in high performance BiCMOS processes and have similar specifications, such as TLV3270 and LMP7701, the results are in a same range. The possible discrepancy between the published class A and class AB amplifiers is partly due to their different operating voltages and additional class AB control of quiescent current consumption, but also to the design approach, which emphasizes general capacitive and resistive load stability, which allows the capacitive load and load current to vary without fear of instability.

The small-signal figures of merit can be considerably improved either by using a simple two-stage amplifier topology, as was done in [VI] and [VIII], or by adding a series resistor to isolate the large load capacitor from the feedback node, as was done in papers [III] and [IV]. The series or isolation resistor technique is an industrial standard for driving large capacitive loads [65, 66] and it is also commonly used on mixed-signal chips, e.g. to obtain a low pass filter buffered reference signal without destabilizing the voltage buffer. The alternative isolation resistor technique SSMC introduced here, in which the internal compensating capacitor is connected directly to the load node, is not as generally applicable as the *de facto* industrial standard, where the compensation capacitor is connected directly to the feedback node. There is also no benefit to be achieve by using the SSMC technique when the series resistance to be added is large, as is the case when this large series resistor is part of a first-order low pass filter. The benefits of the alternative series resistor technique can be seen only if it is used in applications where the expected single load capacitor is much larger than the required Miller capacitor, e.g. as a SAR ADC input buffer load capacitance [64], and where the isolating resistor can be placed on chip. Measurements suggest that in these applications the SSCM technique allows a bandwidth improvement of approximately 30% without increasing the system complexity and also permits a more closely spaced pole-zero doublet, which improves the settling behavior of the amplifier [82, 83].

The PSRR of class A amplifiers in general, and particularly the poor high frequency PSRR of Miller-compensated amplifiers, which was addressed in [V], [VI] and [VIII], is discussed extensively in graduate-level analogue electronics textbooks [14, 38, 42], but despite the fact that many applications, such as linear regulators or on chip supply pre-regulators, need accurate control of supply disturbances over a wide frequency range and that many new industrial class AB amplifiers such as LMP7701 have an asymmetrical PSRR, for improving power supply ripple rejection in class AB amplifiers do not often appear in the literature, which makes it difficult to make a fair comparison with the results obtained here.

The PSRR improvement techniques that have been published and patented to date can be divided roughly into four categories: those based on cascode compensation [38, 54], a low impedance-driven PMOS output stage [84, 85], a feedback loop [86] and disturbance feed-forward techniques [59, 61]. The techniques used in [V] and [VI] fall into the last category, whereas [VIII] belongs to the feedback group. Using a figure of merit which compares the frequency up to which the amplifier maintains its DC PSRR level with the amplifier unity gain frequency

$$FOM_{PSRR} = \frac{f_t}{f_{PSRR,DC}}, \tag{46}$$

one can say that the results achieved by feed-forward techniques ($\sim$1000) are almost as good as those of the feedback-based solution ($\sim$500). These figures also compare favorably with state-of-the-art industrial amplifiers such as TLV3270 and LMP7701, the FOM_{PSRR} of which varies from approximately 1000 to 2000.

5 Conclusions

5.1 Summary

The goal of this thesis was to improve the performance of existing class AB amplifier topologies by investigating their compensation, input and output stages and PSRR. The focus was on simple two and three-stage amplifiers which either drive heavy resistive and capacitive loads or which need extremely good positive power supply noise rejection performance. Emphasis was placed on a simple operating principle and robustness, because in practise these facilitate intellectual property re-usage and are more power-efficient than more complex solutions.

The compensation techniques employed, which use either an additional series isolation resistor, a high bandwidth voltage gain stage or a current buffer, gave improved performance relative to basic solutions, but their applicability depends greatly on the application and on the high bandwidth voltage gain stage/current buffer power efficiency.

The amplifier topologies developed here make efficient use of available process options and already existing transistors to shield the DC gain in the amplifier from impact ionization, to improve the positive power supply PSRR of Miller-compensated amplifiers positive power supply PSRR and to implement mismatch and supply-insensitive class AB output stages which can be used differentially or, as in this thesis, in a single-ended manner.

The amplifier topologies measured here are summarized qualitatively in Tables 6 and 7.

Table 6. Qualitative summary of the measured two-stage amplifiers

Qualitative measure	SMC [VI,VII],	SMC+HBW [I]	SSMC [VIII]
I_Q stability	++	-	+
Bandwidth efficiency	o	+	++
High frequency PSRR	++	o	++
Compact	-	-	++

Table 7. Qualitative summary of the measured three-stage amplifiers

Qualitative measure	NMC+HBW	FBNMC [II]
I_Q stability	+	+
Bandwidth efficiency	+	+
High frequency PSRR	o	o
Compact	+	+

5.2 Future work

Amplifier research has been largely application-driven, and the increasing environmental awareness, which also requires good power efficiency in circuits not targeted for portable devices, will become another factor directing this research in the future. This will render future amplifier research highly specific, e.g. concentrating on high voltage/low voltage or super fast on chip regulation applications which approach the limits of the process by means of nonlinear control techniques, self-calibration techniques using the possibilities offered by area-efficient digital logic and improved interference insensitivity, of which National Semiconductor's EMI robustness initiative is a good example. Self-calibration/environmental awareness in particular has a great potential for improving power efficiency and reliability of amplifiers if it can be used to measure capacitive loading accurately at the amplifier output, for example, or the presence of a supply decoupling capacitor.

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