Low Noise LDO Architecture with Consideration for Low Voltage Operation

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***Abstract*—High performance low dropout regulator (LDO) is presented in this paper. An analysis of low noise architecture incorporating reference amplifier followed by a low-pass filter (LPF) and an error amplifier (EA) connected as a voltage follower is done, with a special focus on the low voltage operation implementation. By introduction of special design approach of error and reference amplifiers, low voltage operation of the regulator was achieved. This LDO is ideal for supplying sensitive loads in low power applications.**

Keywords— low dropout regulator; low noise; low power; low voltage

I. INTRODUCTION

With the emerging trend to lowering fabrication process sizes and power dissipation the need in low voltage power supplies has evolved. Together with that the need of clean supplies for sensitive circuits is still valid. With that in mind the demand in low voltage LDOs with good noise performance has become crucial in a number of applications ranging from remote sensors to high performance data converters. Apart from that in some systems where switching DC-DC converters are used to step down voltage from the main supply, LDOs are often used as post regulators for suppressing the output voltage ripple. In this case low voltage operation can also become a critical factor.

Several techniques exist to make LDO capable to work in a sub 1 V domain ranging from integration of a digital controlled loop as done in [1] to deliberate decrease of transistors' threshold voltages (V_{TH}) by using body effect phenomenon [2]. However it is not simple to get both good performance in sense of noise and low voltage operation in a single LDO. In current paper an effort is taken to fulfil such a combination in a working solution. In order to accomplish that, first low noise LDO architecture was taken which was afterwards adopted to low voltage operation by using corresponding techniques in designing the amplifiers.

As a result a high performance low input low output regulator with improved noise was achieved capable of supplying loads highly sensitive to any kind of disturbances.

The concept of the proposed LDO is presented in section II. Circuit design and implementation are explained in section III. Experimental results and conclusions are drawn in sections IV and V, respectively.

II. THE CONCEPT OF THE PROPOSED LDO ARCHITECTURE

Current section will present the analysis of conventional LDO architecture (Fig.1) with the focus on the main noise contributors and propose an architecture which eliminates the main noise sources and is suitable for implementation of the low voltage operation feature.

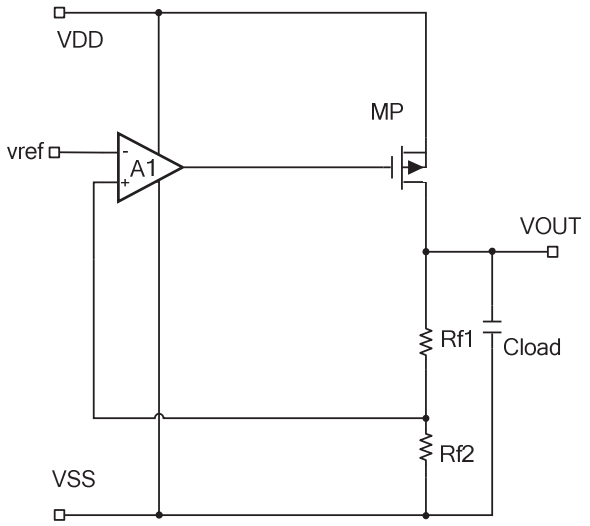

Fig.1. Conventional LDO structure

Fig. 2 represents the most significant noise sources of the conventional LDO structure. From the work done in [3] the total output noise spectral density of the LDO system *Sn,o(f)* can be written as

$$Sn,o(f) = \left(S(n,ref) + Sn,e(f)\right)\left(1+\frac{Rf1}{Rf2}\right)^2 + \\ +Sn,rf2\left(\frac{Rf1}{Rf2}\right)^2 + Sn,rf1 \quad (1)$$

It can be seen that the most significant noise sources in this LDO are reference produced noise at vref node, A1 noise and noise associated with output resistor divider (*Rf1*, *Rf2*).

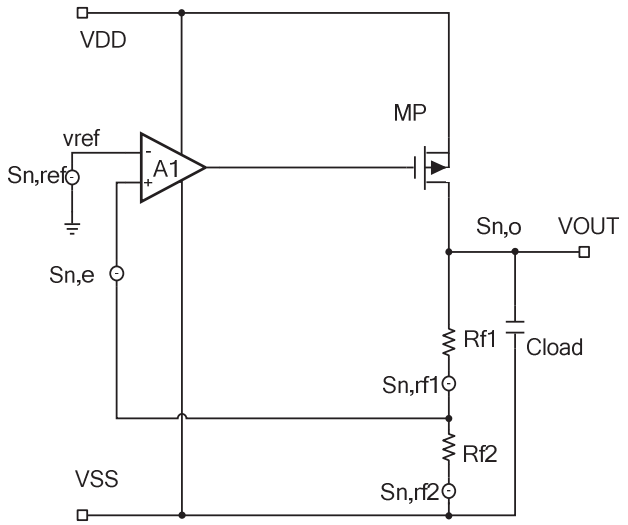

Fig.2. LDO's main noise sources

In order to reduce the number of noise generating sources without degradation of other performance, an updated low noise LDO structure was used which can be found in Fig. 3.

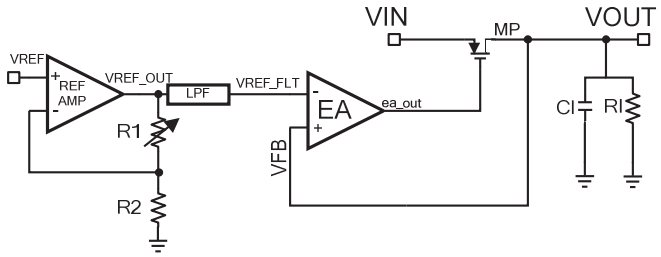

Fig. 3. A proposed low noise LDO structure

Unlike the standard architecture here voltage selection which is normally performed by a resistive divider was moved to the reference part where a reference amplifier with a varying upper resistor is used to perform this function. In this case the needed output voltage can be easily selected by changing the resistance ratio. LPF in the reference path is used to suppress noise to the EA input stage, while the amplifier itself operates as a voltage follower with unity gain [4]. This way reference induced noise and noise associated with the resistor divider is mostly filtered out and total output noise from (1) becomes dominated only by the EA's noise:

$$Sn,o(f) \approx Sn,e(f). \tag{2}$$

III. Circuit Implementation

This section will explain how the architecture presented in Fig. 3 is implemented on the circuit level. The main focus here will be made onto securing low voltage operation of the solution. In order to make the understanding of the implementation more straightforward, the description of the LDO is divided into three subsections each describing its own block.

A. Reference Amplifier

The main limiting factor for low voltage operation of reference amplifier is input voltage which should be as low as possible. An A class operational amplifier with NMOS FET input pair is used in proposed architecture and depicted in Fig. 4. In this structure minimum input voltage can be defined as

$$VDD_{min} = V_{TH4} + V_{DS0}. \tag{3}$$

In case of A class operational amplifier with PMOS FET input pair minimum input voltage is the same as in (3). However the maximum common mode voltage for NMOS amplifier is

$$V_{CMMAX} = VDD - V_{SG4} + V_{TH0}, \tag{4}$$

while for PMOS amplifier

$$V_{CMMAX} = VDD - V_{TH0} \tag{5}$$

Thus V_{CMMAX} in NMOS amplifier is approximately one V_{TH} larger than in case of PMOS input pair. LDO output voltage of the proposed architecture can be calculated by

$$V_{out} = V_{ref}\frac{R_1+R_2}{R_2} \tag{6}$$

For normal operation of reference amplifier its reference voltage should be $V_{ref} < V_{CMMAX}$. Thus the choice between NMOS and PMOS input pair is dictated by available reference voltage value.

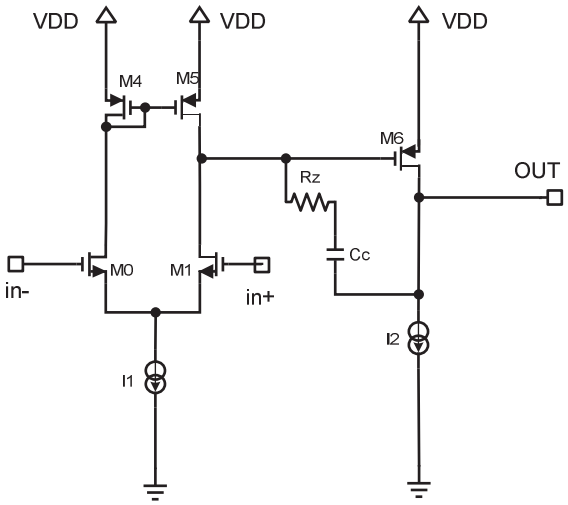

Fig. 4. Reference amplifier

B. Filter Implementation

As this structure is concentrated on low output noise and the main noise sources have been described earlier, the reference amplifier together with resistive divider are isolated by a low pass filter with an ultra high time constant.

To achieve such a time constant the filter output resistance should be in the range of GOhms, but this would occupy significant silicon area when using passive resistor. In current

approach the low pass filter is implemented by a very high resistive MOS transistor acting as a resistor with a capacitor of order of 10pF to 100pF (Fig. 5). The filter's capacitor can be either poly/poly cap or a MOS transistor. The latter is more effective in sense of occupied area.

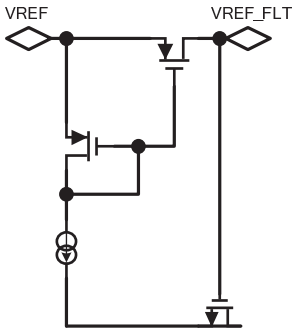

Fig. 5. Reference low pass filter's schematic

The MOS resistor is relatively simple and is a very area effective approach for obtaining large resistance values. The main problems are related to the high impedance output of the filter. This means that any leakage above 1 pA cause inadmissible errors. Since the PMOS resistor is placed in an n-well, which is connected to the input of the filter (a low impedance node), the leakage between resistor and n-well is suppressed (Fig. 5 and Fig. 6). The MOS resistor pn-junction, connected to the high impedance node, should not leak because of zero bias. No other pn-junctions are connected to that node except a startup transistor, which acts as a similar MOS resistor with much lower resistance, biased exactly the same way.

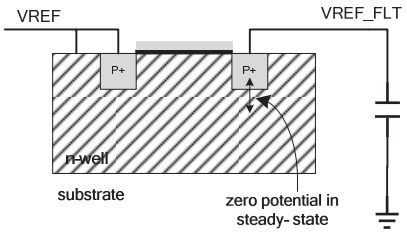

Fig. 6. Reference low pass filter's MOS resistor

This approach is area and noise effective and depends on final compromise between the filter resistance and capacitance values which in its turn depend on the available silicon area.

C. *Error Amplifier*

As the EA in a newly formed structure works as a voltage follower, i.e. regulated voltage at the output of LDO is fed back directly to the EA's input; the common mode voltage (V_{CM}) should be able to swing up to the supply or at least very close to it, so that low dropout operation could remain functional. For that reason simple two-stage Miller compensated amplifier with NMOS input pair, like the one used as a reference amplifier, served as a basis for EA design (Fig.4). The maximum common mode voltage in this amplifier is (4). This way V_{CMMAX} is still slightly lower than VDD. In order to increase V_{CMMAX}, the original structure was modified. The updated structure can be seen in Fig.7. In this newly formed amplifier transistor M9 eliminates the need for M4 to have voltage drop higher than V_{TH}. As a result the maximum common mode voltage changed to

$$V_{CMMAX} = VDD - V_{DS4} + V_{TH0} \quad (7)$$

This means that input of the OP-AMP can be safely swept up to supply without degrading amplifier's performance.

Another reason for the changes in the original circuit is VDD_{min} optimization, which was achieved by the elimination of the diode-connected PMOS in the load path of the input stage and resulted in the transformation of (3) into:

$$VDD_{min} = V_{DS4} + V_{DS0}. \quad (8)$$

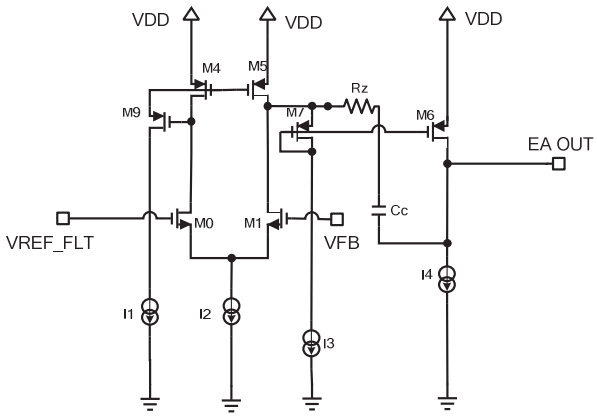

Fig. 7. Error amplifier circuit.

IV. Experimental Results

The circuit was designed and fabricated using 0.18 µm 1.8 V CMOS process with typical threshold voltages around 500 mV. Input voltage V_{IN} range is from 0.9 V to 1.8 V while output can be regulated down to 0.65 V. All blocks inside LDO except MP can be supplied either from V_{IN} or from a separate supply, making it ideal to be used as post regulation LDO.

Layout view of the LDO can be found in Fig. 8. Placement optimization of the blocks and efficient routing minimized the area of the device to 0.14 mm^2.

Full circuit evaluation confirmed good functionality within the input voltage range of 0.9 V to 1.8 V and the output range of 0.65 V to 1.5 V. Fig. 9 represents simulated output noise waveforms with different input and output voltage settings covering the entire specified range. As it is seen there is no substantial difference between the results starting from 10 Hz onwards and thus the integrated noise of all the cases in the range of 10 Hz to 100 kHz is roughly equal (around 20 μV_{RMS}).

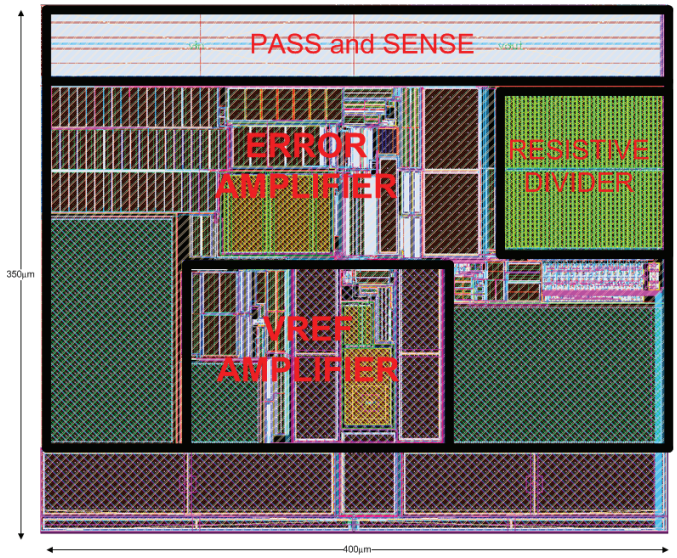

Fig. 8. Layout view of the LDO

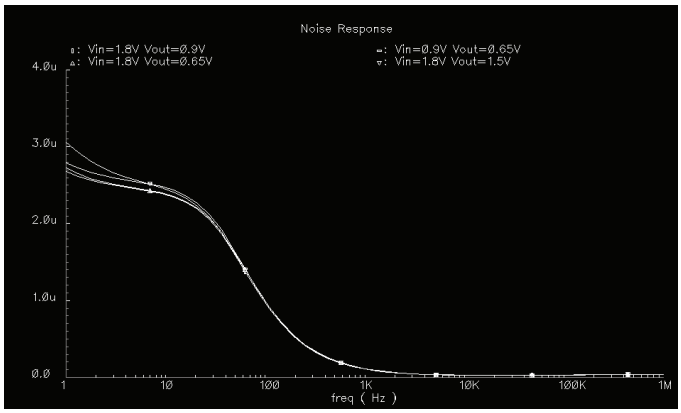

Fig. 9. Simulated noise results in different test conditions

Table I summarizes the LDO parameters achieved by measurement of the fabricated prototype. As it can be seen the use of low noise architecture resulted in 17 μV_{RMS} total integrated noise which perfectly correlates with the simulated results.

TABLE I. MEASURED PARAMETERS OF THE PROPOSED LDO

Parameter	Conditions	Value
Supply voltage	I_{OUT}=150mA	0.9...1.8V
Output voltage	I_{OUT}=150mA	0.65…1.5V
Maximum load current		150mA
Quiescent current	I_{OUT}=0mA	24µA
Noise	I_{OUT}=150mA f = 10Hz to 100kHz	17μV_{RMS}
Dropout voltage	I_{OUT}=150mA V_{IN}=1.5V	68mV

V. CONCLUSIONS

The presented work had the aim to combine so far non-combinable features like low voltage operation and low noise in a single LDO. In order to achieve this goal separate actions were taken to improve each of these two parameters. Special low noise architecture was implemented to improve noise performance. This was achieved by taking out all the main noise contributors like resistive divider with a reference amplifier into a separate group and than passing the resulting signal through a low pass filter with a very large time constant onto a voltage follower. This resulted in extremely low output noise which was verified by both simulation and measurement. Additionally special design practices implemented in the error amplifier and the reference amplifier schemes ensured low voltage operation of the LDO.

As a result of the work done, a sub 1 V low noise LDO was designed and fabricated that is ideally suitable for post regulator application capable of supplying highly sensitive loads.

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REFERENCES

[1] Chen J.-J., Lin M.-S., Lin H.-C., Hwang Y.-S.: “Sub-1V Capacitor-Free Low-Power-Consumption LDO with Digital Controlled Loop” Proc. APCCAS 2008. IEEE Asia Pacific Conference on Circuits and Systems, 2008, pp. 526-529.

[2] Huang W.-J., Liu S.-I.: “Sub-1V capacitor-free low-dropout regulator” IET Electronics Letters, Nov. 2006, Vol. 42, No. 24, pp. 1395 – 1396.

[3] Oh W., Bakkaloglu B.,Wang C., Hoon S.K.: “A CMOS Low Noise, Chopper Stabilized Low-Dropout Regulator with Current-Mode Feedback Error Amplifier” IEEE Transactions on Circuits and Systems—I: Regular Papers, nov. 2008, Vol. 55, No. 10, pp. 3006 – 3015.

[4] Mannama V., Sabolotny R., Strik V., Tiikmaa R.: “Low noise, low power, fast startup, and low drop-out voltage regulator” US Patent 7397226, 8 July 2008.