A CMOS Low Noise, Chopper Stabilized Low-Dropout Regulator With Current-Mode Feedback Error Amplifier

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***Abstract*—Low $1/f$ noise, low-dropout (LDO) regulators are becoming critical for the supply regulation of deep-submicron analog baseband and RF system-on-chip designs. A low-noise, high accuracy LDO regulator (LN-LDO) utilizing a chopper stabilized error amplifier is presented. In order to achieve fast response during load transients, a current-mode feedback amplifier (CFA) is designed as a second stage driving the regulation FET. In order to reduce clock feed-through and $1/f$ noise accumulation at the chopping frequency, a first-order digital $\Sigma\Delta$ noise-shaper is used for chopping clock spectral spreading. With up to 1 MHz noise-shaped modulation clock, the LN-LDO achieves a noise spectral density of 32 nV/$\sqrt{}$Hz and a PSR of 38 dB at 100 kHz. The proposed LDO is shown to reduce the phase noise of an integrated 32 MHz temperature compensated crystal oscillator (TCXO) at 10 kHz offset by 15 dB. Due to reduced $1/f$ noise requirements, the error amplifier silicon area is reduced by 75%, and the overall regulator area is reduced by 50% with respect to an equivalent noise static regulator. The current-mode feedback second stage buffer reduces regulator settling time by 60% in comparison to an equivalent power consumption voltage mode buffer, achieving 0.6 μs settling time for a 25-mA load step. The LN-LDO is designed and fabricated on a 0.25 μm CMOS process with five layers of metal, occupying 0.88 mm^2.**

***Index Terms*—Chopper stabilization, current feedback amplifier, low-dropout regulators, power supply rejection.**

I. Introduction

As CMOS technology is rapidly moving towards deep submicron gate lengths, supply voltages for analog, mixed signal and RF circuits are continuously decreasing. With the reduction of the supply voltage, noise and cross-coupling on the power supply line start playing a dominant role in an RF transceiver noise budget. Nonlinearities associated with LNAs, mixers and oscillators upconvert or intermodulate low frequency noise with the signal band. Specifically, synthesizer and TCXO phase noise, LNA and mixer noise figure, and adjacent channel power ratios of the PA are heavily influenced by the supply noise and ripple. Linear low dropout (LDO) regulators shield sensitive blocks from high frequency fluctuations on the power supply while providing high accuracy, fast response supply regulation [1]–[4], [15], [16].

A typical RF transceiver application that requires a low-noise LDO is shown in Fig. 1. In addition to RF sections, baseband and analog sections of RF transceivers, especially transmitter power control DACs and receive channel ADCs have finite PSR; therefore, at lower supply rails, they require low noise power supplies [5]–[7].

In order to suppress thermal and flicker noise, conventional LDOs utilize highly filtered voltage references at their inputs and bypass capacitors at their outputs. However, with technology scaling, $1/f$ noise increases significantly [8]. Since $1/f$ corner frequency is a weak function of most transistor parameters, suppression of low frequency noise from supply regulators in sub-micron CMOS processes is becoming a critical design problem.

Chopper stabilization techniques have been used for $1/f$ noise reduction and DC offset suppression of low noise instrumentation amplifiers [9], [10]. Chopper stabilization modulates the low frequency noise and offset components to higher frequencies by a mixing operation, followed by filtering low-pass filtering. However, the mixing operation generates discrete tonal content harmonically related to the chopping frequency due to clock feedthrough and insufficient filtering provided by the amplifier. The discrete tonal content can intermodulate with the amplifier input signal, $1/f$ noise and load transients, causing sideband noise around the chopping frequency. In order to reduce the discrete tonal content at the LDO output, a noise shaped clock generator using $\Sigma\Delta$ modulator is utilized in this design. For low $1/f$ noise regulator applications, the error amplifier input pair area can become quite large, causing a parasitic pole at the amplifier input and degrading LN-LDO stability. Relaxed $1/f$ noise requirements due to chopper stabilization reduce the error amplifier silicon area, thereby reducing the parasitic capacitance at the error amplifier input. The proposed LN-LDO also presents a fast-response current-feedback second stage, improving settling time during load transients by 60%. This paper presents the first application of chopper stabilization techniques and noise shaped clocking to linear regulators.

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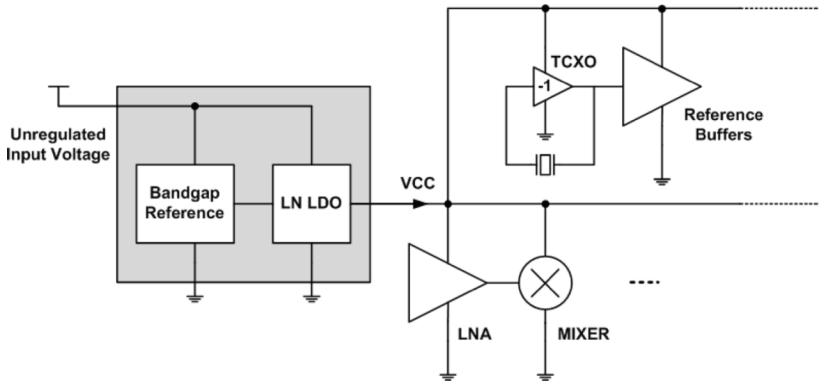


Fig. 1. Typical low noise low-dropout (LN-LDO) regulator application for RF transceiver SOCs.

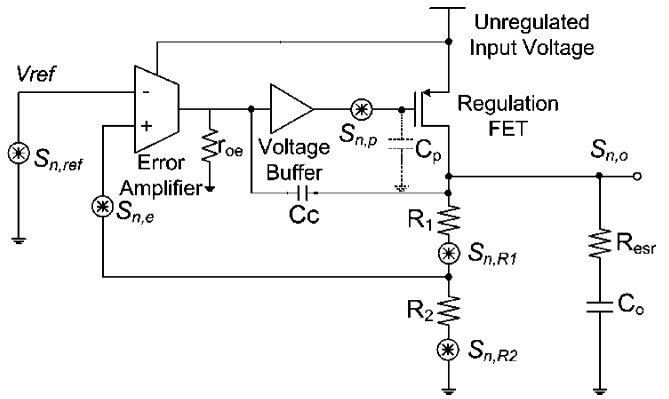


Fig. 2. Block diagram of a typical LDO regulator depicting major noise contributors.

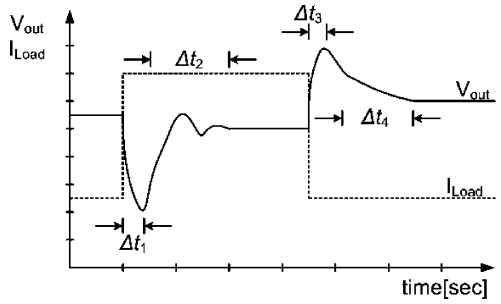


Fig. 3. Typical LDO transient response to a load current step.

The remainder of the paper is organized as follows. Input referred noise and settling time trade-offs in internally compensated LDO regulators are analyzed and principles of chopper stabilization are introduced in Section II. Section III presents the system and circuit level description of the proposed design. Section IV presents the silicon evaluation results.

II. Low Noise, Low-Dropout Regulators

A. LDO Noise and Transient Response Analysis

Fig. 2 shows a block diagram of a typical internally compensated LDO regulator, which consists of an error amplifier, a pass device, a high resistance feedback network and an output capacitor C_o. The PMOS regulation FET at the output is configured in common-source configuration. Due to its high transconductance value and large geometry device, input referred noise of the regulation FET, $S_{n,p}(f)$, can be ignored. The input referred noise power spectral density (PSD) of the error and buffer amplifier is denoted by $S_{n,e}(f)$, and total output noise of the voltage reference is defined by $S_{n,ref}(f)$. Total output noise spectral density of the LDO system $S_{n,o}(f)$ is represented by

$$S_{n,o}(f) = (S_{n,ref}(f) + S_{n,e}(f))\left(1+\frac{R_1}{R_2}\right)^2 + S_{n,R2}\left(\frac{R_1}{R_2}\right)^2 + S_{n,R1}. \quad (1)$$

Assuming reference noise $S_{n,ref}(f)$ can be suppressed by sufficient filtering or a chopper stabilized bandgap reference system can be used, the total output noise of an LDO can be approximated as follows:

$$S_{n,o}(f) \approx S_{n,e}(f)\left(1+\frac{R_1}{R_2}\right)^2 + S_{n,R2}(f)\left(\frac{R_1}{R_2}\right)^2 + S_{n,R1}(f). \quad (2)$$

As seen from (2), in order to minimize LDO output noise, the error amplifier contribution and thermal noise contribution of the feedback network should be minimized. However, $1/f$ noise of the error amplifier becomes a dominant factor at lower frequencies due to limited filter attenuation, especially for submicron processes at low frequencies.

The unity-gain frequency of a typical LDO is limited by the parasitic pole generated by the output impedance of the error amplifier and gate capacitance of the regulation FET. As shown in Fig. 2, this pole can be split to a higher frequency by using a low-output impedance voltage buffer between the error amplifier and regulation FET. This helps with the reduction of the output capacitance and improves settling time of the LDO. The zero set by the capacitor ESR ($R_{\rm esr}$) and load capacitor C_o is designed such that stability is guaranteed for all load and feedback conditions [3], [12].

Another important specification of an LDO is its transient response to a transient load current step. Fig. 3 shows the characteristics of a typical load stimulus and response of an LDO [3]. Δt_1 is a function of bandwidth as well as slew rate of the buffer

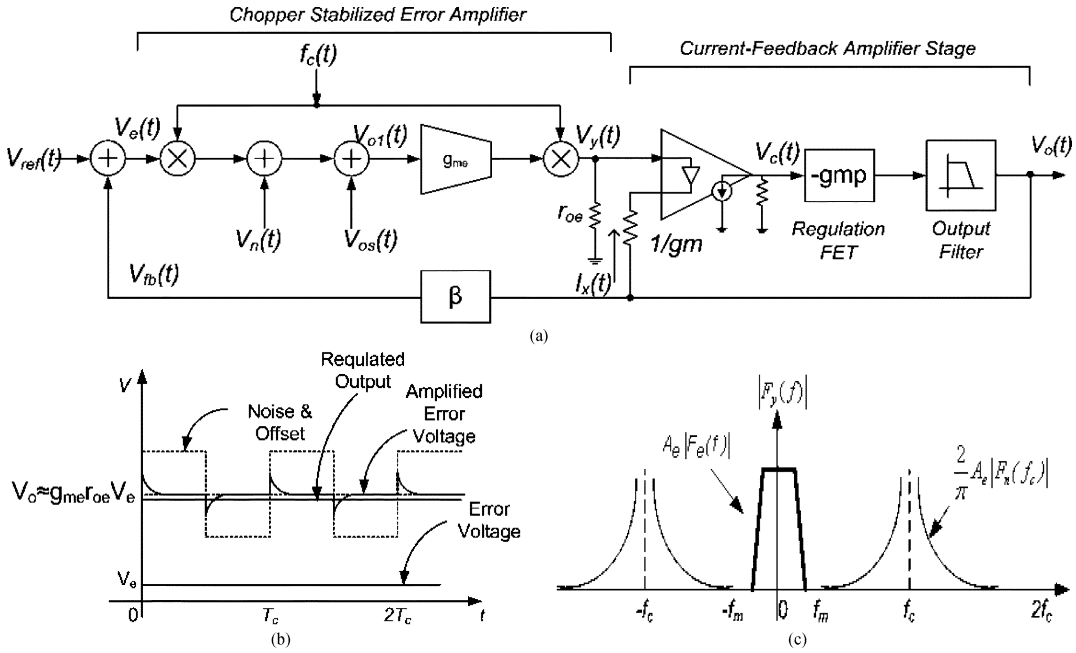


Fig. 4. (a) Diagram of chopper-stabilized LDO regulator with a fixed frequency chopping clock (b) time domain representation of regulation signals (c) frequency spectrum of the regulation signals.

amplifier driving the parasitic gate capacitor (C_p) of regulation FET and is given by

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_p \frac{\Delta V}{I_{sr}} \tag{3}$$

where BW_{cl} is the closed loop bandwidth of the system, t_{sr} is the slew rate time associated with parasitic pole of the pass device, ΔV is the voltage variation at the parasitic gate capacitance C_p, and I_{sr} is the slewing current charging the parasitic pole of pass device of the buffer stage between the error amplifier and regulation FET. Similar to Δt_1, Δt_3 is also inversely proportional to the closed loop bandwidth of LDO. In order to minimize Δt_1 and Δt_3, the LDO requires a higher closed-loop bandwidth and a high slew rate current. The settling time Δt_2 is dependent on the time requirement for the regulation FET to fully charge the load capacitor, which is also related to the phase margin of the regulator. Δt_4 is the time required to discharge the output capacitor to its final value. This is a function of discharge current through the feedback network and voltage variation across the ESR of the load capacitor. As the ESR value increases, settling time reduces, however output voltage variation increases. In order to reduce settling times Δt_2 and Δt_4, the output capacitor (C_o) should be minimized.

As detailed above, dominant contributors to the transient response of an LDO are, slew rate at the regulation FET, output and bypass capacitors, the ESR of the output capacitor, the bandwidth of the system, and the discharge current capability of the LDO. In this design, a second stage current feedback amplifier is used in order to minimize the impact of slew rate on the output settling time, as discussed in Section III.

B. Chopper Stabilized LDO Architecture

System level operation of a chopper stabilized LDO is illustrated in Fig. 4. The error signal at the input is represented by $V_e(t)$ and the error amplifier input referred noise and offset is represented by $V_n(t)$ and $V_{os}(t)$, respectively. After the first modulation, the error signal is transposed to odd harmonics of the modulation signal $f_c(t)$. At the second modulator, low frequency noise and DC offsets are transposed to higher harmonics of the chopping frequency f_c, while the control signal $V_c(t)$ gets downconverted back to the baseband.

The low frequency regulation FET control signal $V_y(t)$ before going through the low pass filtering provided by Miller compensation can be represented as follows:

$$V_y(t) \approx A_e V_e(t) + A_e \sum_{k=-\infty}^{\infty} \left\{ \frac{2\left[V_n(t) + V_{os}(t)\right] e^{j2\pi(2k+1)f_c t}}{j(2k+1)\pi} \right\} \tag{4}$$

where the error signal is

$$V_e(t) = V_{ref} - \beta V_o(t) \tag{5}$$

and A_e represents the DC gain of the error amplifier. Fourier transform of (4) can be represented by

$$V_y(f) \approx A_e(f) V_e(f) + A_e(f) \sum_{k=-\infty}^{\infty} \left\{ \frac{2\left[V_n(f+(2k+1)f_c) + V_{os}(f+(2k+1)f_c)\right]}{j(2k+1)\pi} \right\}. \tag{6}$$

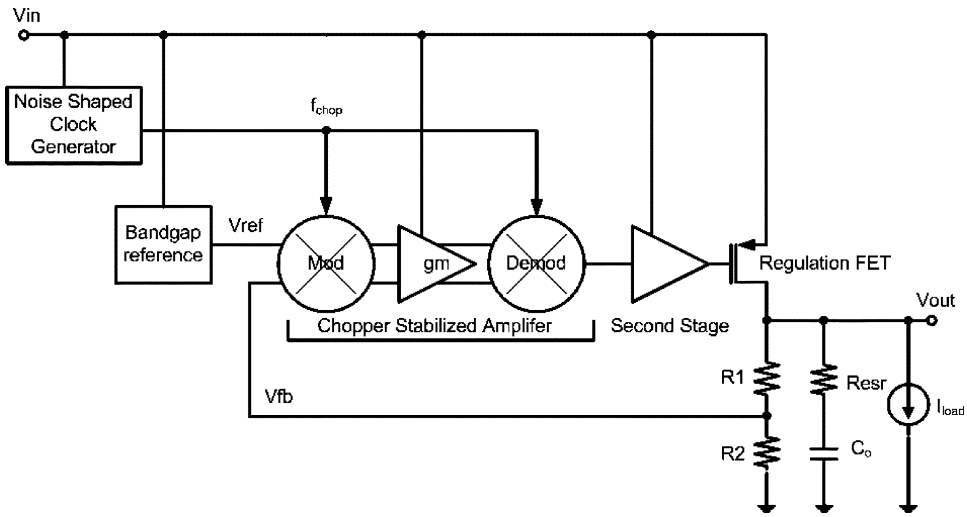


Fig. 5. Architecture of chopper stabilization LDO with noise shaped clock.

Therefore, the PSD of the control signal before bandlimiting can be represented by:

$$S_y(f) \approx |A_e(f)|^2 S_e(f) + |A_e(f)|^2 \sum_{k=-\infty}^{\infty} \left\{ \frac{4\left[S_n(f+(2k+1)f_c) + S_{os}(f+(2k+1)f_c)\right]}{|(2k+1)\pi|^2} \right\}. \quad (7)$$

After filtering provided by the Miller compensation and output load capacitance, the PSD of the output signal will contain only the amplified error signal with $1/f$ noise and offset pushed to chopping frequency, yielding

$$|S_o(f)| \approx |A_e(f)|^2 |S_e(f)| |g_{mo} Z_o(f)|^2 \quad (8)$$

where g_{mo} represents the regulation FET transconductance, and $Z_o(f)$ is the load impedance provided by the output impedance of the regulation FET, C_o and R_{esr}.

As seen from (4), the error amplifier should have sufficient gain to amplify the modulated error while rejecting the upconverted $1/f$ noise and DC offset components. The ripple filtering versus $1/f$ noise rejection is a trade-off for the chopper stabilized LDO. The reduction in gain due to chopping is compensated by a secondary current mode feedback (CFA) buffer amplifier, as discussed in the next section. The chopping frequency is three times the error amplifier cutoff frequency in this design.

III. Circuit Design

The proposed low noise LDO is composed of a digital noise shaped clock generator, a voltage reference, a chopper stabilized error amplifier, a current-feedback second stage, regulation FET, and feedback network. Fig. 5 shows the architecture of the proposed low noise LDO. The following sections describe the building blocks of the LN-LDO.

A. Error Amplifier

Fig. 6 shows the top level schematic of the chopper stabilized LDO with a CFA based second stage. A folded cascode amplifier is used as the first error amplifier, where input and output mixing is achieved with high speed NMOS passive mixers. The demodulation stage uses two choppers with opposite clock phasing, ensuring a valid output voltage at both clock edges. By imbedding the mixers across the low-impedance nodes of the folded cascode amplifier, the offset and noise due to rail devices M3/M4/M9/M10 shifts to higher frequencies [9]. Chopping at low impedance nodes of the folded cascode amplifier also enables a high chopping frequency without increasing overall power consumption.

Charge injection and parasitic coupling due to the chopping stages can result in residual offset and voltage ripple at the error amplifier output. Delaying the demodulation clock rising edge with respect to the modulation clock gives enough time for the amplifier to settle, minimizing the residual ripple at the amplifier output. An on chip clock generator is designed to ensure that the demodulation clock rising edge is delayed by $\tau_d = C_p/g_{m5,6}$ of the error amplifier with respect to the modulation clock, where C_p is parasitic pole at the drain node of M1,2. Falling edges of modulation and demodulation clocks can be aligned. If the chopping and de-chopping are not completely synchronized, due to phase shift and delay or non-ideal edges of the chopping clock, output ripple can increase dramatically. As an example, during the brief period where input is chopped, while output is not chopped yet, if the clock phasing is not correct the output can see a considerable transient jump. Also, higher frequency chopping clock may introduce higher ripple due to increased glitch energy. From the point of ripple contribution, the frequency of chopping clock is more dominant factor than non-synchronization.

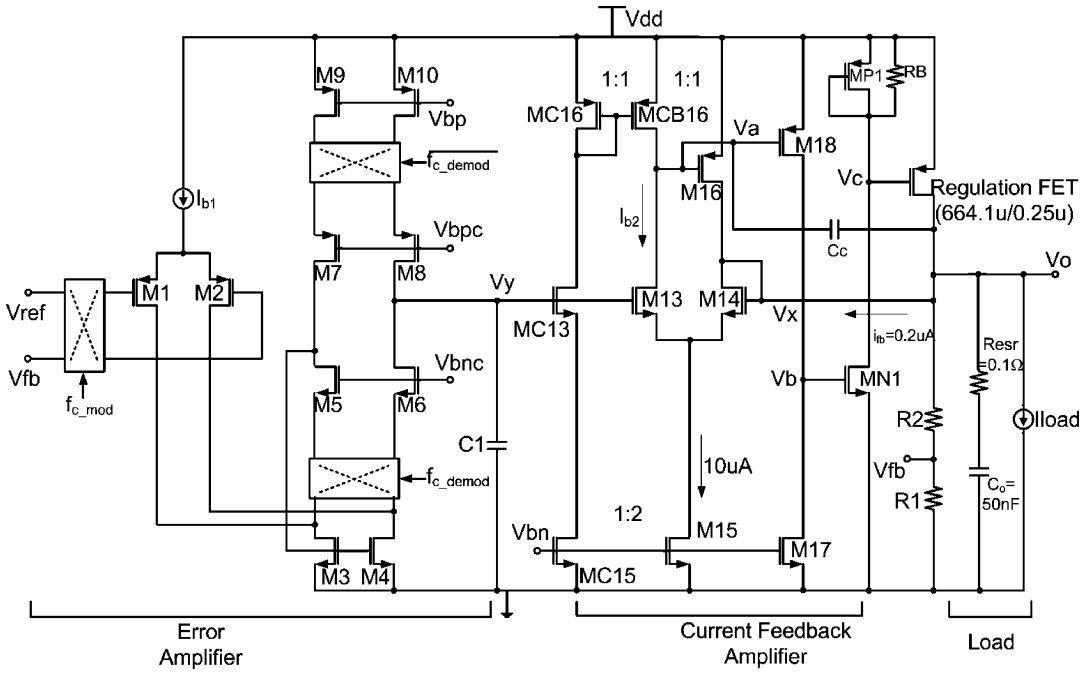


Fig. 6. Top level schematic of the chopper stabilized LN-LDO with CFA.

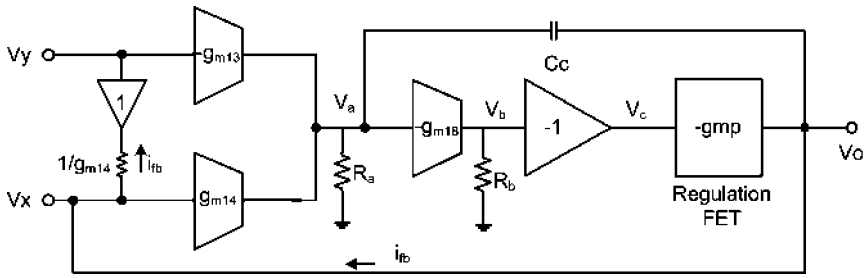


Fig. 7. Equivalent model of the second stage CFA.

B. Current Feedback Second

In order to minimize the impact of slew rate on settling time and improve the transient response of the LDO, a second stage CFA with an asymmetrical input stage is used to drive the regulation FET [13]. A similar CFA structure can be utilized as a stand-alone error amplifier, reducing the circuit complexity of the LDO. However CFA amplifier does not yield itself to chopper stabilization and its $1/f$ noise impact can be higher. The error voltage V_y at the output of the folded cascode error amplifier is connected to the gate input of the CFA, and feedback voltage V_x is connected to the diode connected input transistor M14. This connection ensures that there is no DC current drawn from the primary folded cascode error amplifier. The feedback current i_{fb} is nominally around 0.2 μA.

Fig. 7 shows the small signal operation of the second stage CFA. M13 acts as a source follower while M14 is a level shifter. Due to symmetry, the gate-source voltage of M13 and M14 are equal; therefore, the feedback voltage V_x follows the voltage V_y regardless of the feedback current i_{fb}. In closed loop operation, the feedback current i_{fb} is regulated by the loop formed by M14-M13-MCB16 and M16. M15 and M16 act as a current source ensuring $I_{d15} = 2 \cdot I_{b2}$. Impedance seen by the feedback signal V_x at the gate of the diode connected M14 is $g_{ds13}/(g_{ds13}g_{ds16} + g_{m13}g_{m16})$. The voltage mode loop gain of the secondary CFA is represented by:

$$\left.\frac{V_o}{V_x}\right|_{V_y=0} \approx \frac{-A_{CFA}\left(1+\frac{s}{\omega_{z1}}\right)\left(1-\frac{s}{\omega_{z2}}\right)}{\left[\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)\right]}$$

$$\omega_{p1} \approx \frac{1}{C_o r_{dsmp}}$$

$$\omega_{p2} = \frac{1}{C_c g_{m18} g_{mp} R_a R_b r_{dsmp}}, \quad \omega_{p3} = \frac{1}{C_p R_c}$$

$$\omega_{z1} = \frac{1}{C_o R_{esr}}, \quad \omega_{z2} = \frac{g_{m18} g_{mp} R_b}{C_c}$$

$$GBW = \frac{(g_{m13}R_a)\,(g_{m18}R_b)\,g_{mp}}{C_o} \tag{9}$$

where DC loop gain is $A_{CFA} \approx (g_{m13}R_a)(g_{m18}R_b)(g_{mp}r_{dsmp})$.

The dominant pole frequency of the CFA stage is ω_{p1}. The second dominant pole, ω_{p2}, is designed to cancel out with an LHP zero ω_{z1} by using local feedback capacitor C_c. RHP zero ω_{z2} is located at higher frequency than unity gain frequency. To ensure stability of the dual feedback system, the open-loop bandwidth of CFA is designed to be wider than the error amplifier. For the CFA the lineup for the bandwidths are $GBW < w_{z1} < w_{p3}$,.To achieve wider bandwidth for the CFA, a smaller output capacitor (C_o) value is utilized.

The bandwidth of the error amplifier is determined by C1, and its value is chosen so that the gain bandwidth of the error amplifier is around half the chopper frequency. This ensures that the chopped error signal has sufficient gain. Finally, transistors MN1 and MP1 form a buffer stage to push the parasitic pole associated with the regulation FET to high frequencies and improve PSR. Due to the diode connected to MP1, the quiescent current and speed of this stage is set by the V_{gs} (therefore the load current) of the regulation FET, achieving supply noise suppression [14]. With its low output impedance, CFA has much wider bandwidth compared to the global regulator unity gain frequency. The goal of the slow voltage mode loop is to set the output voltage at steady state and provide the steady state accuracy for the loop. The wider bandwidth current feedback loop is beyond the unity gain bandwidth of the global voltage mode loop, ensuring the stability of the regulator. The lineup for the bandwidths for overall system are $GBW_{err} < GBW_{CFA}$, where GBW_{err} is the bandwidth of error amplifier which is determined by C1. Therefore, system stability is always guaranteed.

There are two critical load transients that need to be considered for the CFA response. In case of a load current increase, feedback voltage V_x drops. Unlike a voltage mode feedback amplifier, the diode connected M14 preserves its gate-source voltage, moving the source voltage of M13 lower and responding with a fast decrease in node voltage V_a. This reduces the gate voltage of the regulation FET, enabling a fast response with minimum slew rate limiting, which is intrinsic characteristic of CFA. Compared to a VFA, ideal CFA does not suffer from slew rate limitation. Also, for a fixed current feedback loop-gain, their settling speed can be setup much faster, enabling faster regulation time at the gate of the regulation FET. In addition, using CFA in the proposed LDO generates low impedance at the output of LDO helps with stability of the regulator. In the opposite case, when the load current is reduced, the diode connected transistor M14 pulls the source of M13 higher, responding with a fast increase in node voltage V_a. This operation ensures a fast response in both transient conditions.

C. $\Sigma\Delta$ *Noise Shaped Clock Generator*

The tonal content from the chopping clock can appear at the output of the LDO due to clock feedthrough of the mixer switches [11]. Fig. 8 shows the typical output ripple for different chopping frequencies and load conditions using fixed chopping clock frequency. Using a noise shaped clock for the chopping mixers, the output noise of the LDO could be reduced further.

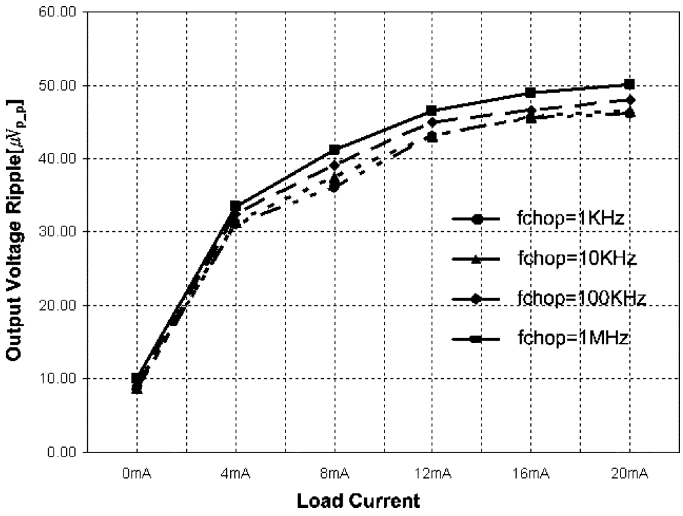


Fig. 8. Measured output ripple for various chopping frequencies (f_c) and loading conditions.

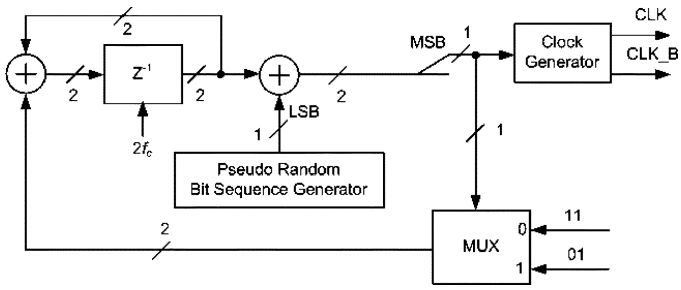


Fig. 9. Block diagram of noise shaped clock generator.

Fig. 9 shows the block diagram of the sigma-delta ($\Sigma\Delta$) noise shaped clock generator that is used for the proposed LN-LDO. The frequency shaped pseudo-random chopper signal generator circuit includes a digital first order $\Sigma\Delta$ modulator that is composed of a delay cell, two adders, a single-bit quantizer, and a MUX. The pseudorandom bit sequence generator is implemented using a shift register and generates $2^{14} - 1$ bit long random sequence. The single-bit pseudo-random signal functions as a dither input to the digital $\Sigma\Delta$ modulator. The MSB of the adder output functions as a single-bit digital quantizer. The quantizer output signal is connected to the control port of a MUX to generate a two's complement feedback signal, closing the $\Sigma\Delta$ modulator loop. Since the pseudo-random signal generator output is added inside the noise shaping loop, the single-bit quantizer output becomes a frequency shaped pseudo-random clock signal. The quantizer output is followed switches. The PSD of the pseudo-random signal generator can be represented by

$$S_{PN}(f) = \frac{1}{f_s}\left(\frac{\sin\left(\frac{\pi f}{f_s}\right)}{\frac{\pi f}{f_s}}\right)^2 \tag{10}$$

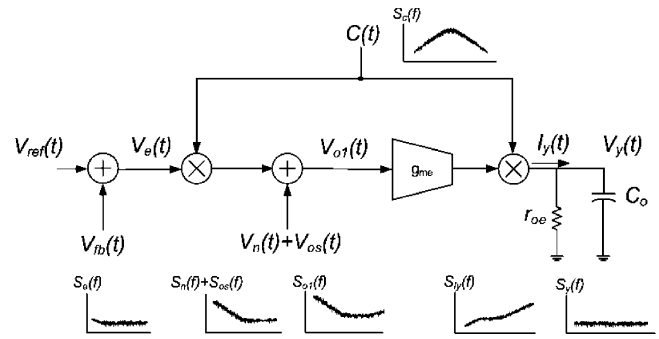


Fig. 10. Conceptual signal flow diagram and PSDs for noise-shaped chopper stabilized LN-LDO.

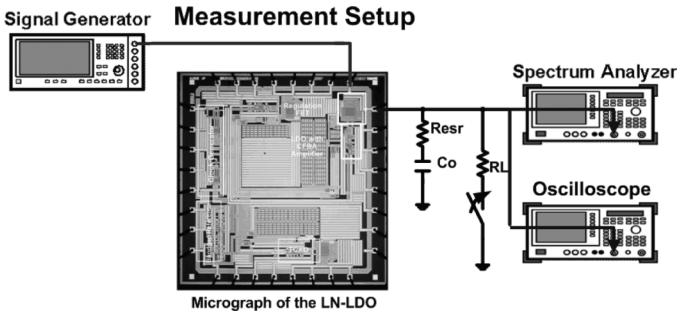


Fig. 11. Measurement setup for the output noise, PSR, and load regulation.

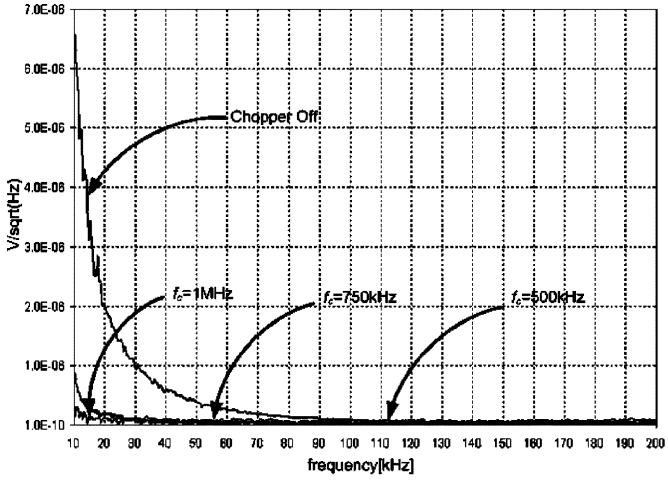
where f_s is sampling frequency of the shift register. After passing through the first order digital noise-shaper, the PSD of the noise-shaped chopping clock $S_{C,NS}(f)$ becomes

$$S_{C,NS}(f) = \left|1 - z^{-1}\right|^2 S_{PN}(f) = \frac{1}{f_s}\left|2\sin\left(\frac{\pi f}{f_s}\right)\right|^2 \left|\frac{\sin\left(\frac{\pi f}{f_s}\right)}{\frac{\pi f}{f_s}}\right|^2. \quad (11)$$

As seen from (10), the DC component of the clock is eliminated by high pass filtering provided by the first-order digital noise shaper, and fundamental and higher harmonics of the clock is spread over a broad frequency spectrum between DC to sampling frequency (f_s). The PSD of the error signal after noise shaped chopping becomes

$$|S_y(f)| \approx |A_e(f)|^2 S_e(f) + |A_e(f)|^2 (S_n(f) + S_{os}(f)) S_{C,NS}(f). \quad (12)$$

The peak power of the modulated noise and offset signal shows up at the half sampling frequency ($f_s/2$). Fig. 10 shows the conceptual signal flow diagram of the noise-shaped chopper stabilized LDO.



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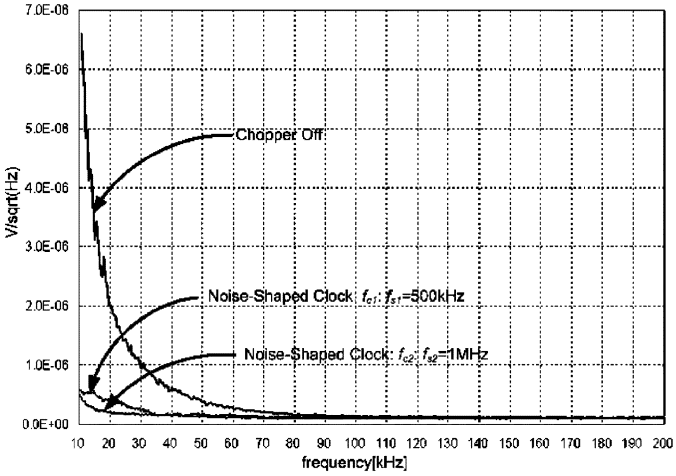

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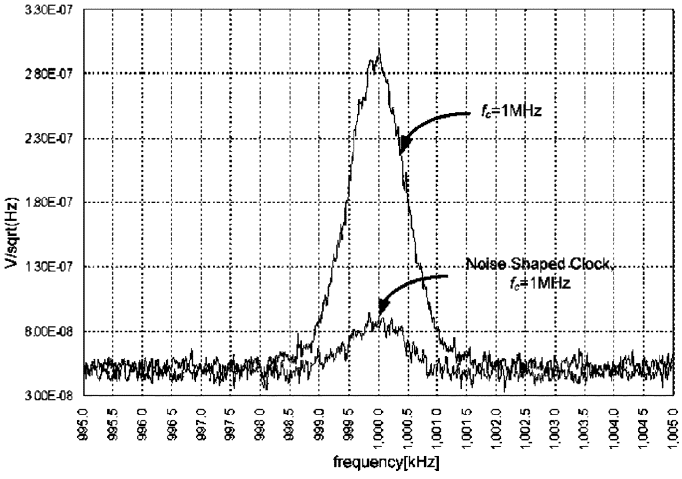

(c)

Fig. 12. (a) Measured LN-LDO output noise spectrum with different single-tone chopping frequencies (b) Measured LN-LDO output noise spectrum with various noise-shaped chopping frequencies, (c) Comparison of tone power at 1 MHz chopping frequency with RBW normalized from 1 kHz to 1 Hz.

IV. Experimental Results

The LN-LDO IC is designed and fabricated in a 0.25-μm digital CMOS process with five layers of metal. Three top metal

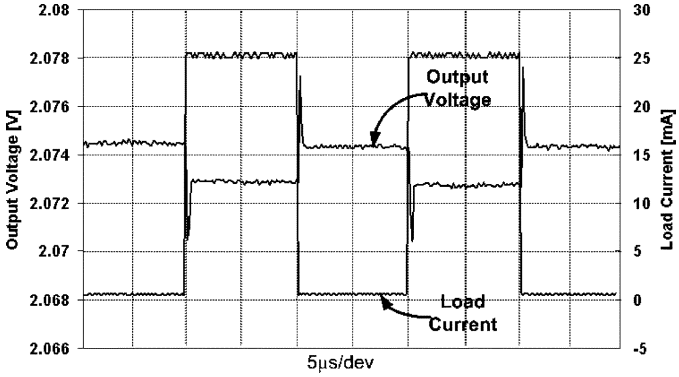

Fig. 13. Measured LN-LDO response to 25-mA load changes with $f_s/2 = 1$ MHz chopping frequency.

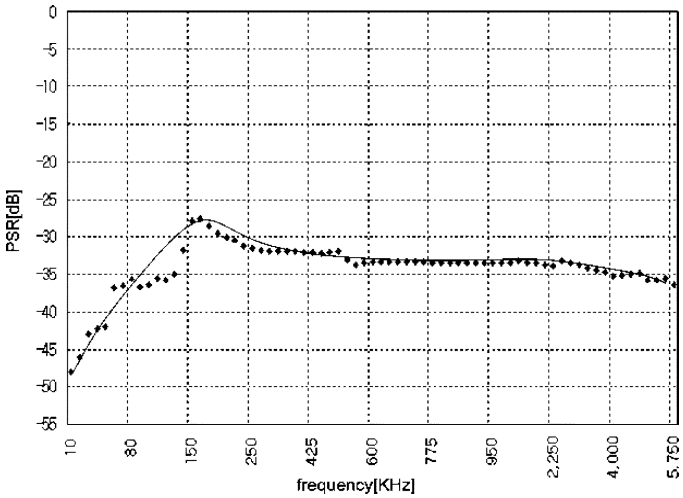

Fig. 14. Measured LN-LDO PSR at 25-mA load condition.

layers have been used for the power train of the regulation FET. The LDO is designed to source a nominal output current of 50 mA. With the help of chopping, input referred flicker noise specifications of the error amplifier have been relaxed by a factor of four. Spot noise power spectral density at 30 kHz is reduced by factor of four. Fig. 11 shows the measurement setup for the output noise, PSR, and load regulation of proposed LN-LDO. Output noise and PSR is measured at the full load condition. The output noise spectral density is measured to be 150 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 10 kHz and 32 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ at 100 kHz. Integrated noise from 1 kHz to 100 kHz with chopping is measured to be 14 $\mu\mathrm{V}_{\mathrm{rms}}$. Without chopping, the output noise is measured to be 122 $\mu\mathrm{V}_{\mathrm{rms}}$, largely dominated by $1/f$ noise. Fig. 12(a) and (b) shows the measured output noise spectrum for different chopping frequencies, and Fig. 12(c) shows the spot noise around the chopping clock at 1 MHz with and without noise shaping. By using a noise shaped chopping clock, $1/f$ noise and DC offsets at the chopping frequency is reduced by more than 12 dB. As shown in Fig. 13, the LN-LDO achieves 2 mV/25 mA load regulation. The LDO achieves 45 dB PSR at 30 kHz offset. Fig. 14 shows the PSR plot of the LN-LDO for different frequencies at 25-mA loading condition.

TABLE I
PERFORMANCE COMPARISON WITH RECENT PRIOR WORK

	[3]	[1]	[12]	[2]	**This work**
Year	1998	2003	2004	2005	**2006**
Process	2µm	0.6µm	0.5µm	90nm	**0.25µm**
Vin[V]	5	1.5~4.5	3.3	1.2	**2~2.5**
Vout[V]	3.3	1.3	2.8	0.9	**1.5~2**
C_o [F]	4.7u	10u	2.2u	0.6n	**50n**
ESR[ohms]	10	1	2.5	0.75	**0~0.1**
Response Time(us)	1.8us	2u	10u	0.54n	**0.6u**
Output noise [nV/√Hz]	-	70 @100kHz	1,360 @100kHz	-	**32 @100kHz**
Integrated output noise(μV_{rms})	-	-	936 @100K	-	**14 @100K**
I_{max}[mA]	50	100	100	100	**50**
I_Q[mA]	0.23	0.028	0.025	6	**0.120**
Current Efficiency [%]	99.5	99.96	99.975	94.3	**99.76**
PSR	-	26dB	20dB @50k	-	**>43dB @30k, >25dB @200k**

As described in Fig. 1, the LN-LDO output is connected to an integrated TCXO power supply in order to characterize the impact of supply noise on the oscillator phase noise. In this test, the proposed LN-LDO drives the TCXO with 32.767 MHz fundamental frequency at 2 V and the phase noise of the TCXO was measured with and without chopping. As seen in Fig. 15, with chopping enabled, the phase noise of the TCXO at 10 kHz offset is reduced by more than 15 dB. Overall noise floor is much lower for the 2 V LiIon battery operated case, however any other load on the same battery would increase overall noise floor due to lack of load regulation. Fig. 16 shows the die micrograph of the designed LDO, and Table I compares the proposed LDO regulator with respect to recently published linear regulators.

V. CONCLUSIONS

A low $1/f$ noise linear regulator with a fast transient response secondary current-feedback amplifier is presented. This is the first application of chopper stabilization and CFAs on linear regulators, enabling a 14 $\mu\mathrm{V}_{\mathrm{rms}}$ integrated output noise from 1 kHz to 100 kHz. In addition, $\Sigma\Delta$ digital noise shaping techniques on the chopping clock is implemented to spread $1/f$ noise accumulation at the chopping frequency. The second CFA stage also helped with a high PSR at a wide frequency band.

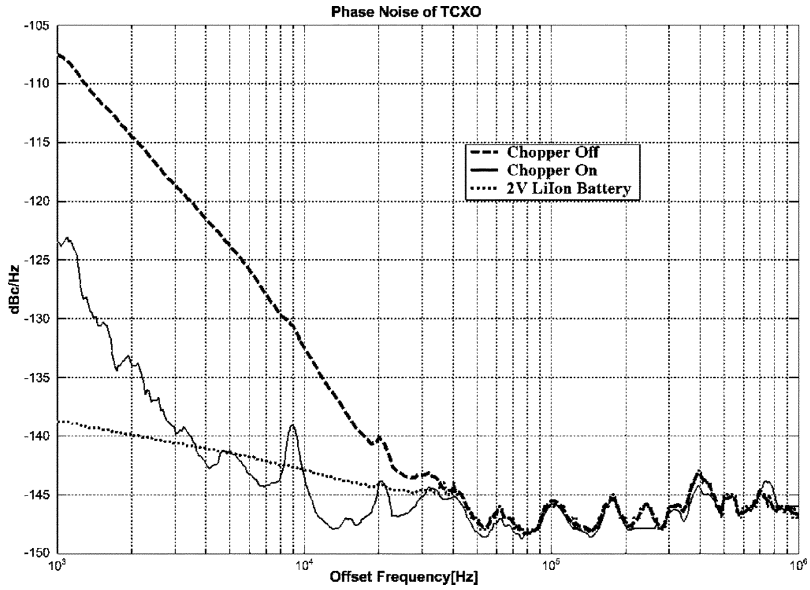

Fig. 15. Phase noise of a TCXO powered by the proposed chopping LDO versus 2 V LiIon battery and same regulator without chopping.

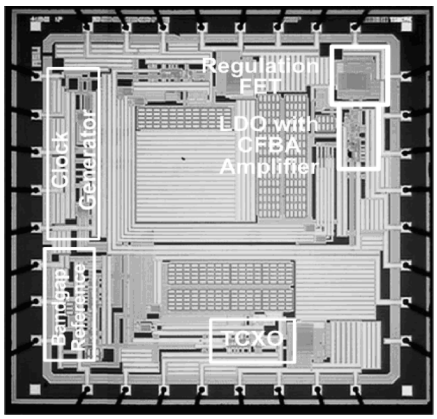

Fig. 16. Micrograph of the LN-LDO and associated circuits.

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