Capacitor-Less Dual-Mode All-Digital LDO With ΔΣ-Modulation-Based Ripple Reduction

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***Abstract*—This brief presents a capacitor-less digital low-dropout (DLDO) regulator, which has low steady-state voltage ripples (V_{RIPP}) and low output noise, suitable for driving analog circuits in system-on-chip devices. To reduce V_{RIPP}, a steady-state control based on ΔΣ modulation and a clock multiplication technique are proposed. Thanks to the ΔΣ operation, the proposed DLDO generates noise-shaped output voltage (V_{OUT}), reducing V_{RIPP} and improving its noise performance without using an output capacitor. The ΔΣ-modulator-based controller is activated just during the steady state, triggered by a lock detector, which continuously tracks V_{OUT} and compares it to a reference V_{REF}. During the steady state, a cyclic time-to-pulse converter and a clock combiner generate an oversampling clock for the controller. The proposed DLDO was fabricated in a 110-nm CMOS process with an active area of 0.07 mm^2. The measurement results demonstrate that at $V_{OUT} = 0.5$ V, $V_{DD} = 0.6$ V, and $I_{LOAD} = 500$ μA, the proposed DLDO achieves <1 mV of V_{RIPP}, 17.5 dB of power supply rejection (PSR) at 1 MHz, and −151 V^2rms/Hz (dB) of power-spectral density at 51.2 kHz. Furthermore, the proposed DLDO achieves 99.77% of current efficiency and 0.25 mV/mA of load regulation while driving the maximum I_{LOAD} of 40 mA.**

***Index Terms*—Digital low-dropout regulator (LDO), steady-state voltage ripples, power-supply rejection (PSR), capacitor-less, ΔΣ modulator, supply noise sensitivity.**

I. Introduction

LOW-DROPOUT regulators (LDOs) are crucial components in system-on-chip (SoC) devices for integrated power management and delivery due to their small voltage ripples, fast-transient response, high current efficiency, and small form factor. Conventionally, analog LDOs have been widely used to serve the purposes [1], [2]. As the latest SoC devices operate at near- or sub-threshold supply voltage levels, however, the performance of analog LDOs has degraded severely due to their in-sufficient gains of error amplifiers under low-voltage levels [3].

On the contrary, digital LDOs (DLDOs) maintain better performances under low-voltage conditions. Furthermore, DLDOs require less stringent stability requirements, and they are much more process-scalable than analog LDOs. Therefore, DLDOs [4]–[7] are considered more suitable to drive the digital load circuits in SoCs. However, even with substantial research and development on DLDOs so far, they are still considered the inferior alternative of analog LDOs in driving analog load circuits of SoCs [3], [8]. It is because most DLDOs inherently have large steady-state voltage ripples (V_{RIPP}) and output noises [9].

In this brief, we propose a DLDO with a ΔΣ-modulator-based controller to address typical DLDOs' shortcomings in V_{RIPP} and output noise. The remainder of this brief is organized as follows: Section II discusses V_{RIPP} of typical DLDOs and reviews recently proposed techniques for V_{RIPP} reduction. The overall architecture and circuits of the proposed DLDO are presented in Section III. The measurement results are demonstrated in Section IV, and finally, we conclude our paper in Section V.

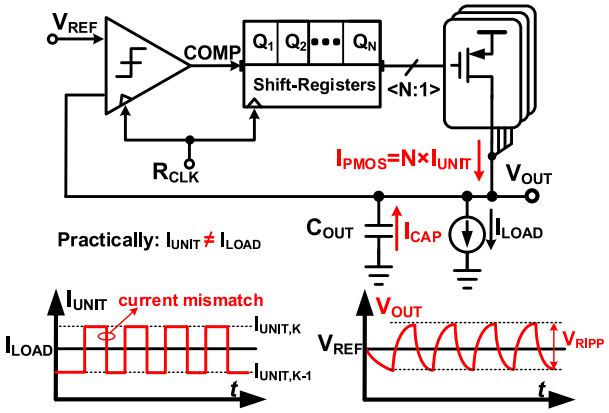

Fig. 1. Block diagram of typical DLDOs illustrating V_{RIPP} induced by the current mismatch between I_{PMOS} and I_{LOAD}.

II. Ripple Reduction Techniques in DLDOs

A block diagram of conventional DLDOs based on bi-directional shift-registers (BiSHRs) [10] is shown in Fig. 1. In

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the DLDO, a comparator senses the voltage difference between V_{REF} and V_{OUT} and generates the comparison output *COMP*. The level of *COMP* decides the shift direction of the BiSHRs, turning on/off the PMOS transistors to provide a matching current (I_{PMOS}) to I_{LOAD}. During the steady state, when $V_{OUT} \approx V_{REF}$, the LSB or a few LSBs of the BiSHRs continue toggling at the reference clock R_{CLK}, while repeatedly switching on/off the corresponding PMOS transistors. This creates voltage ripples V_{RIPP} at the output, and the amplitude and frequency components of V_{RIPP} are strongly related to various design parameters such as the control mechanism, R_{CLK}, the dropout voltage, and the PMOS sizing.

In many conventional DLDOs, the array of PMOS switches is composed of multiple PMOS switches of the same size in a thermometer fashion [4], [10], [11] as the structure shown in Fig. 1, or binary-sized PMOS switches [6], [7], [12]. In both cases, the switch sizes are discrete, so is the output current. The current mismatch between the switch array current I_{PMOS} ($= N \times I_{UNIT}$) and the load current I_{LOAD} should be compensated by I_{CAP} the current from C_{OUT} the output capacitor, while N is the number of turned-on PMOS transistors, as shown in Fig. 1. As a result, I_{CAP}, which is equal to the current mismatch, induces a voltage droop at V_{OUT}. After some period of time, the sign of the voltage difference changes, so the PMOS switches toggles. Then, it results in an opposite-sign I_{CAP}, which induces an opposite-sign voltage rail at V_{OUT}. As shown on the bottom of Fig. 1, these events are repeated continuously, creating a voltage ripple at the output.

There are trade-offs between V_{RIPP} and several design parameters. A smaller size of the unit PMOS switches can reduce V_{RIPP}, but typically slows down the transient response. Having a bigger output capacitor also can reduce V_{RIPP}, but at the cost of the area. The V_{RIPP} performance of a DLDO is typically degraded for slower R_{CLK}. Since the control loop operates at a slower R_{CLK}, it takes a longer time for V_{OUT} to charge/discharge C_{OUT}. Besides, V_{RIPP} gets larger substantially at light-load or no-load conditions where the current mismatch creates a larger ripple because of a larger load resistor at the output node. In addition, V_{RIPP} gets worse for larger dropout voltages (V_{DO}). The power transistors are in the triode region, and V_{DO} is the source-drain voltage of the transistors. Thus, as V_{DO} increases, the unit current (I_{UNIT}) increases. As a result, V_{RIPP} becomes larger. To sum up, V_{RIPP} is difficult to reduce for the cases with small or no C_{OUT}, small I_{LOAD}, slow R_{CLK}, and large V_{DO}.

Various techniques have been proposed for V_{RIPP} reduction in DLDOs [13]–[16]. A ripple-cancellation amplifier in [13] and a hybrid LDO in [14] were proposed to supply a sub-LSB current for V_{RIPP} mitigation, but at the cost of complex stability and large V_{DO}. A large V_{DO} inevitably results in a limited regulation range, so these hybrid architectures cannot operate at near-threshold-voltage (NTV) levels. The auxiliary PMOS switching based on the comparator output was proposed to reduce V_{RIPP} [15]. But, the sizing of the auxiliary PMOS switches is tricky to meet a wide range of conditions because it may affect the V_{OUT} accuracy. Moreover, its reported V_{RIPP} result was still not small enough (30 mV @ 500 μA). A ΔΣ modulator was adopted to do noise-shaping of V_{OUT}, achieving less than 1 mV V_{RIPP} at 3 mA of I_{LOAD} [16]. However,

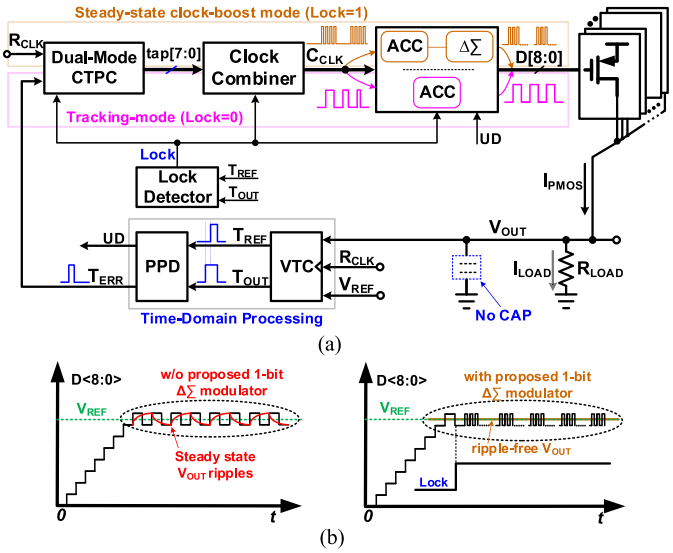

Fig. 2. (a) Detailed block diagram of the proposed DLDO, and (b) illustrations of a DLDO's steady-state behaviors with and without the proposed ΔΣ-modulator-based steady-state control.

such good performance was achieved with a large external C_{OUT} of 100 nF, which is not desired for SoC applications because of an additional pad and board area [3]. Therefore, there remains a critical need for a DLDO that achieves small voltage ripples even with a small or no output capacitor, slow operation clock, and moderate-sized PMOS switches.

III. Proposed Capacitor-Less DLDO

A. Overall Architecture

A detailed block diagram of the proposed capacitor-less DLDO is shown in Fig. 2 (a). It consists of a voltage-to-time converter (VTC), a phase and polarity detector (PPD), a dual-mode cyclic time-to-pulse converter (CTPC), a clock combiner, a lock detector, and a dual-mode power-switch controller that includes accumulators (ACCs) and a 1^{st}-order ΔΣ modulator. All these blocks are powered with the supply voltage (V_{DD}). The VTC generates a pair of pulses, T_{REF} and T_{OUT}, of which pulse widths are modulated according to the voltage levels of V_{REF} and V_{OUT}, respectively [12]. The following PPD, which is implemented with a tri-state PFD, generates a pulse signal T_{ERR} and a single-bit *UD*. The pulse width of T_{ERR} corresponds to the voltage difference between V_{REF} and V_{OUT}. *UD* is pulled high when T_{REF} precedes T_{OUT} in time. Otherwise, it becomes low.

The proposed DLDO operates in two modes: a tracking mode and a steady-state clock-boost mode. These two modes are determined by the lock detector. First, in the tracking mode ($Lock = 0$), T_{ERR} is digitized by the proposed dual-mode CTPC, while the ACC in the controller increments or decrements according to the level of *UD*. Then the 9-bit code $D[8:0]$ from the ACC is fed to the power switch array so that V_{OUT} is adjusted to be equal to V_{REF}. When $V_{OUT} \approx V_{REF}$ after multiple feedback-loop iterations, the pulse width of T_{ERR} becomes zero, and *Lock* the lock signal from the lock detector changes its polarity form low to high. *Lock* transits the mode of operation from the tracking mode to the clock-boost mode,

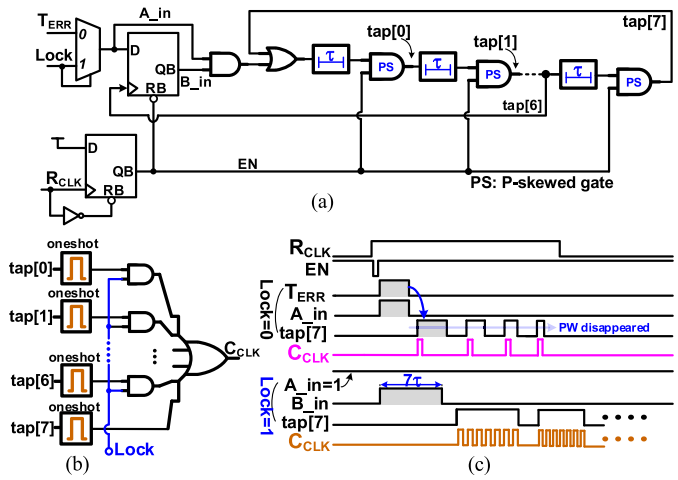

Fig. 3. Circuit diagrams of the proposed (a) cyclic time-to-pulse converter (CTPC) and (b) clock combiner. (c) Their operational waveforms during each of the mode, the tracking mode ($Lock = 0$) and the steady-state clock-boost mode ($Lock = 1$).

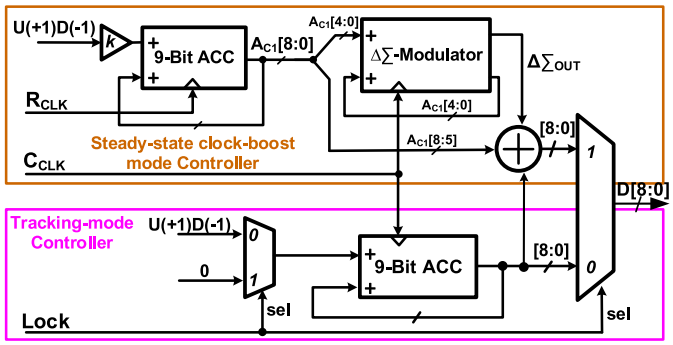

Fig. 4. Block diagram of the dual-mode power-switch controller.

which is the mode of operation during the steady state. The CTPC and clock combiner generates a boosted clock that is >128 times faster than R_{CLK}. Detailed operation about the two blocks is described in Section III-B. In addition, the $\Delta\Sigma$ modulator in the controller is activated and generates oversampled $D[8:0]$ at the boost clock C_{CLK}, thus noise-shaping V_{OUT}, as shown in Fig. 2 (b). The high-frequency noises at the noise-shaped V_{OUT} are filtered out by the parasitic capacitances of the power switch array at V_{OUT}. This significantly eliminates not only the voltage ripples but also the output noise.

The proposed DLDO exhibits a stable operation during both modes of operation. Because the proposed DLDO is output-capacitor-less, there is neither C_{OUT} nor its associated pole at the output node. More accurately, at the output, there is a parasitic capacitance (C_{PAR}), which is from 1) the switch array and 2) the load equivalent capacitance caused by the load circuitry. Because C_{PAR} is very small, the output pole associated with C_{PAR} is typically located at a much higher frequency than the unity-gain frequency. The only pole present in the small-signal analysis of the proposed DLDO is at the DC due to the accumulation in both tracking mode and steady-state clock-boost mode. Hence, the proposed DLDO behaves like a one-pole system which is inherently stable.

B. Cyclic Time-to-Pulse Converter and Clock Combiner

The proposed dual-mode CTPC and clock combiner generates C_{CLK} according to the mode of operation. Their circuit diagrams are shown in Fig. 3 (a) and (b), and waveforms of major voltage nodes for the two modes are illustrated in Fig. 3 (c) During the tracking mode ($Lock = 0$), T_{ERR} is fed to the CTPC loop through a multiplexer, as shown in Fig. 3 (a). The pulse width of T_{ERR} gets reduced by the P-skewed gates with every turn of the R_{CLK} as the pulse travels through the CTPC loop. After a few turns, the T_{ERR} pulse disappears. The number of turns is proportional to the pulse width of T_{ERR}. During this mode, only *tap*[7] is converted into one-shot pulses at the clock combiner, as shown in Fig. 3 (b). These one-shot pulses are then accumulated in the ACC in the power-switch controller to determine $D[8:0]$ the power-switch control bits. As the voltage error between V_{OUT} and V_{REF} decreases, the pulse width of T_{ERR} decreases. Thus, as it enters into the locking state ($V_{OUT} \approx V_{REF}$), the T_{ERR} pulse disappears. These key waveforms of the CTPC loop operation are illustrated on the top side ($Lock = 0$) of Fig. 3 (c).

In the steady-state clock-boost mode ($Lock$ = 1), the CTPC receives $Lock$ (= 1) as the input of the multiplexer instead of T_{ERR}, as shown in Fig. 3 (a). Then, a pulse of the maximum pulse width (width = 7τ) is generated at *B_in*. The CTPC continuously generates pulses at all the outputs *tap*[7:0], all of which are combined to a burst of clock pulses at the clock combiner. This clock burst (C_{CLK}), which is >128× faster than the system clock R_{CLK}, serves as the oversampling clock for $\Delta\Sigma$ modulation during the steady state.

C. Dual-Mode Power-Switch Controller

Fig. 4 shows detailed block diagram of the dual-mode power-switch controller, which consists of a 1^{st}-order $\Delta\Sigma$ modulator and two accumulators. The controller operates in the same two modes depending on the state of the lock signal *Lock*. When $Lock = 0$, the lower 9-bit ACC is activated only, and the upper ACC and the $\Delta\Sigma$ modulator are deactivated. This ACC counts the number of the turns of clocks C_{CLK} provided by the CTPC and controls the output $D[8:0]$. Once the lock becomes high ($V_{OUT} \approx V_{REF}$), the upper ACC and $\Delta\Sigma$ modulator are activated, controlling $D[8:0]$. The value of $+1$ and -1, indicating U(UP) and D(DN) at the input (Fig. 4), which is provided by the PPD at every cycle of R_{CLK}, is multiplied by a gain constant k and accumulated in the 9-bit ACC. The gain k, which is implemented with a shift register, is programmable from ×1 to ×16. The ACC output is split into the MSB 4 bits ($A_{C1}[8:5]$) and the LSB 5 bits ($A_{C1}[4:0]$). The LSB bits $A_{C1}[4:0]$ are fed to the $\Delta\Sigma$ modulator and are converted into a 1-bit $\Delta\Sigma$ bit stream ($\Delta\Sigma_{OUT}$) at the output. This bit toggles at C_{CLK}, which is the boosted clock synthesized from the CTPC. This scheme provides an oversampling ratio greater than 128 to the $\Delta\Sigma$ modulator. The modulated bitstream increases the resolution and accuracy of V_{OUT} during the steady state. Thus, the proposed DLDO can achieve significantly reduced V_{RIPP}, as compared to typical DLDOs.

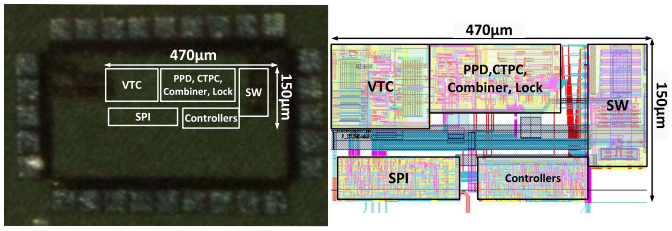

Fig. 5. Chip micrograph and layout.

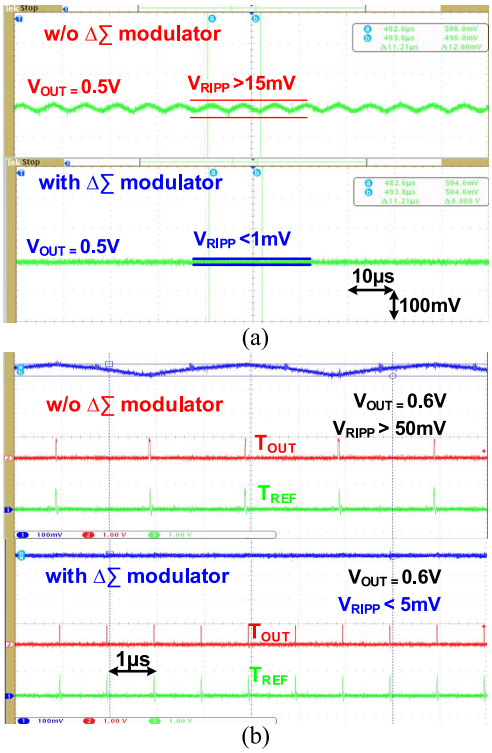

Fig. 6. Oscilloscope screen captures showing V_{RIPP} of the DLDO with and without using the ΔΣ-modulator-based ripple reduction technique at (a) V_{OUT} = 0.5 V, V_{DD} = 0.6 V, I_{LOAD} = 500 µA, and (b) V_{OUT} = 0.6 V, V_{DD} = 0.9 V, I_{LOAD} = 500 µA.

IV. Measurement Results

The proposed capacitor-less dual-mode DLDO was fabricated in a 110-nm CMOS process. It occupies an active area of 0.07 mm^2, as shown in Fig. 5. The proposed DLDO is designed to produce V_{OUT} in the range of 0.5 – 1.1 V from a V_{DD} of 0.6 – 1.2 V while driving I_{LOAD} in the range of 500 µA to 40 mA.

A V_{RIPP} performance comparison of the DLDO with and without using the proposed ΔΣ modulation is shown in Fig. 6 (a), where V_{DD} = 0.6 V, V_{OUT} = 0.5 V, and I_{LOAD} = 500 µA. As shown, V_{RIPP} is reduced by 92% from >15 mV to <1 mV by using the proposed technique. At a large V_{DO} of 300 mV, V_{RIPP} is increased to more than 50 mV without using the proposed technique, as shown in Fig. 6 (b). After applying the proposed technique, V_{RIPP} is maintained below 5 mV. Fig. 7 shows Fast-Fourier Transform (FFT) of the V_{OUT} before and after using the proposed ΔΣ-modulation-based control at V_{DD} = 1.2 V, V_{REF} = 1.05 V,

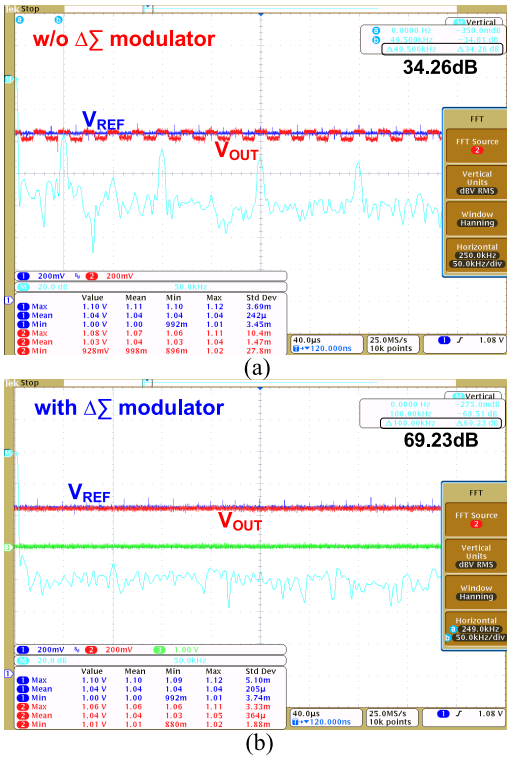

Fig. 7. Oscilloscope screen captures showing the Fast-Fourier Transform (FFT) of V_{OUT} (a) without using the proposed ΔΣ modulator, and (b) with the proposed ΔΣ modulator.

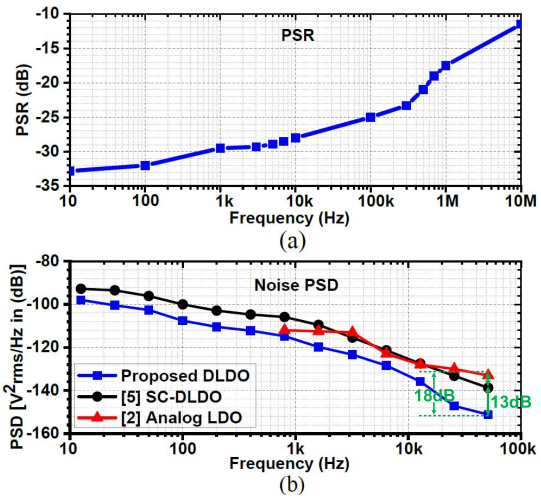

Fig. 8. Measured (a) power supply rejection (PSR), and (b) noise PSD performances of the proposed DLDO.

I_{LOAD} = 500 µA. As shown in Fig. 7 (a), V_{OUT} includes an oscillating ripple when the proposed technique is not applied. The Fast-Fourier Transform (FFT) waveform shows that there are a tone of −34.26 dBc (compared to the DC signal) at 49.5 kHz and its harmonics. When the proposed ripple-reduction technique is applied, as shown in Fig. 7 (b), almost all the tones are gone, resulting in a spurious-free range of 69.23 dB.

Measured power supply rejection (PSR) and noise power spectral density (PSD) the proposed DLDO are shown in

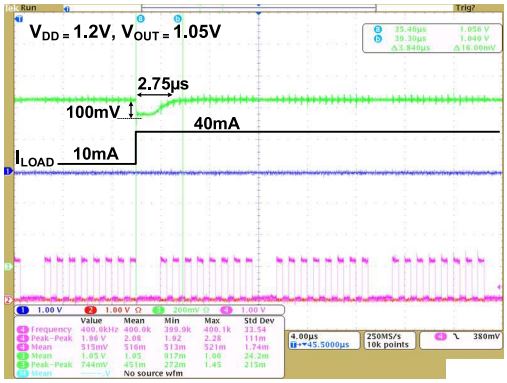

Fig. 9. Oscilloscope screen capture demonstrating the measured load transient response of the proposed capacitor-less DLDO. The load current was changed from 10 mA to 40 mA.

TABLE I
PERFORMANCE COMPARISON OF THE PROPOSED DLDO WITH STATE-OF-THE-ART DLDOS

Parameters	This Work	[4]	[8]	[12]	[13]
Process [nm]	110	130	40	110	180
V_{DD} [V]	0.6 – 1.2	0.5 – 1.2	0.6	0.6 – 1.2	1.43 – 2.0
V_{OUT} [V]	05 – 1.1	0.45 – 1.14	0.4	0.5 – 0.9	1 – 1.57
$I_{LOAD,MAX}$ [mA]	40	4.6	200	80	100
C_{OUT} [nF]	Cap-free	1	Cap-free	1	Cap-free
V_{RIPP} [mV]@ I_{LOAD} [mA]	< 1@0.5	10@1.4	8@0.1	4@80	2@10
PSR [dB]	17.5@1MHz	5@1MHz	16@1MHz	N. R	10@40kHz
ΔV_{OUT}[mV]@ΔI_{LOAD}[mA]	100@30	90@1.4	N. R	53@80	400@80
Load Reg. [mV/mA]	0.25	< 10	0.08	0.3	0.01
I_Q [µA]	94	751	25.1	12 – 32	1000
Current Efficiency [%]	99.77	98.30	99.99	99.97	99.11
FOM [ps]	0.021	34500	N. R	0.26	N. R
Area [mm^2]	0.07	0.114	0.0375	0.04	0.697

FOM = $(C_{OUT}\times\Delta V_{OUT})\times(I_Q)/(\Delta I_{LOAD})^2$
In this work C_{OUT} = 0. Therefore, parasitic capacitances are estimated for FOM calculation. $C_{PAR} \leq$ 2pF.

Fig. 8. For a switching noise of 200 mV (0.6 V - 0.8 V) on V_{DD} at 1 MHz of noise frequency, the proposed DLDO exhibits 17.5 dB of PSR while supplying 500 μA of I_{LOAD} at V_{OUT} = 0.5 V. Also, the noise PSD of the proposed DLDO is measured in the range of 10 Hz to 100 kHz at the same operating condition. As shown in Fig. 8 (b), the proposed DLDO exhibits PSD of -98 and -151 V^2_{rms}/Hz (in dB) at 12.5 Hz and 51.2 kHz, respectively. The measured PSD of the proposed DLDO is compared with a state-of-the-art DLDO [5] and an analog LDO [2] in Fig. 8. As shown, the proposed DLDO achieves 13-dB and 18-dB better PSDs than [5] and [2], respectively, at 51.2 kHz.

Fig. 9 shows a measured load transient response of the proposed capacitor-less DLDO (V_{OUT} = 1.05 V, V_{DD} = 1.2 V, ΔI_{LOAD} = 30 mA (10 mA - 40 mA) and R_{CLK} = 500 kHz). As shown, the proposed DLDO recovers from an undershoot of 100 mV within 2.75 μs. The proposed DLDO consumes 94 μA of quiescent current while driving 40 mA of I_{LOAD}, thus achieving a current efficiency of 99.77%. The measured load regulation of the DLDO is 0.25 mV/mA. The performance summary and comparison with state-of-the-art DLDOs are given in Table I. The proposed DLDO outperforms in V_{RIPP}, PSR, and the figure-of-merit (FOM).

V. CONCLUSION

We presented an all-digital capacitor-less LDO with a steady-state ripple reduction technique based on clock multiplication and $\Delta\Sigma$ modulation for small V_{RIPP}. The proposed clock multiplication and $\Delta\Sigma$-modulation-based control are activated on demand by the lock detector during the steady state only. The measurement results show the minimum V_{RIPP} of $<$ 1 mV and PSR of 17.5 dB at 1 MHz. Furthermore, we showed that the DLDO outperforms recent DLDOs in V_{RIPP}, PSR, and FOM.

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