LDO Design

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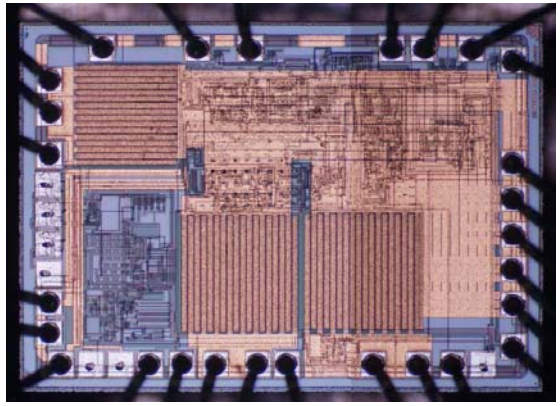
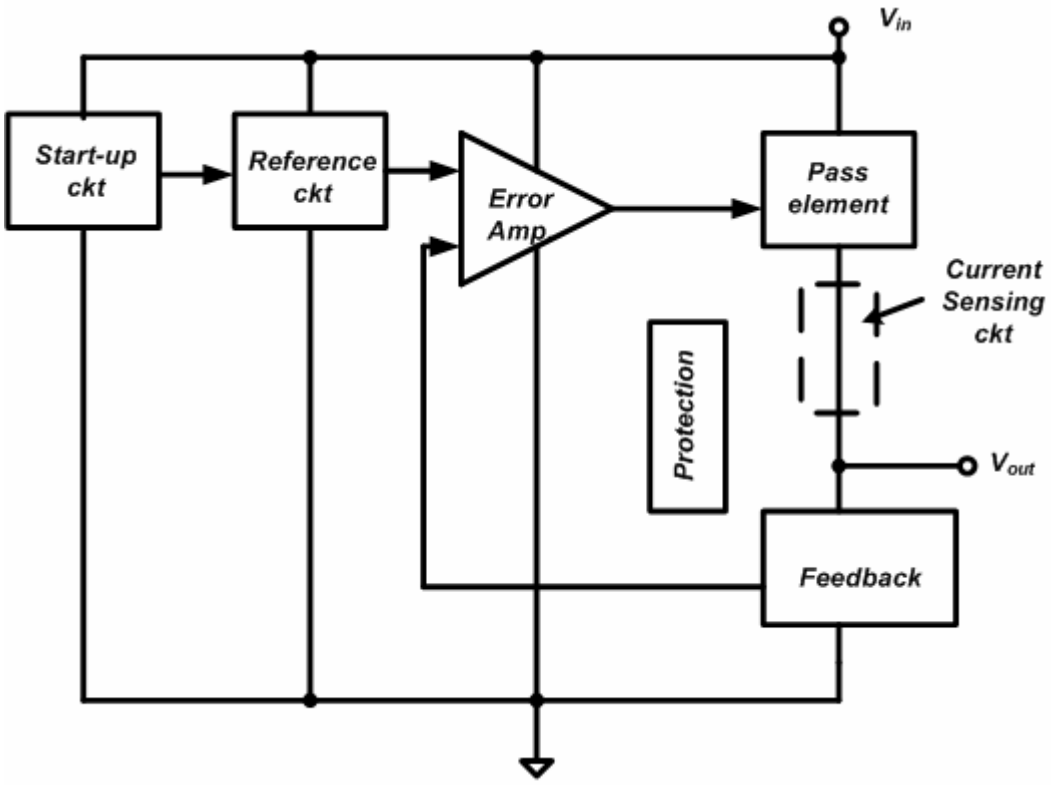
LOW DROP-OUT REGULATORS

- Low-power-consumption LDO have been developed to increase the lifetime of battery effectively
  - When the LDO is implemented in CMOS technologies, the low-ground-current feature is an advantage to portable applications
  - These circuits operate under lower voltage condition
  - High current efficiency become necessary to maximize the lifetime of the battery



Characteristic

- Block Level Description –
  - Start-up circuit
  - Reference
  - Protection circuit
  - Current sense element
  - Error amplifier (EA)
  - Pass element
  - Feedback network



Specifications

- Drop-out voltage
- Line regulation
- Load regulation
- Tolerance over temperature
- Output voltage variation resulting from transient load-current step
- Output capacitor and ESR range
- Quiescent current flow
- Maximum load current
- Input/output voltage range

$$V_{drop-out} = I_{Load} R_{on}$$

$$Line-regulation = \frac{\Delta V_o}{\Delta V_S}$$

$$Load-regulation = \frac{\Delta V_o}{\Delta I_L} = \frac{R_{o-pass}}{1+A\beta}$$

$$TC = \frac{1}{V_o}\frac{\partial V_o}{\partial T_{emp}} \approx \frac{1}{V_o}\frac{\Delta V_{TC}}{\Delta T_{emp}}$$

$$= \frac{[\Delta V_{TC,ref} + \Delta V_{TC,V_{os}}]\frac{V_o}{V_{ref}}}{V_o \Delta T_{emp}}$$

$$\Delta V_{tr} = \frac{I_{load-\max}}{C_o + C_b}\Delta t + \Delta V_{esr}$$

$$Accuracy_{system} = \frac{V_{o(\max)} - V_{o(\min)}}{V_o}$$

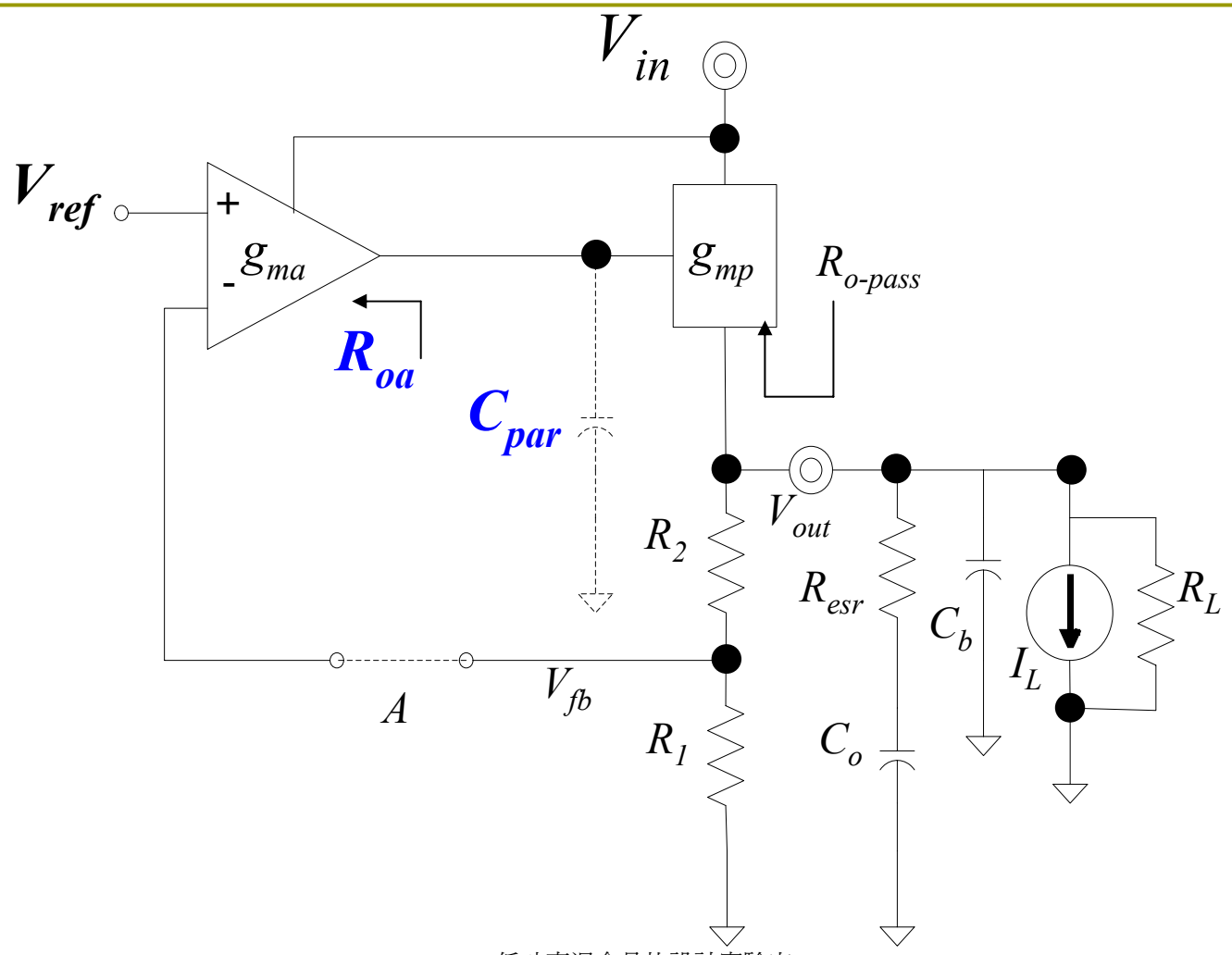
$$V_{o-\min} \le \Delta V_{LNR} + \Delta V_{LDR} + \Delta V_{TC} + \Delta V_{tr} + V_{refrence}\left\langle \frac{V_o}{V_{ref}} \right\rangle \le V_{o-\max}$$

$$V_{refrence} = V_{ref} + \Delta V_{TC_{ref}} + \Delta V_{LNR_{ref}} \pm V_{os}$$

System Design Considerations

- Enhance performance of LDO regulators for battery powered electronic
  - Low quiescent current flow for increase battery life
  - Low voltage operation
  - High output current
- The intrinsic issues in design :
  - Stability
  - Maximum output current
  - Regulating performance
- Analysis
  - AC Analysis
  - Transient Analysis

System Model under Loading Conditions



Frequency Response

$$\frac{V_{fb}}{V_{ref}} = |A_v| = \frac{g_{ma} R_{oa} g_{mp} Z}{\left[1 + sR_{oa}C_{par}\right]} \times \frac{R_1}{\left[R_1 + R_2\right]}$$

$$Z = R_X \parallel \frac{1 + sR_{esr}C_o}{sC_o} \parallel \frac{1}{sC_b}$$

$$= \frac{R_X\left[1 + sR_{esr}C_o\right]}{s^2 R_X R_{esr} C_o C_b + s\left[R_X + R_{esr}\right]C_o + sR_X C_b + 1}$$

$$R_X = R_{o-pass} \parallel (R_1 + R_2)$$

If $C_o \gg C_b$ (Typical condition)

$$Z \approx \frac{R_X\left[1 + sR_{esr}C_o\right]}{\left[1 + s(R_X + R_{esr})C_o\right] \cdot \left[1 + s(R_X \parallel R_{esr})C_b\right]}$$

$R_1 + R_2 \gg R_{o-pass}$ (Especially at high current)

$$\Rightarrow R_X \approx R_{o-pass}$$

- g_{ma} and g_{mp} refer to the transconductance of the amplifier and the pass element respectively
- R_{oa} is the output resistance of the amplifier
- C_{par} refers to the parasitic capacitance introduced by the pass element
- Z is the impedance seen at V_{out}

Frequency Response (cont'd)

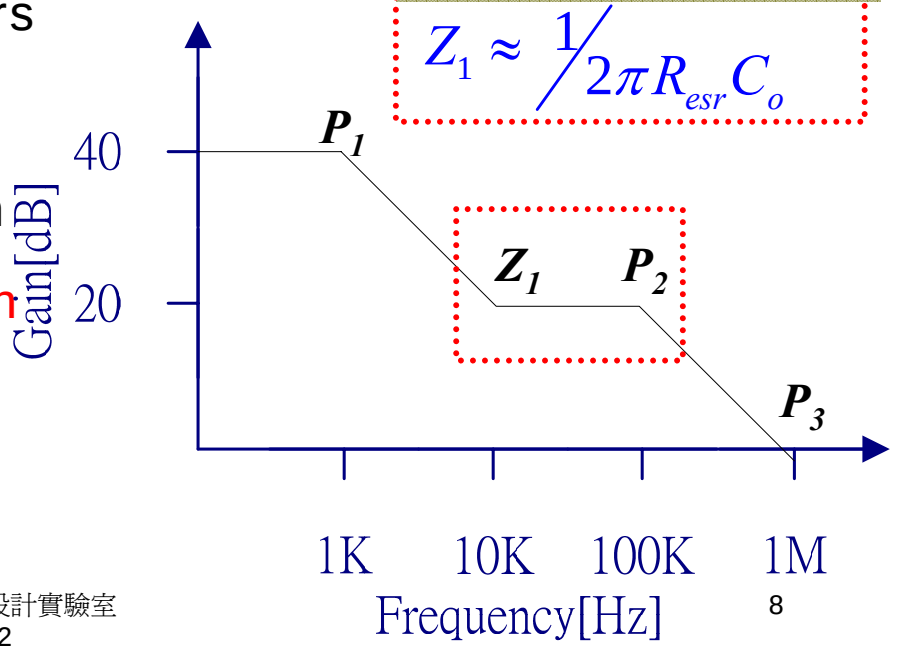
- In a conventional LDO, ESR of output capacitor generates this zero to guarantee phase margin better than *45* degrees
- The ESR is not properly specified and varies with temperature
- The high-frequency bypass capacitors placed in parallel with the output capacitor form a pole further decrease the phase margin
- Ceramic capacitors are cheaper than tantalum capacitors, but ESR of ceramic capacitors typically less than *50m Ω*
- ESR increases the overshoot drastically if large resistors are used

$$P_1 \approx 1/2\pi R_{o-pass} C_o$$

$$P_2 \approx 1/2\pi R_{esr} C_b$$

$$P_3 \approx 1/2\pi R_{oa} C_{par}$$

$$Z_1 \approx 1/2\pi R_{esr} C_o$$

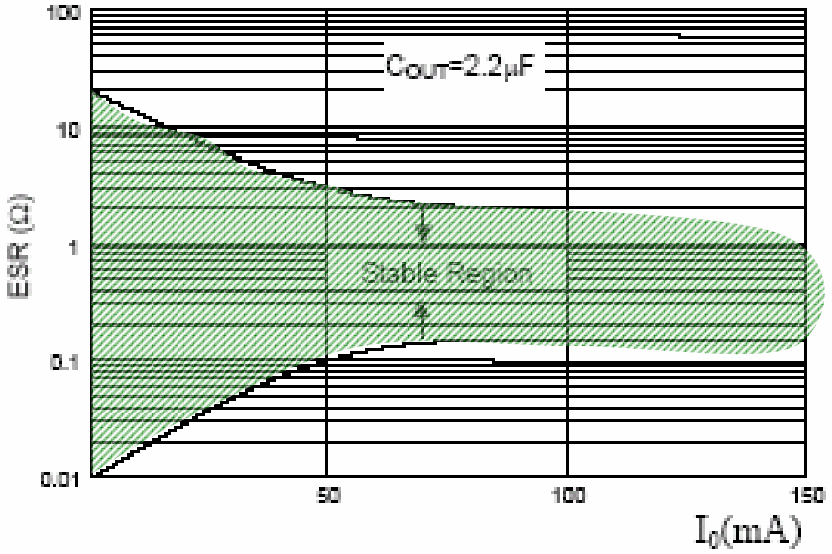


Design Challenge

- The worst-case stability condition arises when the phase margin is at its lowest point (UGF goes high)
  - This happens when the load-current is at its peak value
- P_1 increases at a faster rate than *the gain of the system decrease*
- The type and value of the output capacitor determine the location of P_1, P_2, and Z_1

$$\uparrow\uparrow \quad P_1 = \frac{1}{2\pi R_{o-pass} C_o} \propto \lambda I_o \propto I_o$$

$$\downarrow \quad \text{Gain} = g_{mp} R_{o-pass} \propto \sqrt{I_o} \times \frac{1}{\lambda I_o} \propto \frac{1}{\sqrt{I_o}}$$



Parasitic Pole Requirements

- The parasitic pole of the system can be identified as P_3 and the internal poles of the error amplifier
  - Requirement：parasitic pole must be greater than UGF
  - Ensuring that P_3 is at high frequencies is an especially difficult task to undertake *in a low current environment*
- The pole is defined by
  - The large parasitic capacitance (C_{par}) resulting from a large pass device
  - The output resistance of the amplifier (R_{oa})
- Low quiescent current and frequency design issues have conflicting requirements that necessitate compromises

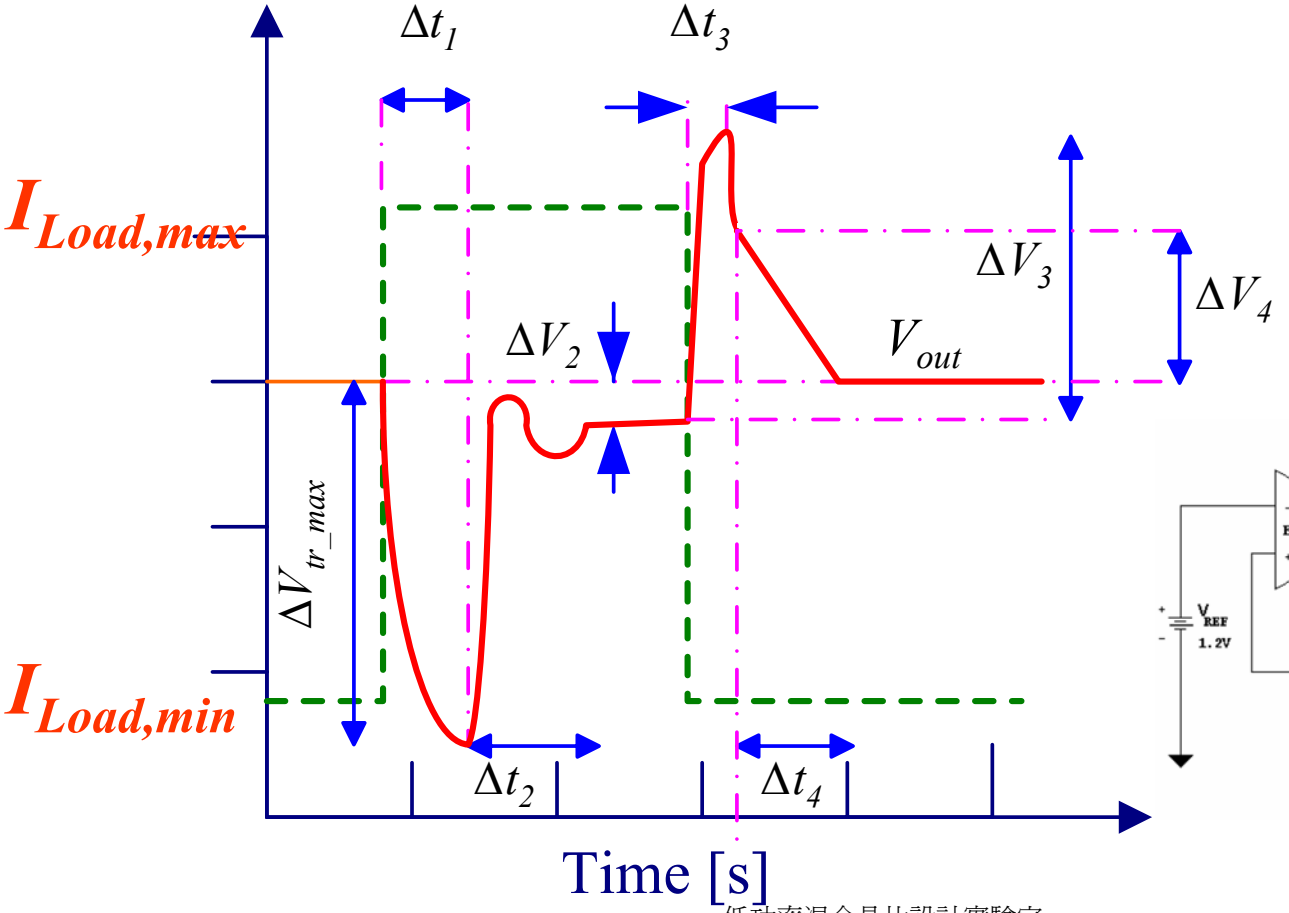
Maximum Load Regulation Performance

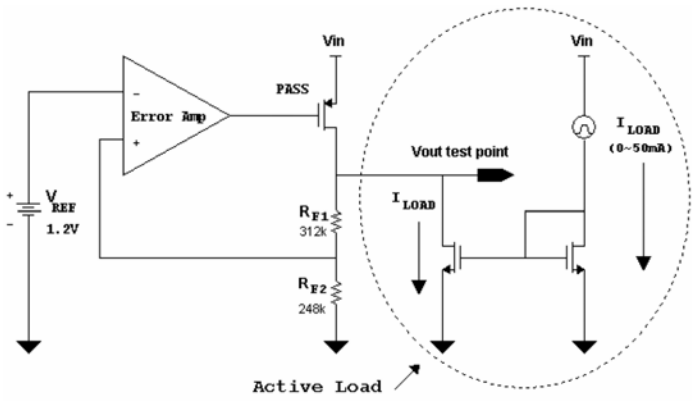
- Load regulation performance is a function of the open-loop gain of the system and can be expressed as:

$$R_o = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}$$

- The regulator yields better load regulation performance as the open-loop gain increases
  - The gain is limited by the closed-loop bandwidth of the system
    - ***The closed-loop bandwidth is equivalent to the open-loop UGF***
  - The worst-case condition occurs when Z_1 is at low frequencies and P_2 is at high frequencies
    - Which corresponds to the maximum value of ESR and the lowest bypass capacitance C_b

Typical LDO Transient Response to a Load-current Step





Transient Analysis: Typical response

- The worst-case time (Δt_1) required for the loop to respond is specified by $\Delta V_{tr\text{-}max}$, which is a function of C_o , ESR of C_o , C_b , and $I_{Load\text{-}max}$

$$\Delta V_{tr-\max} \approx \frac{I_{Load-\max}}{C_o + C_b} \Delta t_1 + \Delta V_{esr}$$

$$\Delta t_1 \approx \frac{[C_o + C_b]}{I_{Load-\max}} \left[\Delta V_{tr-\max} - \Delta V_{esr} \right]$$

Typical Response (cont'd)

- Δt_1 is not only a function of bandwidth but also defined by the internal slew-rate associated with the parasitic capacitance C_{par} of the pass element

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V}{I_{sr}} = 2\mu + 20\mu = 22\mu$$

  - Where BW_{cl} is the closed-loop bandwidth of the system, t_{sr} is the slew-rate time associated with C_{par}, ΔV is the voltage variation at C_{par}, and I_{sr} is the slew-rate limited current
- For instance, if BW_{cl} is 500kHz, C_{par} is 200pF, ΔV is 0.5V, I_{sr} is $5\,\mu$A, C_o is $10uF$, R_{esr} is 0, and $I_{load\text{-}max}$ is 100mA
  - The maximum output voltage variation is approximately 220mV

Typical response (cont'd)

- Once the slew-rate condition is terminated, the output voltage recovers and settles to its final value

$$\Delta V_2 \approx R_{o-reg} I_{Load-\max}$$

  - $R_{o\text{-}reg}$ is the closed-loop output resistance of the regulator
- The settling time (Δt_2) is dependent on
  - The time required for the pass device to fully charge the load capacitors
  - The phase margin of the open-loop frequency response

Transient Analysis

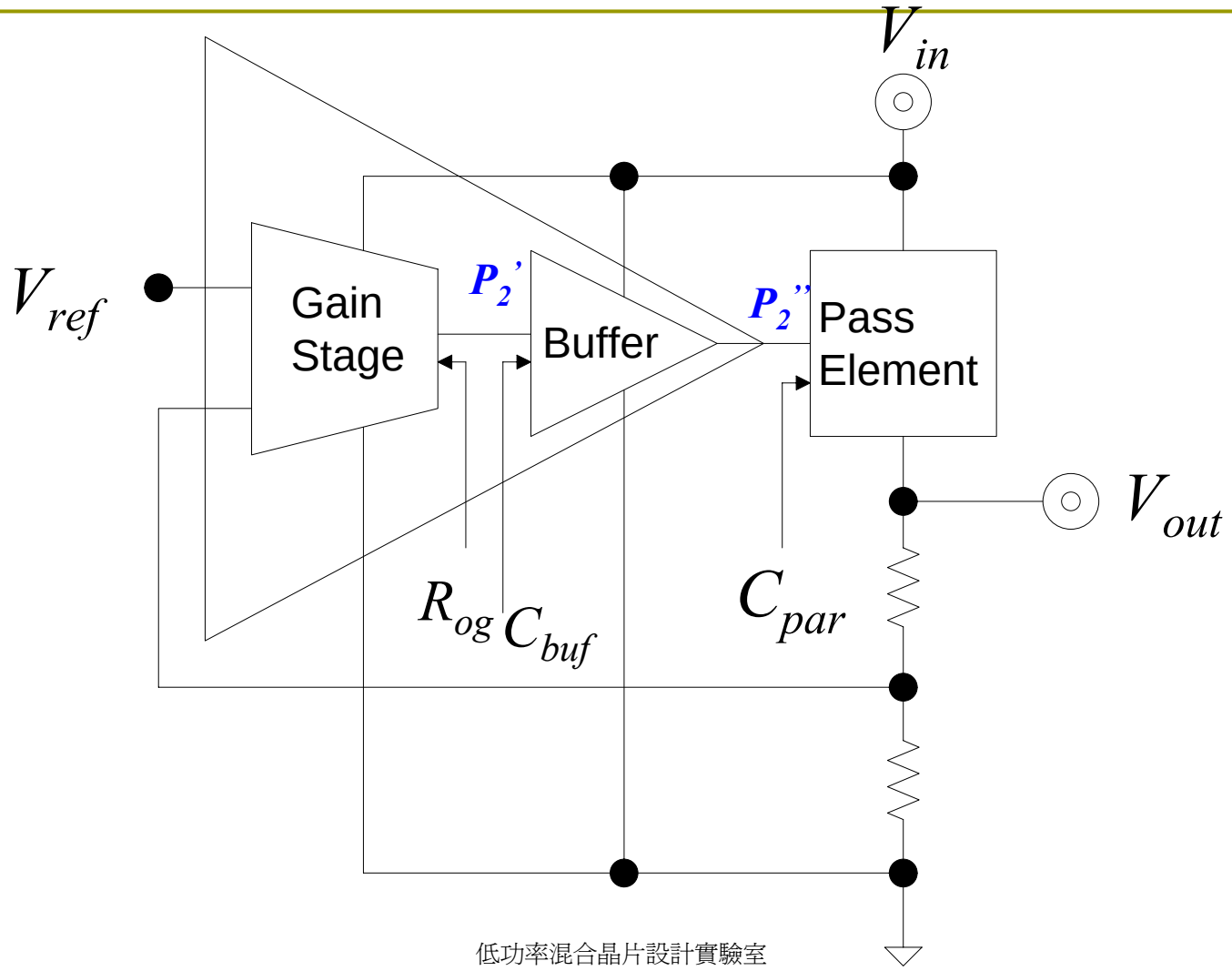
- The momentary current supplied by the power device ($I_{Load\text{-}max}$ until the circuit reacts to shut it off) flows to the output capacitor C_o and the C_b (the current is no longer flowing to the load)
  - Consequently, the capacitors charge up and a temporary voltage drop is created across R_{esr}

$$\Delta V_3 \approx \frac{I_{Load-\max}}{C_o + C_b}\Delta t_3 + \Delta V_{esr} \approx \frac{I_{Load-\max}}{C_o + C_b}\cdot\left(\frac{1}{BW_{cl}} + t_{sr}\right) + \Delta V_{esr}$$

- When the output transistor is finally shut off (after Δt_3) the variation settles down to ΔV_4 , the voltage charged on the capacitors ($\Delta V_4 \approx \Delta V_3 - \Delta V_{esr}$)

$$\Delta t_4 \approx \frac{C_o + C_b}{I_{pull-down}}\Delta V_4 = \frac{[C_o + C_b]R_1}{V_{ref}}\Delta V_4$$

Amplifier Design Issues



Performance Enhancements

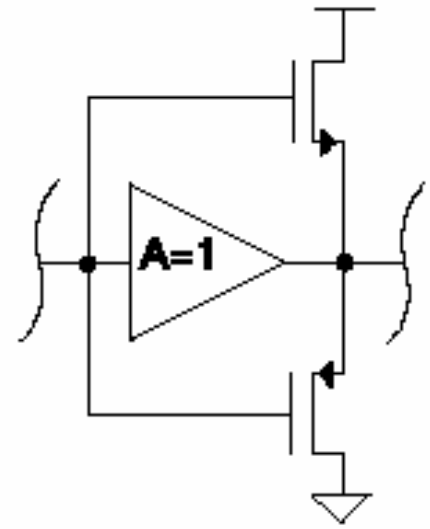
- Enhancing performance without incurring significant costs in quiescent current or voltage headroom benefit the overall design of LDOs
  - Current Efficiency → Quiescent current flow (must be low)
  - Current Boosting → Maximum output current capabilities
  - Load Regulation → Regulation performance

Current Efficiency

- $$Efficiency_{current} = \frac{I_{Load}}{I_{Load} + I_q}$$
- The limitation of current efficiency of low drop-out regulators are maximum load-current and transient output voltage variation
  - They typically require more I_q for increased performance
- Maximum output current and low input voltage affect the characteristics of the pass element which defines the I_q requirement of the error Amp
- When the maximum load-current specification increases
  - The size of the pass devices ↑
  - The EA's load capacitances ↑
  - Phase-margin ↓ (P_3 ↓)
  - The stability ***is compromised*** unless the output impedance (R_{oa}) of the EA is reduced accordingly → **more I_q**

Slew-Rate Dependent Boost Circuit

- Handling an instantaneous load-current stimulus is translated to the slew-rate requirement of driving the pass device
  - Two normally off switches are added around a unity gain buffer constituting the output stage of the amplifier
  - Conduct significant current⇔where a voltage difference across the unity gain buffer develops to be large enough to turn either of the MOS devices on



Adjust the threshold voltage by using a double gate MOS device

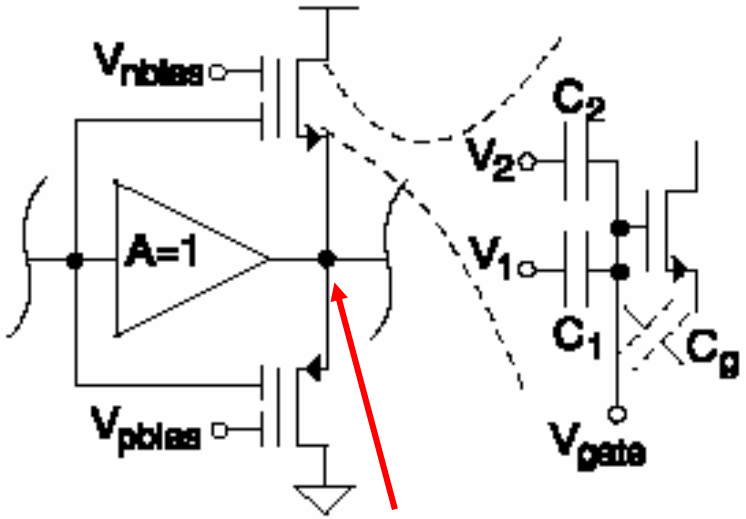
- The voltage at the floating gate (V_g), assuming that the source is grounded, is dictated by

$$V_g = \frac{V_1 C_1}{C_{total}} + \frac{V_2 C_2}{C_{total}} \quad \left[C_{total} \text{ is } C_1 + C_2 + C_g \right]$$

- V_{th1} is the effective threshold voltage of terminal one and V_{th} is the threshold voltage seen at the floating gate

$$V_{th1} = \frac{V_{th} C_{total}}{C_1} - \frac{V_2 C_2}{C_1}$$

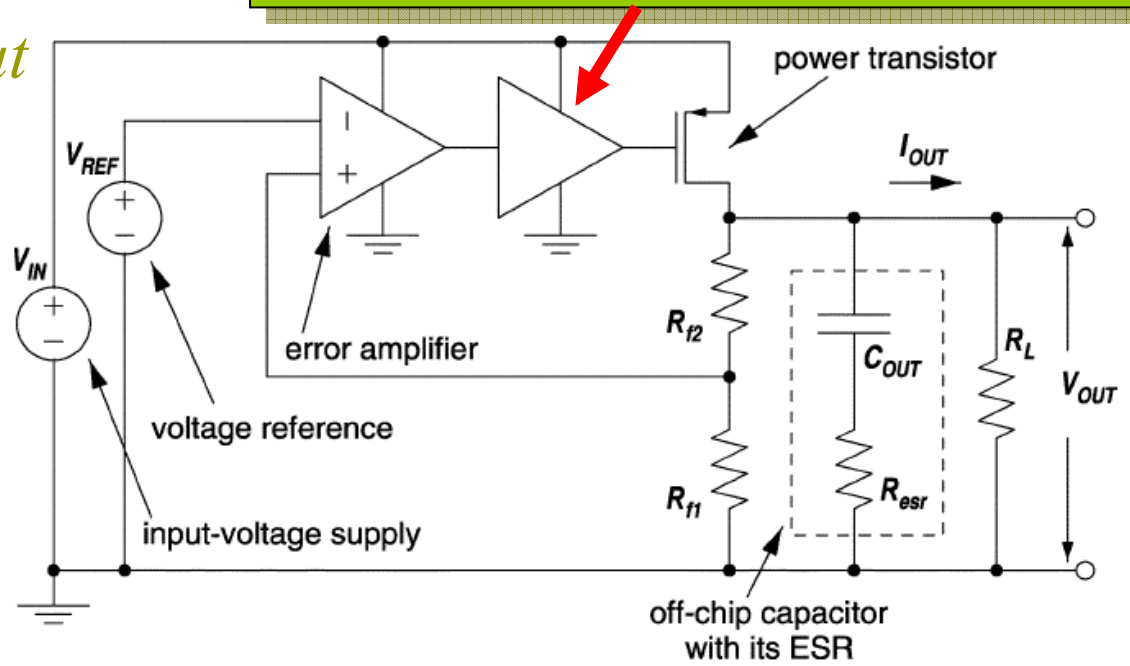
- If $C_1 = C_2 = 8C_g$, V_2=1.0V, and V_{th}=0.7V then
  - Yield a lower effective threshold voltage V_{th1}=0.49V
- **Disadvantage:** generate V_{nbias} and V_{pbias}



Connect to the gate of the pass devices

Slew-Rate Enhancement Circuits for CMOS Low-Dropout Regulators

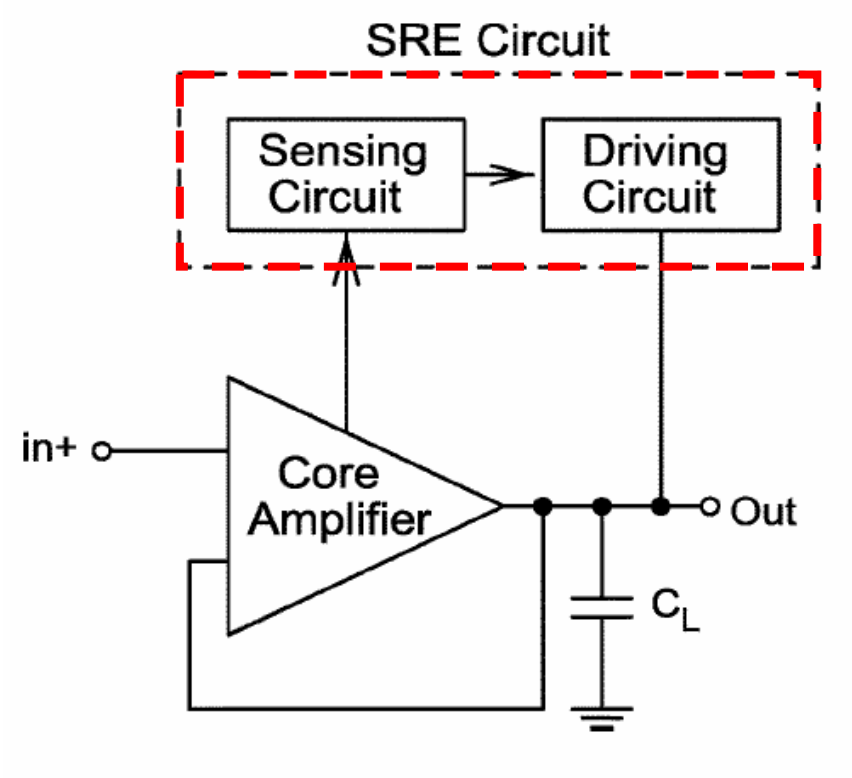
Proposed analog driver using SRE circuit



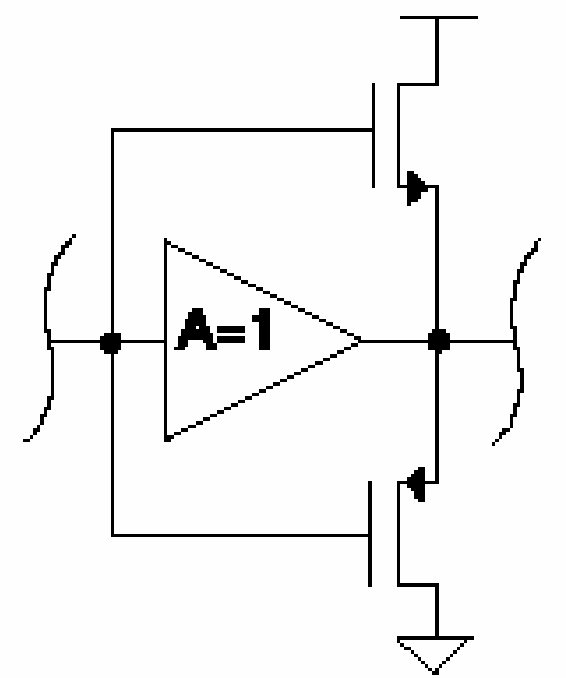
- Design problem
  - Large gate capacitance of power transistor degrades the loop-gain bandwidth and slew rate at the gate drive of the LDO
- Solution
  - A voltage buffer/driver can be inserted between the error amp. and the power transistor
  - It is difficult to realize a good voltage buffer to meet the requirements

Design considerations of proposed analog driver

- Proposed block diagram



- Rincon-Mora's proposed



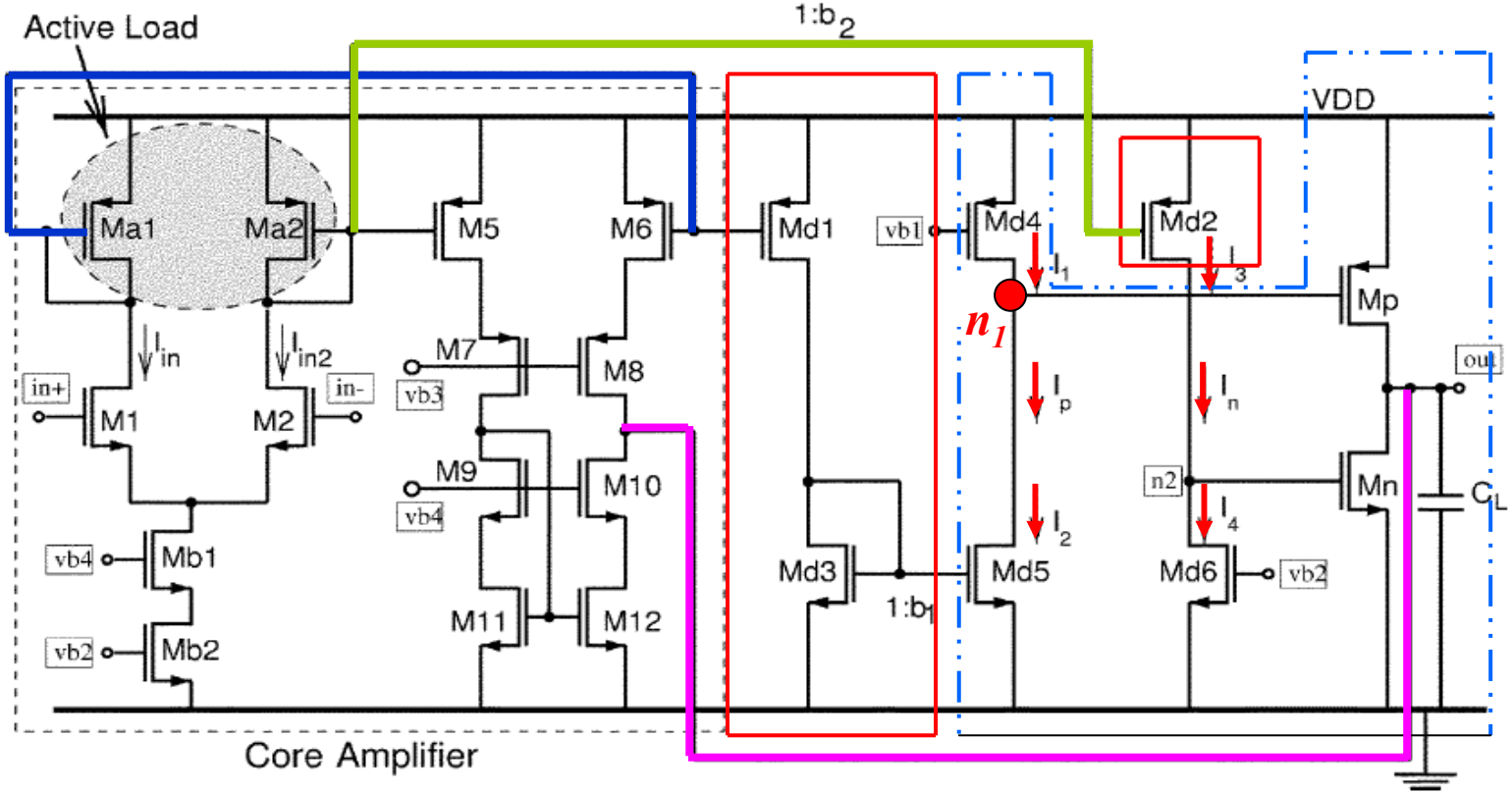
  - Need low threshold device and forward bulk-biasing

Current detection SRE circuits

- Principle of operation
  - ***Static state***
    - M_{d4} and M_{d5} both operation in saturation region, their drain currents equal to I_1 and I_2, and $I_2<I_1$
    - M_{d4} operates in the triode region such that node n_1 pull up
    - The drive transistor M_p is off
  - ***Transient state***
    - Input positive voltage step, leading to I_2 increase and node n_1 pull down
    - The drive transistor M_p is on

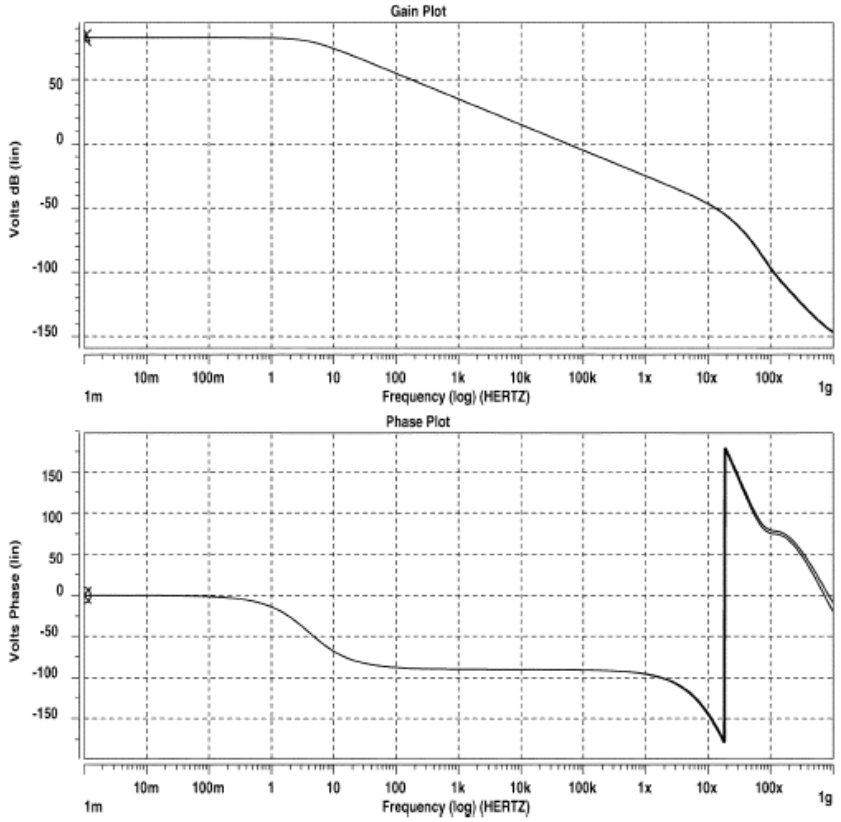
Sensing circuit

Drive circuit



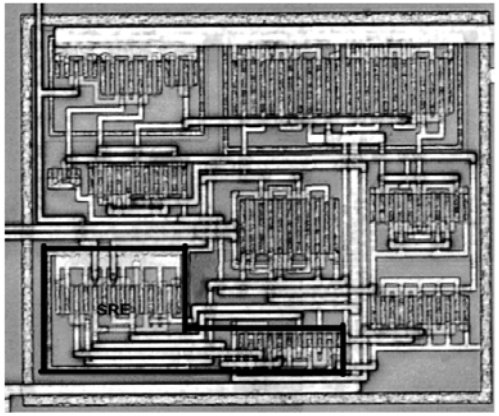
Simulation result

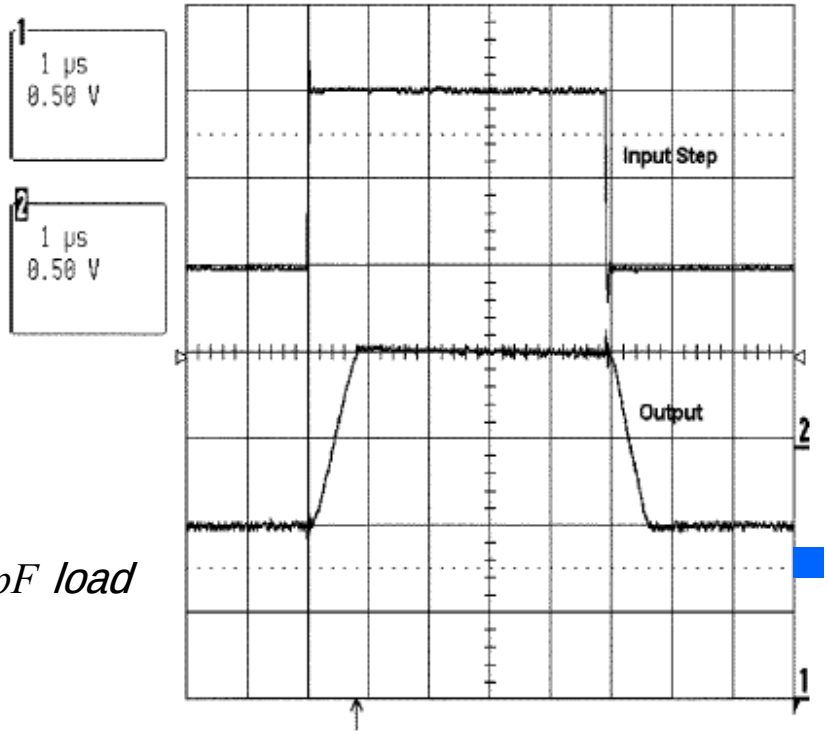
- The simulation results of ac responses of the core amplifier with and without the SRE circuit driving a load capacitance of $470pF$
  - The SRE circuit does not affect the ac responses of the core amplifier



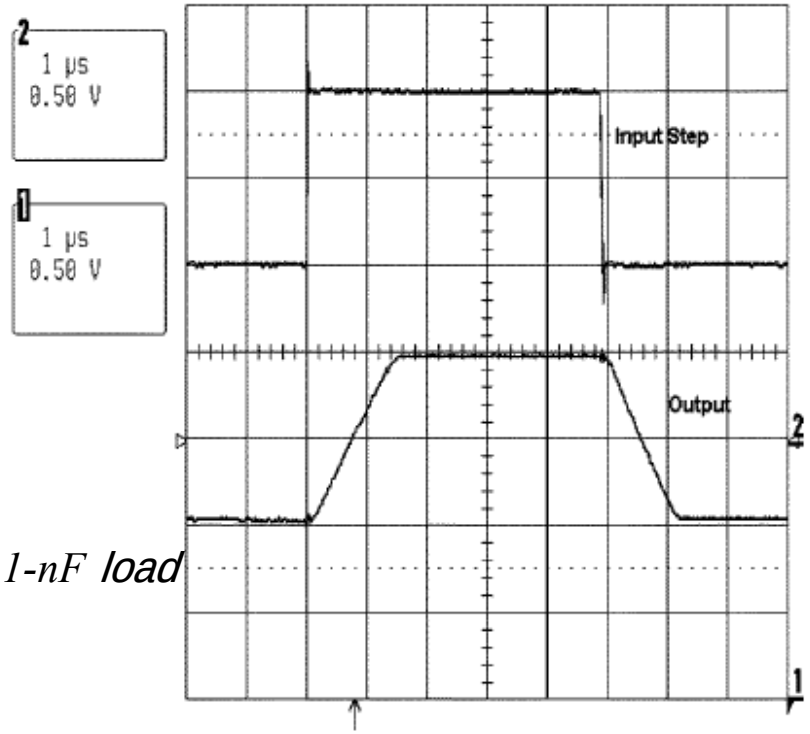
Experiment results

- It does not have significant transient overshoot even if the load capacitance is changed by more than two times
  - The SRE circuit ***is properly shut down before and end of the slewing periods***





470-pF load



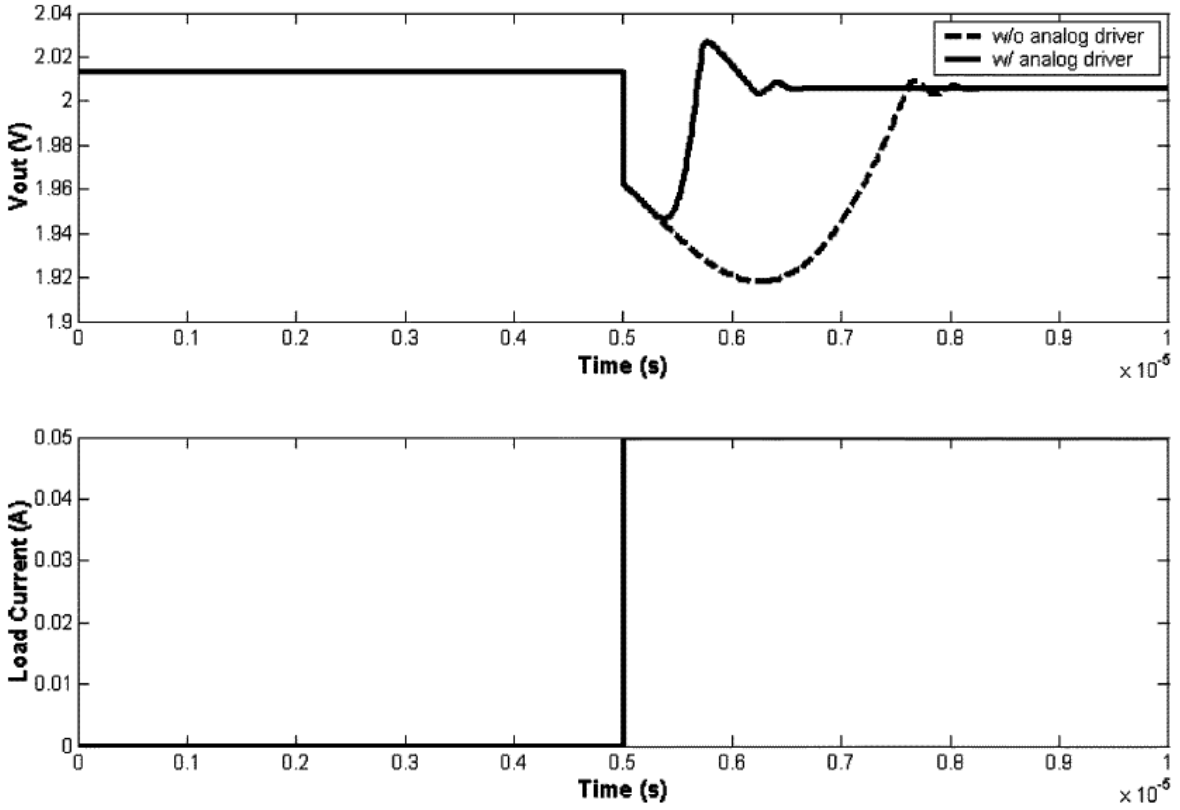
1-nF load

Experiment results

	Current-Mirror Amp. without SRE*	**Current-Mirror Amp. with SRE**	
Static Power (mW)	0.22	**0.28**	***27.3%***
Gain@10Hz	74 dB	**73 dB**	
GBW	56 kHz	**57 kHz**	
Phase Margin	89.7°	**90°**	
SR+/SR- (V/μs)	0.037/0.0368 (C_L=470pF) 0.017/0.017 (C_L=1nF)	**1.5/1.73** (C_L=470pF) **0.7/0.81** (C_L=1nF)	***43X***
Ts+/Ts- (1%) (μs)	31.3/31.4 (C_L=470pF) 66.7/66.7 (C_L=1nF)	**0.79/0.61** (C_L=470pF) **1.44/1.09** (C_L=1nF)	***44X***
Area (mm^2)	N.A.	**0.027**	
Supply Voltage	3 V		
Loading capacitor	1 MΩ // 470 pF		

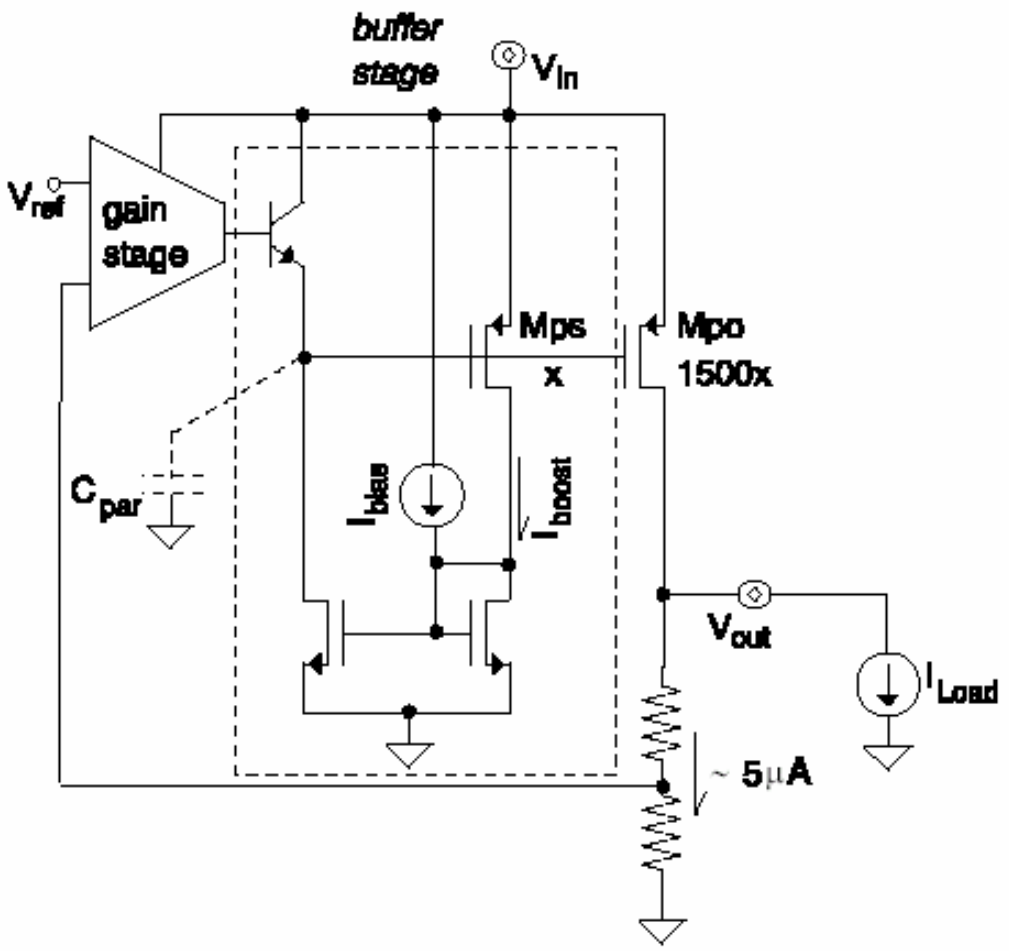
Experiment results

- The load transient response of the LDO is improved by 2.3 times with 50mA output-current change



Current Efficient Buffer

- The increase in current in the buffer stage aids the circuit
  - By pushing the parasitic pole at its output (P_3) to higher frequencies
  - And by increasing the current available for slew-rate conditions
- Thus, the biasing conditions for the case of zero load-current can be designed to utilize a minimum amount of current
  - Which yields maximum current efficiency and prolonged battery life



Frequency Response

- Low load current :

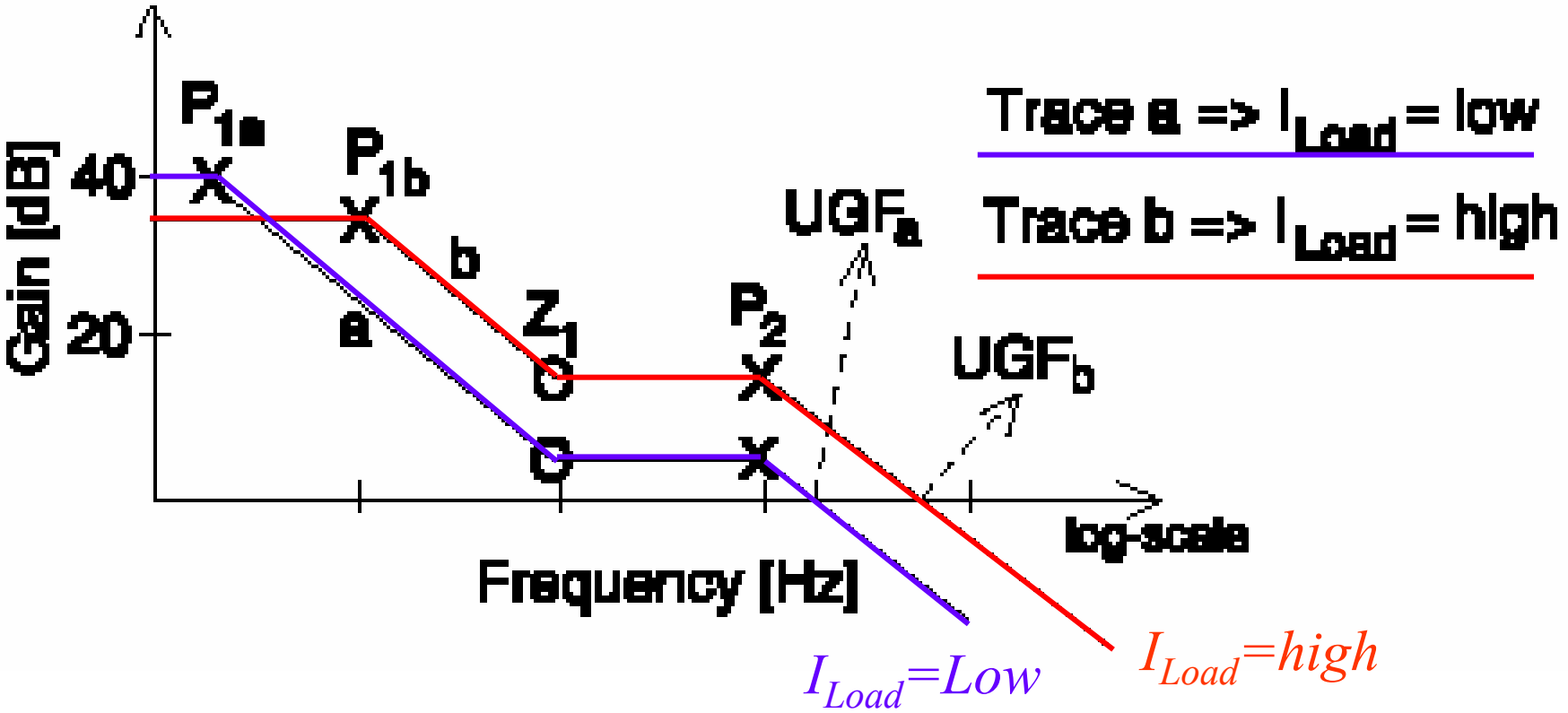
$$P_1 \approx \frac{1}{2\pi R_{o-pass} C_o} \approx \frac{\lambda I_{Load}}{2\pi C_o}$$

$$P_{3no-load-current} \approx \frac{g_{mnpn}}{2\pi C_{par}} = \frac{I_{bias}}{2\pi V_t C_{par}} \geq UGF_{\min}$$

- High load current : ??

$$A_v \approx A_{amp} g_{mp} R_{o-pass} \propto \frac{\sqrt{I_{Load}}}{I_{Load}} = \frac{1}{\sqrt{I_{Load}}}$$

Frequency Response



Frequency Response

- As I_{Load} increases , P_1 ↑ ↑ (UGF ↑ ↑) faster than A_v ↓ $\rightarrow P_3$ is also required to increase with I_{Load}, which is achieved by the load dependent boost current
- Load dependent boost current :

$$P_3 \approx \frac{g_{mnpn}}{2\pi C_{par}} = \frac{I_{bias} + I_{boost}}{2\pi V_t C_{par}} \approx \frac{I_{bias} + kI_{Load}}{2\pi V_t C_{par}}$$

- As I_{Load} ↑ , design P_3 increases at a faster rate than the UGF

$$P_{3-rate} = \frac{\partial P_3}{\partial I_{Load}} \approx \frac{k}{2\pi V_t C_{par}} \geq P_{1-rate} \approx \frac{\lambda}{2\pi C_o} > UGF_{rate} \Rightarrow k \geq \frac{\lambda V_t C_{par}}{C_o}$$

  - Where $P_{3\text{-}rate}$, $P_{1\text{-}rate}$ and UGF_{rate} are the rates with respect to load-current of pole P_3, pole P_1, and the unity gain frequency respectively

Transient Response

- During a load-current transition from zero to maximum value :

$$\Delta t_1 \approx t_{amp} + t_{Mpo} + t_{Mps-on} + t_{latch-up}$$

$$\approx \frac{1}{BW_{cl}} + t_{Mps-on} + t_{latch-up} \quad \left[\text{where } \frac{1}{BW_{cl}} \approx t_{amp} + t_{Mpo} \right]$$

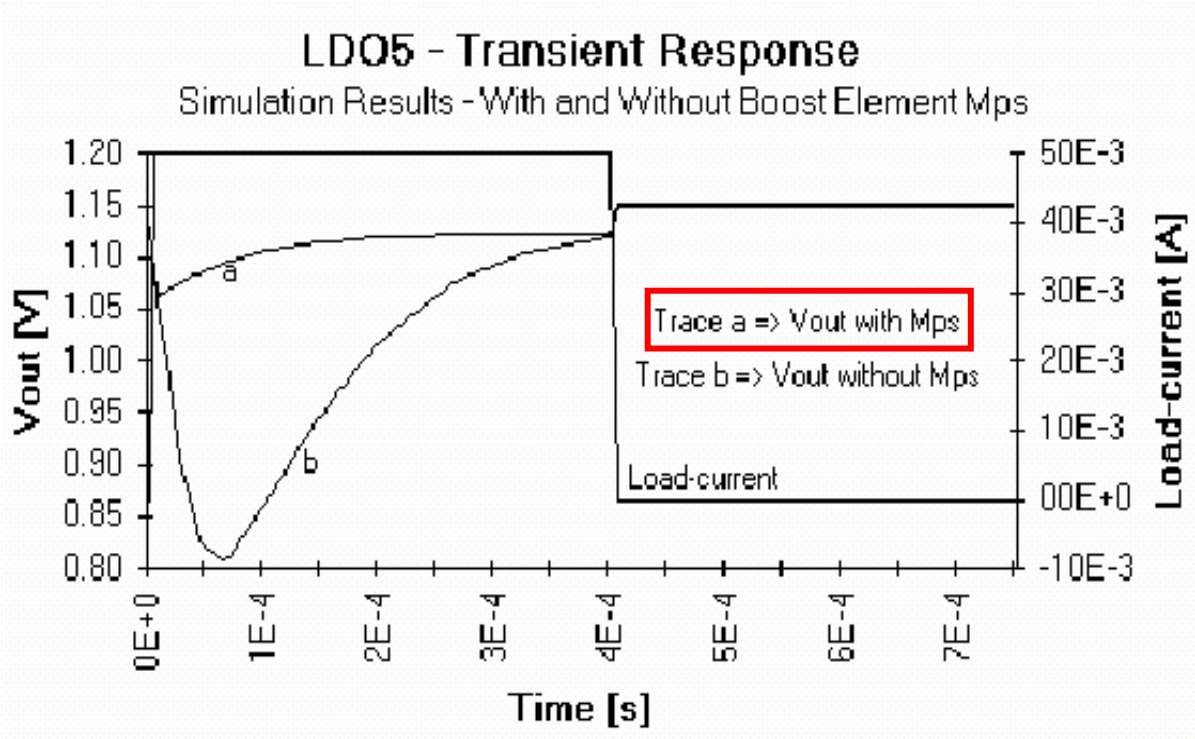
- The composite buffer stage
  - A localized positive feedback circuit
    - The positive feedback gain is ***less than one***
  - Attempts to latch up until the output transistor is fully turned on
    - At which point , the error amplifier forces the circuit back into the linear region

An Example

- $C_{par}=200pF$, the voltage change required for the output PMOS transistor (ΔV_{sg}) is 0.5V, the closed-loop bandwidth of the system is $1MHz$, and the response time (Δt_1) is confined to be less than 5us
  - The slew-rate current ($I_{sr}=I_{bias}$) required for a class A buffer is approximately 25uA
  - For the case of "current efficient-transient boost LDO buffer stage", a dc current bias (I_{bias}) of only 1uA can provide the same performance

Transient Response

- The output voltage variation is decreased as a result of a reduction in response time
- Does not come at the expense of additional quiescent current flow during zero-load-current conditions
- Achieve maximum current efficiency and battery life



Maximum Output Current

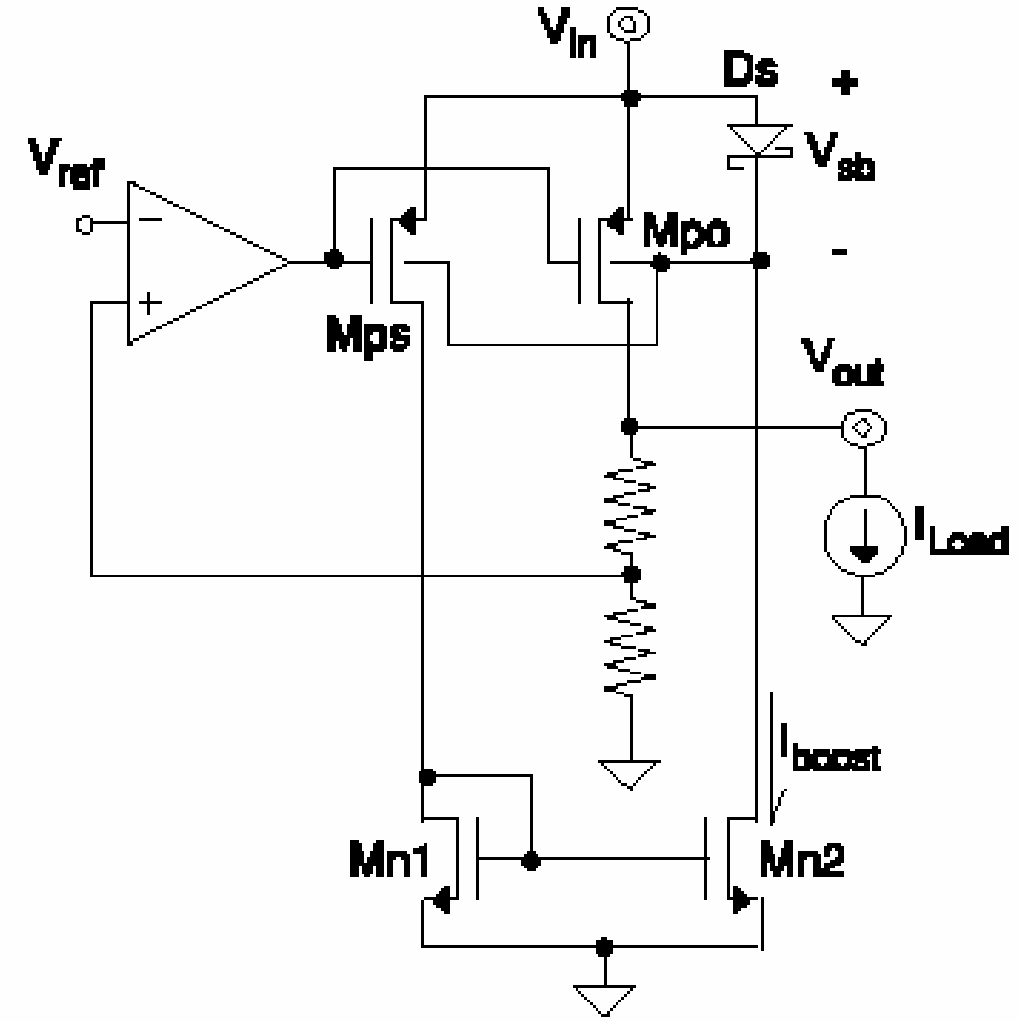
- The two main limitations of low voltage operation lie in the output current capabilities of the pass device (power switch) and voltage headroom
- The threshold voltage decreased as V_{sb} increases thereby effectively increasing the gate drive of the power PMOS transistor (pass device)

$$I_{sd} \approx \frac{K_p W}{2L}\left[V_{sg} - V_{th}\right]^2$$

$$\approx \frac{K_p W}{2L}\left\langle V_{sg} - |V_{t0}| - \gamma\left[\sqrt{2|\phi_f| - V_{sb}} - \sqrt{2|\phi_f|}\right]\right\rangle^2$$

Current Boosting

- The ability to shut off M_{po} is not degraded since the forward bias voltage is a function of load-current
  - *At low load-currents* I_{boost} is low and V_{sb} is close to zero
  - *At high load-current*, I_{boost} and V_{sb} increase thereby decreasing the threshold voltage and increasing the effective gate drive of the output PMOS device



Drop-out Voltage

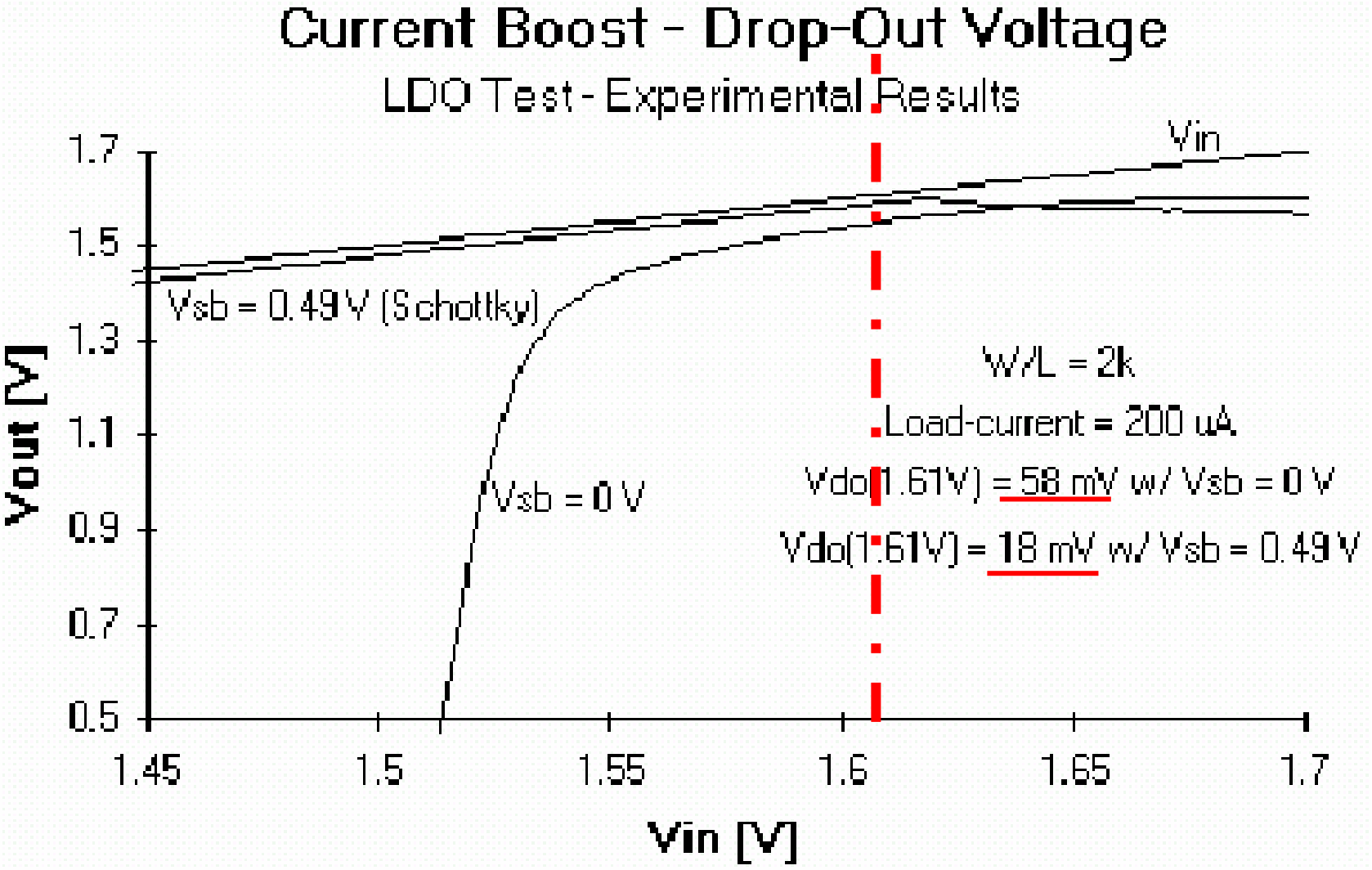
- The method of forward biasing the source to bulk junction also yields lower drop-out voltages
  - The on resistance of the pass device (M_{po}) is **reduced**
  - When the regulator is in drop-out, M_{po} is characteristically in the **triode region** and exhibits the well known current relationship

$$I_{sd} \approx \frac{K_p W}{2L}\left\langle\left[V_{sg}-V_{th}\right]V_{sd}-V_{sd}^2\right\rangle \approx \frac{K_p W}{2L}\left[V_{sg}-V_{th}\right]V_{sd}$$

$$\downarrow\ R_{on} \approx \frac{V_{sd}}{I_{sd}} \approx \frac{2L}{K_p W}\cdot\frac{1}{\left[V_{sg}-V_{th}\right]} \approx \frac{2L}{K_p W}\cdot\frac{1}{\left\langle V_{sg}-\left|V_{t0}\right|-\gamma\left[\sqrt{2\left|\phi_f\right|-V_{sb}}-\sqrt{2\left|\phi_f\right|}\right]\right\rangle}$$

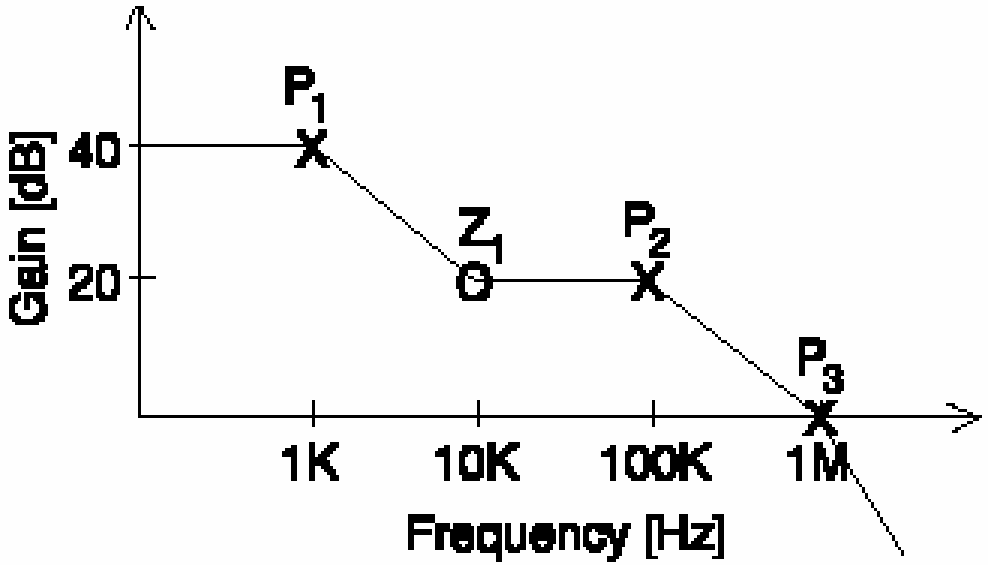
$$\downarrow\ V_{do} \approx R_{on} I_{Load} \approx \frac{2L}{K_p W}\cdot\frac{I_{Load}}{\left\langle V_{sg}-\left|V_{t0}\right|-\gamma\left[\sqrt{2\left|\phi_f\right|-V_{sb}}-\sqrt{2\left|\phi_f\right|}\right]\right\rangle}$$

Drop-out Voltage (cont'd)



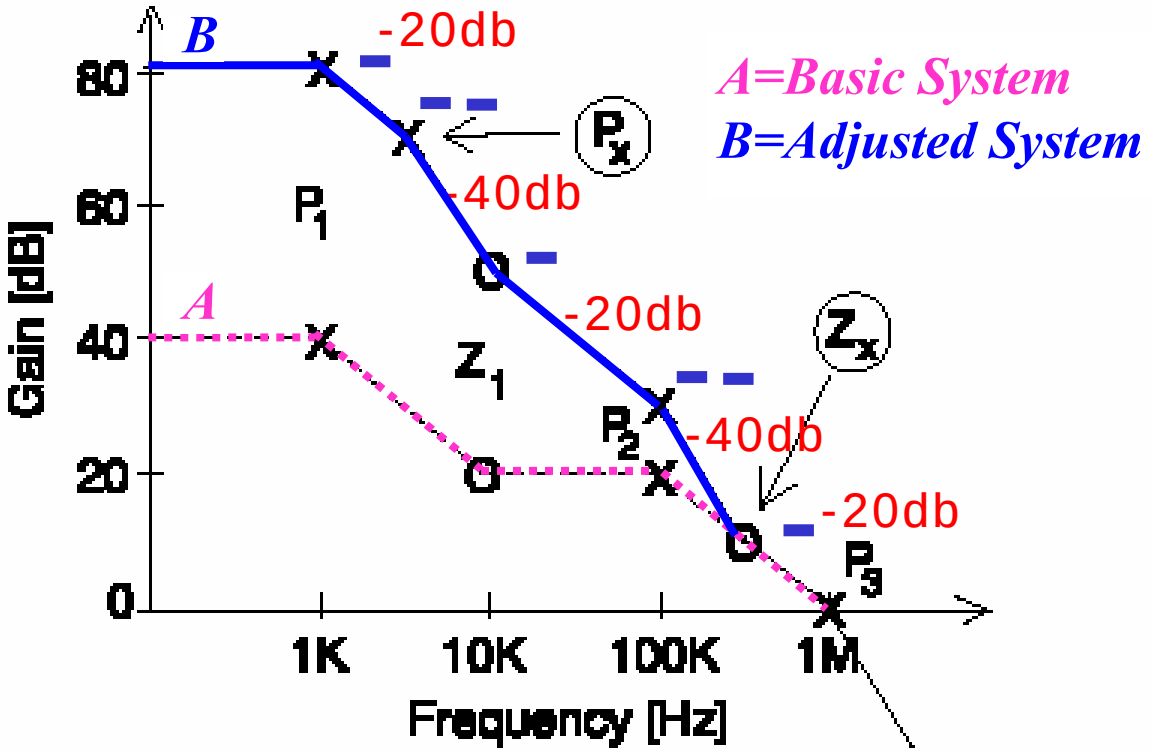
Load Regulation

$$R_{o-reg} = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta}$$



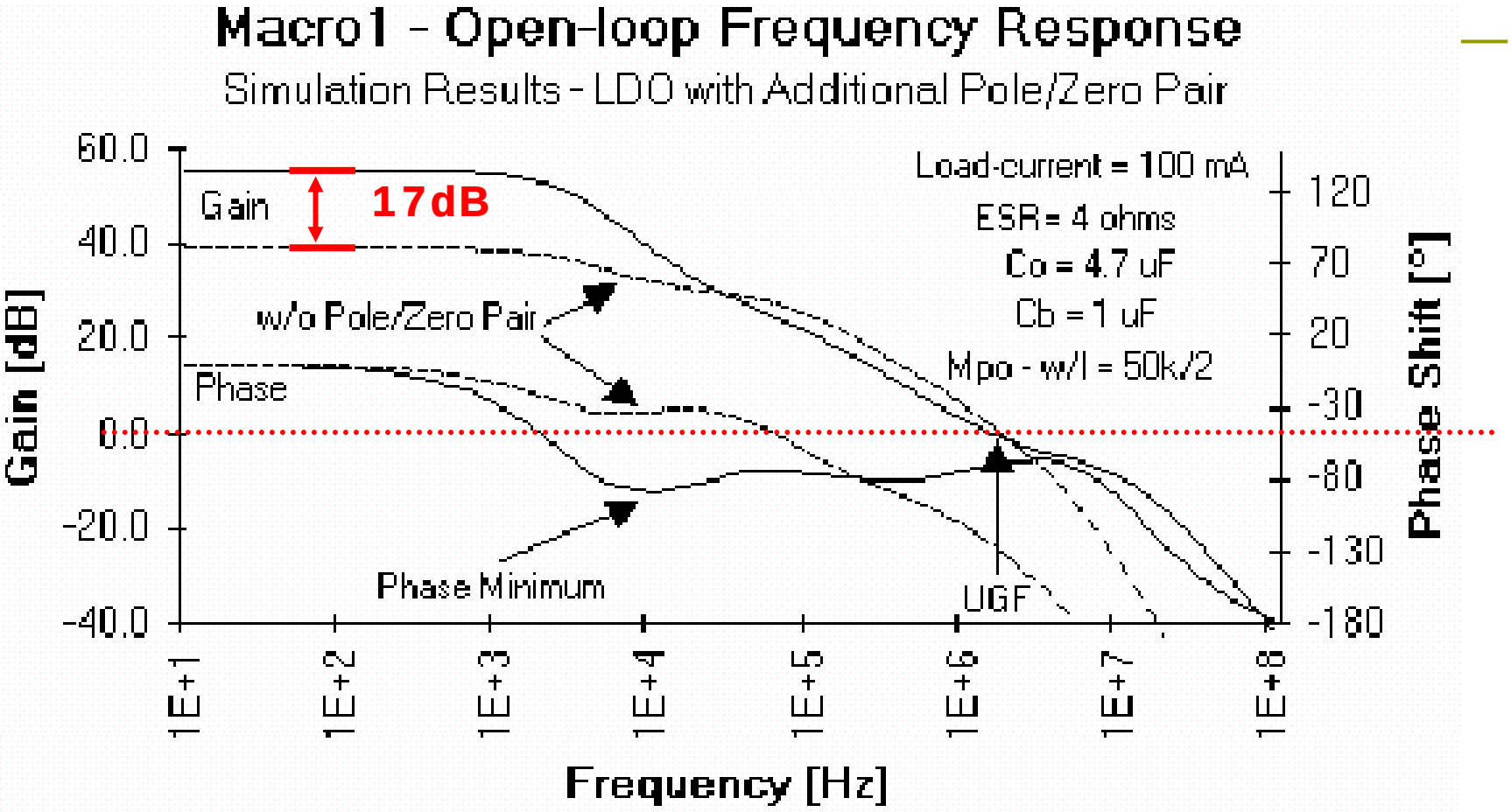
- The load regulation performance is determined by the open-loop gain of the system
  - Unfortunately, the dc gain is limited by the frequency response of the regulator
- The UGF, in particular, is determined by
  - The maximum allowable response time
  - The frequency range where the parasitic poles of the system reside, such as the internal poles of the error amplifier

Pole/Zero Pair Generation



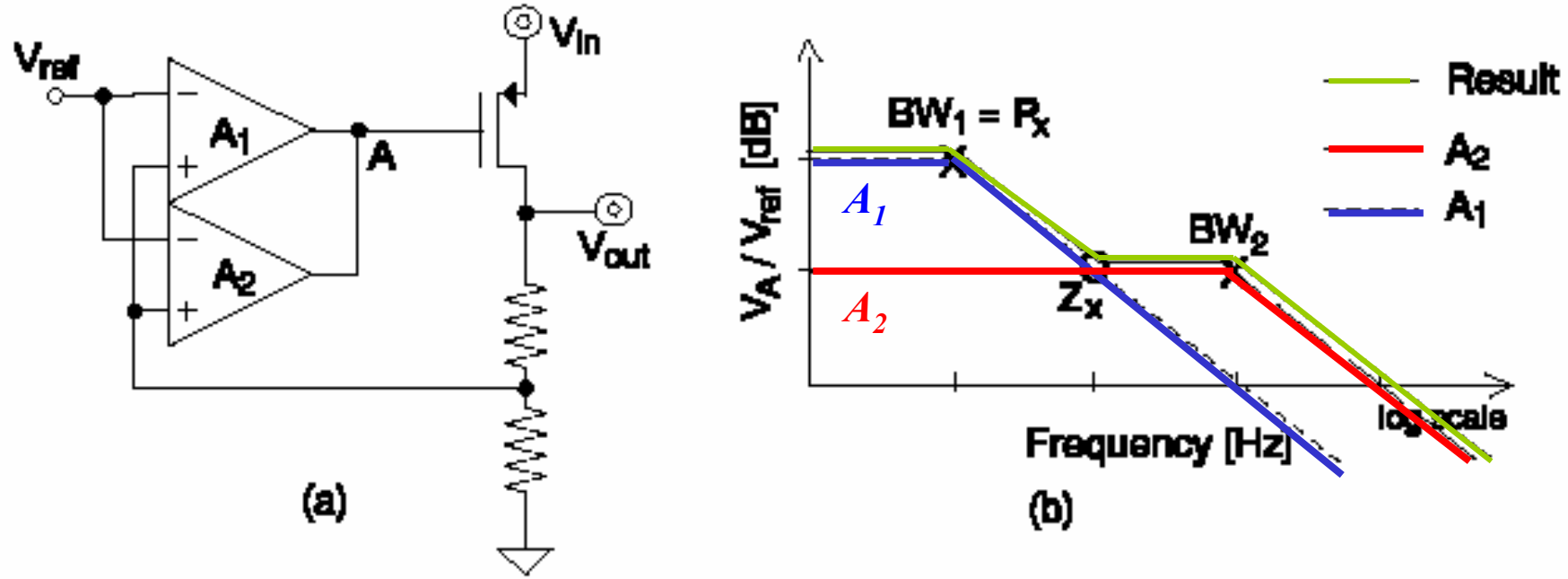
- Add a pole/zero pair
  - For a given unity gain frequency (UGF), the upper limit of the open-loop gain can be increased by manipulating the frequency response as depicted by trace B
  - The basic idea is for the gain to drop quickly as the frequency increases so that a larger dc gain is possible
  - Regulation is improved while keeping the UGF away from parasitic poles
- The fact that P_2 and Z_1 track each other can be used to optimize the design

AC simulation of LDO with an additional pole/zero pair



- Load regulation performance improved from approximately 41 to 12mV/100mA, corresponding to a 71% reduction

Parallel Amplifier Structure



Frequency Shaping Amplifier

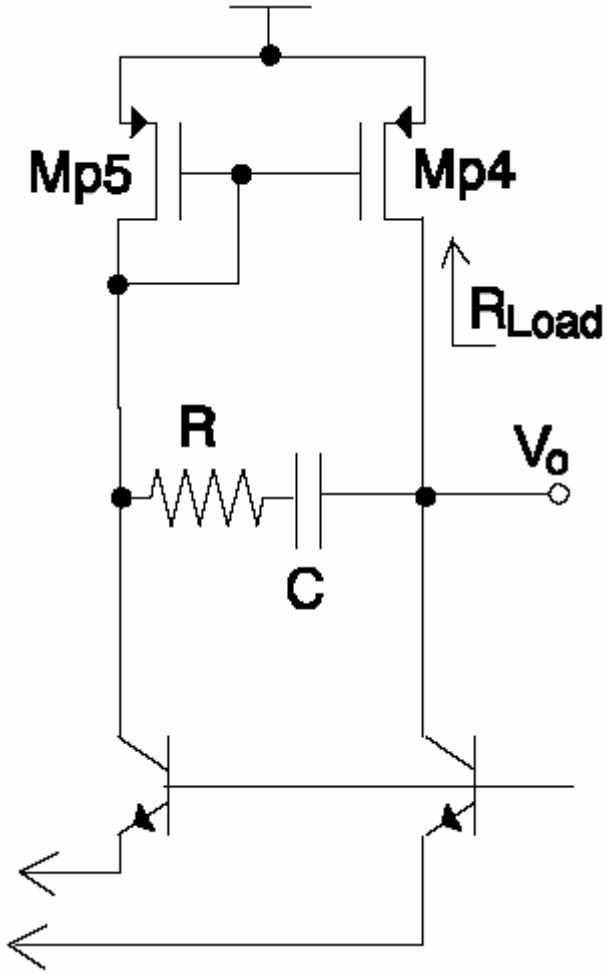
- The main disadvantages of the Parallel Amplifier Structure
  - The circuit is complexity
  - The realization of the two amplifiers may prove to be costly in terms of quiescent current flow
- A pole/zero pair can also be generated through the use of a feed-forward capacitor in a folded topology
  - ***At low frequencies***, the amplifier is unaffected by the feed-forward capacitor (C_{ff})
    - The gain is that of a typical **folded topology**, which is characteristically high
  - ***At high frequencies***, the capacitors acts like an electrical short
    - Give rise to the gain of a **non-cascoded** architecture (**lower gain**)

Another realization of the Frequency Shaping Amplifier

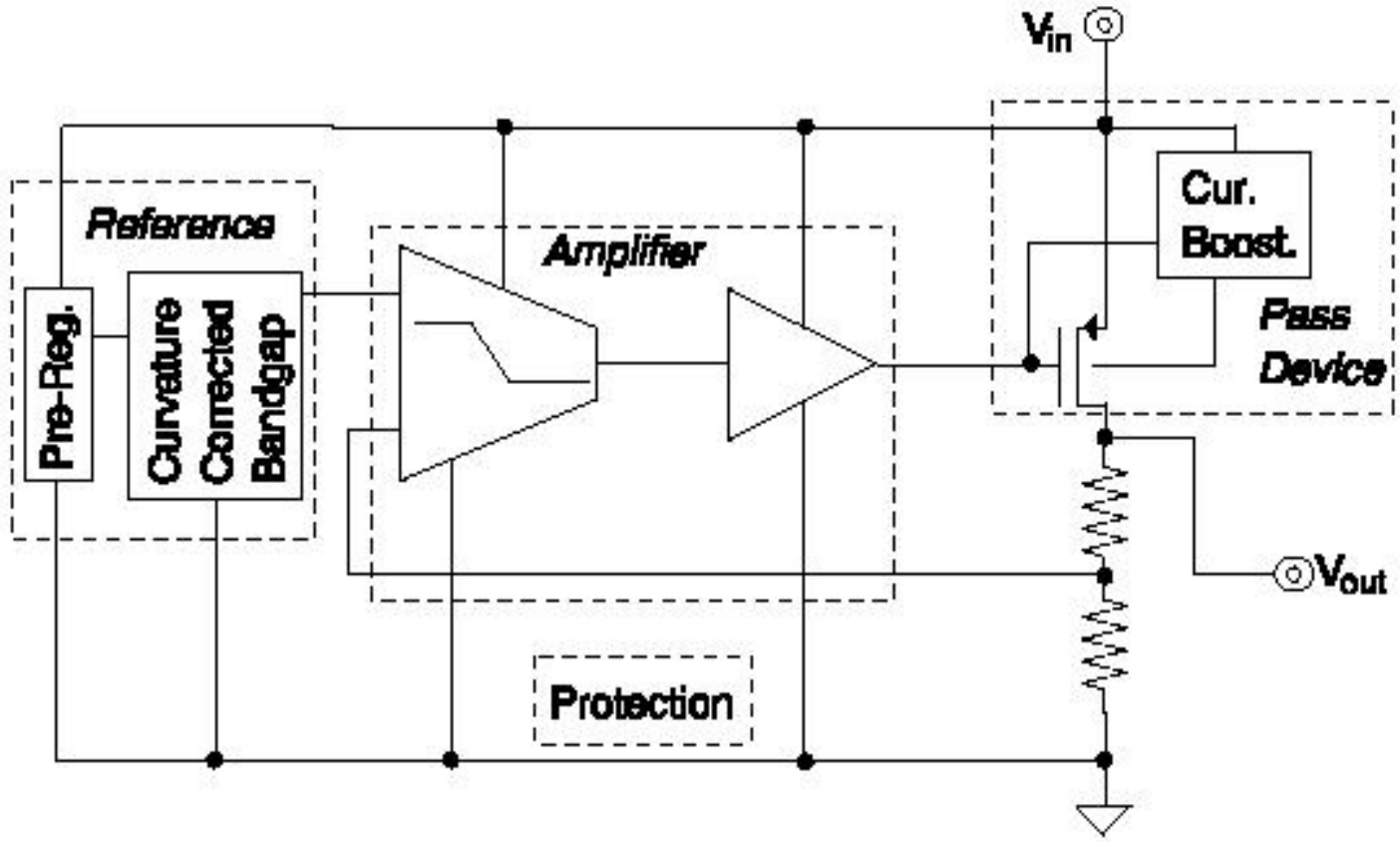
- The circuit takes advantage of the input and the output impedance of the mirror load, composed of M_{p4} and M_{p5}, to help shape and define the frequency response of the amplifier

$$Z_X = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}}\right\rangle C}$$

$$\text{and } P_X = \frac{1}{2\pi\left\langle R + \frac{1}{g_{m5}} + r_{ds4}\right\rangle C}$$

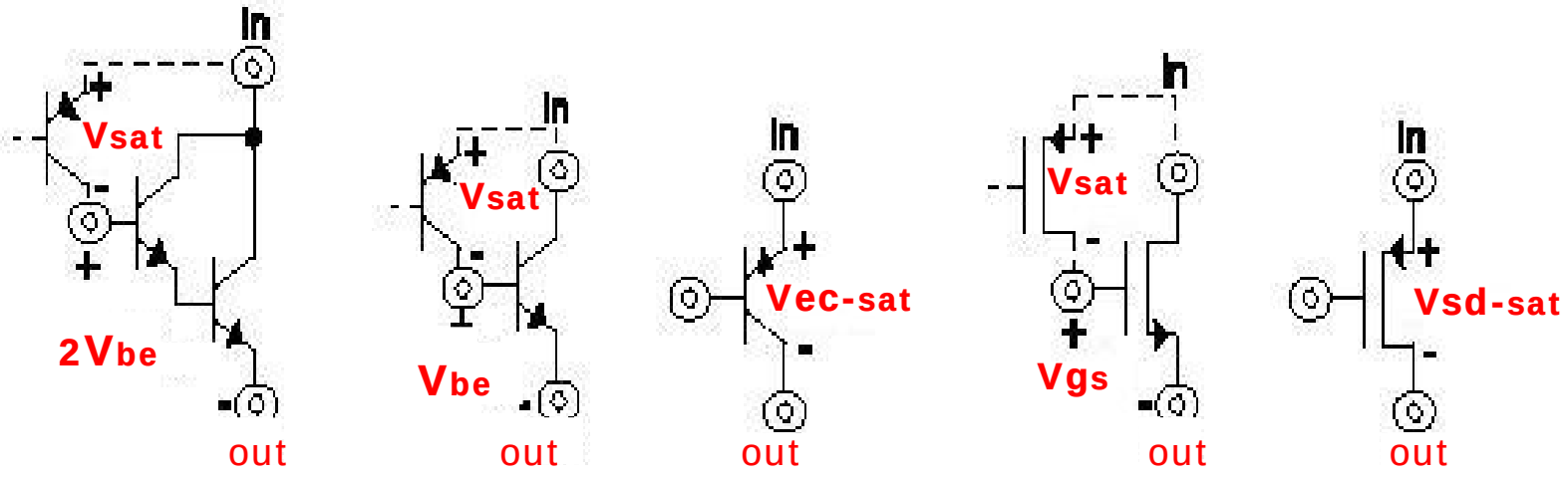


Circuit Design: Block Level Diagram



Pass Device

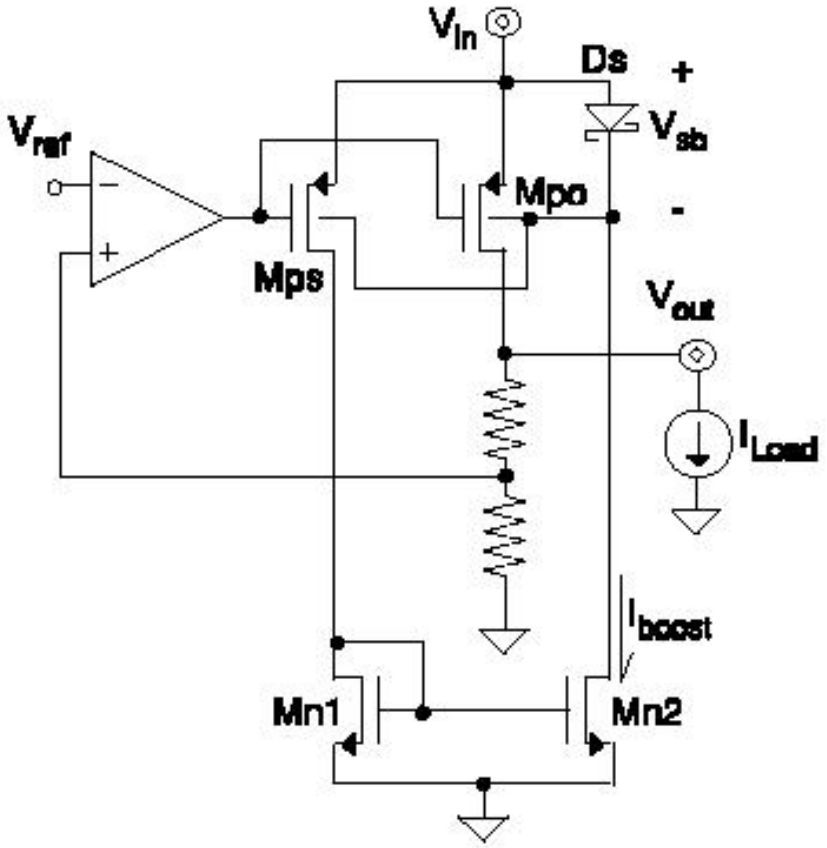
Basic configurations :



NPN Darlington **NPN** **PNP** **NMOS** **PMOS**

Pass Device (cont'd)

- Use **schottky diode**
  - $|V_{SB}|$ increase
  - $|V_{tp}|$ decrease
  - Can use lower V_{in} to drive M_{po}
- **Problem:**
  - During drop-out condition, M_{ps} and M_{po} are in different regions of operations. (V_{sd} are different)

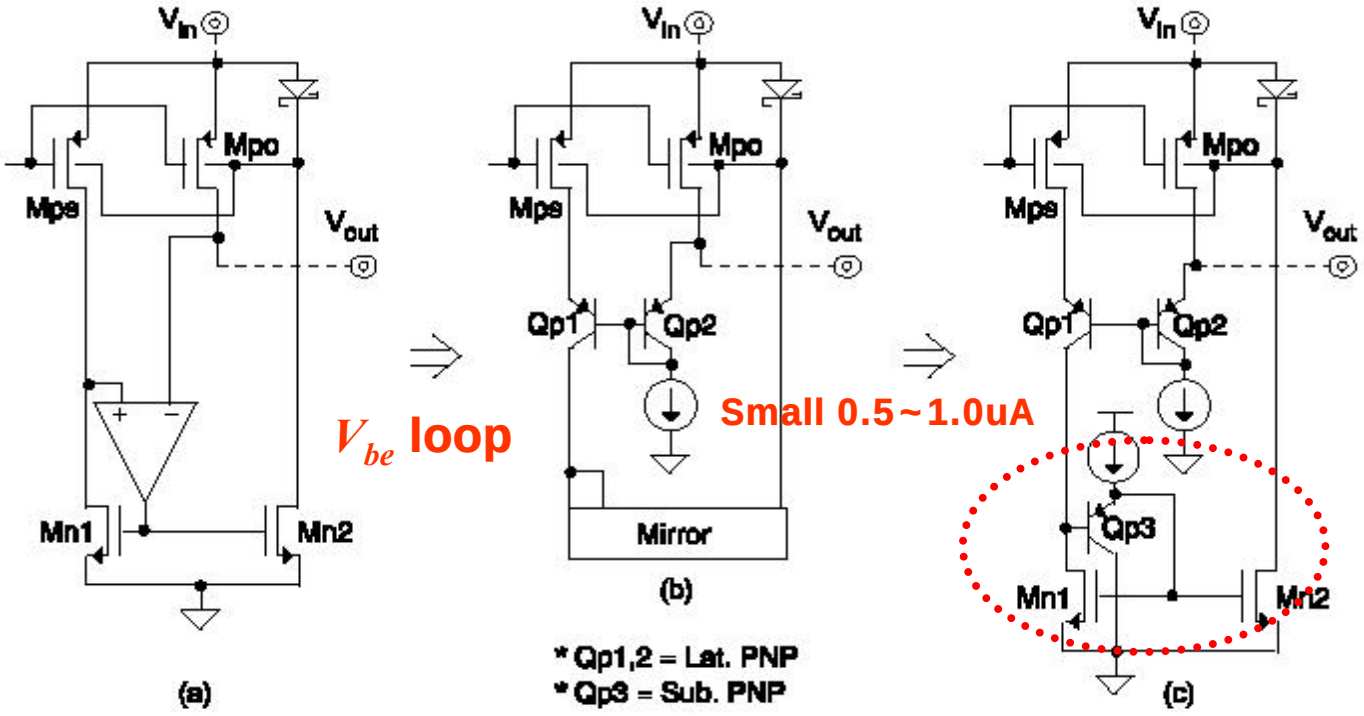


Pass Device (cont'd)

Solution : make V_{sd} of M_{ps} and M_{po} to be equal

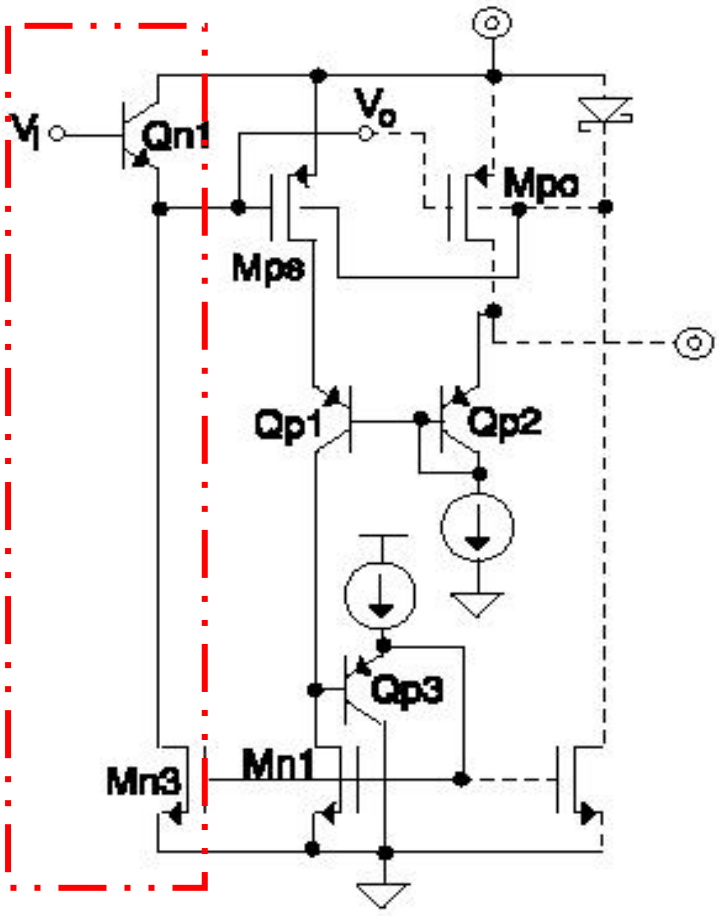
(b) $V_{in} > V_{sd\text{-}Mps} + V_{ec\text{-}Qp1} + V_{gs\text{-}Mirror}$

(c) $V_{in} > V_{sd\text{-}Mps} + V_{ec\text{-}Qp1} + V_{gs\text{-}Mirror} - V_{eb}$



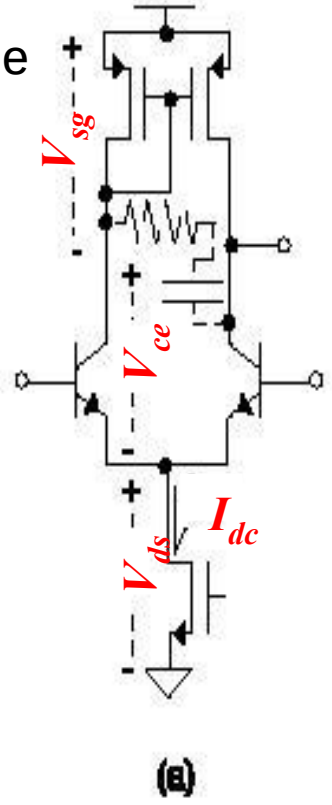
Amplifier (cont'd)

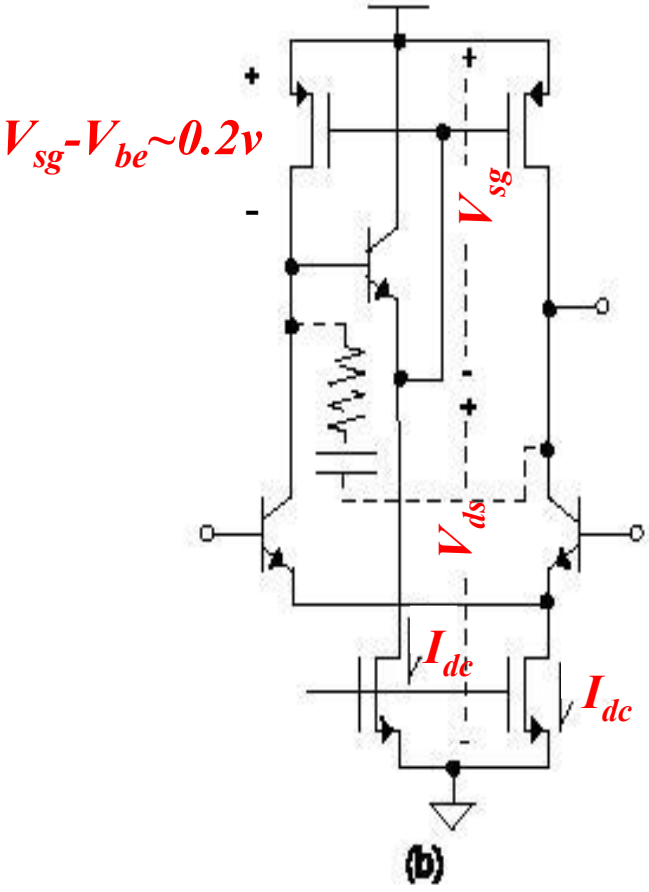
- Buffer :
  - A low input capacitance for gain stage
  - A low output impedance for pass-element
  - Q_{n1} : a class A NPN emitter follower



Amplifier (cont'd)

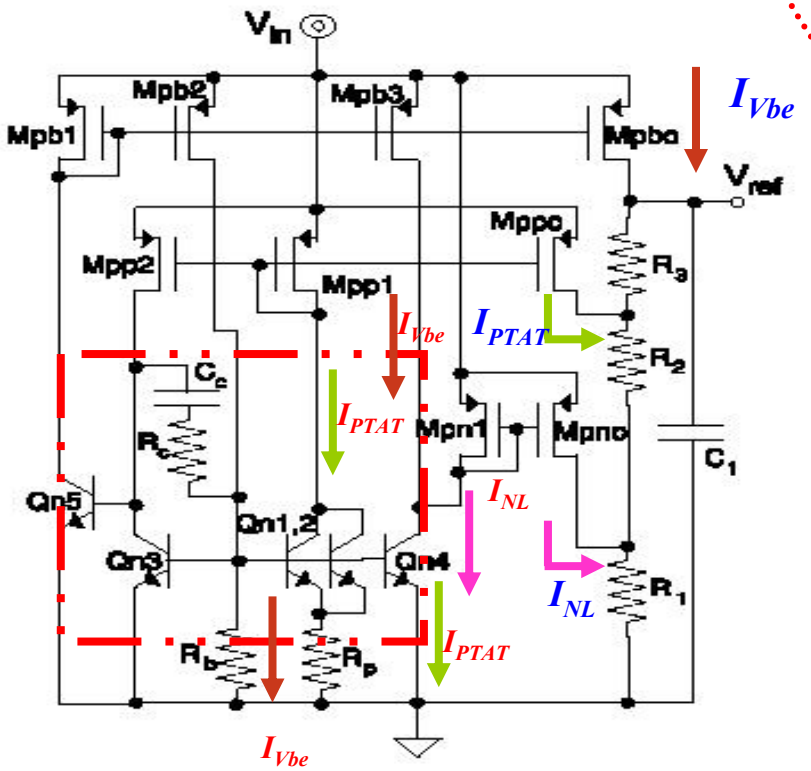
- Gain stage :
  - Use NPN transistor to be the differential pair
    - $NPN: V_{be} = 0.6 \sim 0.7$
    - $MOS: V_{gs} = 0.9$
  - $(a): V_{in} > V_{sg} + V_{ce} + V_{ds}$
  - $(b): V_{in} > V_{sg} + V_{ds}$

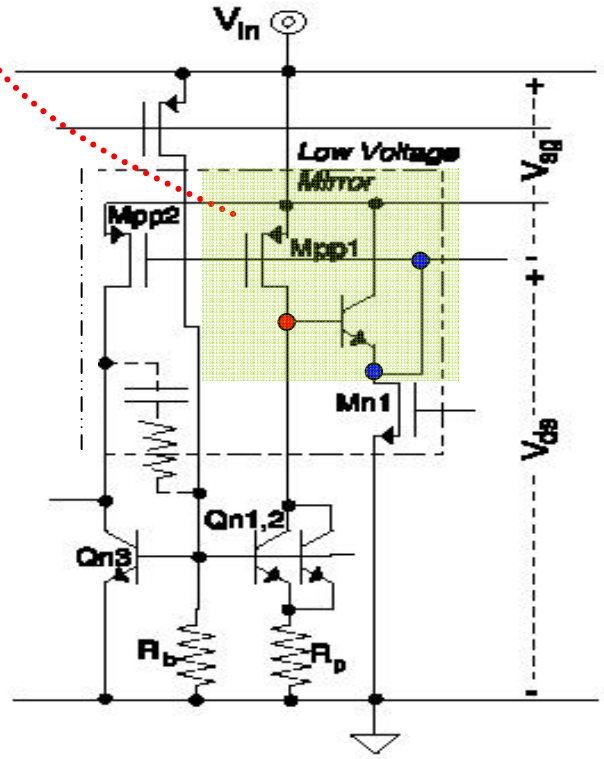




Reference

- M_{pp1} will turn into **Triode region**
- $T \downarrow$; $V_{be} = V_{dg} \uparrow \uparrow > |V_{th}| \uparrow$
- This causes the **temperature stability** of the reference to be **degraded**
  - V_{be} : $-2mV/K$
  - V_{th} : greater than $-2mV/K$ (about $-1.4mV/K$)



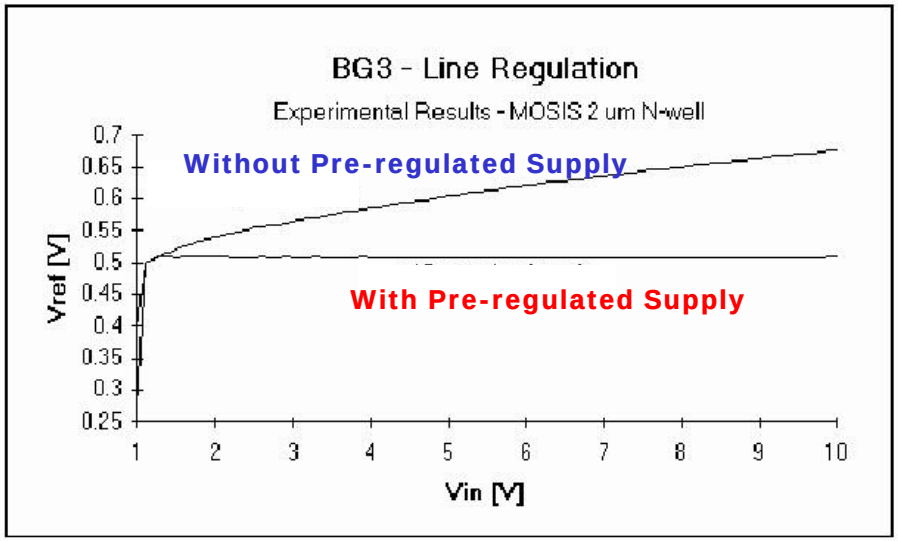


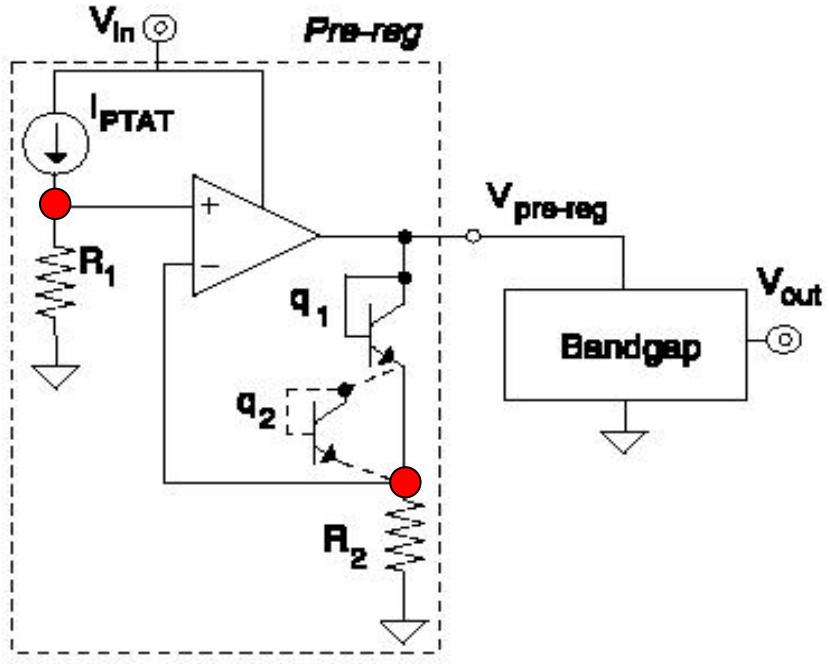
$$V_{in-\min} = V_{sg-Mpp1} + V_{ce-Qn1} + V_{Rp}$$

$$V_{in-\min} = V_{sg-Mpp1} + V_{ds-Mn1}$$

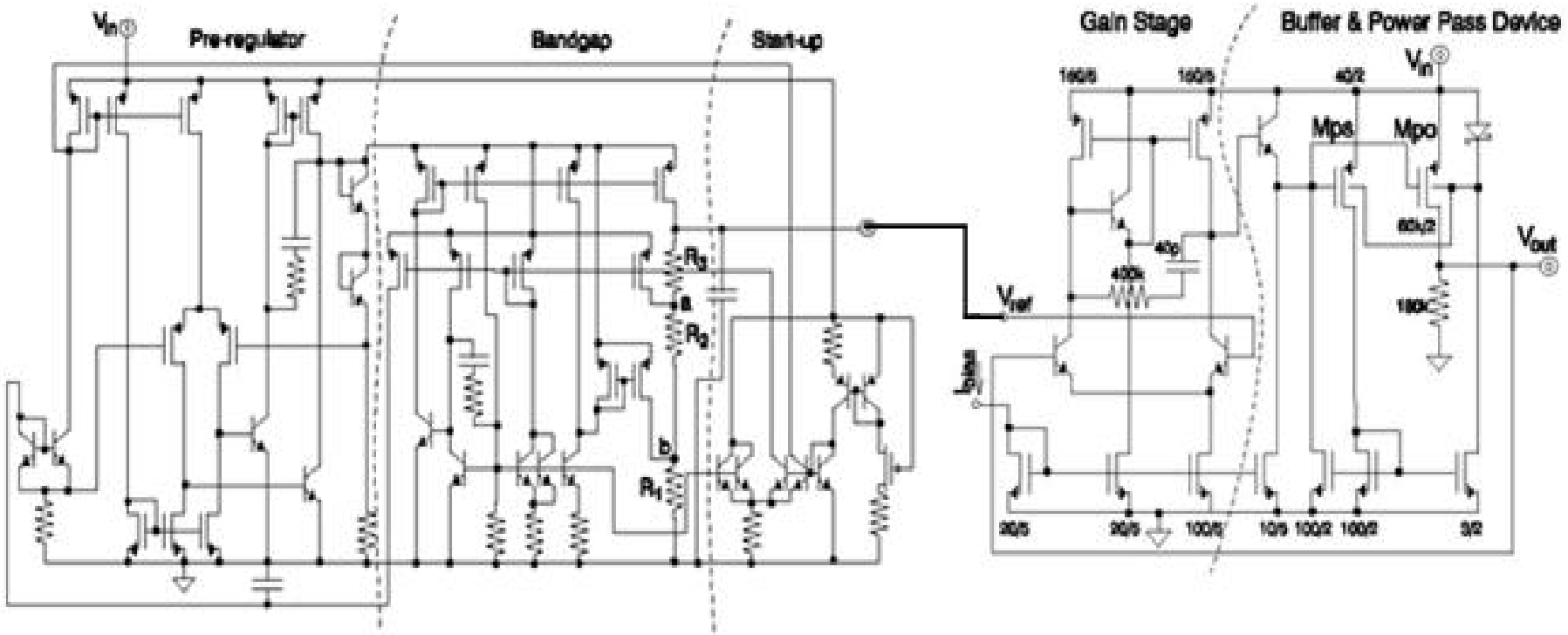
Reference (cont'd)

- Line regulation enhancement
  - Provide a first order voltage-mode bandgap reference

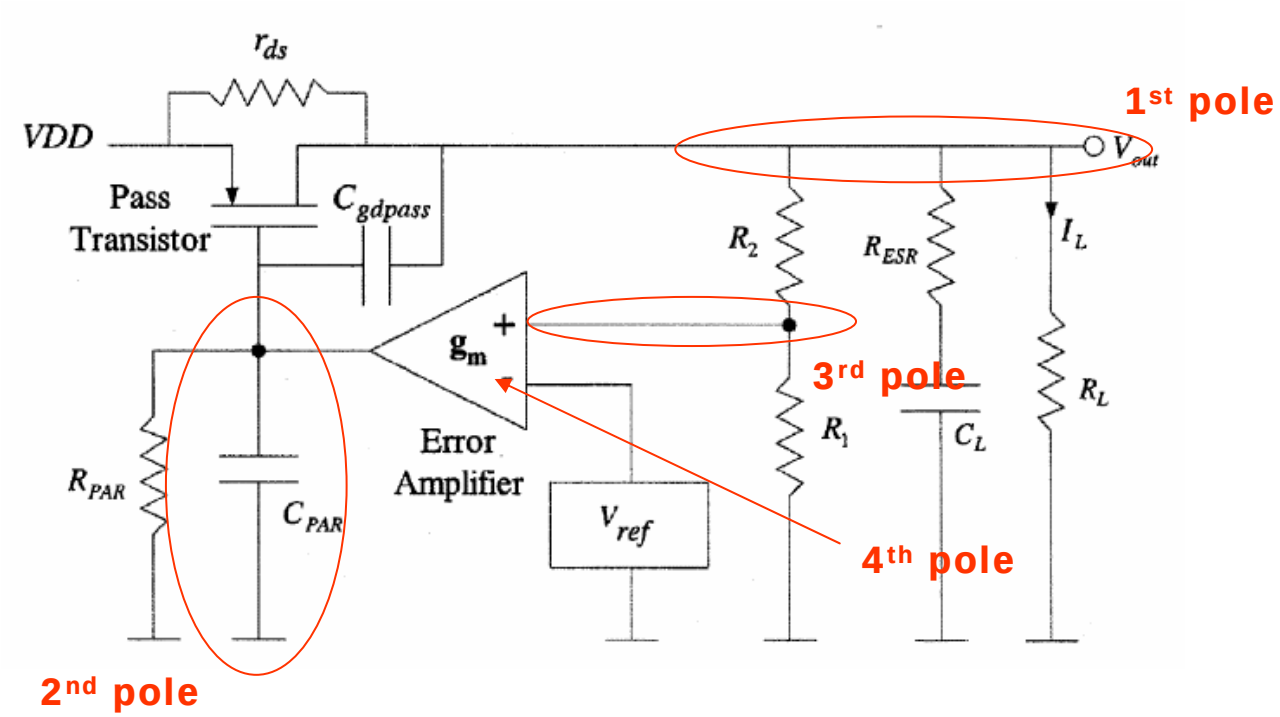




The Whole Chip



Typical LDO Voltage Regulator



- The impedance seen from drain is inversely proportional to load current, so ***pole is heavily dependent on load condition***
- A solution is to introduce a zero that compensates to guarantee ***phase margin better than 45 degrees***
- In a conventional LDO, **ESR of output capacitor** generates this zero

Open-loop gain transfer function

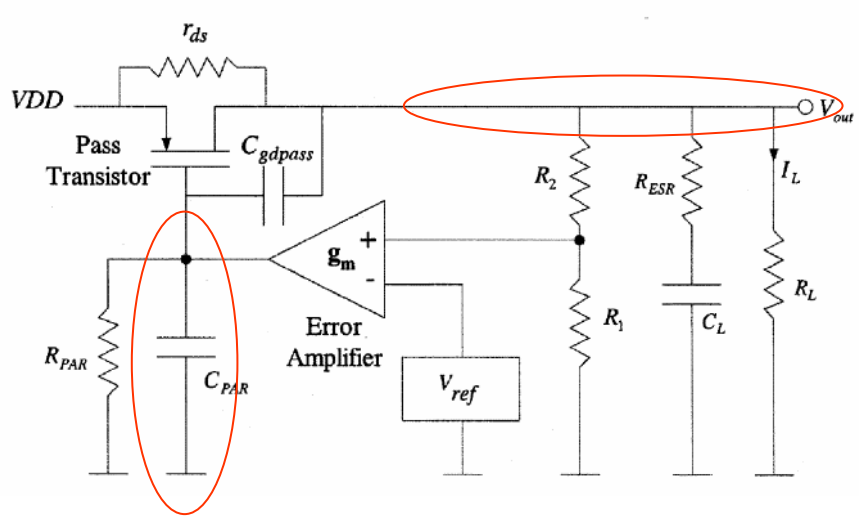
$$H(s) \cong \frac{A_0\left(1+\frac{s}{\omega_{ESR}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$$

$$A_0 = \left(g_m R_{par}\right)\cdot\left[g_{mpass}\left(r_{ds}\,//\left(R_1+R_2\right)//R_L\right)\right]\cdot\frac{R_1}{R_1+R_2}$$

$$\omega_{ESR} = \frac{1}{R_{ESR}C_L}$$

$$\omega_{p1} \approx \frac{1}{\left(r_{ds}\,//\left(R_1+R_2\right)//R_L\right)C_L}$$

$$\omega_{p2} \approx \frac{1}{R_{par}\left[C_{par}+\left(1-A_v\right)C_{gdpass}\right]} \approx \frac{1}{R_{par}\left[C_{par}+g_{mpass}\left(r_{ds}\,//\left(R_1+R_2\right)//R_L\right)C_{gdpass}\right]}$$



- There is no simple rule to decide the exact location of the zero
- The zero must be located below the unity gain frequency
- All high frequency poles must be located at least three times the unity gain frequency

RHP Zero and Two Dominant Poles

- A more detailed analysis shows that a right-hand side zero is also present

$$V_{in}g_{mpass} = sV_{in}C_{gdpass} \Rightarrow s = \frac{g_{mpass}}{C_{gdpass}}(RHP)$$

  - Can easily be placed **at high frequency**

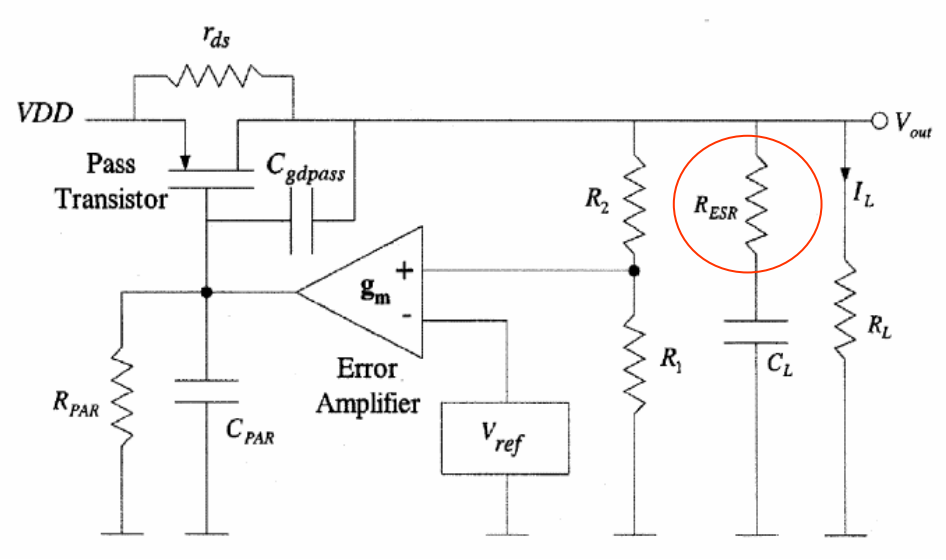
- C_{gdpass} **links the two dominant poles**

$$assume\ C_L >> C_{gdpass}\ and\ R_{LT} = r_{ds}\ //(R_1 + R_2)\ //\ R_L$$

$$\omega_{p1,2} \approx \frac{1 \pm \sqrt{1 - 4\dfrac{\dfrac{1}{R_{PAR}R_{LT}\left(C_{PAR}+C_{gdpass}\right)C_L}}{\left(\dfrac{1}{R_{PAR}\left(C_{PAR}+C_{gdpass}\right)} + \dfrac{1}{R_{LT}C_L} + \dfrac{g_{mpass}C_{gdpass}}{\left(C_{PAR}+C_{gdpass}\right)C_L}\right)^2}}}{2 \Big/ \left(\dfrac{1}{R_{PAR}\left(C_{PAR}+C_{gdpass}\right)} + \dfrac{1}{R_{LT}C_L} + \dfrac{g_{mpass}C_{gdpass}}{\left(C_{PAR}+C_{gdpass}\right)C_L}\right)}$$

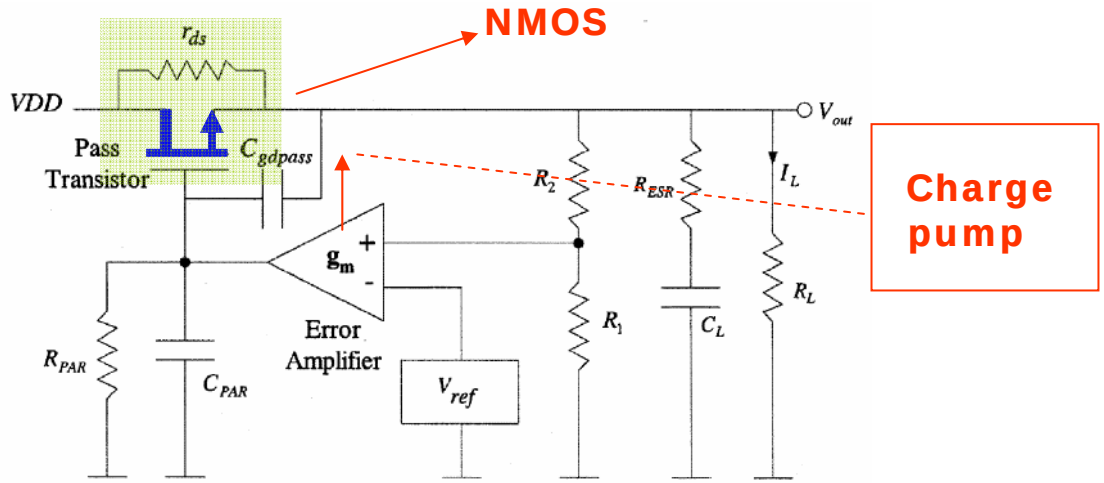
ESR Compensation

- The ESR is not properly specified and varies with temperature
  - The high-frequency bypass capacitors placed in parallel with the output capacitor form a pole further decrease the phase margin
- Ceramic capacitors are cheaper than tantalum capacitors, but ESR of ceramic capacitors typically **less than 0.05 ohm**
  - ESR increases the overshoot drastically if large resistors are used



Use Charge Pump Booster

- Generates a voltage higher than the supply than the supply voltage and the EA utilizes the voltage
  - Provides low output impedance
- Additional circuitry
  - Power consumption & noise performance
- Due to higher voltage generated, might not be well suited for advanced tech (because of HV process)

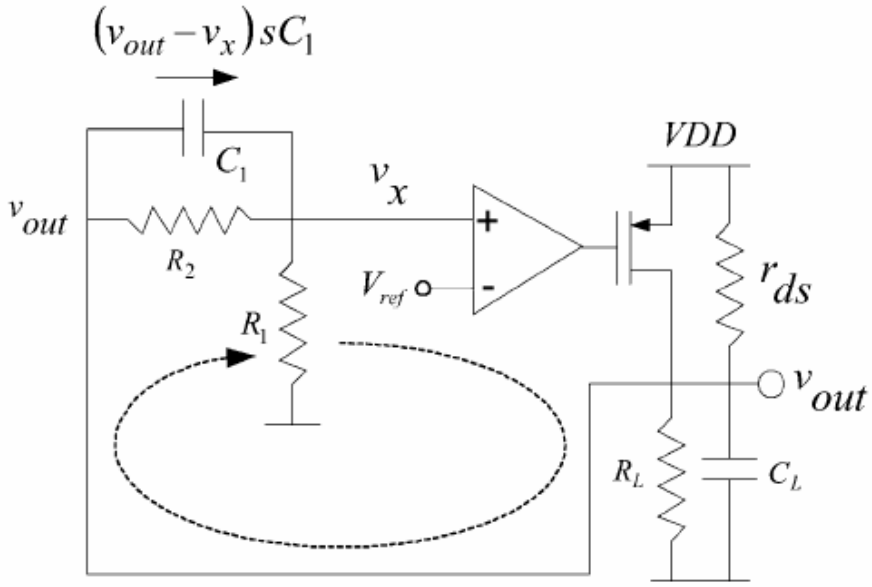


Pole-Splitting

- Miller capacitor must be huge to push the LDO output pole beyond the unity gain frequency
- Miller capacitor with C_{gs} of pass transistor forms a direct path for power supply spurs to output
  - The circuit has to be modified to have an extra buffer stage and this modification introduces additional parasitic poles
- Disadvantages of Miller compensation:
  - Reduces bandwidth, slew rate
  - Need more power, area
- The topology that creates the zero by using feedforward techniques but still Miller techniques are employed

Capacitive Feedback

- Basic idea is to introduce a left-hand plane (LHP) zero in the feedback loop that would replace the zero generated by ESR of the output capacitor
  - Advantages:
    - Precisely controlling the zero
    - Minimize the overshoots
- Add a pole-zero pair:
  - Zero at lower frequency than the pole
  - A drastic improvement in phase margin can be obtained by adding only a zero
  - Previous design added an internal zero by using a series resistor and capacitor combination connected to the output of EA



Capacitive feedback (cont'd)

Open – loop gain transfer function

$$H(s) \cong \frac{A_0\left(1+\frac{s}{\omega_{z1}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)\left(1+\frac{s}{\omega_{p3}}\right)}$$

- ω_{p3} is not far away from the zero
- The topology has to be modified so as to eliminate ω_{p3} without affecting the zero

$$A_0 = \left(g_m R_{par}\right)\cdot\left[g_{mpass}\left(r_{ds} \,//\, (R_1+R_2) \,//\, R_L\right)\right]\cdot\frac{R_1}{R_1+R_2}$$

$$\omega_{z1} = \frac{1}{R_2 C_1} \quad \left[-v_x s C_1 - \frac{v_x}{R_2} = 0 \Rightarrow s = -\frac{1}{R_2 C_1}\right]$$

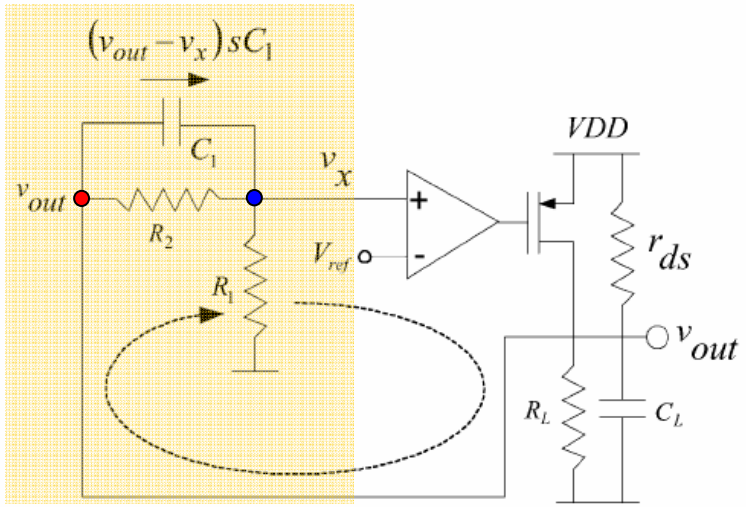
$$\omega_{p1} \approx \frac{1}{\left(r_{ds} \,//\, (R_1+R_2) \,//\, R_L\right) C_L}$$

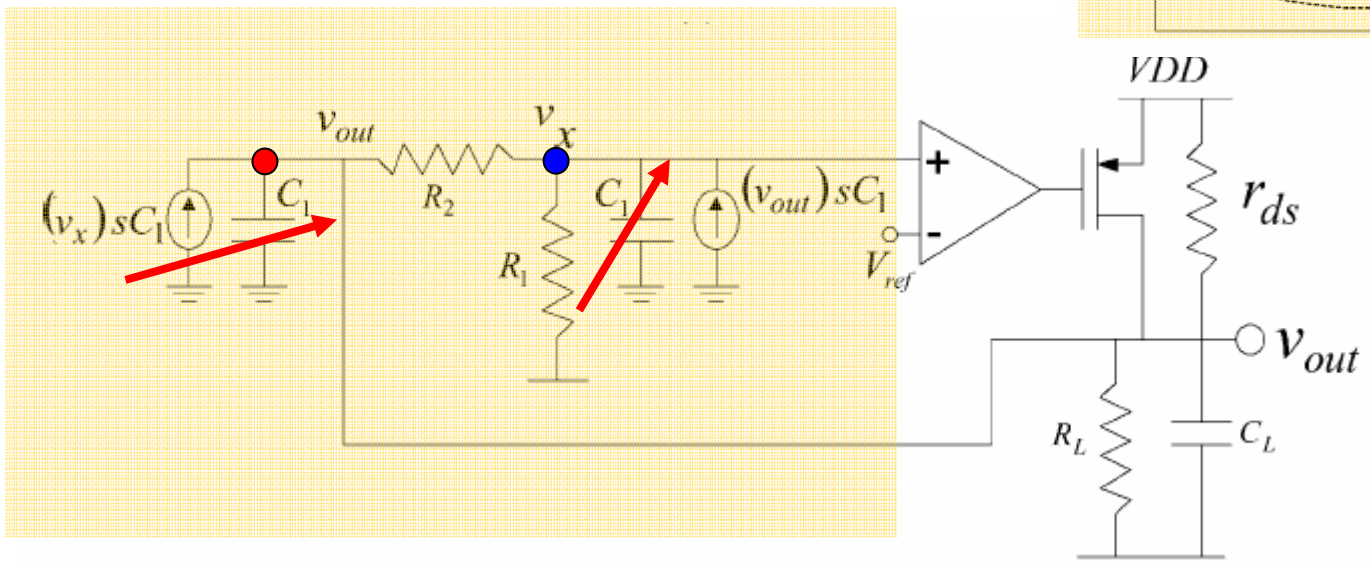
$$\omega_{p2} \approx \frac{1}{R_{par}\left[C_{par}+(1-A_v)C_{gdpass}\right]} \approx \frac{1}{R_{par}\left[C_{par}+g_{mpass}\left(r_{ds} \,//\, (R_1+R_2) \,//\, R_L\right)C_{gdpass}\right]}$$

$$\omega_{p3} = \frac{1}{(R_1 \,//\, R_2) C_1} = \frac{1+\frac{R_2}{R_1}}{R_2 C_1} \longrightarrow \textbf{1.33}$$

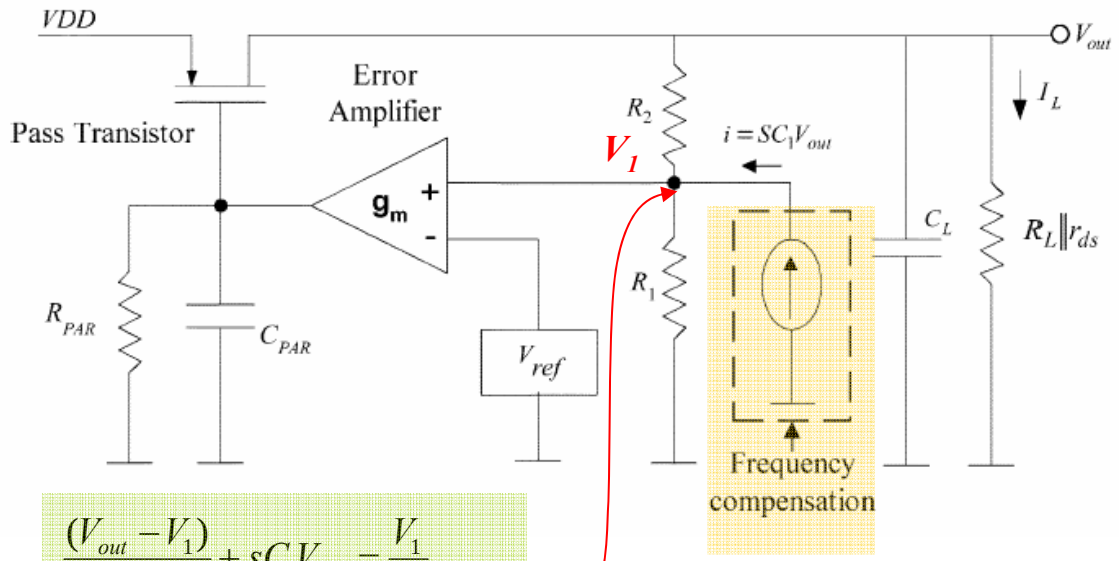
VCCS Method

A drastic improvement in phase margin can be obtained by adding only a zero





- C_1 & $VCCS$ connected to v_{out} do not significantly alter the voltage at that node since C_L is of several μF, whereas C_1 is on the order of few pF
- The capacitor connected to v_x is responsible for the additional pole ω_{p3}
- The $VCCS$ is a differentiator that increases the loop gain



$$\omega_{z1} = \frac{1}{R_2 C_1}$$

$$\omega_{p1} \approx \frac{1}{\left(r_{ds} // \left(R_1 + R_2\right) // R_L\right)\left(C_L - \dfrac{C_1}{1 + \dfrac{R_2}{R_1}}\right)}$$

$$\frac{(V_{out} - V_1)}{R_2} + sC_1V_{out} = \frac{V_1}{R_1}$$

$$V_1 = (R_1 // R_2)(sC_1 + \frac{1}{R_2})V_{out}$$

$$Thus: \frac{V_{out} - V_1}{R_2} = \frac{V_{out}[1 - (R_1 // R_2)(sC_1 + \frac{1}{R_2})]}{R_2} = V_{out}\left[\frac{1}{R_1 + R_2} - \frac{R_1}{R_1 + R_2} sC_1\right]$$

$$\omega_{p2} \approx \frac{1}{R_{par}\left[C_{par} + \left(1 - A_v\right)C_{gdpass}\right]} \approx \frac{1}{R_{par}\left[C_{par} + g_{mpass}\left(r_{ds} // \left(R_1 + R_2\right) // R_L\right)C_{gdpass}\right]}$$

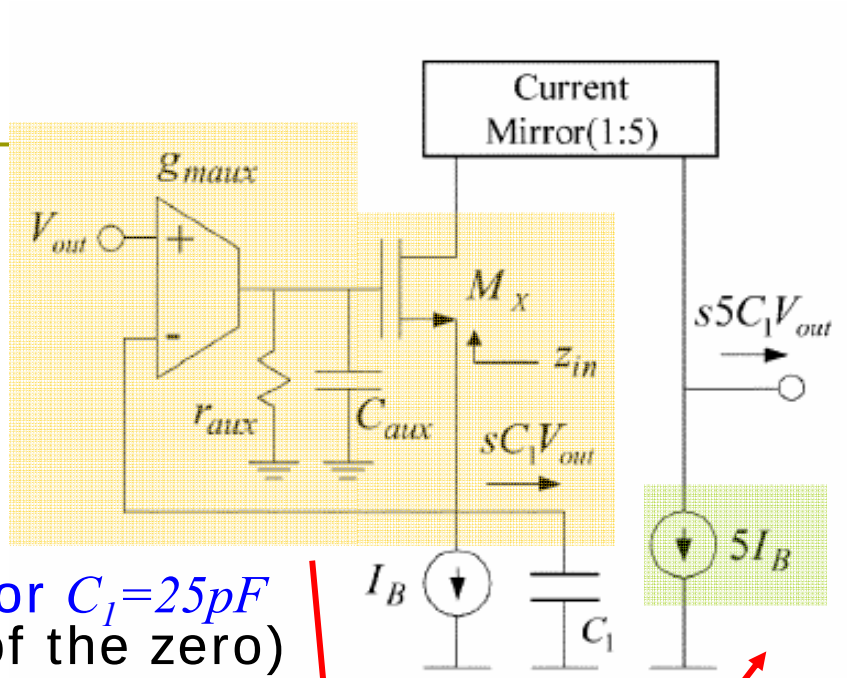
- Pole is almost **not altered** by C_1
- This circuit works only with low *ESR* capacitors as co-existence of *VCCS* generated zero and *ESR* generated zero at low frequencies might make loop gain undesirably high

Parasitic Pole of VCCS Schematic

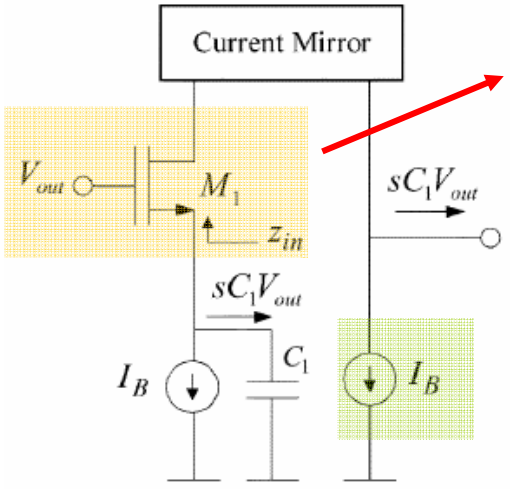
$$Z_{in} = \frac{V_{out}}{i_{out}} = \frac{1}{g_{m1} + sC_1} = \frac{1/C_1}{g_{m1}/C_1 + s}$$

$$pole\ is\ at\ \frac{g_{m1}}{C_1}$$

$$around\ 400kHz\ for\ I_B = 0.5\mu A\ \&\ C_1 = 5pF$$



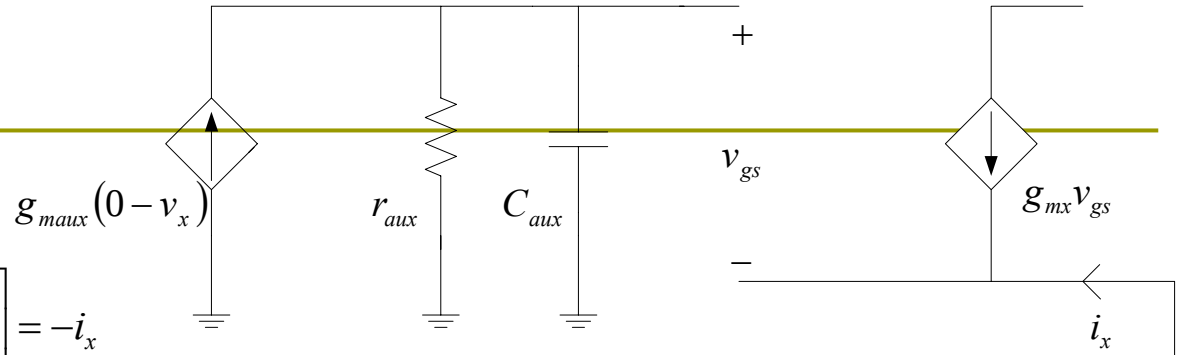
- Push parasitic pole beyond *1MHz* for C_1=*25pF* (required for the proper location of the zero)
  - We need to improve effective g_{m1}



$$G_m = A_{VOTA} \cdot g_{mx}$$

Increase **the effective capacitance** from *5* to *25pF*

Reduced Z_{in}



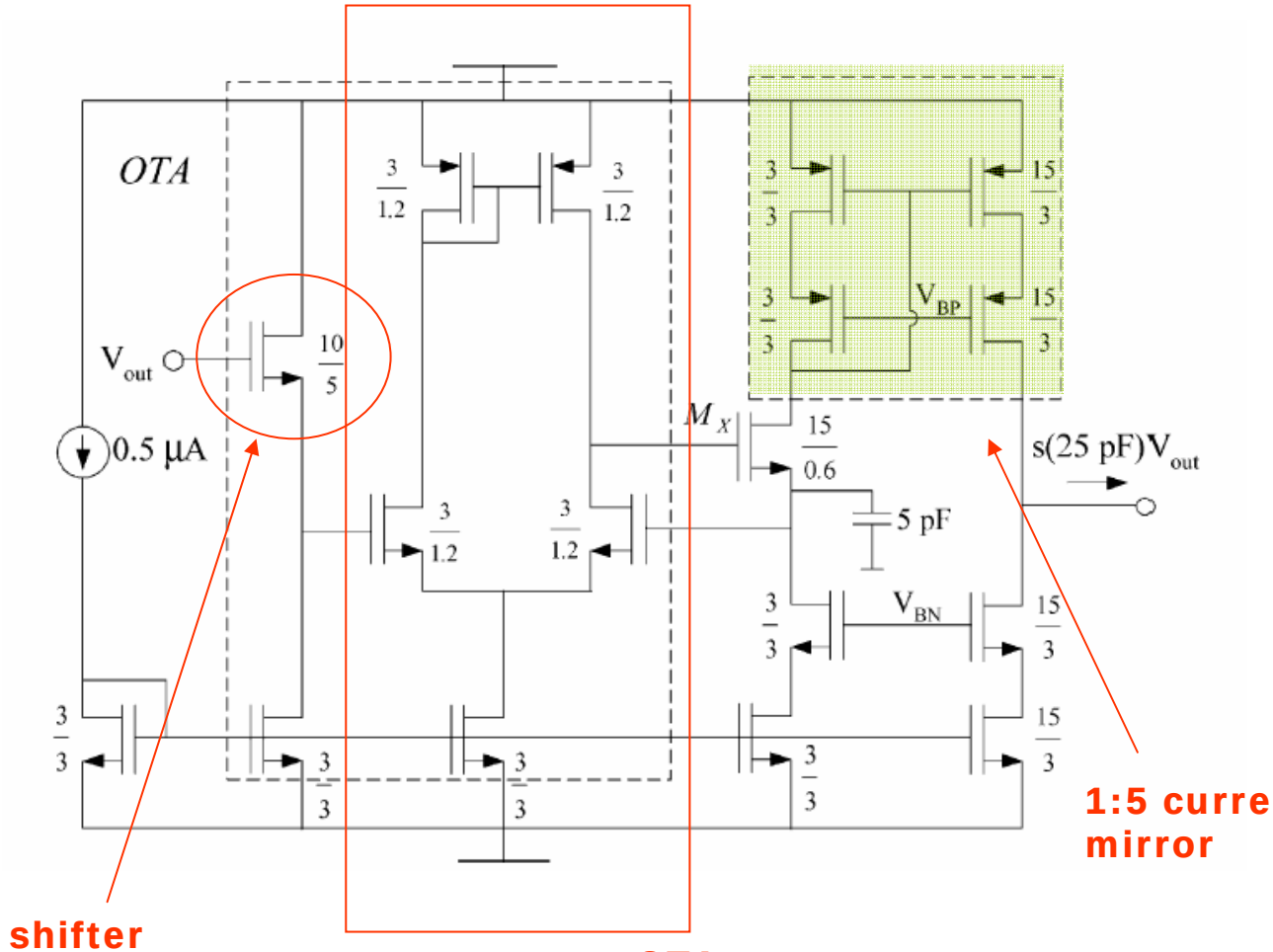
$$g_{mx}\left[g_{maux}(-v_x)\left(r_{aux}\,//\,\frac{1}{sC_{aux}}\right)-v_x\right]=-i_x$$

$$\therefore Z_{in}=\frac{1}{g_{maux}g_{mx}}\left(\frac{r_{aux}+\frac{1}{sC_{aux}}}{\frac{r_{aux}}{sC_{aux}}+\frac{r_{aux}}{g_{maux}}+\frac{1/g_{maux}}{sC_{aux}}}\right)\approx\frac{1}{g_{maux}g_{mx}}\left(\frac{sC_{aux}r_{aux}+1}{r_{aux}+\frac{r_{aux}sC_{aux}}{g_{maux}}}\right)\approx\frac{1}{g_{maux}g_{mx}r_{aux}}\left(\frac{1+s(r_{aux}C_{aux})}{1+\frac{s}{g_{maux}/C_{aux}}}\right)$$

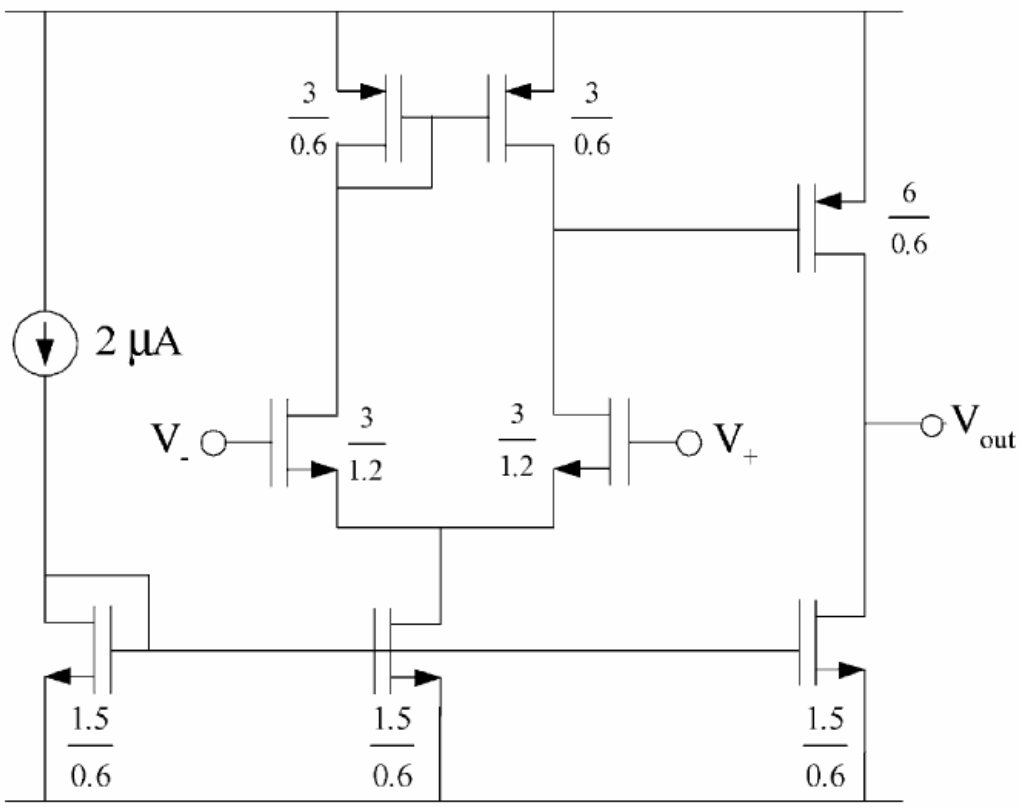
Beyond 2π *5MHz

- The input impedance is very small at low frequencies, collecting all current generated by C_1
  - It is mandatory to reduce $r_{aux}C_{aux}$ to extend the frequency capabilities
- At high frequencies, the Z_{in} increases to $1/g_{mx}$; if $|Z_{in}|<<1/\omega C_1$, the circuit can properly drive C_1 (since the pole is at $sC_1Z_{in}+1=0$)

Transistor level implementation of VCCS with GM enhancement



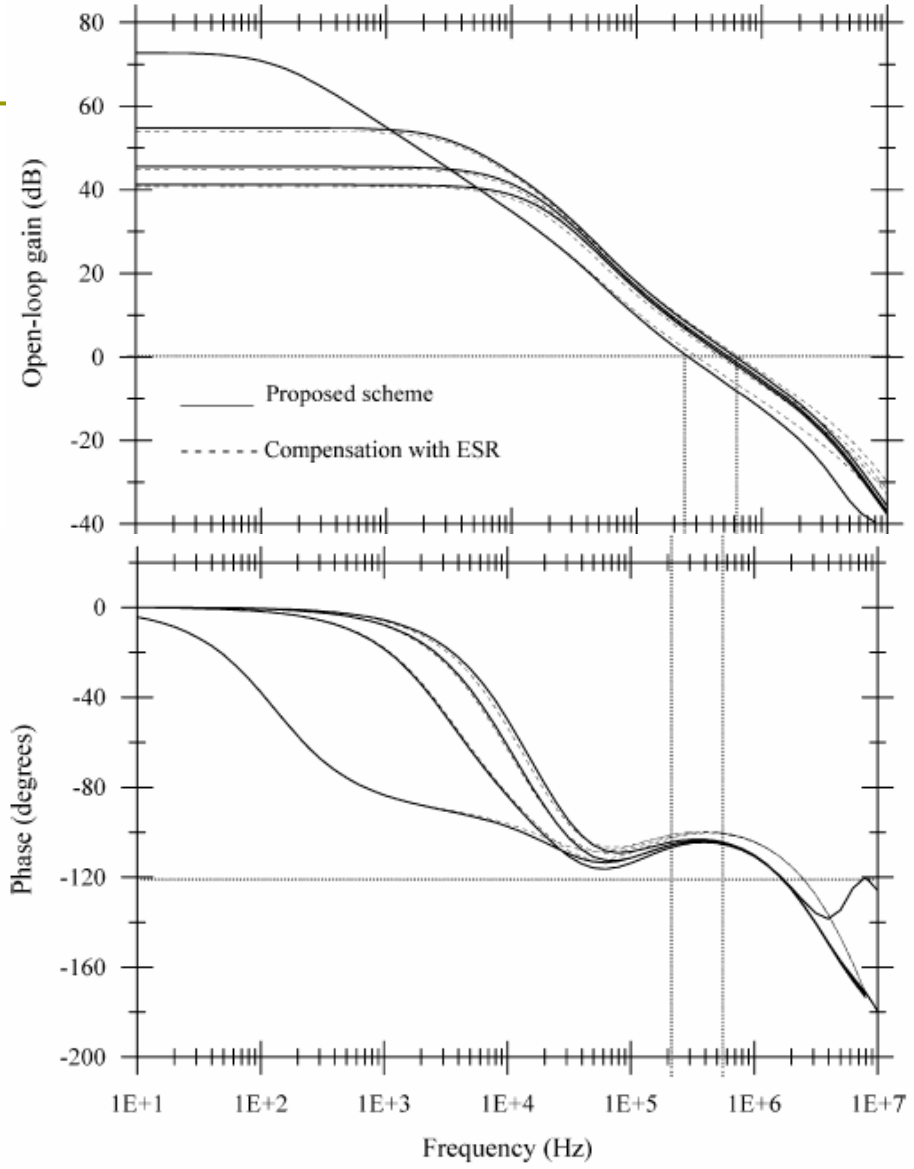
Error Amplifier



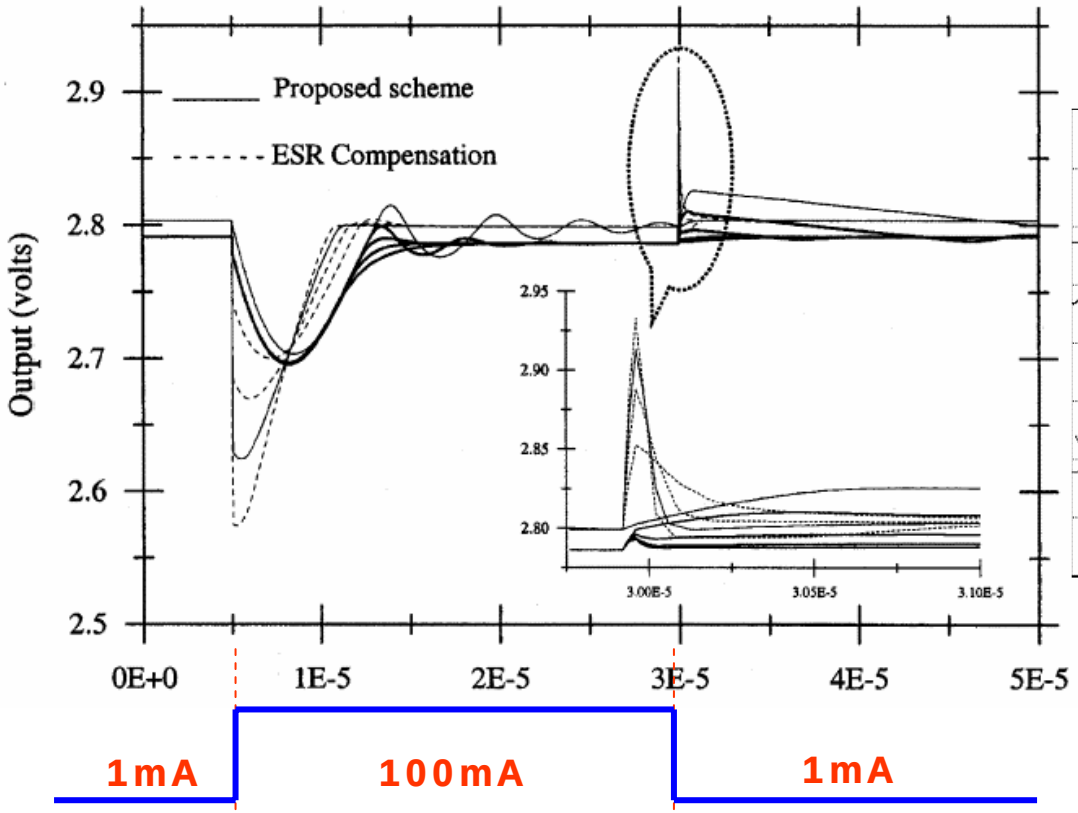
- High dc gain (>60dB) for all loads
- Low output impedance to keep the pole at the input of the pass transistor at high frequencies
- Positive rail output to turn off pass transistor
- Internal poles at significantly higher frequencies compared to cross over loop frequency

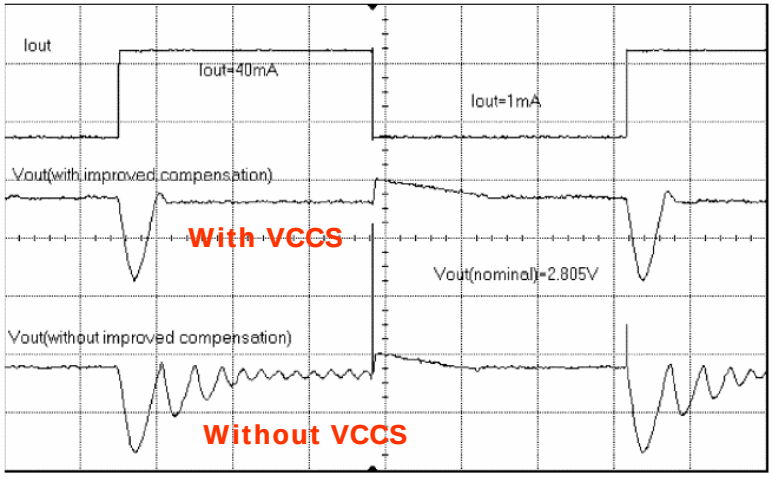
Open-loop Gain

- R_1=120k ohm, R_2=160k ohm
- V_{dd}=3.3V, V_{ref}=1.2V
- C_L=2.2uF
- ESR of C_L < 100m ohm
- Dc output is 2.8V
- Current consumed by LDO is 25uA
- Current consumed by VCCS is 5uA
- Unity gain frequency is in 250 ~ 650kHz
- Phase margin > 60 deg



Load Regulation



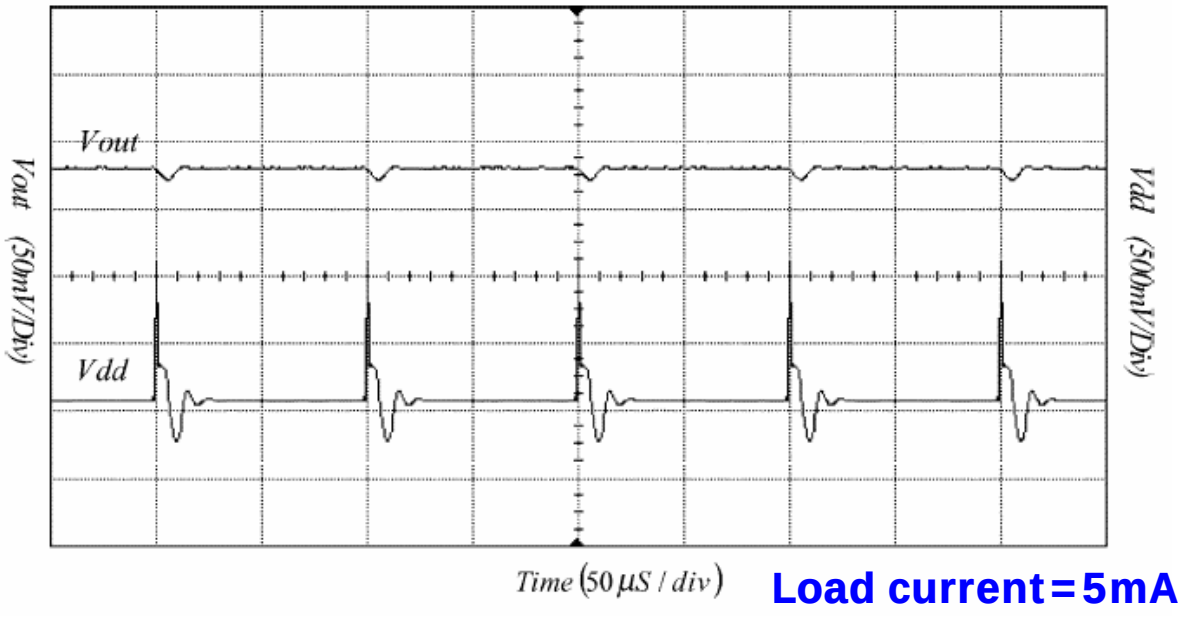


- The compensating circuit is a differentiator, it helps increasing the loop feedback for fast output variations
- ESR increase overshoots

Line Regulation

$100mV_{p\text{-}p}$

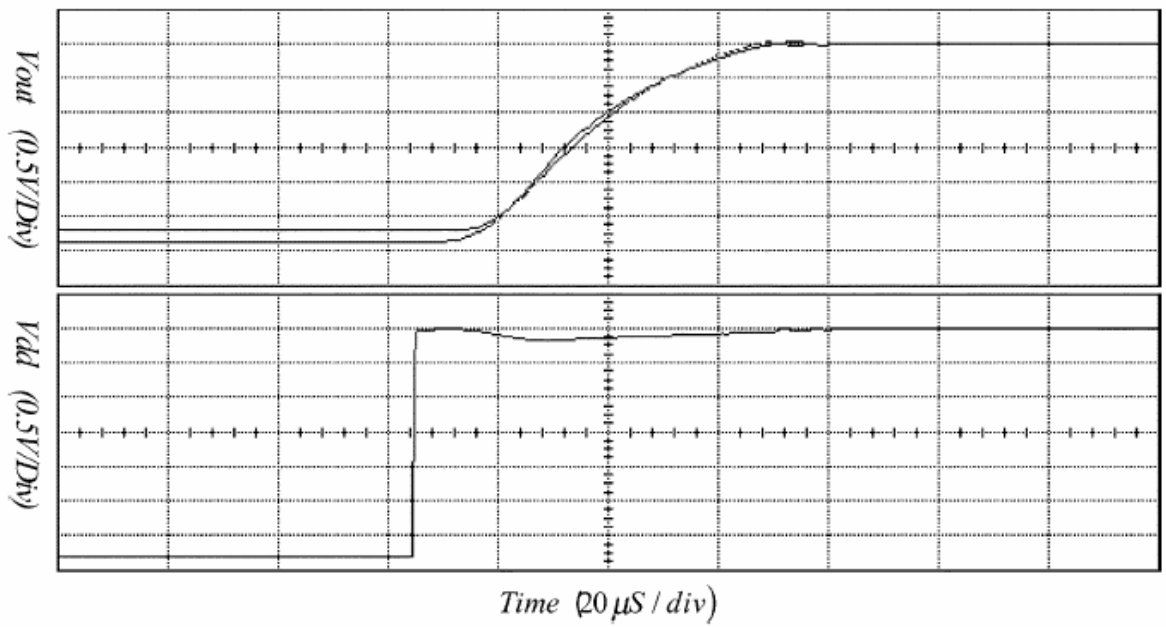
$1V_{p\text{-}p}$



Load current=5mA

- At low frequencies, line regulation (power supply rejection) of the regulator is determined by the loop dc gain since VCCS does not change the loop gain
- High-frequency line regulation is not degraded since VCCS does not add any significant parasitic capacitance from supply voltage to the output

Start-up Time

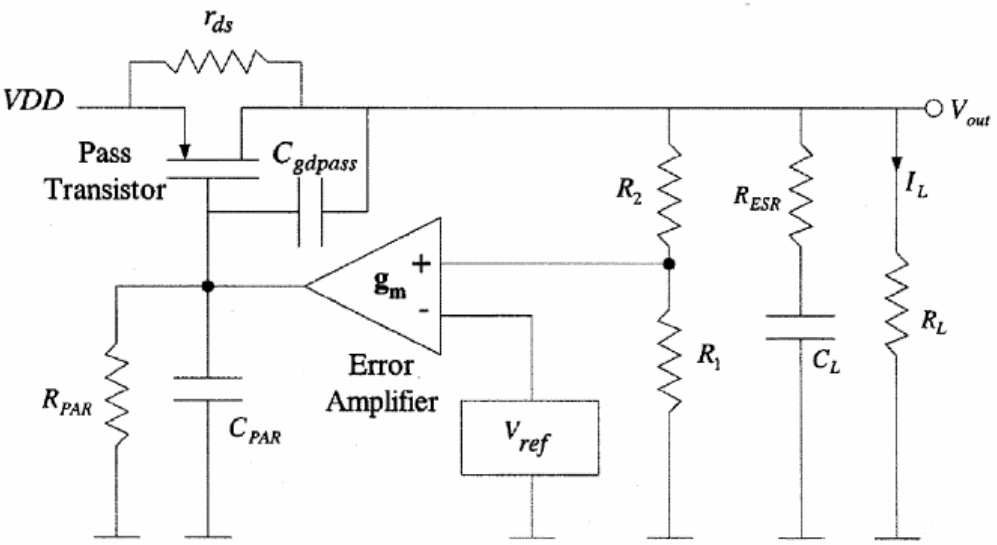


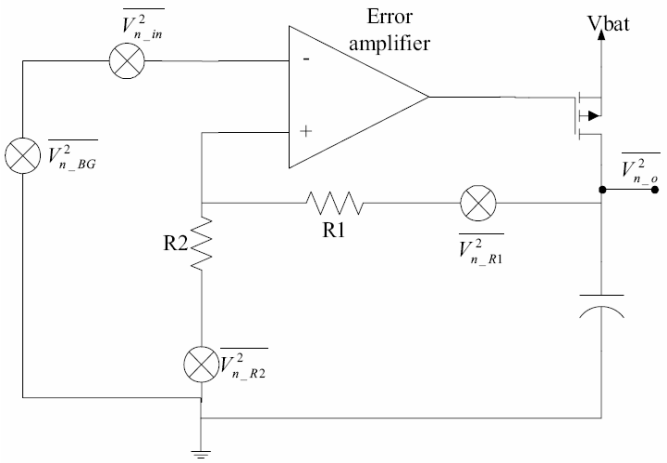
Load current=5mA

- The proposed circuit has similar start-up time compared to the scheme with ESR generated zero
  - The speed limitation comes from the fact that the VCCS has an ideal behavior up to a few megahertz
  - The start-up behavior could be slight different for both cases depending upon high-frequency behavior of the VCCS

Noise Response

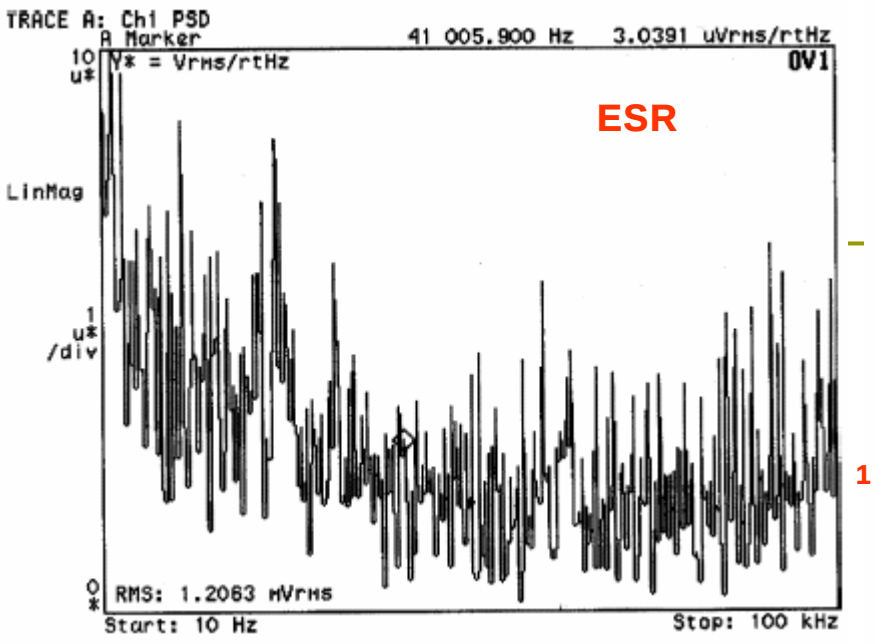
- Four noise components :
  - V_{ref} generator
  - EA
  - Pass transistor
  - Feedback resistor



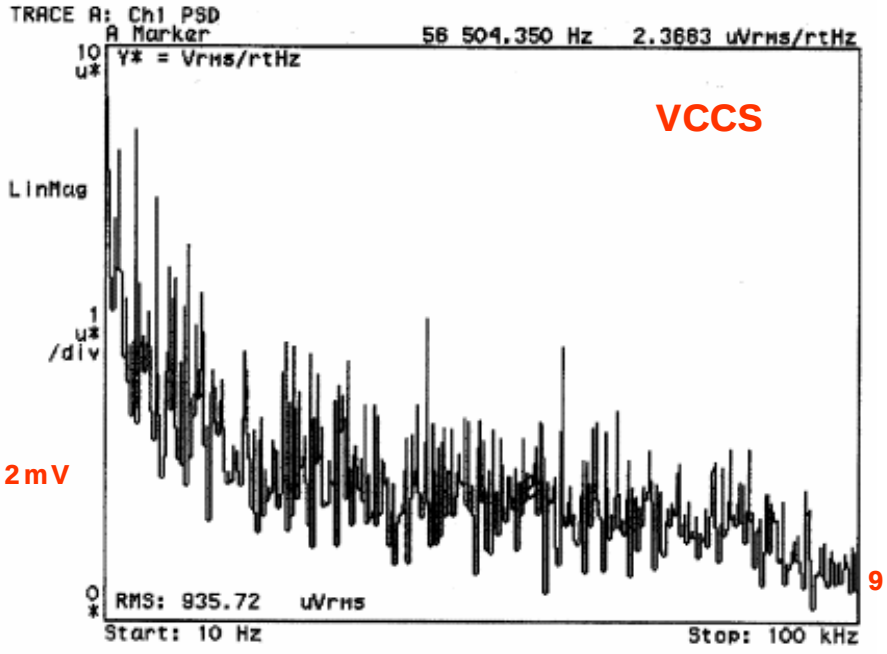


$$\left| \frac{v_{out} / v_{ref,proposed}}{v_{out} / v_{ref,ESR}} \right| = \left| \frac{1}{1 + \frac{s}{\omega_{ESR}}} \right|$$

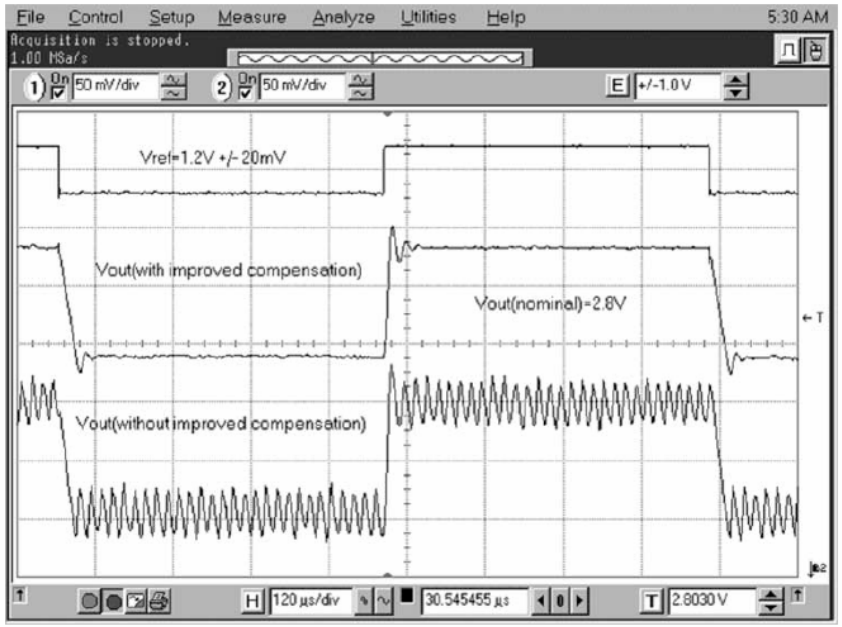
- The zero is generated by additional circuitry (lumped to the VCCS) that is not in the direct path of the noise transfer function
- The high-frequency noise due to the V_{ref} generator, EA, pass transistor is therefore attenuated



1.2mV



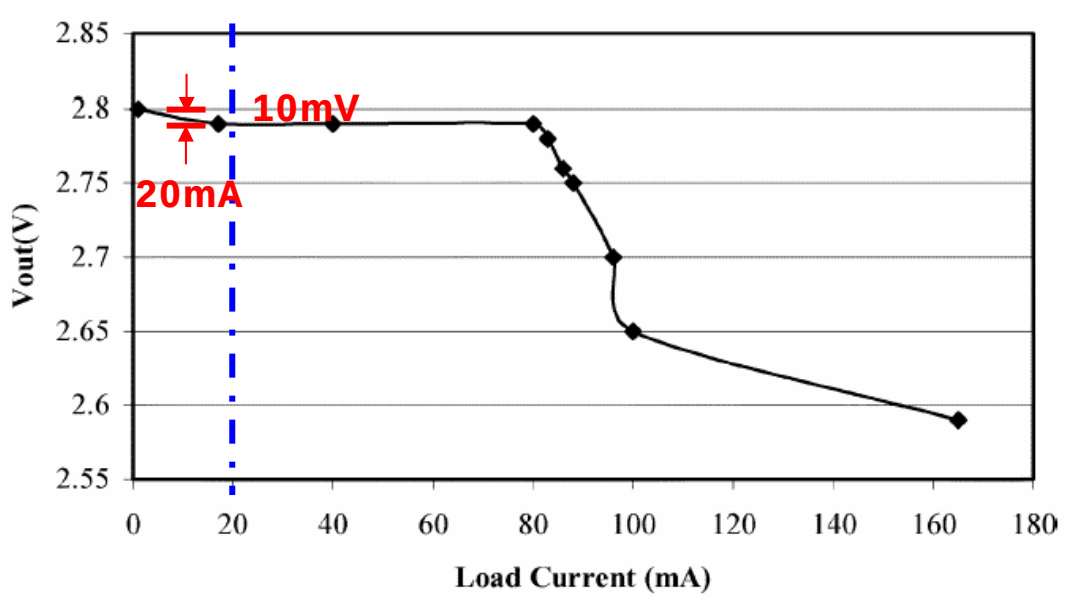
936uV



With VCCS

Without VCCS

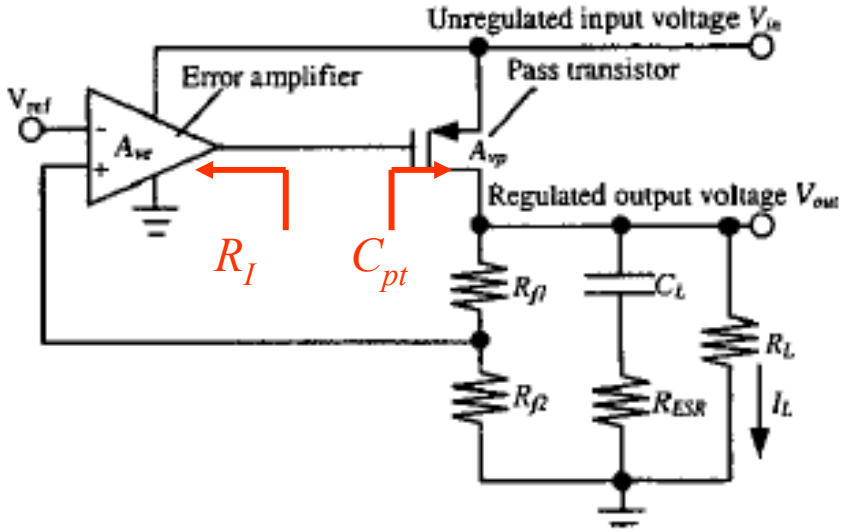
Output Voltage vs. Load Current



- Loop gain increases further for very small current (pass transistor go into subthreshold region and the output resistance of both pass transistor and load increase)
- Another voltage drop in the output voltage occurs when the pass transistor goes into triode region thereby reducing the open-loop gain

Structure of Generic CMOS LDO

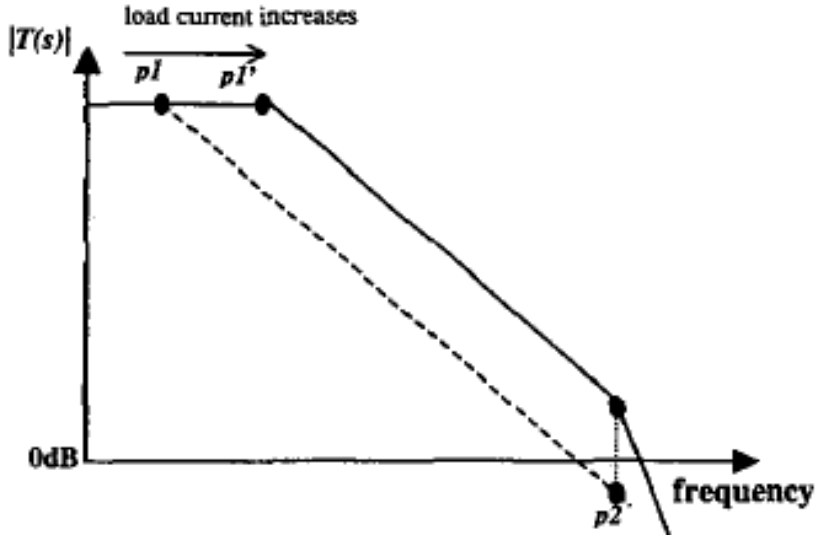
- There are two poles and one zero:
  - $p_1=1/C_L(R_L+R_{esr})$
  - $p_2=1/C_{pt}R_I$
  - $Z_{esr}=1/C_LR_{esr}$



- The pass transistor is CS configuration with negative voltage gain, the feedback signal is connected to positive input of the error amplifier in order to achieve negative feedback loop
- Voltage reference is commonly using a bandgap reference that can work below 5V (The others are zener and buried-zener voltage)

Stability of LDO using Dominant-Pole Compensation

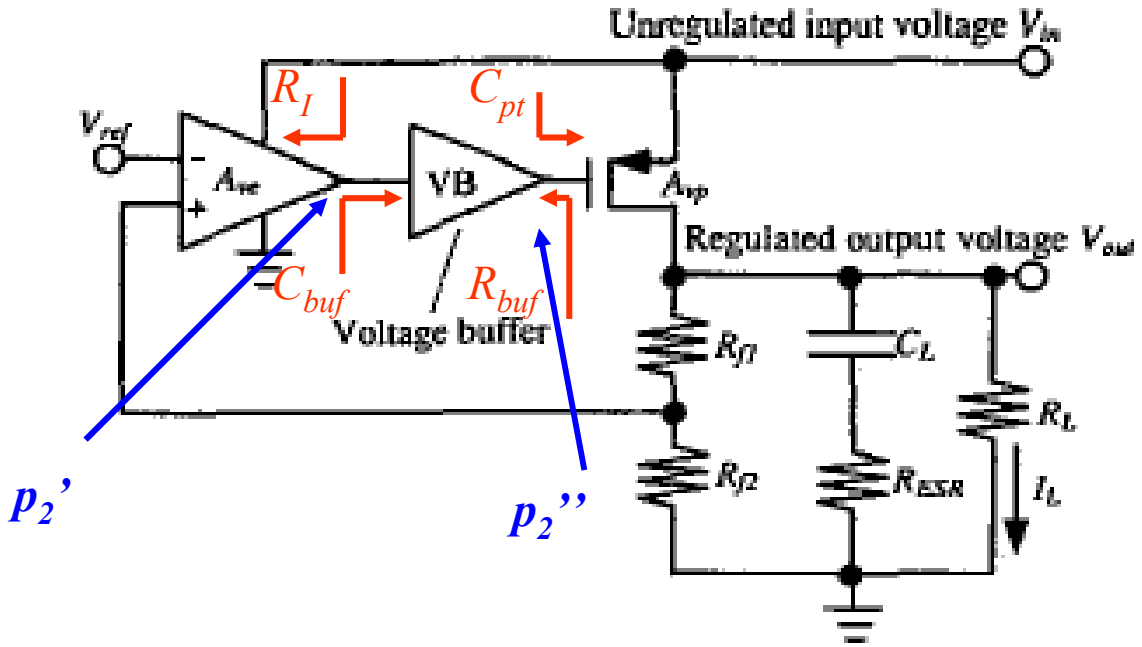
- The smaller ESR has the better load transient performance that is less overshoots and undershoots
  - The ESR zero would not be involved since it locates at a very high frequency
- The dominant pole p_1 is located at a very low frequency, so the required value of C_L is huge



Stability of LDO using Dominant-Pole Compensation (cont'd)

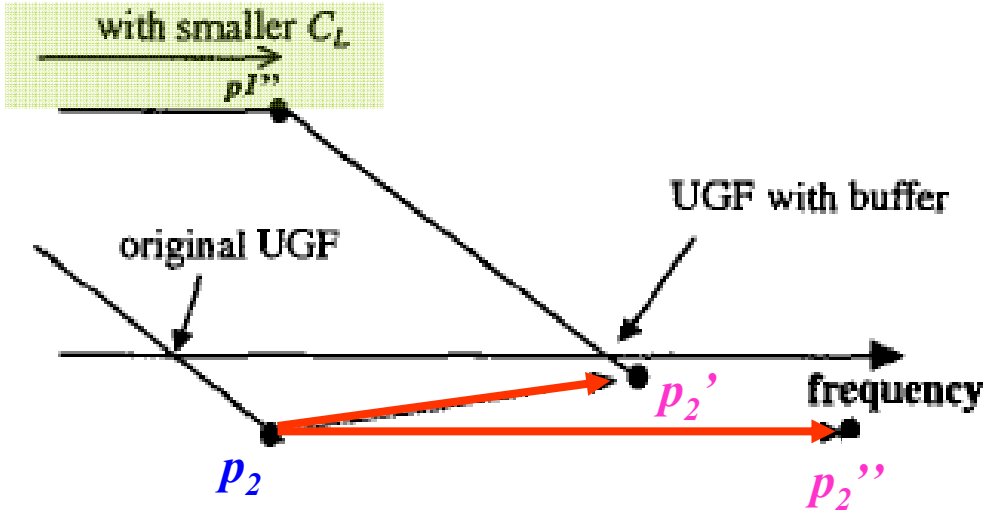
- The dominant pole p_1 is shifted to higher frequency(p_1') for a higher load current and the LDO may be unstable at a certain load
  - P_2 may locate before the unity-gain frequency
  - The generic LDO should be compensated at the maxiumum load current (worst case)
  - The unity-gain frequency of loop gain is constrained by p_2,
    - B.W. is small, loop response is slow.. ($p_2=1/C_{pt}R_1$)
- The LDO using the dominant-pole compensation usually has a narrow Bandwidth and requires a huge capacitor

Stability of LDO using Buffer



- In order to increase the UGF ,a buffer stage can be interposed between the output of the error amplifier and input of the power pass transistor
  - The low frequency p_2 is split into two higher frequency poles p_2' and p_2''
  - $p_2'=1/C_{pt}R_{buf}$, $p_2''=1/C_{buf}R_1$

Stability of LDO using Buffer (cont'd)



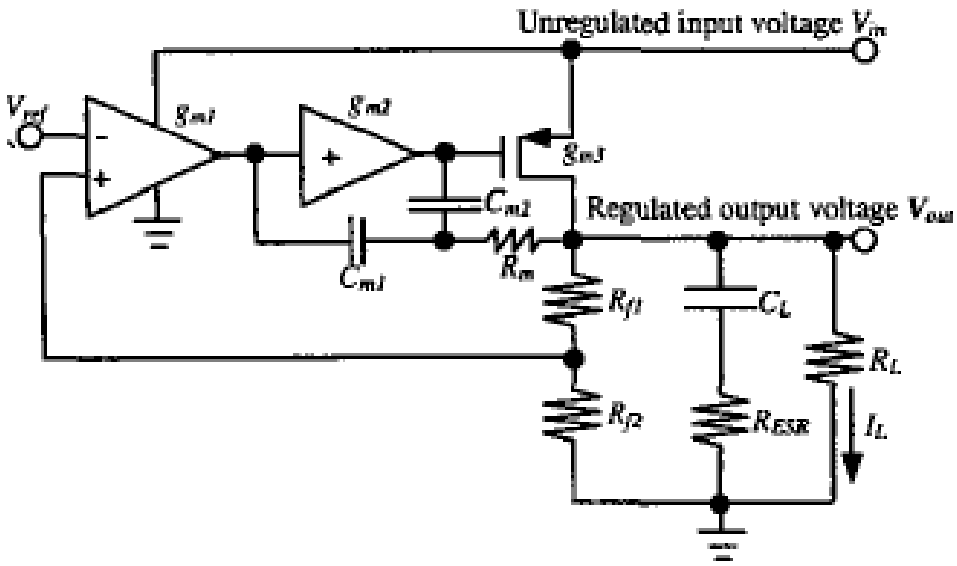
- p_2' and p_2'' are much higher than p_2, because the value of C_{pt} is usually quite large (due to power MOS), therefore p_2' is lower than p_2''
- Since the two split poles are at much higher frequencies, a small C_L can be used where the new dominant pole p_1'' is at a higher frequency, the UGF of LDO increases

Problems of LDO with Buffer in Low-Voltage Design

- A simple way to implement the buffer stage is use a PMOS or NMOS in source-follower
  - There is one V_{GS} drop across the buffer, for low-voltage design (V_{in}~$1.2V$), the power pass transistor can't be either
    - **Fully turned ON** (using PMOS buffer) or
    - **Fully turned OFF** (using NMOS buffer)
  - If the buffer implemented by PMOS transistor, when I_L increases the output transistor of the error amplifier are forced ***to operate in triode region***
    - **So R_I decreases and loop gain decreases**
    - Due to reduction of the loop gain, ***the performance of the load regulation, line regulation and load transient would be greatly degraded***

Advantage and Stability of Nested Miller Compensation for Low-Voltage LDOs

- An error amplifier with two gain stages is used to provide a sufficient voltage gain (g_{m1}, g_{m2})



- Nested Miller compensation technique with nulling resister (R_m) is used to achieve stability *(Cancel Zero)*
- Compensation capacitors C_{m1} and C_{m2} are $4pF$ and $1pF$, respectively
- No large filtering capacitor C_L is required, the whole LDO including the C_L can be integrated into a single chip

Compare three Compensation Type

- Parameters of the LDO with different compensation scheme

	Generic LDO	LDO with a buffer	Three-stage topology
V_{dd}			
C_L	*5uF*	*0.1uF*	*100pF*
R_{ESR}	*20m Ω*	*20m Ω*	
C_{m1}, C_{m2}, R_m			*4pF, 1pF, 10 Ω*

- UFG, PM and low-frequency loop gain of the LDO in different compensation schemes

		I_L=5mA	I_L=10mA	I_L=15mA	I_L=20mA
Generic LDO	UGF	118kHz	162kHz	186kHz	200kHz
	PM	61°	53.4°	50.4°	49°
	A_o	62.4dB	59.6dB	56.4dB	52.9dB
LDO with buffer	UGF	1.53MHz	789kHz	418kHz	237kHz
	PM	60.9°	74.9°	83.3°	89.1°
	A_o	50.6dB	38.6dB	29.9dB	23.2dB
Three stage topology	UGF	4.47MHz	4.41MHz	4.37MHz	4.34MHz
	PM	42.3°	43.3°	43.5°	43.5°
	A_o	96dB	94.9dB	93.8dB	92.6dB

Nested Miller Compensation (NMC)

- The stability condition as per the separate pole approach is given by

$$GBW \le \left(\frac{1}{2}\right) p_2 \le \left(\frac{1}{4}\right) p_3$$

$$\Rightarrow (g_{m1}/C_{m1}) \le \left(\frac{1}{2}\right)(g_{m2}/C_{m2}) \le \left(\frac{1}{4}\right)(g_{mL}/C_L)$$

$$\Rightarrow C_{m1} = 4\left(\frac{g_{m1}}{g_{mL}}\right) C_L \quad \text{and} \quad C_{m2} = 2\left(\frac{g_{m2}}{g_{mL}}\right) C_L$$

This yields large compensation capacitors for large load capacitors

  - Large load capacitors ***limit the GBW to a great extent*** as :

$$GBW = (g_{m1}/C_{m1}) = \left(\frac{1}{4}\right)(g_{mL}/C_L)$$

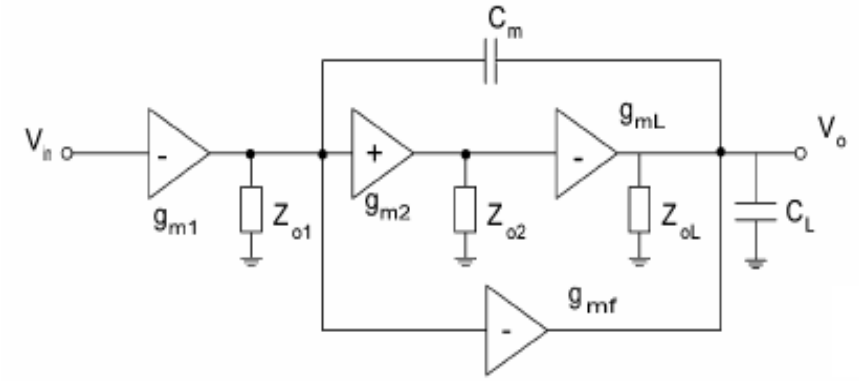
  - ***Smaller compensation capacitors are obtained for larger values of g_{mL}***
    - Not suitable ***for low-power design***, especially when driving large capacitive loads

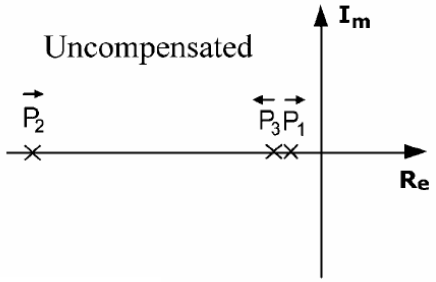
SMC and SMFFC

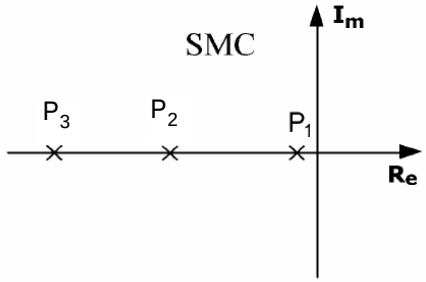
- Two new amplifier topologies
  - SMC (single miller capacitor amplifier)
  - SMFFC (single miller capacitor feedforward frequency compensation amplifier)
- Advantages:
  - Only a small compensation capacitor (C_m)
    - ***Small area***
  - Gain-bandwidth product is improved
  - Large signal and small signal performance is improved
    - Because of the reduction of the size of the compensation capacitor C_m
    - ***No pole-zero doublets*** in the passband for SMC
    - The ***high-frequency pole-zero doublet*** for SMFFC

Single Miller Capacitor Amplifier (SMC)

- Single Miller Capacitor Amplifier (SMC)
  - An additional transconductance stage, g_{mf}, from the output of the first stage to the final output
    - This **forms a push-pull stage** at the output that helps in ***improving the transient response of the amplifier***
  - A single Miller compensation capacitor (C_m) is used to split p_1 and p_3
  - *A judicious distribution* of the total gain among the three stages can stabilize the amplifier
    - p_2 is dictated by the gain of the second stage







Small-Signal Analysis of SMC

$$z_1 = \frac{G_{meff}}{C_m} \text{ (RHP)}$$

$$z_2 = -\left(\frac{g_{p2}}{C_{p2}} + \frac{G_{meff}}{C_m}\right) \text{ (LHP)}$$

$$|z_2| > z_1 \gg p_{1,2,3}$$

- SMC

Two high-frequency zeros

$$A_{v(SMC)}(s) = \frac{A_{dc}\left(1 + s\frac{C_{p2}g_{mf} - C_m g_{o2}}{g_{m2}g_{mL}} - s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}}\right)}{\left(1 + \frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} \cong \frac{\left(1 + s\frac{C_{p2}g_{mf} - C_m g_{o2}}{g_{m2}g_{mL}} - s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}}\right)}{\left(\frac{s}{GBW}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)}$$

Three poles

where $A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$, $P_{-3dB} = \frac{g_{o1}g_{o2}g_L}{g_{m2}g_{mL}C_m}$, $GBW = A_{dc} \bullet P_{-3dB} = \frac{g_{m1}}{C_m}$

Closed-loop with unity-gain feedback $A_{cl(SMC)} \cong \frac{1}{1 + \left(\frac{sC_m}{g_{m1}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)} = \frac{1}{a_0 s^3 + a_1 s^2 + a_2 s + a_3}$

$1/p_2$ $1/p_2 p_3$

$$p_2 = \frac{g_{m2}g_{mL}}{C_L g_{o2}} = \frac{(A_{v2}g_{mL})}{C_L} = \frac{(G_{meff})}{C_L}, \quad p_3 = \frac{g_{o2}}{C_{p2}} - \frac{G_{meff}}{C_L}$$

- Stability: by Routh-Hurwitz Criterion $a_1 a_2 - a_0 a_3 > 0 \Rightarrow \frac{g_{o2}}{C_{p2}} > \frac{g_{m1}}{C_m} = GBW$

Small-Signal Analysis of SMC (cont'd)

- The complex poles and hence high frequency peaking are avoided if

$$\left(\frac{g_{o2}}{C_{p2}}\right)^2 \gg \frac{4g_{m2}g_{mL}}{C_{p2}C_L} \Rightarrow A_{v2}=\frac{g_{m2}}{g_{o2}}<\frac{1}{2}\sqrt{\frac{g_{m2}C_L}{g_{mL}C_{p2}}}$$

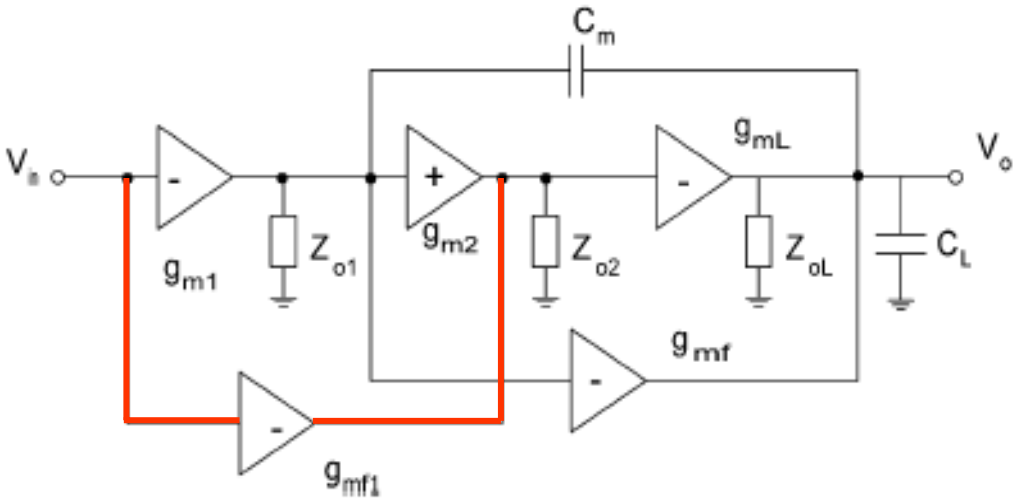
- $GBW<\frac{1}{2}p_2<\frac{1}{4}p_3 \Rightarrow \frac{g_{m1}}{C_m}\le\frac{1}{2}\frac{G_{meff}}{C_L}\le\frac{1}{4}\left(\frac{g_{o2}}{C_{p2}}-\frac{G_{meff}}{C_L}\right) \Rightarrow C_m=\frac{1}{2A_{v2}}\left(4\frac{g_{m1}}{g_{mL}}C_L\right)$
  - Reduce the size of C_m by a factor of $1/(2A_{v2})$ (Slewing better than NMC)
  - The requirement of $g_{mL}>>g_{m1}$ ***no longer needs*** to be satisfied
    - Reduce the power consumption of the amplifier
- Settling response is obtained by
  - ***Maximizing*** the phase margin and
  - ***Avoiding*** pole-zero doublets in the passband of the amplifier
    - No pole-zero doublets in the passband for SMC
- Phase margin: 50 degree

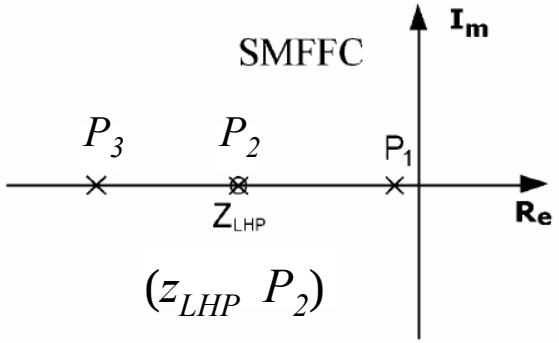
$$PM=180^\circ-\tan^{-1}\left(\frac{GBW}{p_1}\right)-\tan^{-1}\left(\frac{GBW}{p_2}\right)-\tan^{-1}\left(\frac{GBW}{p_3}\right)=180^\circ-90^\circ-\tan^{-1}\left(\frac{1}{2}\right)-\tan^{-1}\left(\frac{1}{4}\right)$$

  - *Use **a feedforward stage** (a LHP zero) to increase the phase margin*

Single Miller Capacitor Feedforward Frequency Compensation Amplifier (SMFFC)

- A feedforward pathe to provide an LHP zero to compensate the first nondominant pole
  - Adds current at the second-stage output
    - ***Increases the output conductance of the stage***
    - Pushes the pole at the output of the second stage ***to higher frequencies***





Small-signal Analysis of SMFFC

- SMFFC

$$A_{v(SMFFC)} = \frac{A_{dc}\left(1 + s\frac{C_m g_{mf1}}{g_{m1}g_{m2}} - s^2\frac{C_m C_{p2}}{g_{m2}g_{mL}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)}$$

z_{LHP}: $+$ term; z_{LHP}, z_{RHP}: $-$ term

LHP: low frequency
RHP: high frequency

where $A_{dc} = \frac{g_{m1}g_{m2}g_{mL}}{g_{o1}g_{o2}g_L}$, $p_{-3dB} = \frac{g_{o1}g_{o2}g_L}{g_{m2}g_{mL}C_m}$, $GBW = A_{dc} \bullet p_{-3dB} = \frac{g_{m1}}{C_m}$

Closed-loop with unity-gain feedback $A_{cl(SMFFC)}(s) \cong \frac{1 + s\frac{g_{mf1}C_m}{g_{m1}g_{m2}}}{1 + s\frac{g_{mf1}C_m}{g_{m1}g_{m2}} + \frac{sC_m}{g_{m1}}\left(1 + s\frac{C_L g_{o2}}{g_{m2}g_{mL}} + s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}}\right)}$

- Stability: by Routh-Hurwitz Criterion: $\frac{g_{o2}}{C_{p2}} > \frac{g_{m1}}{C_m}\left(\frac{1}{1+g_{mf1}/g_{m2}}\right)$
- z_{LHP}, z_{RHP}: $z_{LHP} = \frac{g_{m1}g_{m2}}{g_{mf1}C_m}$, $z_{RHP} = \frac{g_{mf1}g_{mL}}{g_{m1}C_{p2}} + \frac{g_{m1}g_{m2}}{g_{mf1}C_m} \approx \frac{g_{mf1}g_{mL}}{g_{m1}C_{p2}}$

Small-signal analysis of SMFFC (cont'd)

- Phase margin: 75°

$$PM = 180^\circ - \tan^{-1}\left(\frac{GBW}{p_1}\right) - \tan^{-1}\left(\frac{GBW}{p_2}\right) - \tan^{-1}\left(\frac{GBW}{p_3}\right) + \tan^{-1}\left(\frac{GBW}{z_{LHP}}\right)$$

$$= 180^\circ - 90^\circ - \tan^{-1}\left(\frac{1}{2}\right) - \tan^{-1}\left(\frac{1}{4}\right) + \tan^{-1}\left(\frac{1}{2}\right)$$

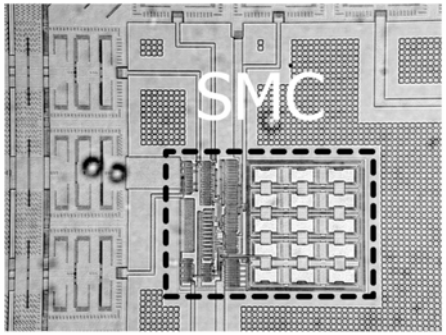
- ***Exact pole-zero cancellation:***

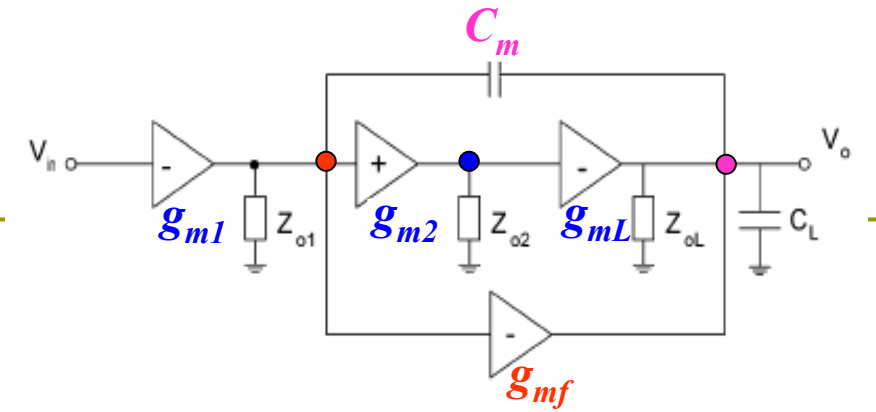
$$p_2 = z_{LHP} = \frac{g_{m1}g_{m2}}{g_{mf1}C_m} \Rightarrow g_{mf1} = \frac{1}{A_{v2}}\frac{g_{m1}g_{m2}C_L}{g_{mL}C_m}$$

  - The pole-zero doublet will ***appear at high frequency*** (around twice the bandwidth), the performance of the amplifier is not significantly disturbed

- C_m can be further reduced to achieve a still higher bandwidth without sacrificing the stability of the amplifier
  - Improve the slew rate of the amplifier

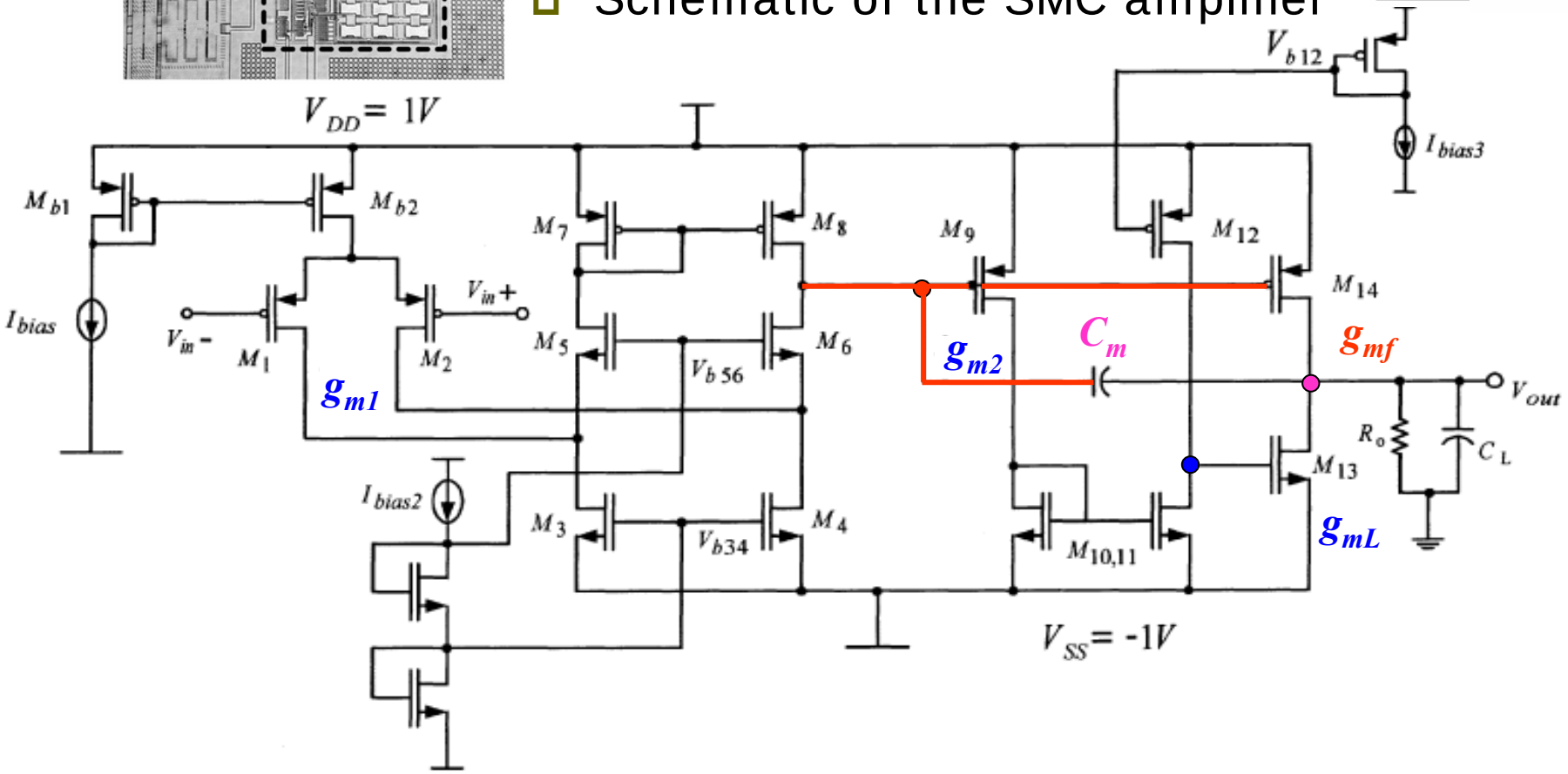
SMC



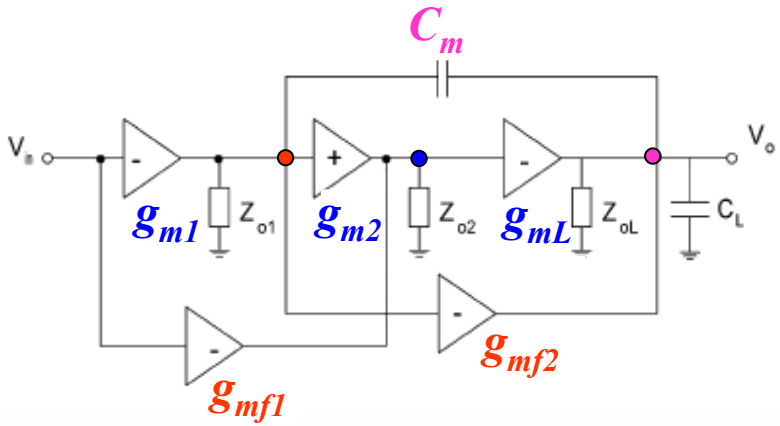


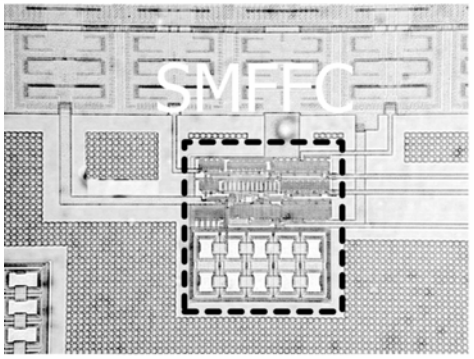
TRANSISTOR	SMC
Mb1	2*(5.55/1.05)
Mb2	8*(5.55/1.05)
M1,2	8*(6.15/0.6)
M3,4	6*(10.05/1.05)
M5,6	2*(10.05/1.05)
M7,8	6*(6.15/1.95)
M9	6*(6.3/0.6)
M10,11	2*(9/0.75)
M12	6*(5.55/0.6)
M14	10*(10.05/0.6)
M13	2*(9.3/0.6)
Mf1,2	-
Mb3	-

- Schematic of the SMC amplifier

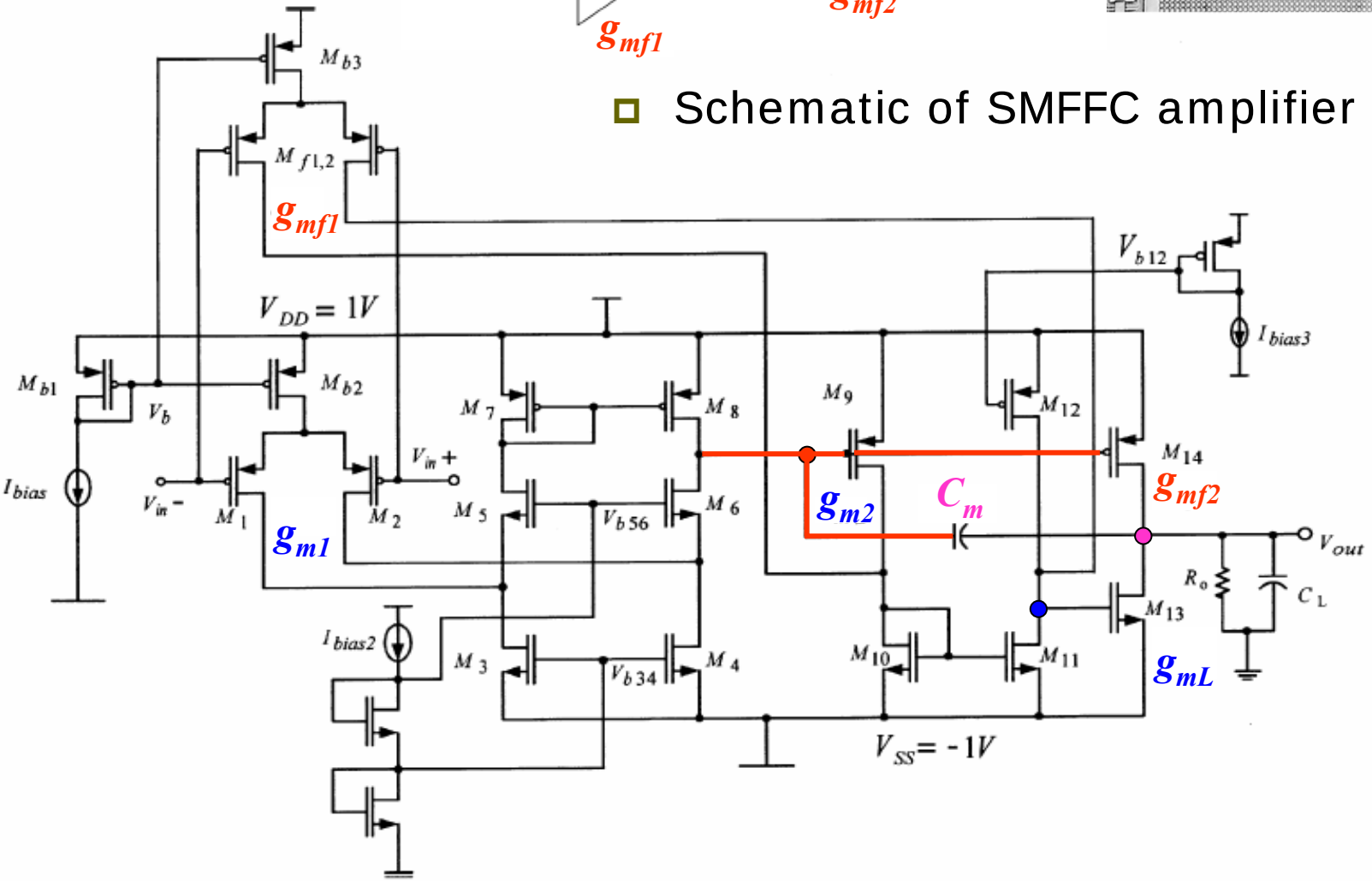


SMFFC





- Schematic of SMFFC amplifier



TRANSISTOR	SMFFC
Mb1	2*(5.55/1.05)
Mb2	8*(5.55/1.05)
M1,2	8*(6.15/0.6)
M3,4	6*(10.05/1.05)
M5,6	2*(10.05/1.05)
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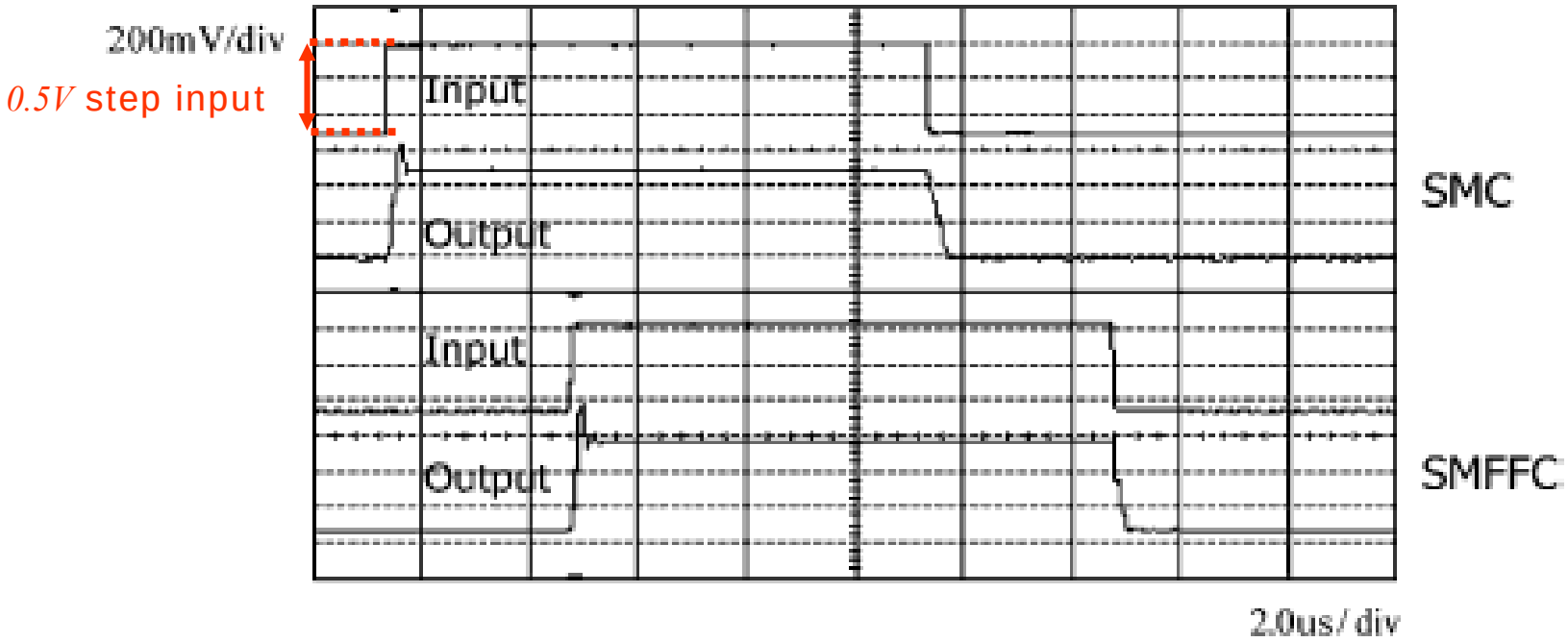
M9	6*(6.3/0.6)
M10,11	2*(9/0.75)
M12	6*(5.55/0.6)
M14	10*(10.05/0.6)
M13	2*(9.3/0.6)
Mf1,2	6*(5.55/0.75)
Mb3	6*(5.55/1.05)

Experimental results (cont'd)

- Transient response



- For the low voltage and the high voltage, the operating points of the transistors in the circuit are different, which means that the effective pole, zero locations of the amplifier are different for rising and falling signals
  - This is the reason why overshoot appears for up-going signal, and not for down-going signal

Comparison

COMPARISON OF DIFFERENT MULTISTAGE AMPLIFIERS WITH LARGE CAPACITIVE LOADS

PARAMETER	NMC [10]	DFCFC [8]	AFFC [10]	DLPC [11]	THIS WORK SMC	THIS WORK SMFFC
Load pF/KΩ	120/25	100/25	120/25	120/25	120/25	120/25
DC gain(dB)	>100	>100	>100	>100	>100	>100
GBW(MHz)	0.4	2.6	4.5	7	4.6	9
Phase margin	61°	43°	65°	46°	58°	57°
Power(mW@Vdd)	0.38 @2	0.42 @	0.4 @2	0.33@1.5	0.38@2	0.41@2
Capacitor Value (pF)	C_{m1}=88 C_{m2}=11	C_{m1}=18 C_{m2}=3	C_m=3 C_a=7	C_a=4.8 C_b=2.5	C_m=7 (one)	C_m=4 (one)
SR+(V/μS) SR-(V/μS)	0.15 0.13	1.32 1.27	0.78 2.20	2.2 4.4	3.28 1.31	4.8 2
+1% TS (μs) -1% TS (μs)	4.9 4.7	0.96 1.37	0.42 0.85	0.315 0.68	0.53 0.4	0.58 0.43
Area(mm^2)	0.140	0.110	0.060	0.050	0.020	0.015
Technology	0.8μm CMOS	0.8μm CMOS	0.8μm CMOS	0.6μm CMOS	0.5μm CMOS	0.5μm CMOS