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A Transient-Enhanced Output-Capacitor-Free Low-Dropout Regulator With Dynamic Miller Compensation

Chenchang Zhan, Guigang Cai, and Wing-Hung Ki

***Abstract*— A transient-enhanced output-capacitor-free low-dropout regulator (LDR) based on dynamic Miller compensation (DMC) is presented in this brief. By utilizing different Miller capacitors to compensate the LDR at different load ranges, the proposed DMC technique can extend the loop bandwidth and enhance the transient performances. The DMC scheme is simple and effective. A proof-of-concept LDR with DMC is designed in a 0.18-μm CMOS process. It has a 100-mA maximum load capability with a quiescent current of 8.5 μA. Measurement results show that the output undershoot/overshoot and recovery time of the proposed LDR with DMC are only 38 mV/0.4 μs and 37 mV/1.22 μs when the load current changes between 100 μA and 100 mA, respectively, whereas they are 45 mV/1.3 μs and 200 mV/4.97 μs without DMC. Line transient responses are also significantly improved by the DMC technique.**

***Index Terms*— Dynamic Miller compensation (DMC), low-dropout regulator (LDR), output-capacitor free (OCF), transient response.**

I. Introduction

Output-capacitor-free (OCF) low-dropout regulators (LDRs) are important building blocks for portable devices to reduce printed circuit board space, cut down the bill of materials cost, and affiliate convenient on-chip power delivery [1]–[3]. However, removing the traditionally employed external capacitor imposes critical design challenges [3]–[6]. In particular, the tradeoff among stability, current consumption, and transient responses is very serious. Various strategies for the design of performance improved OCF LDRs were proposed recently [1]–[10]. Advanced compensation techniques such as Q-reduction [1], active-feedback compensation [2], weighted current feedback [8], and multiple feedback loops [9] were developed to improve loop stability with reasonable silicon estate. Voltage-spike detection techniques [3]–[5] and adaptive biasing combined with subthreshold undershoot reduction [6] were utilized to improve the transient responses. However, the aforementioned compensation techniques were complicated that either introduces serious tradeoff between quiescent current and response speed, or required a large amount of minimum load current such as 1 mA in [4] and 3 mA in [5]. The traditional adaptive biasing was not fast enough which limits the transient response speed and it does not work for light load since the biasing current is not enlarged [6], [10]. Furthermore, the dedicated transient enhancement circuits take a large chip area [3]–[7] and consume extra quiescent current.

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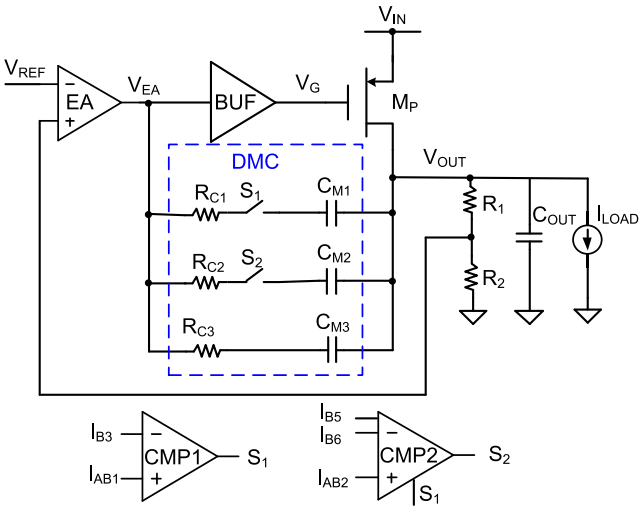

Fig. 1. Topology of the proposed LDR.

In this brief, a transient-enhanced and unity gain frequency (UHF) extended OCF LDR based on dynamic Miller compensation (DMC) is proposed. The compensation network is separated into a number of pieces, and different compensation strengths are used for different loads. Area and power overheads are hence negligible. The remainder of this brief is organized as follows. Section II details the proposed LDR. Measurement results are shown in Section III, and the conclusion is given in Section IV.

II. Proposed LDR With DMC

A. Topology of the Proposed LDR

Fig. 1 shows the structure of the proposed OCF LDR, which consists of an error amplifier (EA), a voltage buffer (BUF), a DMC block with its switches controlled by current comparators, a power MOS transistor, and a voltage divider composed of R_1 and R_2. C_{OUT} represents the effective on-chip loading capacitance. The EA uses adaptive biasing to extend the loop UGF at heavy loads when the output nondominant pole is at high frequency. The buffer is inserted between the EA and the power transistor to improve the slew rate of power FET gate. The DMC block that includes a few Miller compensation paths from V_{EA} to V_{OUT} is proposed to further enhance the transient response and extend the UGF even at light loads.

The DMC control circuit includes two hysteresis current comparators CMP1 and CMP2. At no load, both S_1 and S_2 are "0" and all the three Miller compensation paths are turned ON to make the equivalent Miller capacitor between V_{EA} and V_{OUT} the largest to best stabilize the regulation loop. As I_{LOAD} increases, the output nondominant poles are pushed to a higher frequency, so it is allowed to push the dominant pole to a higher frequency by decreasing the equivalent Miller capacitor. Hence, when I_{LOAD} increases to a certain value, the current comparator CMP1 forces S_1 to be "1" to reduce the

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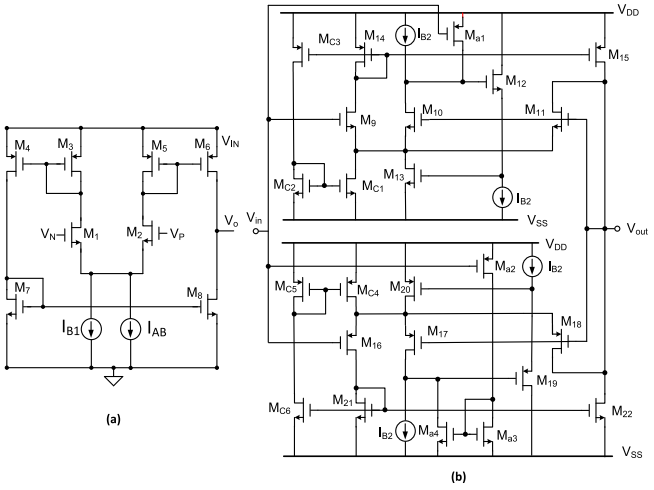

Fig. 2. Schematic of (a) EA and (b) BUF.

equivalent Miller capacitor. As $I_{\rm LOAD}$ further increases to a larger value, the current comparator CMP2 forces S_2 to be "1" to further reduce the equivalent Miller capacitor to its minimum of C_{M3}. In this way, the transient response and loop bandwidth are both improved significantly, compared to using adaptive biasing only, in which case the light load speed is very poor due to the small biasing current of EA and deep subthreshold operation of the power transistor [6]. Furthermore, since the worst case stability at no load requires a large compensation capacitor anyway, the DMC scheme does not consume extra compensation estate. As explained next, it does not take much extra current either. In this brief, the two current thresholds for CMP1 and CMP2 are set to be about 110 μA and 1.25 mA, respectively. At these light loads, the adaptive biasing technique does not help with extending UGF due to the small biasing currents. On the other hand, the DMC technique effectively extends UGF, as the nondominant poles are pushed to high-enough frequencies to allow for cutting C_{M1} and C_{M2} off from the compensation network while still maintaining sufficient phase margins.

B. Implementation of EA and BUF

Fig. 2 shows the schematic of the EA and the buffer. The EA is an adaptively biased current mirror amplifier with a small fixed biasing current and a linear adaptive biasing current $I_{\rm AB}$ proportional to $I_{\rm LOAD}$ generated by a current sensor. The buffer (BUF) is a slew rate-enhanced class-AB unity gain buffer, similar to the class-AB rail-to-rail amplifier introduced in [11]. Note that, for the OCF LDR, the parasitic capacitance at the buffer input is helping with the stability since the dominant pole is at EA output, unlike the typical LDR with an external capacitor, whereby the dominant pole is at the output and the buffer input parasitic capacitance degrades the stability [12]. Therefore, the class-AB amplifier with both nMOS and pMOS input pairs helps to achieve a wide swing buffer without compromising the LDR loop stability. A dynamic biasing network implemented by $M_{a1} - M_{a4}$ is added to the buffer to further enhance the slew rate. Under the light load condition of the LDR, $V_{\rm in}$ for the buffer is high, so $V_{\rm sg}$ of M_{a1} and M_{a2} is small, and the additional current consumption of the buffer is very small. When load current increases, $V_{\rm in}$ drops, $V_{\rm sg}$ of M_{a1} and M_{a2} increases, so as the current through M_{a1} and M_{a2} which improves the speed. Take the pMOS-input part of the buffer as an example, the bias current of M_{16} and M_{18} is determined by the size ratio of $(W/L)_{M16}$:$(W/L)_{M17}$:$(W/L)_{M18}$. Hence, the current through $M_{a2} - M_{a4}$ will increase the current of M_{17} and also that of M_{16} and M_{18} to improve the speed. At heavy load, $V_{\rm in}$ and $V_{\rm out}$ are small, the nMOS-input part of the buffer will not work because of the small $V_{\rm gs}$ of $M_9 - M_{11}$ which saves power.

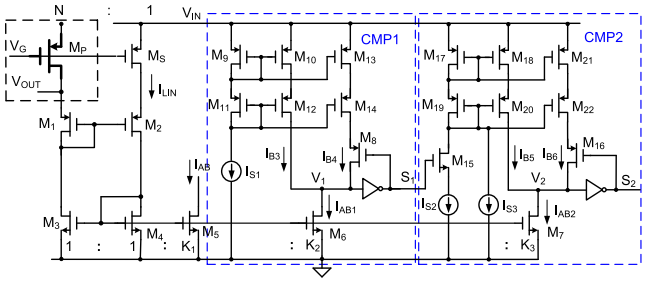

Fig. 3. Schematic of the load current sensor and CMP1 and CMP2.

C. Load Current Sensor and Hysteresis Current Comparators

Fig. 3 shows the load current sensor and the hysteresis current comparators CMP1 and CMP2. Transistors M_1–M_4 act as a common-gate amplifier (startup circuit not shown) and forces the sensing transistor M_S to have the same drain voltage as that of a power transistor. In this design, M_S/M_P = 1/400 and K_1, K_2, and K_3 are 0.025, 2, and 0.4, respectively. Since M_S and M_P share the source and gate terminals as well, we have $I_{\rm AB} = I_{\rm LOAD}/16\,000$, $I_{\rm AB1} = I_{\rm LOAD}/200$, and $I_{\rm AB2} = {\rm I_{LOAD}}/1000$. $I_{\rm AB}$ is used by EA for adaptive biasing, while $I_{\rm AB1}$ and $I_{\rm AB2}$ go through CMP1 and CMP2 for current comparison, respectively.

For CMP1, $I_{\rm S1}$ is 0.1 μA, and $(W/L)_{M9}$:$(W/L)_{M10}$:$(W/L)_{M13}$ = 2:8:1. At zero load, $I_{\rm AB1} = 0$ and so V_1 = "1," $\rm S_1$ = "0," and M_8 is turned ON to allow for I_{B4}. When V_1 = "1," the currents I_{B3} and I_{B4} are almost zero. Therefore, the total quiescent current consumed by CMP1 is only around 0.1 μA. As $I_{\rm LOAD}$ increases to over 110 μA, the current $I_{\rm AB1}$ rises to larger than the sum of I_{B3} and I_{B4}, then V_1 = "0," $\rm S_1$ = "1," and M_8 is turned OFF to disconnect I_{B4}. When $\rm S_1$ = "1," the equivalent compensation capacitance becomes smaller, and hence, the load transient performance and the UGF are improved. As the load current decreases to about 100 μA, the current $I_{\rm AB1}$ falls to be smaller than I_{B3}, then V_1 = "1," $\rm S_1$ = "0," and M_8 is turned ON again. The current hysteresis of the two turning points is about 30 μA when taking channel length modulation into account.

For CMP2, $I_{\rm S2}$ is 0.2 μA and $I_{\rm S3}$ is 0.05 μA, and $(W/L)_{M17}$:$(W/L)_{M18}$:$(W/L)_{M21}$ = 2:8:1. When $\rm S_1$ = "0," M_{15} is turned OFF, so only $I_{\rm S3}$ goes to transistor M_{17}. When $\rm S_1$ = "1," M_{15} is turned ON, so both $I_{\rm S2}$ and $I_{\rm S3}$ go to M_{17}. At zero load, $I_{\rm AB2} = 0$ and so V_2 = "1," $\rm S_2$ = "0," and then M_{16} is turned ON. When V_2 = "1," the currents I_{B5} and I_{B6} are almost zero. Therefore, the total quiescent current consumed by CMP2 is only 0.05 μA. As $I_{\rm LOAD}$ increases to about 1.25 mA, the current $I_{\rm AB2}$ rises to larger than the summation of I_{B5} and I_{B6}, then V_2 = "0," $\rm S_2$ = "1," and M_{16} is turned OFF. When $\rm S_2$ = "1," the equivalent compensation capacitance becomes further smaller to enhance the LDR speed. As the load current decreases to about 1 mA, the current $I_{\rm AB2}$ falls to smaller than I_{B5}, then V_2 = "1," $\rm S_2$ = "0," and M_{16} is turned ON again. The current hysteresis of the two turning points is about 0.25 mA. Put it qualitatively, with the hysteresis introduced in the current comparators, small variations of $I_{\rm LOAD}$ will not switch ON or OFF the dynamic compensation paths, avoiding the oscillations that may otherwise occur. For large load changes, appropriate compensation network is used, and the Miller compensation of the whole LDR helps guarantee the loop stability.

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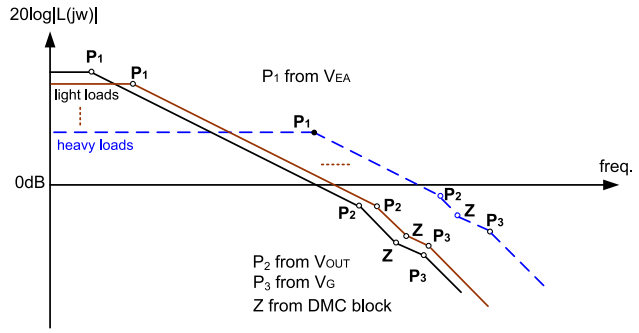

Fig. 4. Loop gain of the proposed LDR (magnitude plot only and not in scale).

D. Stability Analysis

Loop stability of the whole LDR is briefly analyzed in this section. The loop-gain transfer function of the LDR with Miller compensation is approximately given as

$$T(s) = \frac{G_{m1}G_{m2}R_{O1}R_{\rm OUT}[1+sC_m(R_C-1/G_{m2})]}{(1+sC_mG_{m2}R_{O1}R_{\rm OUT})(1+sC_{\rm OUT}/G_{m2})(1+sC_{\rm GP}R_{\rm BUF})} \quad (1)$$

where G_{m1} and G_{m2} and R_{O1} and $R_{\rm OUT}$ are the effective transconductances and output resistance of EA and power stage, respectively; R_C and C_m are the equivalent connected Miller compensation resistance and capacitance; and $R_{\rm BUF}$ and $C_{\rm GP}$ are the output resistance of the buffer and the gate capacitance of M_P. The dominant pole $p_1 = 1/(C_mG_{m2}R_{o1}R_{\rm OUT})$ is produced at the EA's output ($V_{\rm EA}$) due to its large equivalent output resistance and the large Miller compensation capacitor. The nondominant poles $p_2 = 1/(C_{\rm GP}R_{\rm BUF})$ and $p_3 = (G_{m2}/C_{\rm OUT})$ occur at the gate of the power transistor M_P (V_G) and the LDR output ($V_{\rm OUT}$), respectively. The resistors R_{C1}, R_{C2}, and R_{C3} help to reduce the voltage glitches caused by switching networks during the transition. In addition, when the equivalent $R_C > 1/G_{m2}$, a left-half-plane (LHP) zero will be created which helps improve the phase margin. However, a too large R_C will affect the Miller frequency compensation and the pole-splitting effect. In this brief, C_{M1}, C_{M2}, and C_{M3} are 7, 2, and 1 pF, while R_{C1}, R_{C2}, and R_{C3} are 46.6, 46.6, and 9.6 kΩ, respectively.

Fig. 4 illustrates the main poles and zeros of the loop gain at different load currents. At no load, the full DMC network is used for compensation and the loop-gain UGF is small. When $I_{\rm LOAD}$ increases to beyond 110 μA and 1.25 mA, C_{M1} and then C_{M2} is disconnected from compensation to improve the UGF, while without compromising stability due to the enlarged output nondominant pole. At heavy load, due to adaptive biasing, the UGF is extended as well by enlarging the transconductance of EA transistors. Fig. 5(a) and (b) shows the simulated loop-gain Bode plots at various load currents comparing the case with and without DMC technique, respectively, when the output parasitic capacitor $C_{\rm OUT}$ is 100 pF. As can be observed, the no-load (1-μA load, exactly) loop gains are similar for with and without DMC since both cases use the largest compensation network. However, compared with the design with only adaptive biasing but without DMC, the loop-gain UGF at 200 μA, 2 mA, and 100 mA are extended from 549 kHz, 909 kHz, and 16.4 MHz to 1.8, 4.7, and 22.5 MHz, respectively, due to the smaller Miller compensation capacitances. As a result, further enhanced speeds can be achieved effectively without requiring much extra area or power consumptions. Note that for the case of without DMC, the larger compensation capacitor together with the resistors lead to lower LHP zero which helps improve UGF and PM, so the UGF extension at heavy load is not much significant.

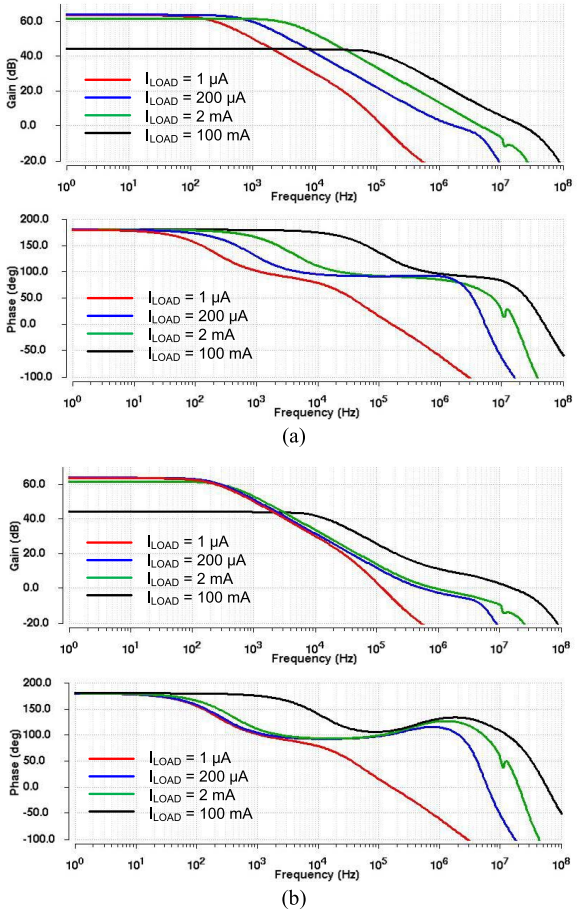

Fig. 5. Frequency responses (a) with proposed DMC and (b) without DMC ($V_{\rm IN}$ = 1.2 V, $V_{\rm OUT}$ = 1.0 V).

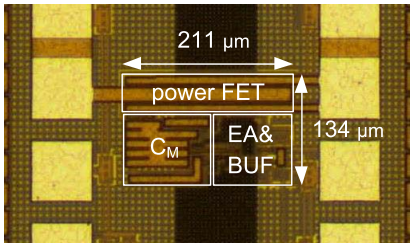

Fig. 6. Chip micrograph of the proposed LDR.

III. Measurement Results

The proposed DMC LDR was fabricated in a standard 0.18-μm CMOS technology. Fig. 6 shows the chip photograph. For comparison, the DMC technique can be turned ON and OFF by an off-chip control signal. The total active area of the LDR is 0.028 mm^2. The input voltage ranges from 1.2 to 1.8 V with 1.0 V output voltage and a maximum load current of 100 mA. A capacitor of 100 pF is used to emulate the parasitic load capacitance. Measured load regulation and line regulation is 0.13 mV/mA and 5 mV/V, respectively. Measured PSR at 100 mA is -30 and -17.5 dB at 10 kHz and 1 MHz, respectively. The measured quiescent current at no load is 8.5 μA.

Figs. 7–9 show the measured load transient responses of the LDR when $I_{\rm LOAD}$ steps between 0 and 100 mA, 0.1 and 100 mA, and

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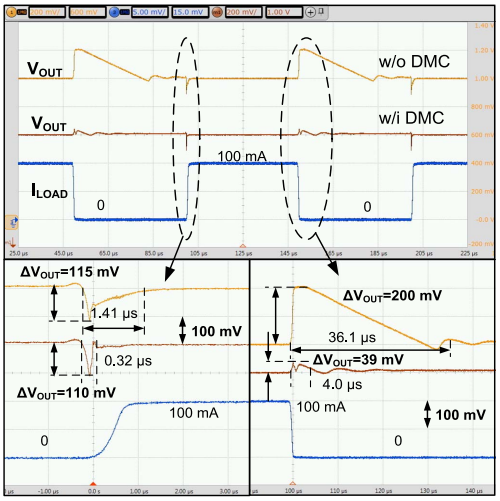

Fig. 7. Measured transient response with I_{LOAD} steps between 0 and 100 mA.

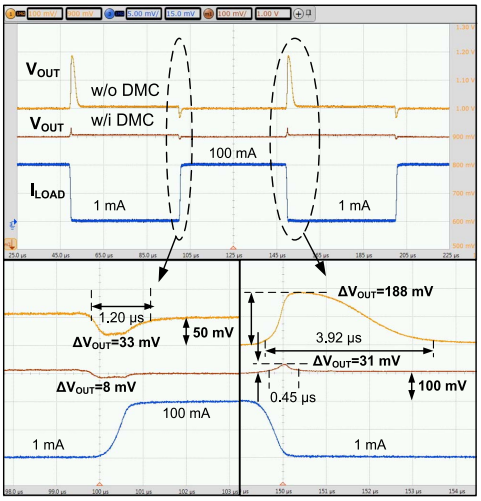

Fig. 9. Measured transient response with I_{LOAD} steps between 1 and 100 mA.

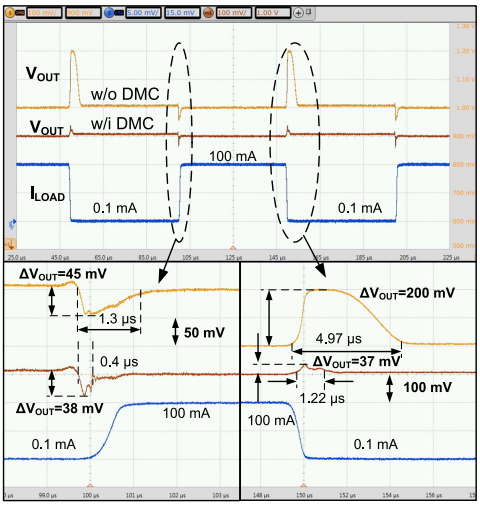

Fig. 8. Measured transient response with I_{LOAD} steps between 0.1 and 100 mA.

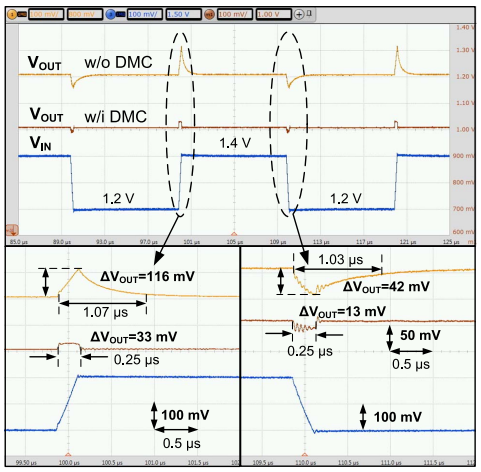

Fig. 10. Measured Line transient responses at 10-mA load current.

1 and 100 mA with around 500-ns edge time, respectively, comparing the case of with and without DMC (both with adaptive biasing). The undershoot/overshoot voltages are reduced from −115/+200 mV, −45/+200 mV, and −33/+188 mV for LDR without DMC to −110/+39 mV, −38/+37 mV, and −8/+31 mV for LDR with DMC, respectively. In addition, the undershoot recovery/overshoot recovery time for the LDR with DMC are 0.32/4.0 μs, 0.4/1.22 μs, and 0.1 and 0.45 μs, respectively, much shorter than those without DMC which are 1.41/36.1 μs, 1.3/4.97 μs, and 1.2/3.92 μs, respectively.

Fig. 10 shows the measured line transient response at 10-mA load current when V_{IN} jumps between 1.2 and 1.4 V with an edge time of around 200 ns. The overshoot and undershoot are 33 and 13 mV for LDR with DMC, whereas they are 116 and 42 mV without DMC, reduced by 71.6% and 69.0%. Moreover, the recovery time is significantly reduced from 1.07/1.03 μs to 0.25/0.25 μs when using DMC. Fig. 11 shows the quiescent current I_Q and current efficiency η_C versus load current I_{LOAD}. The maximum current efficiency is 99.7%. Small quiescent current at light load and high current efficiency at heavy load are both maintained.

Table I summarizes and compares the performances of the proposed LDR with some recently reported designs. The OCF LDR

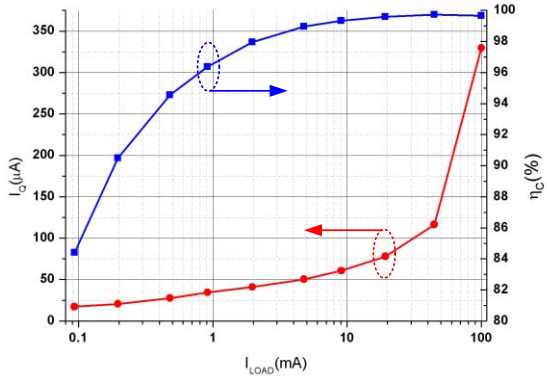

Fig. 11. Quiescent current I_Q and current efficiency η_C versus load current.

figure of merit (FOM) in [5] is adopted for load transient comparison, given by FOM $= K * \Delta V_{\mathrm{OUT}} * I_Q / \Delta I_{\mathrm{LOAD}}$, where K is the edge time ratio between the measurement setup and the smallest one in the comparison group. The proposed LDR with DMC achieves competitive performances.

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TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ARTS

Parameter	[4]	[5]	[6]	[7]	[8]	[9]	[10]	**This Work**		
Year	2010	2010	2012	2014	2014	2016	2015	**2017**		
Technology /µm	0.35	0.09	0.35	0.065	0.065	0.5	0.13	**0.18**		
V_{IN} /V	1.4	0.75	1.2	0.75-1.2	0.75-1.2	2.3-5.5	1	**1.2**		
V_{DROP} /V	0.2	0.25	0.2	0.25	0.2	>0.1	0.2	**0.2**		
$I_{LOAD(MAX)}$ /mA	100	100	100	50	50	150	100	**100**		
$I_{LOAD(MIN)}$ /mA	1	3	0	0	0	0	0.001	**0.005 (for PM≥45°)**		
I_Q /µA	43	8	28	16.2	15.9	40	2.9	**8.5**		
Compensation capacitor	6 pF	7 pF	10pF	2 pF	4.1 pF	29 pF	3.8pF	**10 pF**		
PSR (dB) @ freq	N/A	0dB @ 1MHz	-13.2dB @ 1MHz	-46dB @ 1KHz	-51dB @ 1KHz	57.75dB @ 10KHz	N/A	**-30dB@ 10kHz -21dB@ 1MHz**		
ΔI_{Load} /mA	99	97	100	50	50	150	100	**100**	**99.9**	**99**
Edge time Δt/µs	1	0.1	1	0.1	0.1	1	0.8	**0.5**	**0.5**	**0.5**
$-\Delta V_{OUT}$ /mV	70	76	105	103	113	96	120	**110**	**38**	**8**
$+\Delta V_{OUT}$ /mV	70	114	50	100	29	120	90	**39**	**37**	**31**
Edge time ratio K	10	1	10	1	1	10	8	**5**	**5**	**5**
FOM /µV	304.0	9.4	294.0	33.4	35.9	320	27.84	**46.75**	**16.17**	**13.31**

IV. CONCLUSION

An OCF LDR with fast transient response using DMC has been presented. By utilizing different compensation strengths at different load currents, the DMC technique effectively extends the loop-gain UGF even at the light loads. Hence, speed is dramatically improved, with the simple strategy which does not incur much cost overhead. Measurement results demonstrated the LDR with DMC achieves fast load and line transient responses, making it a good candidate for SoC power management.

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