

Two-Stage Large Capacitive Load Amplifier with Embedded Capacitor-Multiplier Compensation

Zushu Yan

Beijing Microelectronics Technology Institute, Beijing, China

E-mail: yanzushu@yahoo.com.cn

Abstract—This paper proposes a low-voltage, low-power, two-stage operational transconductance amplifier (OTA) for driving large capacitive loads. The embedded capacitor-multiplier compensation mechanism facilitates using a very small Miller capacitor which generates widely separated left-half-plane (LHP) poles without introducing a right-half-plane (RHP) zero. Besides, it provides a feedforward signal path to create a LHP zero and therefore significantly improves the stability of the OTA. Furthermore, a simple but efficient Class AB output stage is used to achieve fast setting response and avoid extra static power dissipation. The proposed OTA was designed in a standard 0.35- μm CMOS technology. Detailed simulation results demonstrate that when driving 1000pF capacitive load, the OTA has 77-dB gain, 1.41-MHz unit-gain frequency (UGF) and 0.6-V/ μs average slew rate while dissipating only 45 μW under 1.5-V supply.

I. INTRODUCTION

Two-stage operational transconductance amplifier (OTA) is a fundamental building block widely used in most analog and mixed-signal electronic systems. An increasing number of applications in modern portable devices such as error amplifiers in LDOs and analog buffers in CMOS image sensors place ever more stringent performance requirements on two-stage OTAs [1]. These requirements include larger capability for driving heavy capacitive loads, low power consumption, fast transient response, and high chip-area efficiency.

To drive large capacitive loads, it seems appropriate to choose two-stage OTAs employing current buffer compensation for the reason that this technique offers an order of magnitude improvement in capacitive load capability for the same performance compared to compensation approaches that includes the usage of voltage buffer [2], nulling resistor [3], and multipath zero compensation [4]. Nevertheless, such improvement is still insufficient for capacitive loads up to several nanofarads because when driving so large capacitive load the OTA will result in huge power dissipation, unbearable chip size, and slow circuit speed. Besides, conventional circuit realization of current buffer has several drawbacks which make this solution less attractive.

In addressing the above problems, a two-stage OTA adopting embedded capacitor-multiplier compensation is presented in this paper. By exploiting the capacitor-amplifying function of the capacitor-multiplier, the proposed

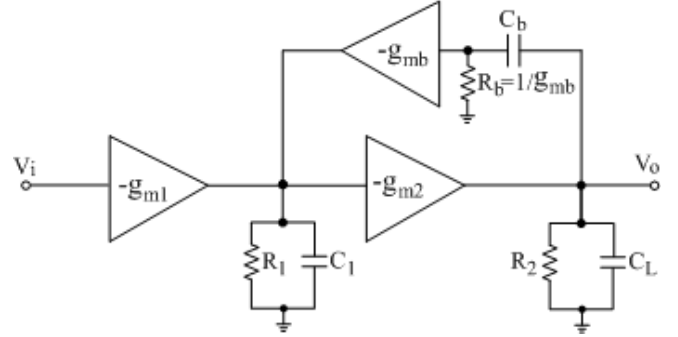


Fig. 1. Two-stage OTA with traditional current buffer

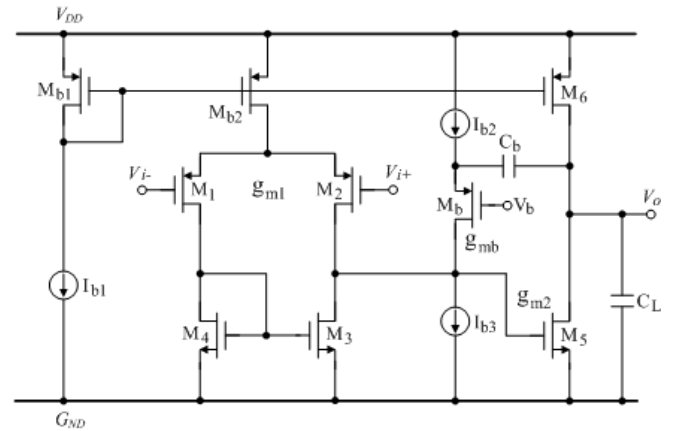


Fig. 2. Circuit realization of two-stage OTA with traditional current buffer

method provides extended capacitive driving capability for small size of the compensation capacitor without incurring extra power [5]. Moreover, the presence of a feedforward path creates a LHP zero to improve the stability of the OTA. Furthermore, the embedded capacitor-multiplier overcomes the limitations of traditional current buffer at the circuit level. Finally, a free but efficient class AB output stage is added to enhance transient response of the proposed OTA [6].

II. TWO-STAGE OTA WITH TRADITIONAL CURRENT BUFFER

A typical block diagram of two-stage OTA with conventional current buffer compensation is shown in Fig. 1. The compensation capacitor C_b is connected from the output

of OTA to the current buffer stage g_{mb} . The current buffer allows the capacitor current to flow from the output back toward the input of the second stage but effectively blocks the feedforward current through C_b . Therefore, the RHP zero is eliminated and a dominant pole due to the Miller effect is still produced at the first stage. By analyzing the small-signal model in Fig. 1, the transfer function of this type of OTA is given by [7]

$$A_v(s) = \frac{g_{m1}g_{m2}R_1R_2\left(1+s\frac{C_b}{g_{mb}}\right)}{(1+sC_bg_{m2}R_1R_2)\left(1+s\frac{C_1C_L}{C_bg_{m2}}+s^2\frac{C_1C_L}{g_{m2}g_{mb}}\right)} \quad (1)$$

As shown in (1), two complex conjugate poles and a LHP zero for pole-zero cancellation are also generated. The complex poles have a natural frequency ω_0 and damping factor ζ that can be expressed as

$$\omega_0 = \sqrt{\frac{g_{m2}g_{mb}}{C_1C_L}} \quad (2)$$

$$\zeta = \frac{1}{2C_b} \sqrt{\frac{C_1C_Lg_{mb}}{g_{m2}}} \quad (3)$$

Supposing that ζ is set to be $1/\sqrt{2}$ for small overshoot and UGF is half of the natural frequency to achieve a phase margin (PM) of 60° , the dimension condition of C_m is obtained as

$$C_b = \sqrt{\frac{C_1C_Lg_{mb}}{2g_{m2}}} \quad (4)$$

Unlike the compensation capacitance in simple Miller compensation technique that is linearly dependent on the load capacitance, C_b depends on the geometric mean of lumped parasitic capacitance of the first stage and the load capacitance. Although this compensation technique has significantly improved capacitive load capability for two-stage OTA, a huge C_b is mandatory for drive C_L up to several nanofarads. Taking some typical design values of a two-stage OTA as given by

$$g_{mb}/g_{m2} = 2, C_1 = 0.1\text{pF}, \text{ and } C_L = 1\text{nF},$$

C_b is required to be as large as 10pF, which apparently occupies almost the entire chip area of the OTA. Thus, a more powerful compensation technique is demanded to overcome this limitation.

The common circuit realization of two-stage OTA with traditional current buffer is depicted in Fig. 2. However, this realization obviously has several disadvantages. The implementation of current buffer adopting common gate transistor M_b introduces additional offset voltage to the OTA due to mismatch of the bias current between I_{b2} and I_{b3} . The

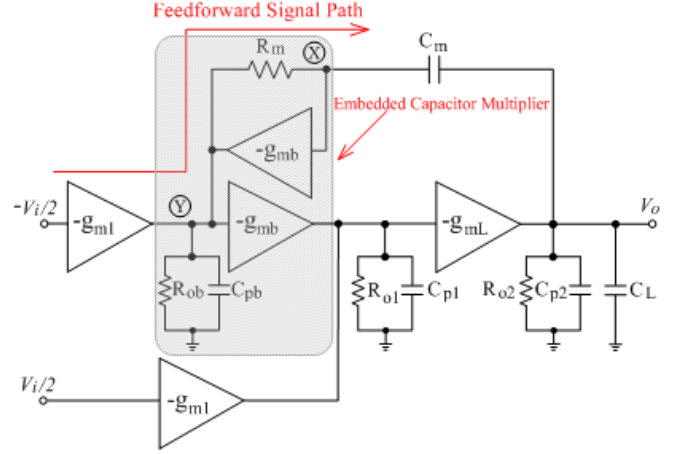


Fig. 3. Structure of the proposed two-stage OTA

added parasitic capacitance from the current buffer also affects the maximum attainable bandwidth of the OTA. Furthermore, this configuration requires extra biasing current for the current buffer and relevant auxiliary circuits such as current mirrors. Besides, the OTA has asymmetric slew rate because its output stage operates under class A style, which significantly lowers the speed of the OTA. Therefore, new circuit implementation also has to be conceived to avoid these drawbacks.

III. PROPOSED TWO-STAGE OTA USING EMBEDDED CAPACITOR-MULTIPLIER COMPENSATION

The proposed two-stage OTA structure is shown in Fig. 3. The transconductance stages g_{m1} and g_{mL} compose the conventional two-stage amplifier. The output resistance and lumped parasitic capacitance of each stage are denoted by $R_{o(1-2)}$ and $C_{p(1-2)}$, respectively, while C_L is the load capacitor. The shadowed part models the capacitor-multiplier embedded in the differential-input stage whose active load is represented by g_{mb} . The shunt-shunt feedback formed by R_m and the upper g_{mb} stage provides two low-impedance nodes X and Y, thereby sensing the feedback current through C_m and converting it into voltage. This voltage is then amplified by the lower g_{mb} stage to reach sufficient magnitude. Thus, a large equivalent capacitance can be seen at the output of the first stage and the dominant pole is effectively pushed to a very low frequency while the output poles are moved toward higher frequencies. Moreover, one half the total input signal at node Y splits into two parts: one part transfers directly from R_m and C_m to the output stage and the other passes through the following transconductance stages. Because of their in-phase characteristic, a LHP zero is created instead of introducing a RHP zero. This LHP zero can be used to compensate the negative phase shift caused by nondominant

$$A_v(s) = A_0 \frac{\left(1+s\frac{(g_{mb}R_m+1)C_m}{2g_{mb}}\right)\left[1+s\frac{1}{g_{mb}R_m+1}\left(R_mC_{p1}+\frac{C_{p1}}{g_{mL}}\right)\right]}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+s\frac{C_{p1}C_L}{g_{mL}(g_{mb}R_m-1)C_m}\right)\left(1+s\frac{C_m}{g_{mb}}+s^2\frac{C_m}{g_{mb}}R_mC_{p1}\right)} \quad (8)$$

poles and therefore significantly increases the phase margin of the amplifier.

A. Transfer Function

Before deriving the transfer function of the proposed amplifier, some useful assumptions are made for simplicity:

$$g_{m1}R_{o1}, g_{mL}R_{o2} \gg 1 \quad (5)$$

$$g_{mb} > 1/R_m \gg R_{ob} \quad (6)$$

$$C_L \gg C_m, C_{p(b,1-2)} \quad (7)$$

The simplified transfer function is given by (8), shown at the bottom of the previous page. Assuming that the high-frequency poles and zeros introduced by the capacitor multiplier can be fairly neglected, the order of the transfer function reduces to two. The dc gain is expressed by $A_0 \approx g_{m1}R_{o1}g_{mL}R_{o2}$. $\omega_{p1} \approx 1/[R_{o1}g_{m2}R_{o2}(g_{mb}R_m-1)C_m]$ is the dominant pole and $\omega_{p2} \approx g_{mL}(g_{mb}R_m-1)C_m/(C_{p1}C_L)$ is the non-dominant pole. The expression of the LHP zero is $Z_{LHP} = (2g_{mb}/[(g_{mb}R_m+1)C_m])$.

B. Capacitance Dimension, GBW, and Phase Margin

Since the capacitor-multiplier can further reduce the size of compensation capacitance by $g_{mb}R_m-1$, a small C_m can be used to drive huge capacitive load C_L of several nanofarads because $g_{mb}R_m-1$ can reach on the order of ten.

The gain-bandwidth product (GBW) of the two-stage OTA is given by $GBW = A_0\omega_{p1} = [g_{m1}/(g_{mb}R_m-1)C_m]$.

By choosing proper g_{m1} and g_{mb} , it is easy to locate Z_{LHP} beyond the UGF of the OTA, which can increase the PM of the OTA greatly compared to traditional compensation techniques of two-stage OTA. The PM of the two-stage OTA is approximately given by

$$PM = 90^\circ - \tan^{-1}\left(\frac{GBW}{\omega_{p2}}\right) + \tan^{-1}\left(\frac{GBW}{Z_{LHP}}\right) \quad (9)$$

C. Circuit Implementation

The transistor-level realization of the proposed two-stage OTA is shown in Fig. 2. The first stage is comprised of transistor M_1 - M_4 with a PMOS differential pair. The embedded capacitor-multiplier is implemented by reusing the modified current mirror M_3 - M_4 through inserting a resistor R_m between the gate and drain of M_4 . In fact, this capacitor-multiplier can be viewed as a kind of current buffer with current gain, which also gets rid of the drawbacks exhibiting in traditional current buffers such as offset voltage, additional parasitic capacitance, and extra power consumption. The second stage is realized by transistors M_5 - M_6 . A small diode connected transistor M_R operating as a very large resistive element and a small C_b act as a floating battery that transfer the voltage variations of the output of the first stage to the gate of M_6 . This provides class-AB operation to the output stage. In addition, given that no dc current flows through M_R the voltage at the gate of M_{b2} is the same as that at the gate of M_6 . Hence, the quiescent conditions are not disrupted. Moreover, this simple structure shifts ω_{p2} to higher frequency than typical

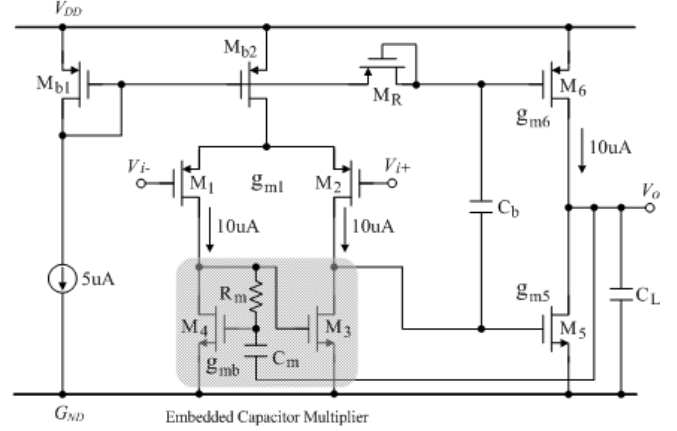


Fig. 4. Circuit implementation of the proposed two-stage OTA

two-stage class-A OTA due to the fact that both M_5 and M_6 are active and therefore the effective g_{mL} is equal to $g_{m5}+g_{m6}$.

IV. SIMULATION RESULTS

To prove the effectiveness of the proposed compensation strategy and circuit techniques, the OTA shown in Fig. 4 driving 1nF capacitive load has been designed in a 0.35- μ m double-poly triple metal (DPTM) CMOS process with 1.5V supply voltage. The biasing current is set to 5 μ A and the drain current of each remaining branch is 10 μ A, thus achieving a total current consumption of 35 μ A. During the simulation step, R_m and C_m have been slightly tuned to 60k Ω and 0.6pF, respectively, to obtain a PM of 60°. The circuit parameters (g_{m1} , g_{mb} , g_{m5} and g_{m6}) of the implemented OTA are 134 μ S, 194 μ S, 211 μ S and 155 μ S, respectively. The value of C_b can be small as long as it is much larger than the gate-capacitance of M_6 to ensure that voltage variations at the gate of M_5 can be transferred to the gate of M_6 with little attenuation. In this design, C_b is set to 2pF. A minimum size diode connected PMOS transistor M_R with source and substrate terminal connected could achieve extremely high resistance, which is essential for this class AB structure to operate effectively starting from quite low frequency.

All transistor dimensions are presented in Table I. Fig. 5 shows the simulated open-loop frequency responses of the proposed OTA under different process corners. The typical case was 77dB dc gain, 1.41MHz GBW and 67° PM. The OTA still has 59° PM under the worst-case condition.

TABLE I: SUMMARY OF TRANSISTOR SIZE

Transistor	Size
M_1, M_2	8x(4 μ m/0.8 μ m)
M_3, M_4	8x(4 μ m/0.8 μ m)
M_5	8x(4 μ m/0.8 μ m)
M_6	4x(12 μ m/1 μ m)
M_R	1 μ m/1 μ m
M_{b1}	8x(12 μ m/1 μ m)
M_{b2}	2x(12 μ m/1 μ m)

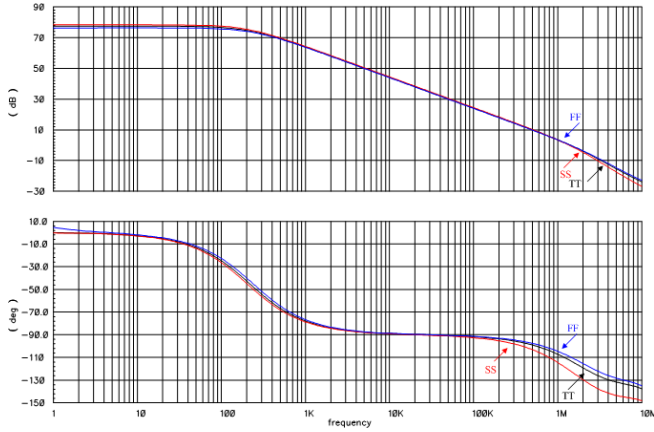


Fig. 5. Frequency responses of the proposed OTA under different process corners

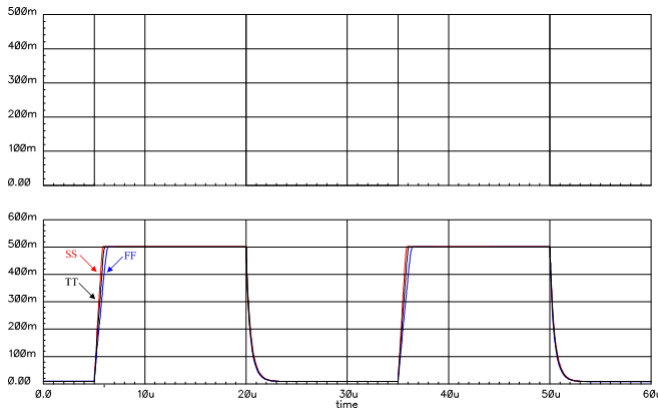


Fig. 6. Transient responses of the proposed OTA under different process corners

Fig. 6 shows the step response in unity-gain configuration to 33.3-KHz 500mVpp input step. The detailed performances of the proposed OTA under the typical case are summarized in Table II.

TABLE II: PERFORMANCE SUMMARY OF THE PROPOSED OTA

Technology	SMIC 0.35- μ m CMOS
V_{DD} (V)	1.5
Loading Capacitance (pF)	1000
Total Bias Current (μ A)	35
DC Gain (dB)	77
Gain-Bandwidth Product (MHz)	1.41
SR+/SR- (V/ μ s)	0.52/0.68
TS+/TS- (1%) (μ s)	1/2.2

V. CONCLUSION

A two-stage OTA based on embedded capacitor-multiplier compensation technique is described in this paper. Compared to traditional methods of compensating two-stage

OTA, the proposed structure not only significantly extends capability for driving capacitive load by using a small compensation capacitor but also enhances the stability of the OTA by generating a useful LHP zero. Moreover, efficient circuit techniques are utilized to implement this OTA and verified by extensive simulation results.

REFERENCES

- [1] A. J. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R. G. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew rate and power efficiency," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1068–1077, May. 2005.
- [2] Y. P. Tsividis and P. R. Gray, "An integrated NMOS operational amplifier with internal compensation," *IEEE J. Solid-State Circuits*, vol. 13, no. 12, pp. 760–768, Dec. 1978.
- [3] W. C. Black Jr., D. J. Allstot, and R. A. Reed, "A high performance low power CMOS channel filter," *IEEE J. Solid-State Circuits*, vol. 15, no. 12, pp. 929–938, Dec. 1980.
- [4] F. You, H. K. Embabi, and E. Sánchez-Sinencio, "A multistage amplifier topology with nested G_m -C compensation," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000–2011, Dec. 1997.
- [5] Z. Yan, L. Shen and Y. Zhao, "A low-voltage CMOS low-dropout regulator with novel capacitor-multiplier frequency compensation," in *Proc IEEE ISCAS'08*, pp. 2685–2688, May. 2008.
- [6] J. Ramirez-Angulo, R. G. Carvajal, J. A. Galan, and A. J. Lopez-Martin, "A free but efficient low-voltage class-AB two-stage operational amplifier," *IEEE Trans. Circuits Sys. II*, vol. 53, no. 7, pp. 568–571, Jul. 2006.
- [7] G. Palmisano and G. Palumbo, "A compensation strategy for two-stage CMOS opamps based on current buffer," *IEEE Trans. Circuits Sys. I*, vol. 44, no. 3, pp. 257–262, Mar. 1997.