Ultra low noise low power LDO design

Vello Mannama, Rein Sabolotny, Viktor Strik

National Semiconductor Estonia

Abstract: A low dropout regulator (LDO) with ultra low output noise is described. The proposed structure of LDO with internal noise filter is discussed and related design problems along with their possible solutions are highlighted.
The LDO ensures output noise below 10uV (10Hz to 100kHz) having quiescent current about 25uA for no load. Maximum output current of 100mA is available. The LDO is stable with a 220nF ceramic output capacitor. In testing, PSRR above 75dB (1kHz), dropout below 80mV (Vout>2.5V), and transient peaks below 30mV (1mA … 80mA output step) were measured. The solution is patent pending and has been introduced to low noise LDO LP5900.

1 Introduction

In several applications Low Dropout Regulators (LDO) with ultra low output noise are needed. Also, often low current consumption and operation without external reference bypass capacitor is required.

Below, main problems and difficulties in solving the task are considered. Design resulted in family of low noise designs used in different Power Management Units (PMU) with next typical features:

- Output voltage noise of approximately $10\mu V_{RMS}$ for 10Hz … 100kHz frequency range
- Low quiescent current (25µA)
- Fast startup (50µs)
- No external bypass capacitor for reference source
- High PSRR (>75dB at 1kHz)
- Stability with low output ceramic capacitors

The structure has been introduced also to a standard low noise LDO LP5900 [1].

2 Noise analysis

Conventional LDO (Figure 1) consists of four main units: Voltage reference: Voltage reference source, Error amplifier, Pass transistor, and Resistive divider [2,3].

Differential error amplifier along with Pass transistor constitutes an amplifier structure with negative feedback through the resistive divider, ensuring the required output level. Often, the resistive divider with

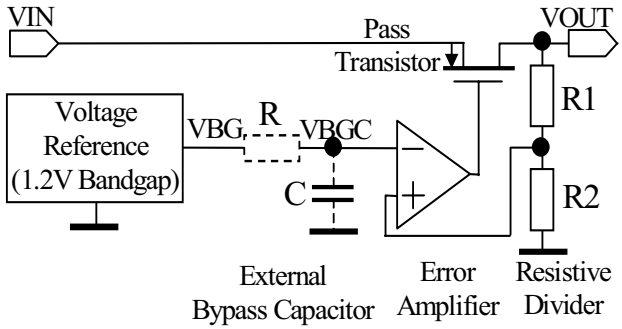

Figure 1 Conventional structure of LDO

parallel capacitor gives an additional zero for stable operation. To suppress reference noise, a Low Pass Filter (LPF) is often used, consisting of an internal resistor and external bypass capacitor.

According to the noise study of LDOs with conventional structure, main contributions to the output noise give:

- Voltage reference source
- Output resistive divider
- Error amplifier

Typically, the noise of the reference source is the most dominant and low-pass filtering with external bypass capacitor is the traditional solution for noise suppressing. In micro-power LDOs the large resistance output divider also substantially increases the total noise level.

For example, in case of a micro power LDO with 250µV specified noise performance, the simulated total output noise for 3V input/1.5Voutput voltage, 1.2V band-gap voltage, and 10Hz to 100kHz bandwidth was 219µV. After removing the reference noise, the output level reduced to 46.3µV, while after removing the noise of the output divider it reduced to 34.5 µV. Hence, in contribution of reference noise to the output noise was 214µV while contribution of the divider noise was 31µV.

To estimate contribution of the divider noise, next expression can be used

$$V_{n\_divt} = E_{n\_R1R2} \cdot \sqrt{\frac{R1}{R2}},$$

1-4244-0415-0/06/$20.00 ©2006 IEEE.

where E_{n_R1R2} represents total noise of divider resistors connected in series. In studied case R1=500kOhm, R2=1950kOhm, and the expression yields: V_{div} = 31.7µV, being quite close to the simulation result. Adjusting the output voltage to 3V (by selecting of R1), the noise contribution of resistive divider increases to 109µV.

3 Proposed structure

In order to meet specification of LDO of the low noise family mentioned above, a modified structure of LDO was used (Figure 2).

The proposed LDO has no output divider while the reference source has a variable (selectable) output voltage corresponding to the output voltage of the regulator. To safely remove noise of the reference voltage, including noise of filter resistor, a first order low-pass filter with ultra low pole frequency (about 0.1Hz) was used. For a reasonable integrated capacitance value (100 - 300pF using an area saving MOS capacitor), a resistive component with resistance of 1 – 10GOhm is needed.

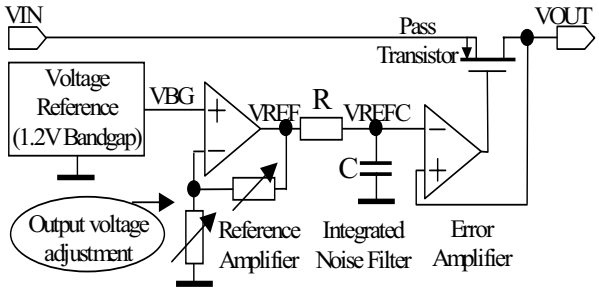

Figure 2 Proposed structure of a low noise LDO

Resistor of the noise filter is based on a pMOS transistor (see Figure 3).

To obtain proper channel resistance of a MOS transistor (in linear range), a relation (W1/L1)=100*(W2/L2) and a value of Ibias about 1nA have been used, where W1, L1 and W2, L2 are width and length of transistors M1 and M2, respectively.

Since the possible leakage through parasitic pnp transistor (see Figure 3) at higher temperatures may cause serious DC shift problems, the area W2*L2 should be as small as possible (to reduce base/emitter current of the parasitic pnp that is proportional to the well area). Also, the L1 must be selected close to minimum to save area (and possible well leakage) of M1. Matching accuracy between M1 and M2 as well as the control current tolerance are not critical because cut-off frequency of the noise filter can be selected with proper margin.

Due to extremely large resistance and small currents, the noise filter needed a carefully designed layout. The p and n guard-rings and covering by metal helped to suppress the light sensitivity of the reference voltage.

4 Results

Some noise simulation and test data are presented below. All tested circuits had no load quiescent current of about 25µA.

4.1 Simulations

Below simulated LP5900 noise voltage vs. output load current is shown for typical model parameters (Figure 4, Vout=2.8V, frequency range from 10Hz to 100kHz). The worst noise performance is close to the 1mA output current, while for larger currents the noise performance is better and is safely lower of 10μV_{RMS} target.

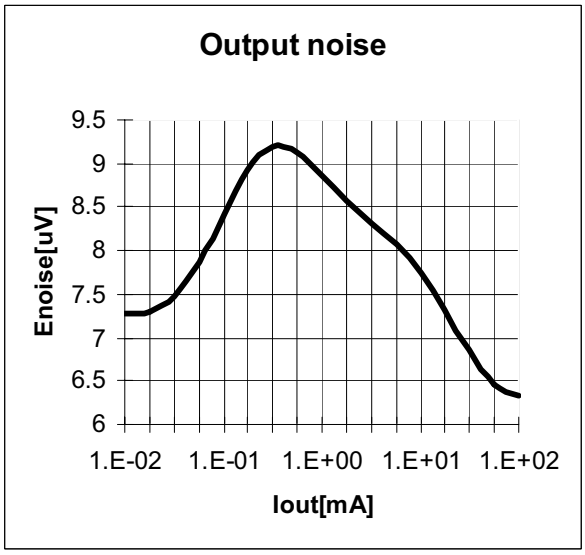

Figure 4 Simulated noise performance

4.2 Testing

Output noise of a typical LP5900 device in 10Hz … 100kHz range including non-correlated noise of ca 2uV of test equipment is shown in table (output voltage of 2.8V).

Table 1 The tested noise performance

Iload [mA]	Vout_noise [µV]
0	7.4
1	10.6
10	8.7
100	6.6

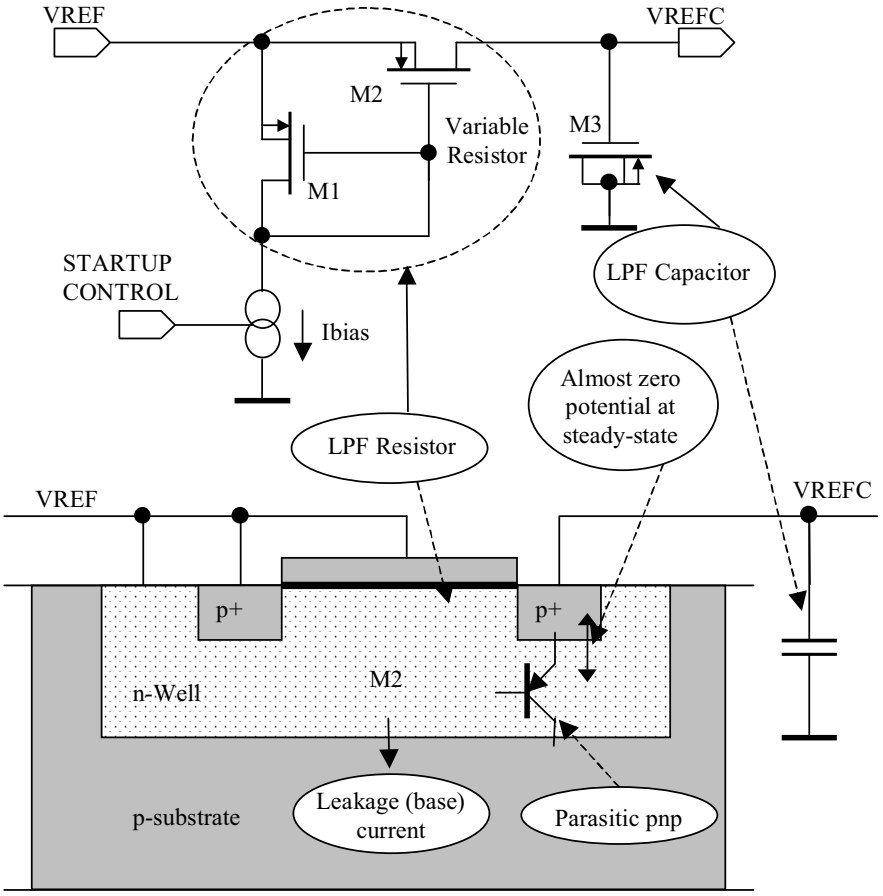

Figure 3 Noise filter on MOS resistor and capacitor

5 Comparison

Some main parameters of the best known LDOs from noise performance point of view (for the moment of the publication of the article) are presented in Table 2.

Table 2 Noise performance comparison

	LP5900	MAS 9162	LT1761	MAS 9123
Bypass Capacitor	No	No	Yes	Yes
Noise, μV_{RMS}	10	30	20	9.5
Iq, µA	25	190	20	170
Manufacturer	NS	MAS	LTC	MAS
Reference	[1]	[4]	[5]	[6]

Some comments:

- LP5900 is manufactured by National Semiconductor (NS) and its structure has been considered in the article
- MAS9162 is manufactured by Micro Analog Systems (MAS) and had the best known noise performance without bypass capacitor before LP5900 production
- LT1761 is manufactured by Linear Technology (LTC) and has comparable to LP5900 quiescent current. At the same time the noise performance is worse notwithstanding of the use of external bypass capacitor
- MAS9123 has the best known noise performance, but it needs for an external capacitor and the quiescent current roughly seven times more than LP5900

From the data above we may conclude that LP5900 has far better noise performance to any known LDO without bypass capacitor and its noise performance is well comparable to the best-known LDOs with external bypass capacitor with much larger quiescent current. One specific feature of LP5900 is even better noise performance at higher load currents where to the circuit has been designed.

6 Other design considerations

Some design problems that were solved in low noise LDO design can be listed as follows:

A. Related to new structure (architecture)

- Ensuring stability of the LDO in case of deepest feedback (gain=1) while output divider with parallel capacitor could not be utilized for frequency correction purposes (extra zero generating); using of MicroSMD encapsulation with minimum output resistance (<5mOhm) and inductance (<3mH) along with minimum-size low ESR ceramic capacitor caused additional stability problems
- Design of a low noise error amplifier with good enough PSRR and transient performance in case of quite restricted quiescent current required specific solutions
- Additional switch transistor connected to the extra high impedance noise filter for short start-up caused extra leakage and dc shift problems

B. Related to internal reference noise filter (DC shift and output voltage instability problems)

- Very high MOS resistor value required usage of very low control currents of 1nA level and suppressing of parasitic leakage of the filter control circuit, especially at high temperature
- Leakage through parasitic pnp transistor must be kept as small as possible to not cause DC shift of reference voltage at higher temperatures
- DC shift that might be caused by light in p-n junction (drain-well) must be suppressed using reduction of junction area and special layout design
- DC shift due to rectification of AC disturbance in noise filter with non-linear MOS resistor was removed using a special reference amplifier with sufficient PSRR

Solutions of the listed problems are obviously not optimal yet and further improvements are desirable. However, fabrication of operating prototypes evidences feasibility of proposed ideas.

7 Conclusion

To achieve the targeted performance of the low noise LDO family (starting from LP5900) a novel (patent pending) LDO structure was used.

In order to minimize output noise of LDO, the reference noise is suppressed using a very low pass on-chip Noise Filter, consisting of a non-linear MOS resistor and MOS capacitor.

Error amplifier and the Pass transistor are connected as a voltage follower without output resistive divider that removes the second main noise source and ensures minimum noise amplification in LDO.

The novel structure of LDO is proved on silicon. At 1mA load current it exhibits $10\mu V_{RMS}$ typical output noise without external reference bypass capacitor. The noise performance is even better at higher and lower load currents (Table 1). The quiescent current of the LDO is 25µA. The noise performance is superior to known devices in production.

References

[1] LP5900 Ultra Low Noise, 100 mA Linear Regulator for RF/Analog Circuits Requires No Bypass Capacitor. LP5900 datasheet, National Semiconductor Website www.national.com

[2] G.A.Rincon-Mora and P.E.Allen, “A Low-Voltage, Low Quiescent Current, Low Dropout Regulator”, IEEE Journal of Solid-State Circuits, vol.33, pp.36-44, 1998

[3] Walt Jung, “Voltage Reference And Low Dropout Linear Regulators”,. In “Analog-Digital Conversion”, edited by Walt Kester, Analog Devices, Inc., 2004.

[4] 80 mA LDO Voltage Regulator IC. MAS9162 datasheet, Micro Analog Systems Website www.mas-oy.com

[5] 100mA, Low Noise, LDO Micropower Regulators in SOT-23. LT1761 Series datasheet, Linear Technology Website www.linear-tech.com

[6] 80 mA LDO Voltage Regulator IC. MAS9123 datasheet, Micro Analog Systems Website www.mas-oy.com