A 1.39-V Input Fast-Transient-Response Digital LDO Composed of Low-Voltage MOS Transistors in 40-nm CMOS Process

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***Abstract*—A fast transient-response digital low-dropout (LDO) voltage regulator comprising only low-voltage MOS transistors was developed. The input voltage can be higher than the withstand voltage of the low-voltage MOS transistors by the proposed withstand-voltage relaxation scheme. The switching frequency of 1 GHz can be achieved using small-dimension low-voltage power-MOS transistors. The LDO occupies only 0.057 mm^2 area using 40-nm CMOS technology, and covers a wide range of load currents from 400 μA to 250 mA. The response time is only 0.07 μs.**

I. Introduction

On-chip voltage regulators present some advantages: the number of off-chip voltage regulators can be decreased, which allows each module on an SoC to have an appropriate supply voltage. Several methods of voltage regulators exist: low dropout (LDO) voltage regulators [1]–[4] and a switching regulator [5]. The LDO voltage regulators present some advantages from the viewpoints of the small output-voltage ripple caused by a power-MOS switching and small area achieved through reduction of external devices. Recently, improvements in the stability of output voltage as well as the efficiency of the LDO have been reported. For power efficiency, when the dropout voltage attributable to the power MOS is reduced using large power MOS, the LDO area necessarily becomes large [1]. For cases in which many LDOs are applied to the SoC to supply suitable voltage to each module individually, reducing the LDO area is an important issue. For stability of the output voltage, when a decoupling capacitor is applied to the LDO, the response time for large load-current transient becomes long [1], [2]. However, reduction of the response time causes low current efficiency because of the large quiescent current [3]. To achieve fast transient response time without current-efficiency degradation is an important issue as well. On the other hand, to improve the LDO performance, a digitally controlled LDO has also been reported [4]. According to power-MOS configuration in this digital LDO, it is difficult to control the power MOS rapidly and accurately for two reasons. First, the control cycle becomes long because the number of levels of the power MOS reaches 256 for wide-range load current. Second, the error of control of power MOS becomes large because the nonlinear scaling of power-MOS resistance results in an inconstant dropout-voltage step. A digital LDO composed of only low-voltage transistors was developed to address three issues: area reduction, fast transient response, and power-MOS configuration.

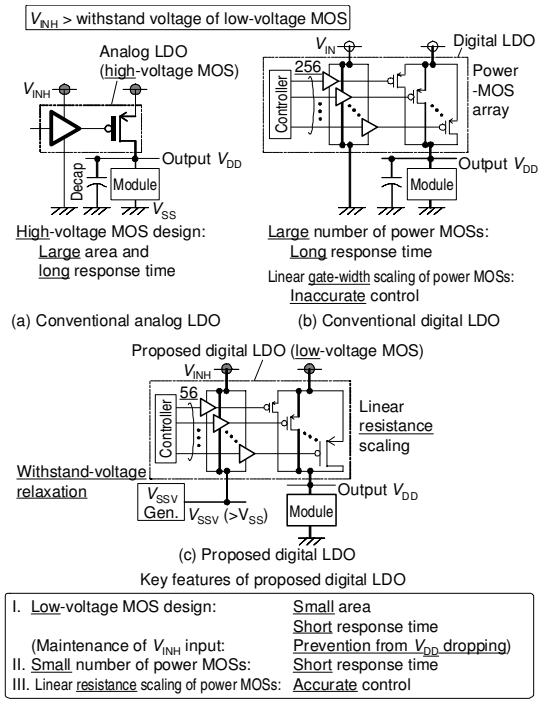


Fig. 1. Comparison among conventional LDOs and proposed LDO.

II. Proposed digital LDO

A. Overview

The concept of a proposed digital low-dropout (LDO) voltage regulator is shown in Fig. 1. In a conventional LDO, the output voltage ($V_{\rm DD}$) is controlled to no more than the withstand voltage of low-voltage MOS transistors using high voltage power MOS, as shown in Fig. 1(a). To reduce the area of the conventional LDO and to achieve rapid transient response, a design using low-voltage MOS transistors is applied for this study. However, if the input voltage to the LDO ($V_{\rm INH}$) is controlled to be low to guarantee the maximum withstand voltage of low-voltage MOS transistors, then $V_{\rm DD}$ drops and the operating frequency of a module falls. Therefore, to prevent this $V_{\rm DD}$ drop, $V_{\rm INH}$ can be as high as that of the conventional voltage by application of developed withstand-voltage relaxation scheme with a $V_{\rm SSV}$ generator, as shown in Fig. 1(c). On the other hand, in a conventional digital LDO, the number of the level of the power MOS reaches 256 for a wide-range load current, as shown in Fig. 1(b). In the proposed LDO, the number of levels of the power MOS is reduced to only 56 based on the developed power-MOS configuration scheme, whereas a wide-range load current is covered. This reduction of the power-MOS level and a digital control without a decoupling capacitor also contributes to a rapid transient response. Moreover, in the

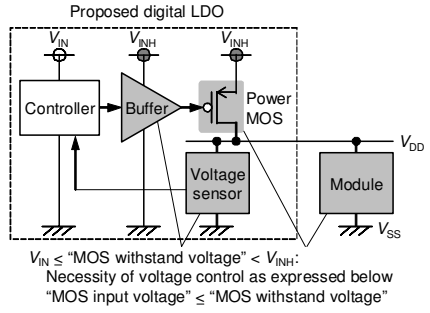


Fig. 2. Supply voltage configuration of the proposed LDO.

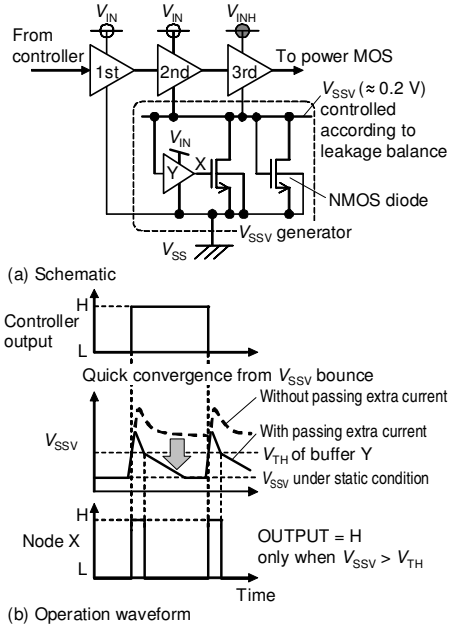


Fig. 3. Withstand-voltage relaxation scheme 1 for buffer.

proposed LDO, because the resistance of the power MOS is linearly scaled (because the gate-width of the power-MOS is nonlinearly scaled), the dropout voltage attributable to the power MOS is controlled accurately.

B. Withstand-voltage relaxation scheme

The proposed LDO consists of a controller, a buffer, the power MOS, and a voltage sensor, as shown in Fig. 2. The input voltage to the controller is $V_{\rm IN}$, the whereas input voltage to the power MOS and the buffer is $V_{\rm INH}$. The relation among these voltages is "$V_{\rm IN} \leq$ MOS withstand voltage $< V_{\rm INH}$". The amplitude of the buffer output is $V_{\rm SSV}$ to $V_{\rm INH}$ because the power MOS is completely off when the output voltage of the buffer is at a high level. To apply this supply voltage configuration, supply voltages to MOS transistors in the buffer, the power MOS, the voltage sensor, and a module must be controlled so as not to exceed their withstand voltages.

The buffer consists of three stages for withstand-voltage relaxation, as shown in Fig. 3(a). Low-level voltage of the buffer at first stage is $V_{\rm SS}$, whereas low-level voltage of the buffer at second and third stages is $V_{\rm SSV}$ ($\approx$ 0.2 V). High-level voltage of the buffer at first and second stages is $V_{\rm IN}$ whereas high-level voltage of the buffer at the third stage is $V_{\rm INH}$. For the buffer at the second and third stage, $V_{\rm SSV}$ is supplied using a $V_{\rm SSV}$ generator. Generally, the $V_{\rm SSV}$ generator consists of two modules: a voltage-reference circuit [6] and an amplifier. However, because these two modules require a large area, $V_{\rm SSV}$ is generated by an NMOS transistor as a diode in this study. In this scheme, the voltage level of $V_{\rm SSV}$ is controlled according to the leakage balance among the buffer at the second and third stages and the NMOS transistor. Because variation of $V_{\rm SSV}$ attributable to process, voltage, and temperature causes error of the power-MOS control, two kinds of margin in propagation delay of the buffer and power-MOS resistance are examined.

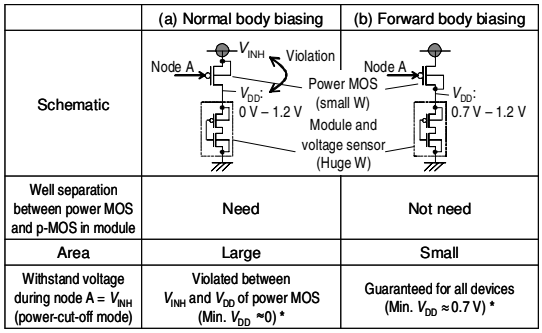


Fig. 4. Withstand-voltage relaxation scheme 2 for power MOS.

In the $V_{\rm SSV}$ generator, a buffer Y controls another NMOS via a node X. When $V_{\rm SSV}$ is bounced because of toggling of a controller output and $V_{\rm SSV}$ is higher than a logical threshold voltage of the buffer Y, the node X becomes *H* and extra current remaining in a node of $V_{\rm SSV}$ is passed to $V_{\rm SS}$, as shown in Fig. 3(b). Thereby, quick convergence from this $V_{\rm SSV}$ bounce can be achieved.

Withstand-voltage relaxation for the power MOS, the module, and the voltage sensor is achieved as follows. When the power MOS is used with normal body biasing as shown in Fig. 4(a), two problems arise. The first problem is the area overhead attributable to well separation between an n-well of the power MOS and an n-well of the PMOS in the module. The second problem is violation of the withstand voltage during node A = $V_{\rm INH}$ (i.e. power to the module is cut off). The total gate width of the power MOS is much less than that of MOS transistors in the module. Therefore, $V_{\rm DD}$ becomes almost 0 V during this *power-cut-off* mode and the voltage between a drain and a source of the power MOS exceeds its withstand voltage. Therefore, in this work, the power MOS is used with forward body biasing, as shown in Fig. 4(b). By applying this structure, the two problems described above are solvable. This structure is applicable without well separation. Moreover, $V_{\rm DD}$ during *power-cut-off* mode can be controlled to 0.7 V based on our simulation. Conditions of our simulation are that $V_{\rm INH}$ = 1.25 V and total gate width of the power MOS : total gate width of MOSs in the module = 1 : 200 (the module is assumed to be the largest module, namely, a CPU core). Although this structure raises the possibility of latch-up, the possibility is decreased to the same level as that of conventional structure by application of techniques on layout as follows:

1) Power MOS is separated from a source of NMOS in the module.
2) NMOS in the module is separated from a P-substrate by a deep N-well.

C. Power-MOS configuration scheme

As shown in Fig. 5, target specifications for the voltage-drop range and resistance range of the power MOS, and the

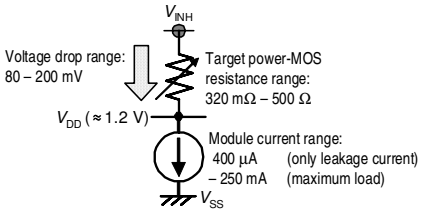


Fig. 5. Target specifications of the load current and power MOS.

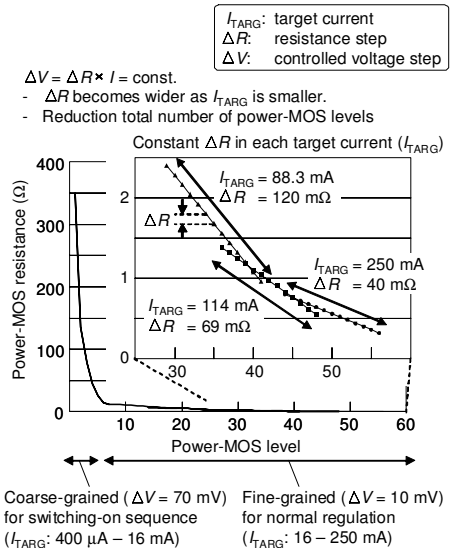


Fig. 6. Power-MOS size configuration.

current range of the module are determined respectively as 400 μA (only leakage current) – 250 mA (the maximum load), 80 mV – 200 mV, and 320 mΩ – 500 Ω.

To cover wide-range variation of power-MOS resistance (320 mΩ – 500 Ω) with a small number of levels, several power-MOS resistances are calculated as follows. First, 13-level resistances are calculated as voltage drops attributable to the power MOS at the maximum target current (I_{TARG} = 250 mA), with voltage drops controlled from 80 mV to 200 mV at 10-mV steps. Second, at another I_{TARG}, another series of 13-level resistances is calculated. Third, each calculated series of power-MOS resistances at I_{TARG} (400 μA – 250 mA) is merged as shown in Fig. 6. In this work, values of I_{TARG} are 250 mA, 114 mA, 88.3 mA, $\cdots$ and the total number of resistance levels is only 56. When the load current range is 16–250 mA in normal regulation, the voltage drop is controlled at 10-mV steps using levels 6–56 of the power MOS. When the load current range is 400 μA – 16 mA in the switching-on sequence, the voltage drop is controlled at the 70-mV step using levels 1–5 of the power MOS. In the proposed power-MOS configuration, the calculated resistance of the power MOS has the following characteristics:

1) Resistance step (ΔR) is wider for smaller I_{TARG}.
2) ΔR (i.e. dropout voltage step) at each I_{TARG} is constant.

Because characteristic 1) contributes to reduction of the total number of power-MOS levels, fast control to the power MOS is achieved. However, characteristic 2) contributes accurate control to the power MOS. The key performance of the proposed power-MOS configuration and comparison with [4] are presented in Table I.

TABLE I
COMPARISON OF POWER-MOS CONFIGURATION

	[4]	This work
Current range	Maximum 0.2 mA	400 μA – 250 mA ($\times$ 625)
Number of level	256	56
Voltage step	Non constant	Constant
Control	Slow and inaccurate	Fast and accurate

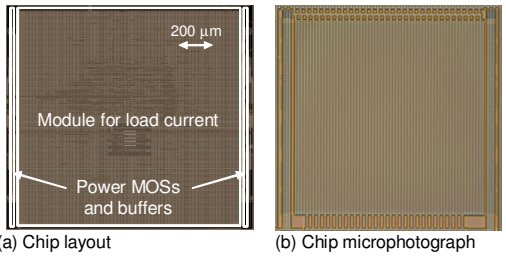


Fig. 7. Layout and chip microphotograph.

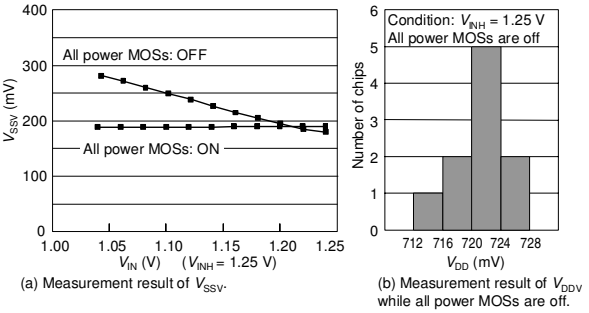
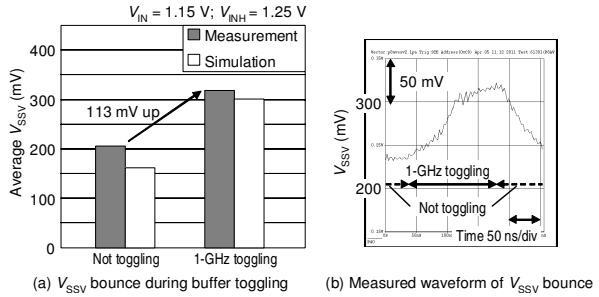


Fig. 8. Measurement results of withstand-voltage relaxation.

III. IMPLEMENTATIONS AND MEASUREMENT RESULTS

The proposed LDO was implemented on a 40-nm CMOS process. The voltage sensor was designed by application of a time-to-digital converter (TDC). The delay of conversion and output resolution for the voltage sensor are less than 10 ns and less than 10 mV, respectively. Because they have a relationship of tradeoff to each other, they are carefully tuned in this study. The layout of the chip and its microphotograph are shown in Fig. 7. The proposed LDO occupies only 0.057 mm^2. The load current of the module is controlled up to 250 mA at 16 steps. The maximum operation frequency of all components is 1 GHz.

Measurement results of withstand-voltage relaxation schemes are presented in Fig. 8. Measurement conditions are given as follows: the voltage range of V_{IN} is 1.04 V to 1.24 V whereas V_{INH} is fixed to 1.25 V. When all power MOSs are on, V_{SSV} is controlled to around 190 mV. When all power MOSs are off, V_{SSV} rises to 280 mV as voltage difference between V_{IN} and V_{INH} becomes larger. The reason for this V_{SSV} rising is that a PMOS in the third stage buffers are not completely off. Measurement results of V_{DD} under conditions in which all power MOSs are off show that values of V_{DD} of all measured chips are around 700 mV. These measurements show that the withstand voltage for the buffers, the power MOS, and the module are guaranteed and that the nominal V_{INH} reaches 1.39 V when the MOS withstand voltage in this process is 1.2 V. Measurement results of V_{SSV} bounce during buffer toggling are shown in Fig. 9. While the largest buffers are toggling, V_{SSV} bounce is suppressed within 100 mV. This bounce quickly finishes ($\leq$ 50 ns). As shown in Fig. 10, measurement results of power-MOS resistance are 326 mΩ to 222 Ω for the voltage range of V_{INH} is 1.20 V to 1.25 V, with V_{IN} fixed to 1.15 V. Measured power-MOS



(a) V_{SSV} bounce during buffer toggling (b) Measured waveform of V_{SSV} bounce

Fig. 9. Bounce of $V_{\rm SSV}$ while the largest buffers are toggling.

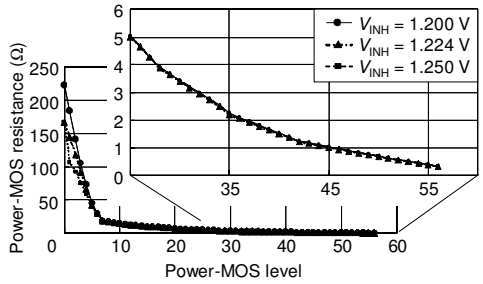


Fig. 10. Measurement result of power-MOS resistance.

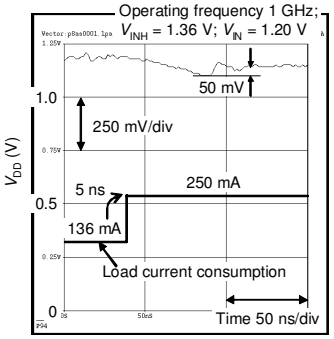


Fig. 11. Measured transient waveform $V_{\rm DD}$ with varied load current.

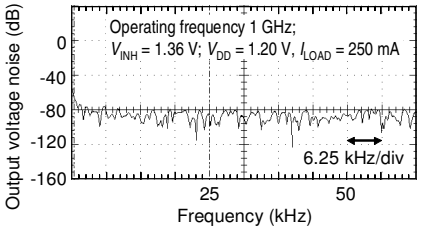


Fig. 12. Measured frequency spectrum of the output voltage $V_{\rm DD}$.

resistance shows partially proportional scaling at each load current without dependence on $V_{\rm INH}$ variation. The measured load transient response is portrayed in Fig. 11. Conditions of this measurement are that a step of $I_{\rm LOAD}$ is from 136 mA to 250 mA and the rise time of the current step is 5 ns. The response time, which is measured from the start of the load step until the output voltage is stable again, is only 0.07 μs because the switching frequency of the power MOS reaches 1 GHz. The measured output voltage noise is shown in Fig. 12. For almost all frequency ranges, the output voltage noise is less than -60 dB.

The key performance summary of the proposed LDO and a comparison with some previous regulators are listed in Table II. In the proposed LDO, the quiescent current is scaled according to switching frequency, except for the leakage current. Therefore, by selecting the switching frequency

TABLE II
KEY PERFORMANCE SUMMARY

	Unit	[1]	[3]	[4]	This work
Process	–	0.35 μm	90 nm	65 nm	40 nm
Control	–	Analog	Analog	Digital	Digital
Active area	mm^2	0.264	0.008	0.042	0.057
Minimum input voltage	V	2	1.2	0.5	1.34
Nominal output voltage	V	1.8	0.9	0.45	1.20
Maximum load current	mA	200	100	0.2	250
Load transient response	mV	$<$1.1%$^{(2)}$	90$^{(3)}$	40$^{(4)}$	50$^{(5)}$
Response time	ns	270$^{(2)}$	0.54$^{(3)}$	N/A	70$^{(5)}$
Decoupling capacitor	μF	1 (off-chip)	0.0006 (on-chip)	0.1 (off-chip)	Not used
Switching frequency	MHz	–		1 (Typical)	1000 (Maximum)
Quiescent current	mA	0.02 – 0.34	6	0.0027	0.13 – 10$^{(6)}$
Current efficiency	%	99.8	94.3	98.7	96.0 – 99.95$^{(7)}$

(1) Without bandgap circuit
(2) $I_{\rm LOAD}$ step is 0–200 mA at with rise time of 100 ns.
(3) $I_{\rm LOAD}$ step is 0–100 mA at with rise time of 100 ps.
(4) $I_{\rm LOAD}$ step is 0–200 μA.
(5) $I_{\rm LOAD}$ step is 136–250 mA at with rise time of 5 ns.
(6) Simulation: 0.13 mA at 10-MHz operation and 10 mA at 1-GHz operation.
(7) 96.0% at 1-GHz operation and 99.95% at 10-MHz operation.

appropriately, both high-current efficiency and fast response time are achieved.

IV. Conclusion

For area reduction and fast transient response, a digitally controlled low-dropout (LDO) voltage regulator with low-voltage MOS transistors was developed. Using withstand-voltage relaxation schemes, nominal input voltage increases to 1.39 V when the nominal output voltage is controlled to 1.2 V. The withstand voltage of low-voltage MOS is guaranteed. This output voltage is sufficiently high for modules that have high-frequency operation. Moreover, the proposed power-MOS configuration covers wide-range load current variation (400 μA – 250 mA) with only 56-level power MOSs. The linear resistance step of the power MOS reduces the control error. The fabricated LDO is only 0.057 mm^2 in a 40-nm CMOS. The measured response time at 1-GHz switching frequency is 0.07 μs.

References

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