

# Design Methodology and Circuit Techniques for Any-Load Stable LDOs with Instant Load Regulation and Low Noise

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**Abstract** Application of the structural methodology to the LDO design creates a new class of circuits: any load stable, with instant transient response, large power supply rejection and low noise. Presented are examples of the embedded in SoC LDOs for the SRAM unit (5 ns reaction time on the load steps), radio transmitter (shaping the required noise vs. frequency curve) and for memory retention in the shutdown state (300 nA quiescent current). These LDOs can operate with or without off-chip load capacitors; they are robust to the process and temperature variations and portable to any CMOS process.

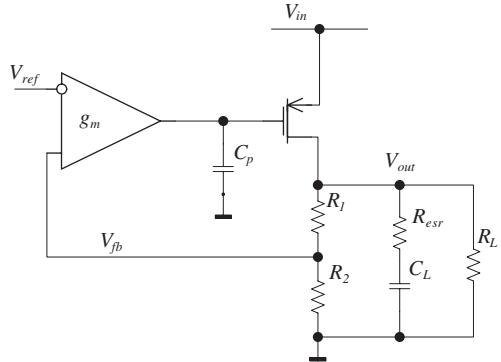
## 1 Introduction

The large drain-source and gate leakage of the core transistors in CMOS processes with a minimum gate length of 90 nm and below create a severe on-chip power management problem. Complicated powering schemes have been developed, implying multiple power domains on the system-on-silicon (SoC) chip. These domains may include DSP core(s), few banks of SRAM, analog units like GSM or Bluetooth radio, and audio units. Chip is powered by the one or two DCDC converters, which are followed by numerous LDOs [1]. LDOs for digital domains require keeping the output voltage within the error window against instant load switching from zero to maximum current (and back). LDOs for analog units may require low noise and large PSRR. Some of these LDOs may control the body biasing inside the power domain. The body biasing demands the bidirectional output current capability. Presence of the 15–20 LDOs in the SoC becomes a common practice. Clearly, use of the external load capacitor for each of these LDOs is prohibitively expensive. We have to learn how to design LDOs while employing the on-chip load capacitors (100 pF to few nF) only.

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**Fig. 1** The standard LDO structure



An LDO with the traditional structure, shown in Fig. 1, comprises the error amplifier connected to the gate of the large PMOS pass device [2]. There are two main problems of this structure for SoC applications.

1. For any compensation scheme, a combination of load current and load capacitance exists when such LDO is unstable, which results in the requirement of some minimum (or maximum) load capacitance and/or its ESR. Uncertain stability leads to the dedicated compensation in each application, multiplying design efforts in the SoC power management.
2. If the quiescent current ( $I_q$ ) is limited below 10% of the maximum load current, reaction time on the load step is in the  $\mu\text{s}$  range. When the on-chip load capacitor only is used, this would be too long for controlling the output voltage transients within acceptable (<10%) error window.

Recently, the dual-loop LDO structures, allowing an improvement of the load step reaction time, have been shown [3–5]. A figure of merit for LDO dynamics has been suggested in [4], which combined the maximum load current  $I_{L\max}$ , load capacitance  $C_L$ , dynamic error  $\delta V_{out}$  and quiescent current  $I_q$ :

$$FOM = C_L \delta V_{out} I_q / I_{L\max}^2 \quad (1)$$

While having dynamic advantages, these dual-loop LDOs are still not fast enough to provide the satisfactory load regulation without support of the external capacitor.

The structural design methodology [6] has been applied to the embedded LDO development. The result is a set of circuits which can operate with or without an external load capacitor, have extremely fast reaction time on the load changes and exhibit low noise and large power supply rejection. These “any load” LDOs can sink and source current to the load, operate in sleep and active modes, and they are robust to the process and temperature variations. As external capacitors are not obligatory, it enables sprinkling of multiple LDOs in the SoC complicated power management structure without extra cost or die area taxation.

Basics of the structural design methodology are presented in the paragraph II, followed by circuit examples and techniques to improve the particular parameters of

interest: quiescent current, transient response, PSRR at different frequencies, worst-case phase margin or dumping factor, and noise. Examples include LDO for the memory retention with low  $I_q$  (paragraph 3), LDO for the Bluetooth transmitter with strict noise requirements (paragraph 5), and LDO for SRAM bank designed for the fast load step response while having low  $I_q$  (paragraph 6). Stability verification problems in the multiloop system are considered in the paragraph 7.

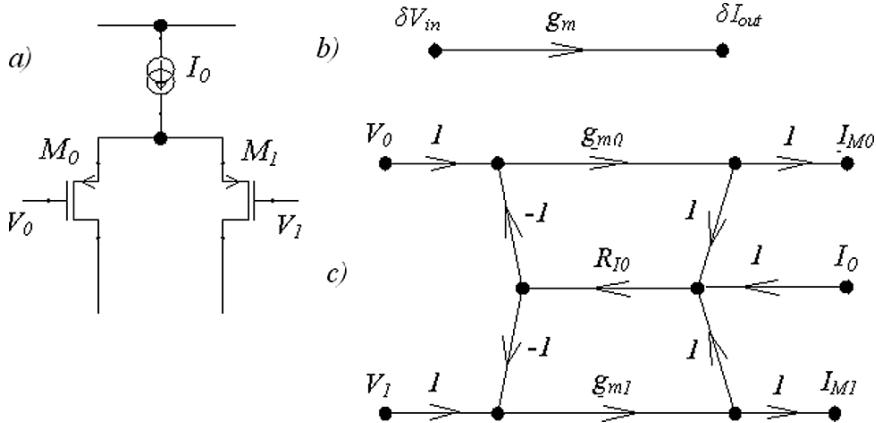
## 2 Basics of the Structural Design Methodology

There are 18,000 different amplifiers that can be created from just 2 transistors – even before the parametric variations (this number is derived from a multiple of options: NMOS/PMOS, common gate/source/drain, 4 kinds of feedback for each transistor, and for the amplifier as a whole). With the typical analog circuit containing more than a 100 transistors, the number of variants is greater than the number of atoms in the galaxy – and only a few can solve a designer's problem. As a result, most of analog designers are using a cookbook approach, creating a new circuit from the existing one with the fewest changes possible. Radically new solutions are rare, and they are considered to be the major intellectual property by designers and their employers. A way of new circuit invention is needed. The structural methodology is such a procedure: how to find a set of acceptable for application solutions and how to weed out bad or inferior circuits instantly. It has a long success record in the design of operational amplifiers [6], references, power amplifiers, DCDC converters, and now LDOs. By following described below steps, a designer can find a set of satisfactory solutions, some of which are known and some are new. Then designer can finally choose circuit based on the personal preference and secondary parameters of importance.

### 2.1 Graphic Presentation of the System

The first step in the circuit design should be a presentation of the problem to be solved in a graphic form. The graphical presentation is much more informative and easier for comprehension than any text description or set of equations. The most common language for such presentation is a structural diagram. Another option is the signal flow graph, which has the advantages of existing formal rules for equivalent transformations [7] and drawing simplicity. Almost forgotten, but preferred by founders of the control theory, like Mason or Bode, the signal flow graphs have recently started to gain popularity [8].

An example of signal flow graphs of the differential stage is given in Fig. 2. The differential stage can be presented in the simple form of a single  $g_m$  link or in more details as illustrated in Fig. 2c. Graph in Fig. 2c includes the transconductance of each transistor and a common-mode feedback. The graph in Fig. 2c is called the "general structure with common-mode feedback". Properties of this graph can be



**Fig. 2** Signal flow graphs of the differential stage

extrapolated to any multi-loop, multi-dimensional structure (or multidimensional structure can be equivalently transformed to this graph), just as complex numbers represent properties of the n-dimensional space.

An analysis of the differential structure with common-mode feedback [6, supplement A] is instrumental in the design of circuits with multiple input/output variables, such as class AB stages or multiple output DCDC converters. It also helps in the single-glance estimation and selection of the circuit within the set of possible options.

## 2.2 Dedicated Feedback Control for Each Important Parameter

The next step in the circuit design is a transformation of system structure to the form where every important variable is controlled by a dedicated feedback loop. Circuits without such feedbacks should be weeded out without any further consideration. The advantage of the system where all significant parameters are controlled is obvious; however, the main obstacle to the universal application of this rule is the problem of stability in the resulting multiloop structure.

Although not necessary, but sufficient, condition for the whole system's stability is the stability in each and every loop within this system [9]. A feedback loop can be unconditionally stable (with any load and signal source impedance) if its open-loop transfer function has only one pole. Consequently, the easy way to ensure system stability is designing each loop with the single-stage (single-pole) amplifiers only.

This restriction immensely simplifies the design process. Although in some cases the exclusive use of the single-stage amplifiers is not possible; here, conventional compensation techniques need to be applied and stability has to be carefully verified.

Standard verification of the stability using the merit of phase margin requires a break in the feedback loop and is not suitable for the multiloop system (which loop

to break?). Method of the multiloop system small-signal stability verification by using AC simulations has been described in [10]. Due to the unavoidable presence of the non-linear effects in the circuit, the small-signal only stability verification is not sufficient. The small- and large-step response transient simulations followed by extraction of the overshoot and dumping factor could be used instead, as discussed in paragraph 7.

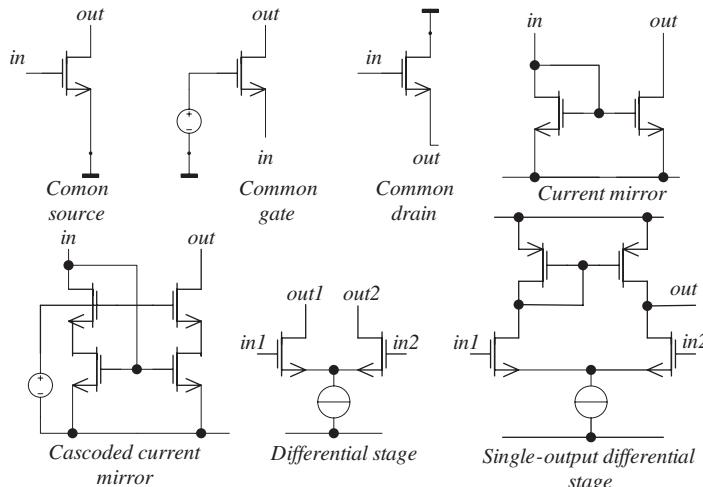
## 2.3 Library of Elementary Cells

The next design step is implementation of the system structure with elementary cells. The library of these cells includes circuits described in every textbook on analog design, shown in Fig. 3.

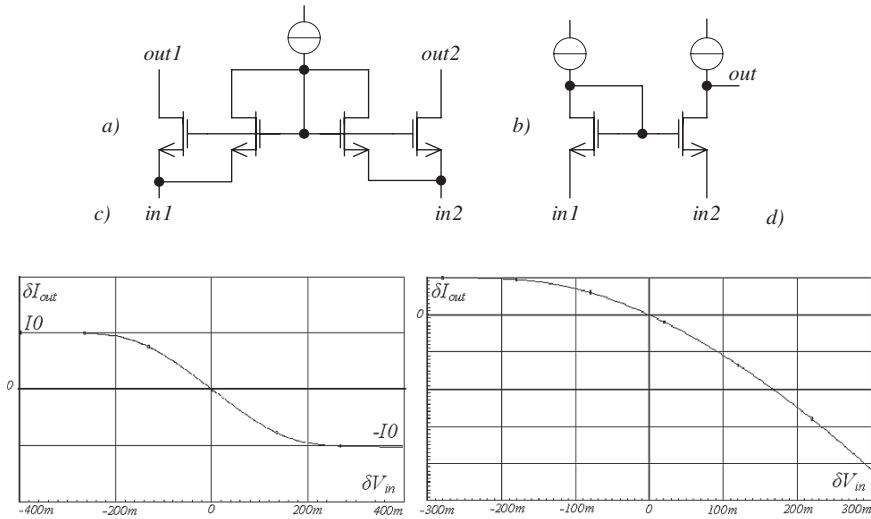
It can be amended by few lesser known cells. In particular, the current-input amplifiers shown in Fig. 4 should be a part of the every designer's arsenal. In the circuit of Fig. 4a,  $M_0$  and  $M_1$  currents are matched, as well as the currents of  $M_2/M_3$ . Consequently, input currents do not depend on the common-mode input voltage, so the common-mode input impedance is high. The differential input impedance is small and equals to  $1/g_m$ . Dependence of the output current vs. input voltage (Fig. 4c) is identical to the standard differential stage.

The single-output version of this amplifier is shown in Fig. 4b. In this cell, the current sinking from output is unlimited and output current vs. input voltage curve (Fig. 4d) is non-symmetrical.

Use of the current-input amplifier cell inside the local feedback loops improves the speed of these loops at least five times for any given current budget. It simplifies



**Fig. 3** Elementary cells library



**Fig. 4** The current-input amplifier cells

the frequency compensation, allowing replacement of the common-source gain stages in the signal path with the common-gate ones, which have much smaller delay.

The extermination of all or most compensation capacitors becomes possible. For example, an operational amplifier described in [11] comprises more than 25 feedback loops, but the only compensation capacitors on its chip are the two Miller capacitors in the main signal path.

## 2.4 Features of the Good Circuit

With structural methodology, we restrict a set of circuits to be considered to “good” circuits only.

1. Good circuit has a dedicated feedback loop controlling each parameter which is important for the reaching of system goals.
2. Dynamically each local loop and system as a whole are stable and their step response looks like the response of the system with first- or second-order transfer function.
3. Good circuit is robust to the variation of the component parameters, process and temperature.
4. Non-linear effects (start-up, power glitch, input/output overload, etc.) have been considered and necessary clamps/limiters added.
5. For embedded in SoC designs, good circuit should not be sensitive to substrate noise.

Acceptable application solutions can and sometimes do exist outside of the “good” circuit domain. However, after 30 years of experience, these “no good” circuits could never outperform circuits from the chosen set.

Nesting of the feedback loops inside the system has been discussed above, as well as the requirement of stability in the each loop. Requirement of the circuit robustness makes parametric optimization efforts practically useless. If optimum of the goal function is dull, then based on a common sense choice of the parameters is good enough; if this optimum is sharp – then this circuit is not robust and consequently is inadequate.

Designing a circuit for a nominal mode of operation normally occupies no more than 20% of total design time. The rest is taken up in consideration of nonlinear effects and in creation of various protective measures. There is no general way to predict such effects. All we can do is study the application and play multiple “what if?” scenarios.

In SoC design, interaction of different units through substrate and supply should be taken into account from the very beginning. Correction measures can be in the layout and process (unit placement, isolation rings, double-well process, separate supply wiring and wirebonds), in the choice of components not sensitive to substrate noise, in the circuit techniques (differential signal processing), and in the choice of the system architecture.

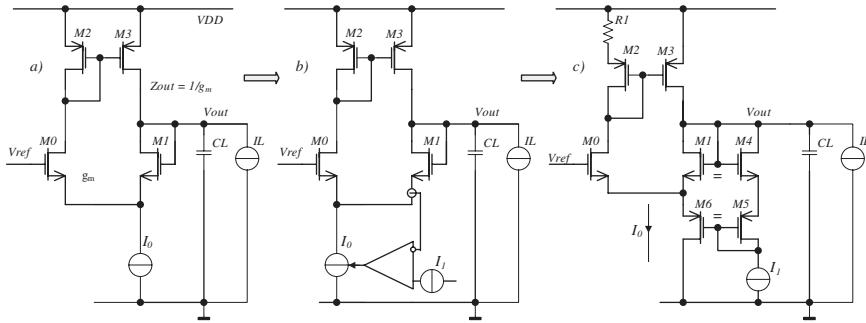
The problem-solving approach in structural design is close to the one described in [12] and to the modern philosophy called “systems thinking” [13].

### 3 Memory Retention LDO

Design of the LDO for memory retention is one of the simplest examples of the structural methodology use. In this application, the supply voltage of the SoC SRAM bank has to be kept at the value which is lower than necessary for operation but sufficient for preserving of information. The only current consumed by the load is the SRAM bank leakage, which can vary from few nA to tens of  $\mu$ A depending on the temperature and process variations. Accuracy better than 100–150 mV is not required, as well as high speed. When the SRAM built-in bypass capacitance only is present, the LDO load capacitance can be merely 200–1000 pF, which can increase up to few  $\mu$ F if the off-chip load capacitor is utilized. The LDO’s most important parameter is the quiescent current, which should be kept within 200–300 nA.

The voltage follower in Fig. 5a is unconditionally stable with any load as it has only one transistor (and one pole  $CL/g_m$ ) in the feedback loop. Its obvious limitations are: a) output current is limited by  $I_0$ ; b) output impedance is high and equals to  $1/g_m$  of the  $M0/M1$  pair.

One of the ways to remove limitation of the maximum load current is controlling the current through transistor  $M1$  by means of the feedback loop varying the  $I_0$  value (Fig. 5b). In this circuit, a rise in the load current decreases current through  $M1$ . It increases  $I_0$  until  $M1$  current returned to the reference value  $I_1$  set by the feedback



**Fig. 5** The memory retention LDO

loop. Increasing  $I_0$  flows through  $M_0$  and mirrors by the  $M_2/M_3$  to the load. This second feedback loop is nested inside the main one of the regulator (around  $M_1$ ). As the main loop is stable, then stability of this additional loop is sufficient for the overall system stability with any load.

One of the possible implementations of this structure is shown in Fig. 5c [14], where the reference, amplifier and actuator of the feedback loop consist of  $M_4/M_5/M_6$  and  $I_1$ . The output current in this circuit is limited only by the size and current capability of  $M_6-M_0-M_2/M_3$ . In order to increase the maximum output current, as well as improve output impedance and efficiency at high load currents, the  $M_2/M_3$  current mirror is non-symmetric (which is implemented with resistor  $R_1$ ).

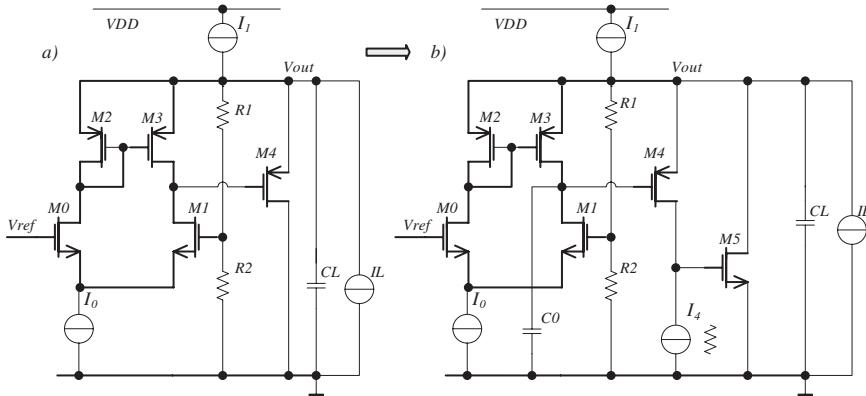
Both feedback loops in the circuit of Fig. 5c have only one gain stage (single pole). Such single-pole system is stable with any load and any biasing above the transistor leakage levels. The main drawback of this circuit is the high output impedance, approximately equaled to  $1/g_{m1}$ , limiting the accuracy.

The LDO of Fig. 5c was implemented in TSMC 0.18 process with 100 nA  $I_1$  and load current within 10 uA. The maximum error of this LDO, consuming at no-load condition less than 300 nA, is about 100 mV.

## 4 The Basic Multiloop LDO Structure

The output impedance of the circuit in Fig. 5a can be improved by the larger gain in the main feedback loop around  $M_1$ . It can be done by the follower between  $M_1$  drain and output, as shown by  $M_4$  in Fig. 6a.

This circuit is not yet a regulator, as it needs current  $I_1$  for functionality, but can be used for the stability estimation. In addition to the pole defined by the  $M_4$ 's output impedance and load capacitance ( $CL/g_{m4}$ ), this circuit has a second pole defined by the  $g_{m0}$  of  $M_0/M_1$  pair and parasitic capacitance at the gate of  $M_4$  ( $C_{p4}/g_{m0}$ ). The worst-case stability occurs when these poles are equal. If this happens, system, in theory, is at the edge of oscillations with zero phase margin. In practice, it may oscillate due to the presence of small poles. Nevertheless, a 2-stage system can be



**Fig. 6** Steps to the any load stable high current LDO

unconditionally stable with any capacitive load. It can be achieved by limiting the voltage gain of the first stage [15]. The direct dependence between the first stage gain and worst-case phase margin for any capacitance load has been shown in [16].

The first stage ( $M0/M1$ ) voltage gain is equal to  $A = g_{m0}R_{p4}$ , where  $R_{p4}$  is an equivalent resistance at the gate of  $M_{P4}$ . Thus, by controlling this resistance, any load stability of the circuit in Fig. 6a can be achieved. This gain control can be done with a real resistor, or, alternatively, the parasitic resistance at the  $M4$  gate can be decreased by choosing a shorter channel length of  $M0/M1$ , as well as of  $M2/M3$ .

Biasing the  $M0/M1/M2/M3$  amplifier from the  $V_{out}$  is another useful feature of the circuit in Fig. 6a. It ensures that DC PSRR of the regulator is virtually unlimited.

If the voltage gain in the  $M0/M1$  stage is small, the overall gain of the regulator may not be sufficient for acceptable load regulation. It is certainly a case if load current is  $\sim 10,000 \times$  larger than  $I_0$ . Additional gain, in accordance with structural design principles, should be achieved by nesting of the stages and boosting the gain of an existing, already stable, amplifier, instead of the cascading gain stages in series.

One of the ways to boost the output conductance of  $M4$  and improve load regulation of the LDO is shown in Fig. 6b. It is done by an additional feedback loop, where the drain current of  $M4$  is being compared to  $I_4$ , and the difference is amplified by  $M5$ . This new loop also has two poles, where the first one is defined by the  $g_{m4}$  and parasitic capacitance at the gate of  $M5$  ( $C_{p5}/g_{m4}$ ), and the second is equal to  $CL/g_{m5}$ . Using the same approach, unconditional stability in this loop can be achieved by decrease in the voltage gain of  $M4$ , which is equal to  $g_{m4}R_{p5}$ . The equivalent resistance  $R_{p5}$  at the gate of  $M5$  can be controlled either by shortening of the  $M4$  channel length or by the partial or full replacement of  $I_4$  with physical resistor ( $I_4 = V_{gs5}/R$ ).

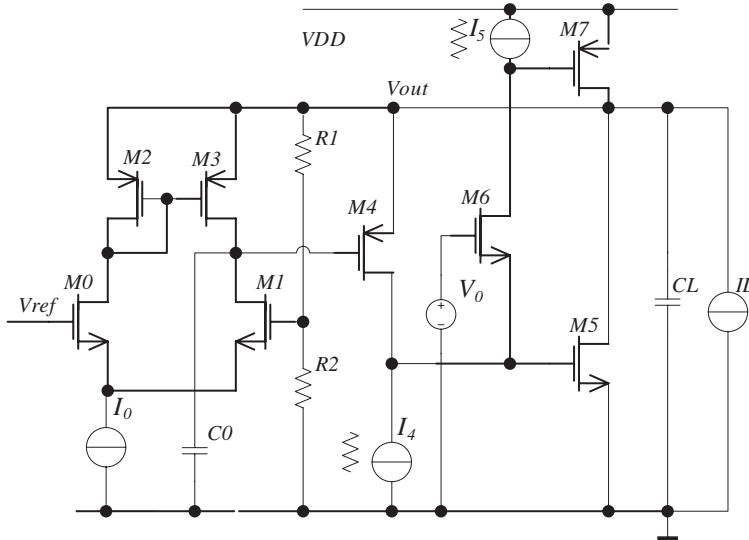
In order to avoid any additional poles in the  $M4/M5$  feedback loop, transistor  $M4$  should operate as a common-gate device, requiring capacitor  $C0$  at its gate. Without such a capacitor, the large high-frequency impedance at the  $M4$  gate in

combination with the  $M4$  parasitic gate-source capacitance will add delay and compromise stability in the  $M4$ - $M5$  loop. The  $C0$  value should exceed the parasitic gate-source and gate-drain capacitances of  $M4$  (it looks like, but it is not a parallel compensation capacitor!).

As a result, both feedback loops in the circuit are unconditionally stable ensuring the overall system stability with any load.

Finally, in order to achieve the pull-up LDO capability, the new gain link is added in parallel to the  $M5$ . This link consists of the cascoding device  $M6$ , current source  $I_5$  and power transistor  $M7$  (Fig. 7). In the same way, stability in this new loop ( $M4$ - $M6$ - $M7$ ) is achieved by the low resistance of the current source  $I_5$  (which can be done by implementation of  $I_5$  with resistor). The value of the voltage source  $V_0$  defines the shoot-through current of  $M5/M7$  in no-load condition.

The LDO of Fig. 7 [17] can sink and source current to the load, it has exceptional bandwidth for any given process and quiescent current, and it is stable with any load capacitance. This circuit is the base for application-specific variations described below.



**Fig. 7** LDO for radio units

## 5 Low-Noise LDO for Radio Units

The LDO for the radio unit does not require instant current switching. Its most important parameter is the noise curve as the supply noise directly affects the quality of radio transmission and reception. Different components affect noise at different

frequencies and the noise curve of circuit in Fig. 7 can be shaped to requirements by means of the parameter choice.

At the low frequency ( $f_1 < g_{m0}/2\pi C0$ ) the noise is dominated by the  $M0-M3$  amplifier. This is primarily the flicker noise, defined almost exclusively by the size of input devices  $M0/M1$  and independent on the biasing  $I_0$ . In the test LDO  $I_0$  has been set to 1  $\mu$ A. Part of the noise originated in the current mirror devices ( $M2/M3$ ) can be decreased to negligible level by the use of source degeneration resistors.

At the frequencies between  $g_{m0}/2\pi C0$  and LDO unity-gain frequency, noise is defined by  $M4$  and  $I_4$ . In the presence of load capacitor, the unity-gain frequency is equal to  $UGF = Ag_{m4}/2\pi CL$ , where  $A$  is the gain in the  $M4-M5$  loop.  $M4$  should be sufficiently large to have a flicker noise corner below  $f_1$  and operate in the weak inversion. Transistors in the current mirror which form  $I_4$  should be heavily degenerated with resistors, or  $I_4$  should be implemented with a resistor. Then, the main source of noise at medium frequencies is the  $M4$  source impedance  $1/g_{m4}$ . In other words, the  $M4$  high frequency noise is inverse proportional to  $\sqrt{I_4}$  and  $I_4$  should be as large as possible within the current budget. In the test LDO the current  $I_4$  has been set to 900  $\mu$ A.

At the frequency above UGF the LDO noise is filtered and defined by the  $CL$ .

An example of shaped by the component parameters noise curve is shown in Fig. 8 (thick line – goal, medium – silicon results and thin – simulations).

The step response time constant of  $M0-M4$  feedback loop, because of very small  $I_0$  and large  $C0$ , is in the order of 20–50  $\mu$ s, as shown in Fig. 9. Due to the very fast reaction in  $M4-M5-M7$  loops, the load is regulated within 30 mV error window

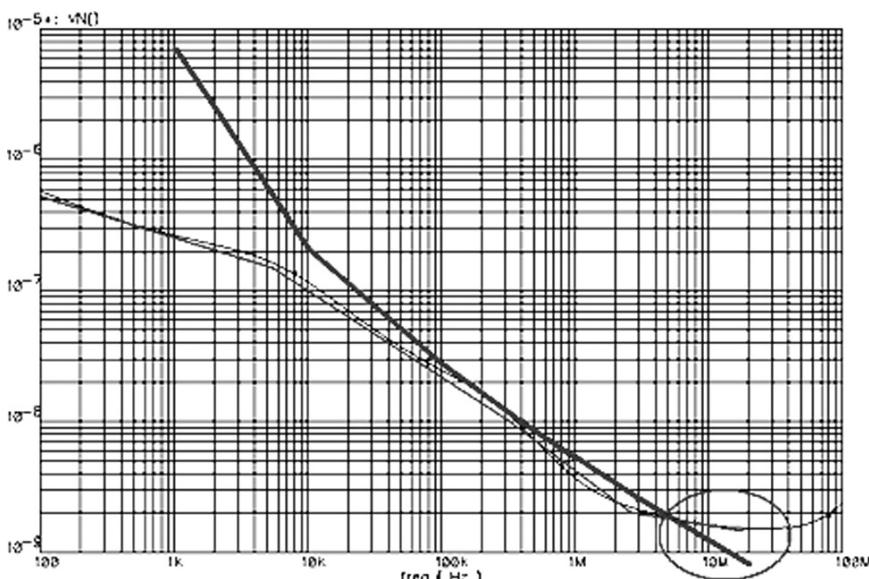
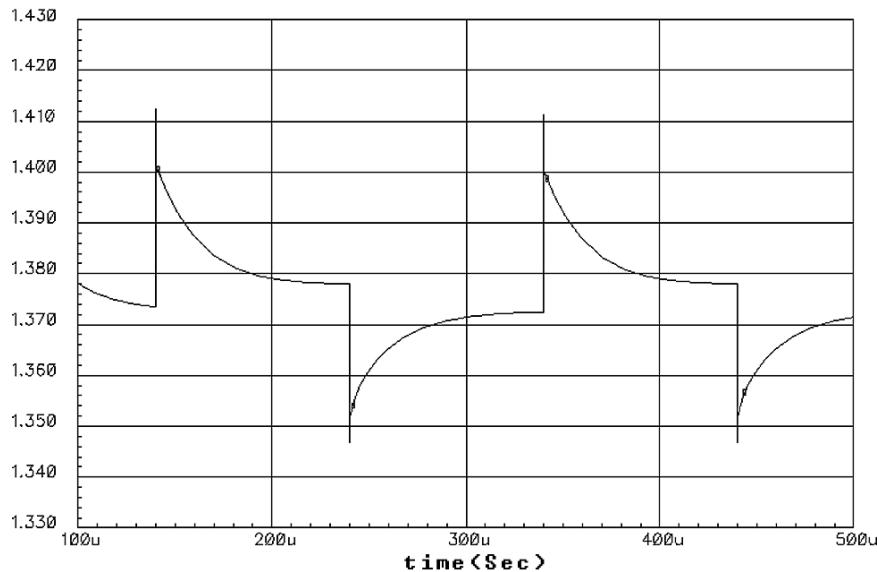


Fig. 8 Shaped noise curve of the LDO



**Fig. 9** LDO zero to 30 mA load step response,  $CL = 100 \text{ pF}$

even with 100 pF load capacitance only. Time constants in these loops, due to the large  $I_4$  and the presence of parasitic capacitances only, are in the order of 1–2 ns. The step response is symmetrical for zero to 30 mA and back load current variation, because this LDO can both sink and source current to the output.

Other parameters of the test LDO made in 65 nm Texas Instruments process are in the table below.

Quiescent current	1 mA
Maximum $IL$	30 mA
Load capacitance	> 100 pF
PSRR at 400 kHz at 20 MHz	25 dB 21 dB
Die area	15,000 $\mu\text{m}^2$

## 6 LDO for Digital Units

The current consumption of the digital unit, such as SRAM bank, can change in the fraction of nanosecond from zero to maximum (50 to 100 mA), or back.

To avoid missing codes, the power management circuit has to keep the supply voltage of this unit within an error window (50–80 mV from target) even with such a steep current variations. The supply voltage of the unit is provided by the LDO and is supported by the built into every gate bypass capacitance (500–2000 pF total).

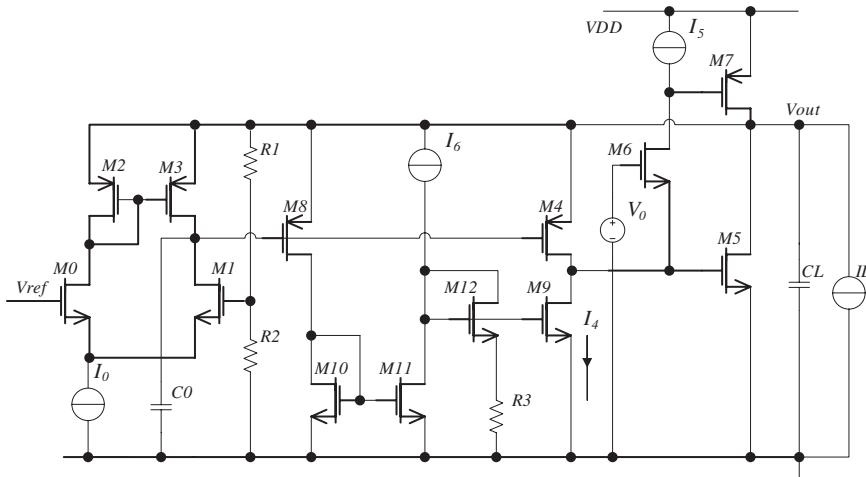
To solve this problem, LDO should have no more than 4–6 ns reaction time on the load changes. Due to the wirebond and board bus inductance, the off-chip capacitor is almost worthless for this task, because of the 100 mV or larger transient voltage spike across 5–10 nH of the total (bus + wirebond + board) inductance between load and capacitor.

Sufficiently fast load regulation has been achieved in the two-loop LDO having a large current consumption ( $\sim 10\%$  of the maximum load current) [4]. As the digital unit can be enabled for long periods of time, such consumption is prohibitive for battery powered devices, and should be below 50–100  $\mu\text{A}$ .

When the load current in the circuit of Fig. 7 is switching from high to low,  $V_{\text{out}}$  is increasing, causing a rise in the current through  $M4$ , followed by an increase in  $V_{gs5}$ . Transistor  $M5$  starts to run excessive current until  $M7$  gate potential is decreased by the current  $I_5$ . As current through  $M4$  is practically unlimited, LDO has fast (3–5 ns) reaction time on the load switching from high to low.

The critical drawback of the circuit in Fig. 7 is a delay in reaction on the instant load step from zero to high current. The gate of the large pass device  $M7$  has to be charged to the new larger  $V_{gs7}$  and the only available current for that is  $I_4$ . As shown in Fig. 9, this is not a problem if  $I_4$  is large. If the total current budget is only 50  $\mu\text{A}$  and  $I_4$  is small, step reaction delay becomes too large.

A new feedback loop ( $M8\text{--}M10/M11\text{--}M9\text{--}M5$ , Fig. 10) is added to improve the reaction time when load is switching from low to high current [18]. While load is constant, current of  $M8$  is matching  $M4$ , so  $I_{M4} = I_{M8} = I_{M10} = I_{M11} \sim I_6$  (some part of  $I_6$  flows through  $M12/R3$ ). This loop has multiple gain stages and needs compensation provided by the gain attenuation by  $M12$ .  $R3$  decreases this attenuation when the current through  $M8\text{-}M10/M11$  becomes small.



**Fig. 10** LDO for digital units

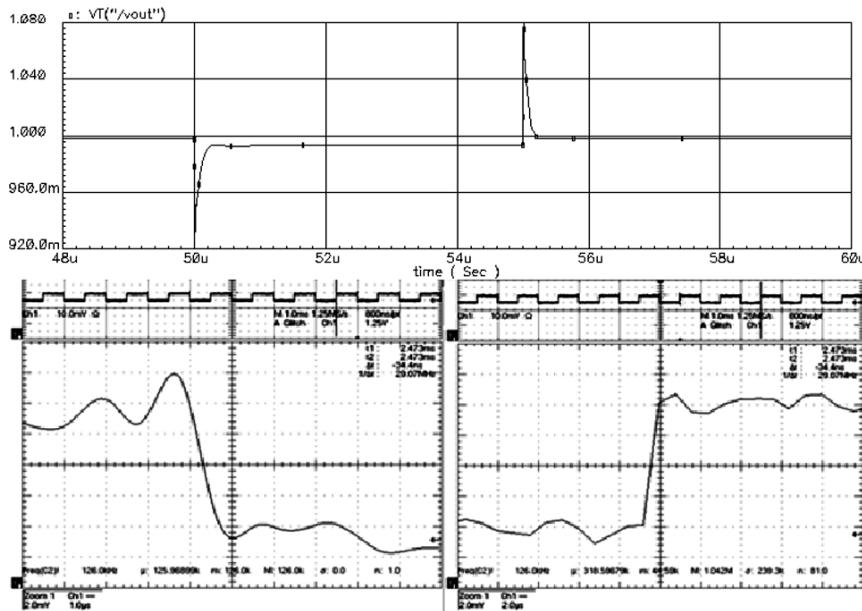


Fig. 11 LDO response on the load step

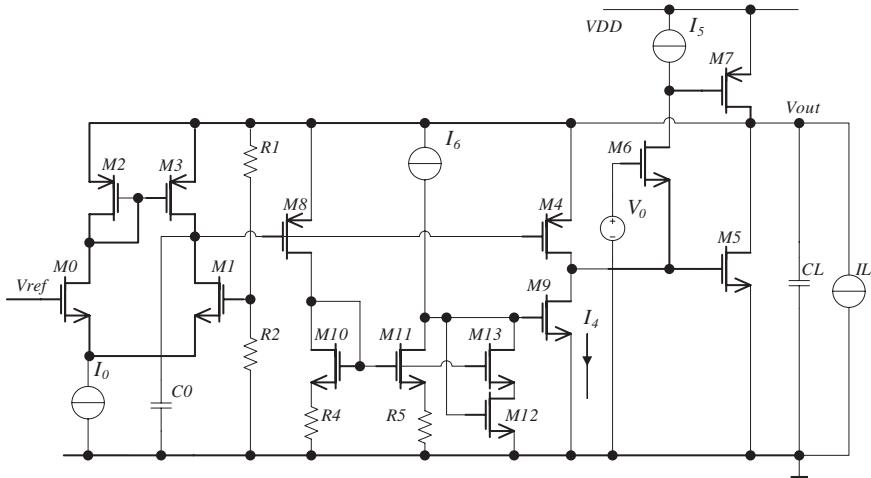
When the load current increases,  $V_{out}$  dips and  $M8$  shuts down, as well as  $M10/M11$ .  $I_6$  turns  $M9$  on; thus,  $I_4$  increases speeding up the charging of the  $M7$  gate capacitance. As a result, LDO reaction time on the load steps becomes as small as 4–5 ns in both directions.

Simulated step response (0–50 mA) of the test LDO is shown in the top part of Fig. 11, and scope picture is below it. As shown, no dynamic error has been found in the silicon – probably, 5 ns/50 mV pulses are too fast to be detected by the available lab equipment.

Other parameters of the test LDO manufactured in the 65 nm Texas Instruments process are in the table below.

Quiescent current	$80 \mu\text{A}$
Maximum $IL$	50 mA
Step settling within 10 mV	< 200 ns
Load capacitance	> 200 pF
PSRR at 1 MHz	25 dB
Die area	14,000 $\mu\text{m}^2$

The value of the figure of merit (1) for this LDO is 0.003, which is 10 times better than 0.032 achieved in the best published circuit, and 50–100 times better than other LDOs of standard structure of Fig. 1 [4].



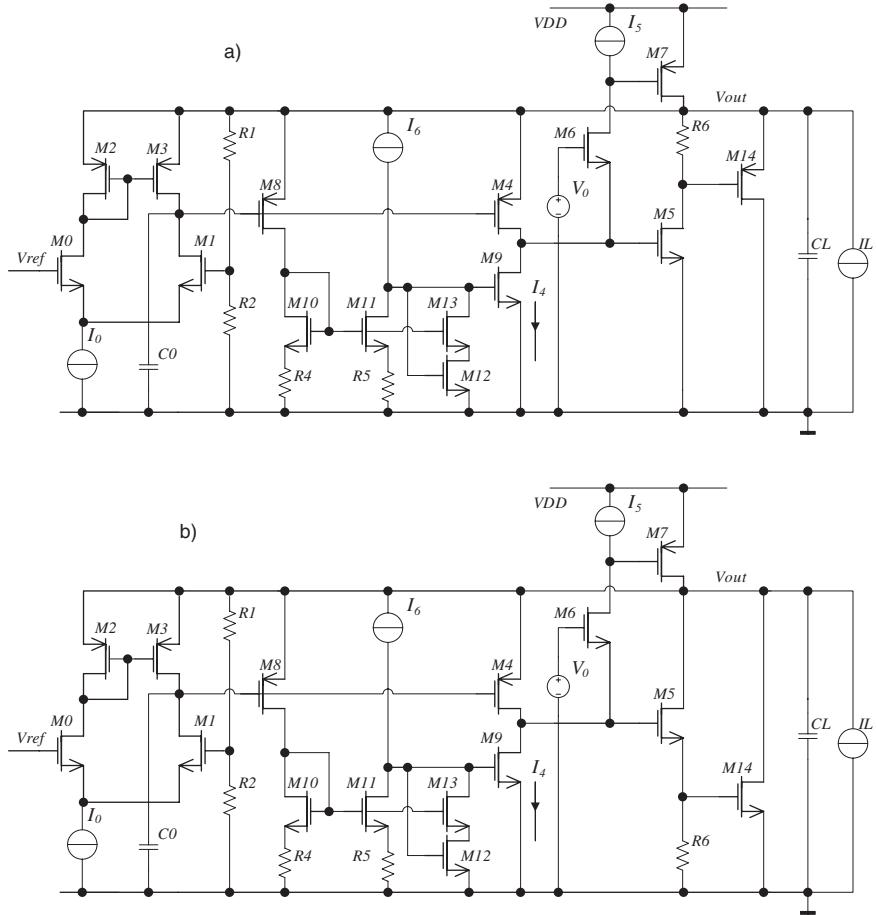
**Fig. 12** LDO with class AB step response boosting

Efficiency of the step response boosting loop in Fig. 10 depends on the absolute value of  $R_3$ . If  $R_3$  is too low, then  $I_6$  can not significantly boost the current through  $M9$  during transient. If  $R_3$  is too large, the gain in the  $M8 - M9$  link may become too large and may cause instability. Sensitivity to the  $R_3$  value can be eliminated by the use of a class AB amplifier with low gain for a small input signal and large gain for the greater input. Such circuit is shown in Fig. 12 [19].

If the load current is constant, current through  $M8$  is large, as well as the matching current in  $M4$ :  $I_{M8} = I_{M4} = I_{M10} = I_{M11}$ . Voltage drop across  $R4/R5$  is equal to the  $M12$   $V_{ds}$ . The value of  $R4/R5$  is chosen to create a 100–150 mV voltage drop, keeping  $M12$  out of the trioding region of operation. At this mode, the gate potential of  $M10/M11/M13$  is high and  $M13$  operates as a cascoding device for  $M12$ . Transistor  $M12$  operates as a diode in parallel with gate-source of  $M9$ , decreasing its gain. Current  $I_6$  is splitted between  $M11$  and  $M12$ , as in the previous circuit in Fig. 11.

If the load current steps up,  $V_{out}$  drops, and  $I_{M8}$  decreases; current through  $M10/M11$  and voltages across  $R5/R6$  decrease as well. The gate potential of  $M13$  drops, forcing down the  $M12$  drain potential. When  $M12$  starts to operate in the triode region, its current decreases.  $I_6$  turns  $M9$  on, increasing  $I_4$  and allowing fast charging at the gate of transistor  $M7$ . As a result, the reaction time on load step of the LDO with  $I_6$  of only 5–10  $\mu$ A and the total consumption of 40–50  $\mu$ A is as small as 4–5 ns. The circuit now is robust and can operate in wide variation of the component parameters and biasing currents.

The current capability of  $M5$  should be sufficient to absorb a full load current during its transient from large to small. However, because of the speed and stability considerations, transistor  $M5$  should have a low gate capacitance and, consequently, be small. To merge these requirements, the additional gain link  $R6-M14$  can be added as shown in Fig. 13.



**Fig. 13** LDOs with increased output current

In both circuits in Fig. 13a and b, transistor  $M_{14}$  is off if the load current is stable. If large pull-down current is required, current through  $M_5$  increases the voltage across  $R_6$ , turning on the  $M_{14}$ . As the current of  $M_5$  still flows from the  $V_{out}$ , this additional gain does not create a stability problem. The circuits in Fig. 13 illustrate method of the loop gain buildup using the stage nesting instead of cascading. It avoids all the compensation problems caused by the series connection of gain stages.

## 7 Verification of the Stability with CAD Tools

When circuit solution is chosen and seems to be operational, the next design step is verification of its robustness, including stability, over the operating temperature range and process variations. When designing the stand-alone LDO, extensive

silicon measurements could be done with various loads, temperatures and production lots. When designing the embedded in SoC unit, such measurements are not always feasible. The quantity of the SoC test chips may be limited, and through measurements may not be possible due to test environment constraints. Providing that good component models are available, insufficiency of the silicon measurements can be compensated by extensive simulations. In these simulations tens of possible environmental combinations have to be checked; therefore, an automated procedure is desirable.

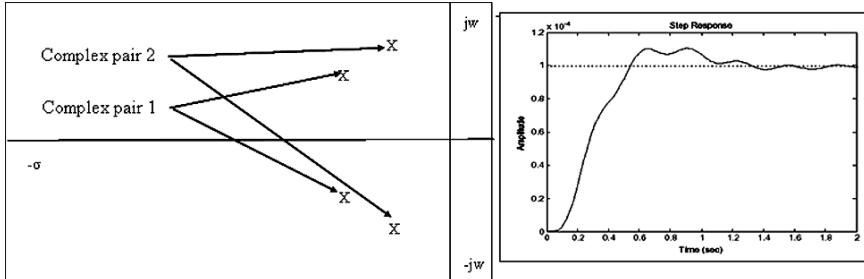
By definition, a system is stable if the transient processes in it are settling over time after any input signal. Traditionally, the robustness of the feedback system stability is estimated by the merit of phase margin. The value of phase margin can easily be extracted from AC simulation results, and a statistical tool can be used after multiple simulation runs. Phase margin estimates the small-signal stability only and can not predict any large-signal, conditional stability effects. Phase margin is not applicable for the multiloop system design, being the open-loop parameter. Another, less obvious, limitation is that phase margin is informative for minimal-phase systems only; and the transistor in the common-source connection already is not a minimal phase unit. As a result, the small phase margin numbers below 40–50° can be either too pessimistic or too optimistic when used as estimation of the system settling behavior.

Bode plots are easy to understand and are instrumental in stability conception and compensation of the single-loop system. AC simulations take much less computation resources, which in the past was another reason for their wide use in design. Today, in abundance of very fast and distributed computation, we do not have to limit ourselves to AC simulations or even use it as a main tool. The role of AC simulations is more for pleasing the tradition and peace of mind of some individuals.

As was mentioned before, each loop in the good system should dynamically behave as a first- or second-order system. That seems to be a limitation, but, from a closer look, it almost always is not. High-order systems in theory can provide faster and more accurate transient process; in real design we normally use non-linear cells to ensure the required large-signal behavior, or add feedforward links which decrease the system order without damaging the mid-frequency behavior [6, Chapter 4].

The transient simulations parameters indicating the system stability are the step response overshoot factor  $M = (y_{max} - y_{set})/y_{set}$ , where  $y_{max}$  and  $y_{set}$  are the maximum and settled output values, and dumping factor  $Q = A_n/(A_{n-1} - A_n)$ , where  $A_n$  is the settling curve peak amplitude during the n-th period of settling. For the minimal-phase, linear and second-order single loop system these parameters have a direct relationship with the phase margin. The second-order system with the transfer function  $A(s) = \frac{A_0\omega_n}{s^2 + 2\xi\omega_n s + \omega_n^2}$  has a dumping factor of  $Q = 1/2\xi$  and a phase margin  $\Theta = \tan^{-1} \frac{2\xi}{\sqrt{\sqrt{4\xi^4+1}-2\xi^2}}$ . For example, a phase margin of 43° is equivalent to the  $Q = 1.25$ , 52° – to  $Q = 1$ , 65° – to  $Q = 0.7$ , and 11° – to  $Q = 5$ .

The dumping factor is much more convenient for stability estimation than phase margin. It can be extracted from both small and large step transient simulations, covering cases with conditional stability. Dumping factor is valid for the non-minimal



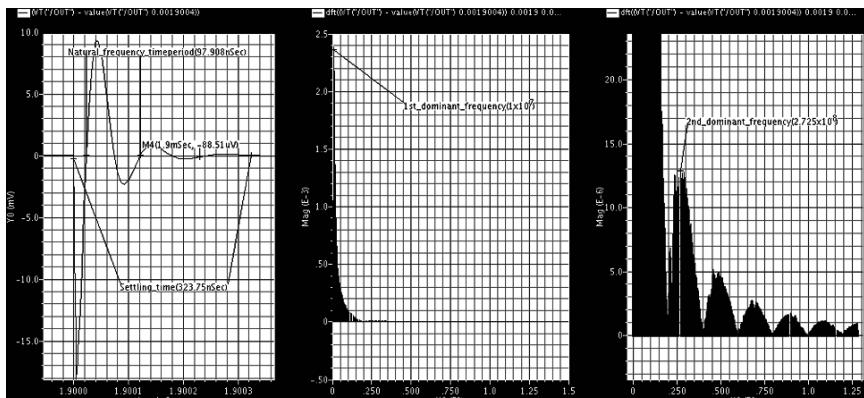
**Fig. 14** Step settling in the two-loop system

phase systems. Extraction of the dumping factor is suitable for stability estimations in the multiloop systems as it does not require breaking a loop.

For the small signal step, the overshoot factor is equivalent to the dumping factor for  $n = 1$ . However, for a large step, overshoot factor helps to discover the conditional stability effects caused by the components nonlinearity, cut-off or saturation.

In the multiloop system transient responses of different loops overlap each other, and step settling may appear as shown in the Fig. 14. Using traditional brute-force approach to the compensation of such system, we would have to extract the transfer function of the full system and then set the poles and zeros with the root stability methods. With an increasing number of loops and uncertainty in the component and load parameters, this approach to compensation becomes prohibitively complicated very soon.

According to structural design methodology, we limit the transfer function of each loop to the second order by design. In the circuits with wide load and environment variations, like LDOs, we can make these first- or second-order loops unconditionally stable (for example, using the approach described in [15]). According to the theorem in [9], the stability in the every loop is not necessary but is a sufficient condition for the overall system stability.



**Fig. 15** Using the Fourier transform for tone detection

Verification of the stability in the nominal case can be done by the step transient simulations, while observing settling processes at the output and key nodes of the each loop in the system.

Statistical CAD verification of the stability with numerous process and temperature variations can be done with the step transient simulations as well. Using the Fourier transform of the step response, the tone frequencies can be extracted (Fig. 15). When tone frequency is known, the consequent dumping factor can be calculated for each of the tones.

Using Texas Instruments ACS tool inside TISpice simulator, this procedure has been automated and employed in the multiple embedded LDO designs.

## 8 Conclusions

The structural design methodology can be the base for break-through in all areas of analog, and is especially efficient in power management and instrumentation IC design. This methodology deserves to be studied by every analog designer. LDOs developed with structural methodology surpass standard designs in each and every parameter, often by the order of magnitude. There hardly exists an excuse to design a standard structure LDO any more.

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