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RESEARCH ARTICLE

Design of a Low-Noise Low Dropout Regulator for CMOS Pixel Sensors

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ABSTRACT A low-noise Low Dropout Regulator (LDO) is designed in a Semiconductor Manufacturing International Corporation (SMIC) 0.18 μm process, aiming at supply of a clean and constant clamping voltage in the operation of Correlated Double Sampling (CDS) for elimination of switching and reset noise in CMOS Pixel Sensors (CPS) applied to high energy physics experiments. In order to decrease noise of the LDO, a noise model of the LDO consisting of blocks, such as a pass transistor, a resistor network, and an error amplifier, is constructed and noise contributions made by these blocks are analyzed in detail. According to results of the noise analysis, the error amplifier is identified as the major noise source. For the purpose of reduction in noise, especially 1/f noise, an error amplifier exploiting a chopper stabilization technique is proposed. Simulation results demonstrate the effectiveness of the proposed method. The Power Spectral Density (PSD) of the LDO's output noise is only 60 nV/$\sqrt{}$Hz at 10 Hz and total integrated noise within the bandwidth is 40 μV.

INDEX TERMS Low noise, low dropout regulator, CMOS pixel sensor, high energy physics experiment.

I. INTRODUCTION

CMOS Pixel Sensors (CPS) are widely used as charged particle tracking devices of high-resolution vertex detectors for high energy physics experiments, taking advantage of their high granularity, low material budget, and tolerance to radiation [1]. To achieve a goal of high-precision tracking, the pixel pitch of CPS becomes smaller and smaller (tens of micrometers), leading to a tiny charge sensing diode and a weak input signal. As a result, low-noise signal-processing circuits integrated in CPS become more demanding [2].

A typical block diagram of CPS and a sketch of signal readout chain in pixels are shown in Fig. 1 and Fig. 2 respectively. In Fig. 2, the tiny charge sensing element (diode) collects electrons induced by minimum ionizing particles and converts them to voltage variations. The variations are magnified by the amplifier (AMP) and then processed by subsequent circuits. To detect the tiny voltage variations exactly, Correlated Double Sampling (CDS) is adopted, resulting in diminution of common-mode noise [3]. Besides, KT/C noise introduced by the CDS operation could be diminished dramatically by an increase in capacitance of C_1 (shown in Fig. 2) on the assumption that the clamping voltage source is ideal. Consequently, the clamping voltage source implemented by a low-noise Low Dropout Regulator (LDO) is demanded urgently, since a bandgap does not meet its requirement because of poor driving capability.

Besides low noise, low dropout voltage, high Power Supply Rejection Ratio (PSRR), good stability, and low load regulation are also required for the LDO design. To eliminate the threshold loss of M1 shown in Fig. 2 and guarantee the power efficiency, the dropout voltage of the LDO is designed to be around one threshold voltage of M1.

The paper is organized as follows. A typical structure and corresponding operation principle of a LDO are introduced briefly in section II. Section III focuses on noise sources contributed by all building blocks and the major noise source is identified. To diminish the noise, chopper stabilization is adopted and the work principle is described in IV. An error amplifier exploiting a chopping technique is proposed, and design of each block of the LDO is described in section V. Simulation results are shown to demonstrate the effective-

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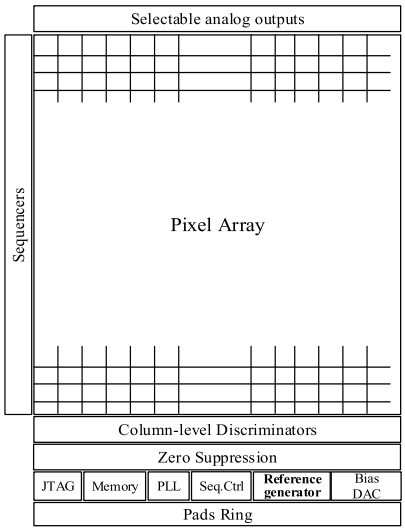

FIGURE 1. Typical block diagram of CMOS pixel sensors.

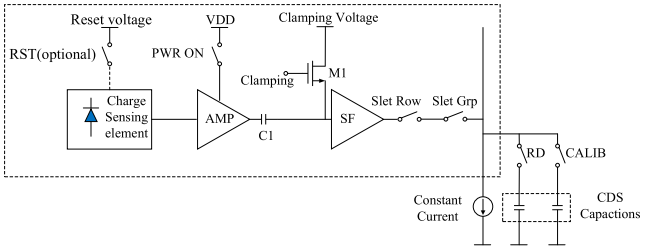

FIGURE 2. Sketch of signal readout chain in pixels.

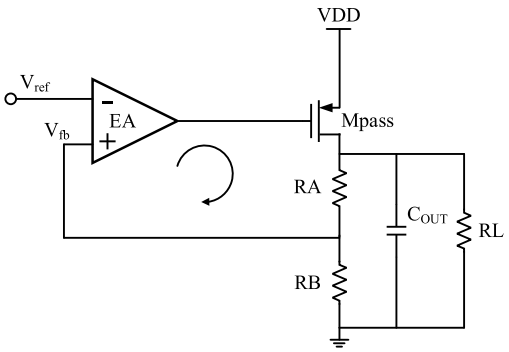

FIGURE 3. Typical structure of a LDO.

ness of design of the low-noise LDO in section VI. Finally, section VII concludes the paper.

II. TYPICAL STRUCTURE AND OPERATING PRINCIPLE OF LDO

A typical structure of a LDO is shown in Fig. 3. It consists of a reference voltage source (Vref), an error amplifier (EA), a feedback resistor network (R_A, R_B), and a pass transistor (Mpass) [4], [5], [6]. Besides, Cout denotes a load capacitor, and R_L represents a load resistor.

The LDO shown in Fig. 3 is capable of outputting a constant voltage V_{OUT} in spite of variations in load currents and supply voltages [7], [8]. For example, when the load current increases suddenly, V_{OUT} decreases at the beginning, resulting in a reduction in the voltage across R_B. Then the EA amplifies the reduction, lowering the gate voltage of Mpass. Consequently, a larger current is induced by Mpass and compensates the load current, maintaining V_{OUT} constant.

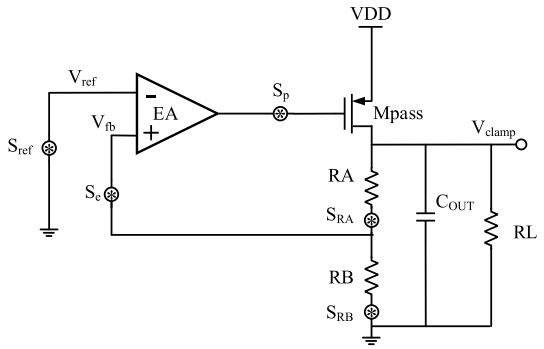

FIGURE 4. Noise in the LDO.

III. NOISE ANALYSIS OF THE LDO

Noise in the LDO illustrated in Fig. 3 consist mainly of output noise of the reference source (S_{ref}), equivalent input noise of the EA (S_e), thermal noise of R_A(S_{RA}) and R_B(S_{RB}) [9], and gate-referred voltage noise of the Mpass (S_p), as shown in Fig. 4. For most applications, Sp could be ignored since the EA is designed with a large gain [10], [11]. Besides, S_{ref} is also out of consideration in the paper because it is typically implemented by a bandgap and could be reduced to a trivial level by careful design. As a result, the Power Spectral Density (PSD) of the LDO output voltage (S_{out}) could be expressed as follows.

$$S_{out} = Se\,(1 + RA/RB)^2 + SRB\,(RA/RB)^2 + SRA \qquad (1)$$

Equation (1) shows that Sout is mainly contributed by the feedback resistors and the error amplifier. In order to effectively decrease the output noise of the LDO, noise generated by the resistors and the error amplifier should be reduced [12]. Smaller resistance values of the feedback resistors lead to better noise performance because that the PSD of a resistor is proportional to its resistance value. However, smaller resistance values also cause larger static power consumption. Consequently, a trade-off between noise and power consumption is required for the design of the feedback resistor network.

According to (1), another effective method for the reduction of the LDO output noise is to decrease the equivalent input noise of the EA, which is typically implemented by an operation amplifier [13]. The equivalent input noise is composed of thermal noise and flicker noise. This paper focuses on the reduction of the flicker noise of the EA since the switch frequency of the load current of the LDO is around 50 kHz, at which flicker noise is much higher than thermal noise [14], especially in submicron CMOS technologies.

In order to decrease the flicker noise of the EA, several techniques are under consideration, including an increase of

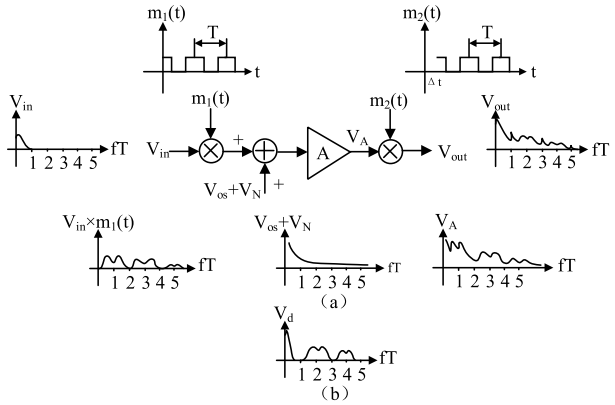

FIGURE 5. Sketch of principle of chopper stabilization.

the device area, autozeroing, and chopper stabilization [15], [16]. Increasing in the device area is not the optimal method because areas of the peripheral circuits should be small to reduce the dead zone in CPS. The technique of autozeroing could diminish the flicker noise at the cost of increase in thermal noise in the bandwidth of the EA, which prevents reduction of the total noise. The chopper stabilization technique could dramatically decrease the flicker noise without raising the thermal noise in the bandwidth of the EA. It should be noted that the chopper frequency should be smaller than the bandwidth of the EA. Consequently, the chopper stabilization technique is adopted in the design of the LDO and its principle of work is presented as follows.

IV. PRINCIPLE OF CHOPPER STABILIZATION

The chopper stabilization technique employs a mixing operation to modulate low frequency noise and offset components of an amplifier to higher frequencies, filtered by a succeeding low-pass filter. A sketch of principle of chopper stabilization is shown in Fig. 5. V_{in} and V_{out} are input voltage signal and output voltage signal respectively; A, V_N and V_{os} represent the gain, the input noise voltage and the offset voltage of the amplifier respectively; V_d is the output volage of the operation amplifier in ideal conditions, whereas $m_1(t)$ and $m_2(t)$ are the modulation signal and the demodulation signal respectively with equal clock period T. However, $m_1(t)$ leads $m_2(t)$ by a time of Δt.

To avoid signal aliasing, the chopping frequency f_{chop}, which equals *1/T*, should higher than twice the cutoff frequency of the input signal. The chopping signal m(t) is typically implemented by a clock signal with a duty cycle of 50%, whose Fourier transform can be expressed by (2).

$$\begin{aligned} \mathrm{m}(t) &= 2\sum_{\mathrm{k}=1}^{\infty} \frac{\sin(\mathrm{k}\pi/2)}{(\mathrm{k}\pi/2)} \cos\left(2\pi f_{chop} kt\right) \\ &= \sum_{\mathrm{k}=1}^{\infty} M_k \cos\left(2\pi f_{chop} kt\right) \\ &\quad \times \left(M_k = (4/k\pi)\sin(\mathrm{k}\pi/2)\right) \end{aligned} \tag{2}$$

The input voltage V_{in} is modulated to frequencies around odd harmonics by the chopping signal $m_1(t)$, yielding $V_{in} \times m_1(t)$ shown in Fig. 5. Subsequently, the modulated signal, together with V_N and V_{OS}, is amplified by the amplifier and then is demodulated to the frequencies around even harmonics of the chopping signal by $m_2(t)$ shown in Fig. 5. The demodulated signal $V_d(t)$ shown in Fig. 5 (b) can be formulated as (3), where k and l are odd numbers.

$$\begin{aligned} V_d(t) = AV_{in}(t) &\sum_{k=1}^{\infty} M_k cos\left(2\pi f_{chop} kt\right) \\ &\times \sum_{l=1}^{\infty} M_l cos\left(2\pi f_{chop} lt\right) \end{aligned} \tag{3}$$

To reduce disturbance, $V_d(t)$ should be filtered further. Assuming that V_N and V_{OS} are demodulated by $m_2(t)$ producing the chopped output signal $V_{cs}(t)$, the bilateral PSD of $V_{cs}(t)$, $S_{cs}(f)$, is given [17] by (4).

$$S_{\mathrm{cs}}(\mathrm{f}) = \left(\frac{2}{\pi}\right)^2 \sum_{\mathrm{n}=-\infty,\mathrm{odd}}^{+\infty} \left(\frac{1}{\mathrm{n}^2} S_N\left(f - \frac{\mathrm{n}}{T}\right)\right) \tag{4}$$

where $S_N(f)$ is the PSD of V_N plus that of V_{os}.

Equation (4) shows that $S_N(f)$ is shifted to odd harmonics of the chopper frequency. It is then filtered by the load capacitor, resulting in $S_N(f)$ composed of only the amplified input signals [18]. Under ideal conditions, V_N and V_{os} could be eliminated by adopting the chopper stabilization technique. Implementation of the chopper stabilization is presented as follows.

V. CIRCUIT IMPLEMENTATION

The paper presents the design of a LDO providing a low-noise clamping reference voltage for correlated double sampling in CPS applied to high-energy physics experiments. Besides the low noise, there are other design constraints placed by the CPS. The first one is the voltage drop. To eliminate the voltage difference between the drain input voltage and the source output voltage of M1 in Fig. 2 and maintain a good energy efficiency of the LDO, the drop voltage of the LDO is set to 0.5 V, which is slightly greater than the threshold voltage of M1. Consequently, the output voltage of the LDO equals 1.3 V since the supply voltage of the LDO is 1.8 V. The second one is the load capacitance. The clamping voltage, which is the output voltage of the LDO, must also be connected to each pixel unit in the CPS. The parasitic capacitance of the on-chip wiring and pixel units increases the load capacitance of the LDO. As the pixel array increases, so does the parasitic capacitance. The total parasitic capacitances are approximately 0.5 nF for the pixel array of 576 rows × 136 columns, and 5 nF for the pixel array of 928 rows × 960 columns, which are extracted by using EDA tools from the layout. Furthermore, the LDO must be stable in the range of varying load capacitances (0.5 nF - 5 nF) to be used in flexible pixel arrays. The third one is load current. Because of the absence of a direct DC path between the clamping voltage and the circuit ground (as shown in Fig. 2), there is no need for the LDO to supply a static load current. However, when the

TABLE 1. LDO design specifications.

Parameter	Requirement
noise (v/sqrt(Hz)@10Hz)	< 100 n
drop voltage (V)	0.5
output voltage (V)	1.3
load capacitance (nF)	0.5 ~ 5
load current (mA)	≤ 1
static current (μA)	≤ 200

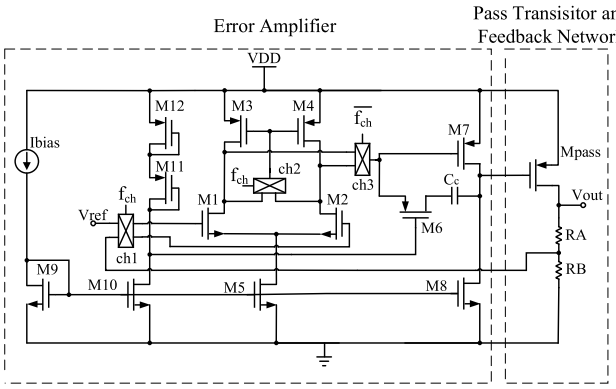

FIGURE 6. Proposed LDO with chopping technology.

pixel array of the CPS is read out row by row (called rolling shutter mode), a dynamic load current of several hundred microamperes should be supplied by the LDO. Finally, the regulator should consume a static current of no more than 200 μA to lessen the burden to the cooling system, whereas, the silicon area occupied by the LDO should be minimized to ensure a large number of pixels manufactured on the chip. Table 1 summarizes main design specifications.

To meet these specifications, a low-noise LDO adopting chopping technology is proposed as shown in Fig. 6. The LDO consists of an error amplifier (two-stage operational amplifier with Miller compensation), three chopper switches (ch1, ch2, ch3), a feedback network and a pass transistor Mpass.

A. ERROR AMPLIFIER DESIGN

The error amplifier of the LDO shown in Fig. 6, is implemented by a two-stage operational amplifier with M1∼M5 forming the first-stage. To achieve a high gain and minimize thermal noise, M1 and M2, which serve as input transistor, require a significant transconductance. In addition, to reduce flicker noise, the area of the input transistors should be large enough. Therefore, long-channel transistors are used to meet noise and gain specifications. Although PMOS transistors have lower flicker noise than NMOS transistors, its transconductance is small. Consequently, NMOS transistors are adopted for the implementation of M1 and M2 to achieve a higher gain.

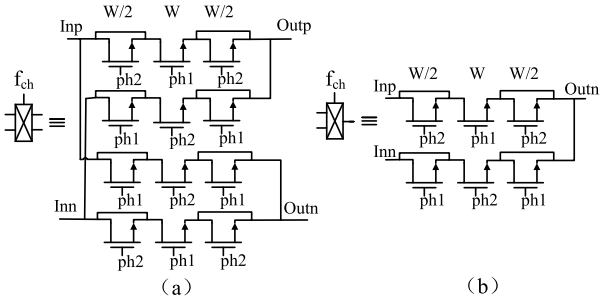

FIGURE 7. (a) Chopper switch with differential input and differential output, (b) chopper switch with differential input and single-ended output.

The second stage of the operational amplifier consists of a common-source amplifier and RC Miller compensation. The common source amplifier, composed of M7 and M8, provides a high output swing for the operational amplifier. M6 operates in the linear region and functions as a linear resistor. It makes a frequency compensation, together with the Miller capacitance Cc, to guarantee that the operational amplifier has an adequate phase margin [5], [19], [20].

B. CHOPPER SWITCH DESIGN

As shown in Fig. 6, three choppers (ch1-ch3) are adopted to implement chopper stabilization, where ch2 and ch3 are controlled by opposite signals. The circuit implementation of ch1 is shown in Fig. 7 (a), whereas that of ch2 or ch3 is shown in Fig. 7 (b). ch1 is used to modulate the input signal, while ch2 and ch3 are employed to demodulate the signal. The chopping frequency should be chosen appropriately to minimize the flicker noise.

Total output noise of the operational amplifier is expressed by (4). Let the cutoff frequency of the operational amplifier be f_c, which usually corresponds to the gain-band-width (GBW) product of the amplifier. Let S_0 be the white noise of the amplifier, and then $S_{cs}(f)$ contributed by the white noise can be approximately calculated by

$$\begin{aligned} S_{CS-white}(f) &\cong S_{CS-white}(f=0) \\ &= S_0 \times \left(1 - \frac{\tanh(\pi f_c T/2)}{\pi f_c T/2}\right) \end{aligned} \tag{5}$$

When f_{chop} is less than twice the input signal frequency f_{in}, chopping modulation will cause aliasing of the input signal. However, according to (5), when $f_{chop} \ll f_c$, the white noise PSD of the output modulated by the chopper will be slightly smaller than that of the original operational amplifier. It can be given by

$$S_{\text{CS-white}}(f) \approx S_0(|f| \le 0.5 f_{chop},\ f_c \gg f_{chop}) \tag{6}$$

When $f_c \gg f_{chop}$, PSD of the flicker noise can be approximately expressed by

$$S_{\text{N-}1/f}(f) = S_0 \times (f_{\text{corner}}/|f|) = S_0(f_{\text{corner}}/|f|) \tag{7}$$

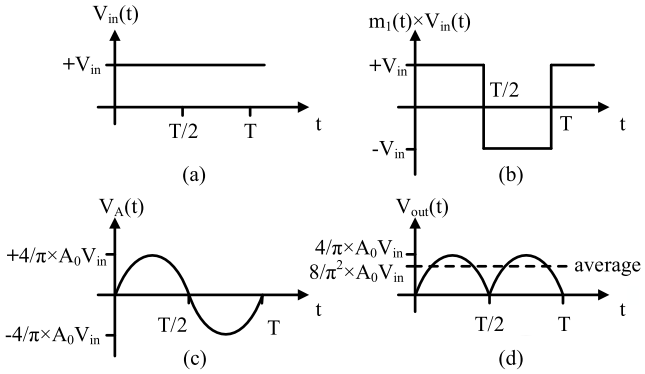

FIGURE 8. (a) DC input, (b) modulated input, (c) output signal of the amplifier with a limited bandwidth, and (d) demodulated output signal.

where f_{corner} is the corner frequency of the amplifier. Substituting (7) for $S_N(f)$ in (4), the low frequency noise is modulated to high frequencies, which are odd harmonics of the chopper frequency, making the flicker noise disappear from the baseband. Then the PSD can be expressed as [17]

$$\begin{aligned} S_{cs}(f) &= S_{\text{CS-white}}(f) + S_{\text{CS-1/}f}(f) \\ &= S_0[1 + f_{\text{corner}}T/(|f|T)] \\ &\approx S_0(1 + 0.8525 f_{\text{corner}}T) \end{aligned} \tag{8}$$

From the above analysis, it can be seen that when $2f_{in} \leq f_{chop} < f_c$, the flicker noise could be reduced dramatically.

Besides noise, degradation of a DC gain of the amplifier should also be under consideration when we determine the chopping frequency. In ideal conditions, an amplifier has an infinite bandwidth. Let the A_0 be the amplifier gain and V_{in} be the DC input as shown in Fig. 8 (a). V_{in} is modulated shown in Fig. 8 (b) and amplified to a square wave with an amplitude of A_0V_{in}. And after demodulation, it returns to a dc signal with a value of A_0V_{in}. However, in practical circuits, the amplifier's bandwidth is limited. Assuming that the amplifier bandwidth is higher than twice the chopping frequency, the amplifier outputs a sinewave signal $V_A(t)$ with an amplitude of $(4/\pi)(A_0V_{in})$ as shown in Fig. 8 (c). After demodulation, it is transformed to a signal shown in Fig. 8 (d), whose dc value V_{avg} can be expressed as (9).

$$V_{avg} = (2/\pi)(4A_0V_{in}/\pi) \tag{9}$$

It can be seen that the dc gain has decreased by 20%. Therefore, when choosing the frequency of f_{chop}, one should make a trade-off between high gain and low noise. In the paper, the chopping frequency is designed to be half of the bandwidth. As the load capacitance varies from 0.5 nF to 10 nF, the position of the secondary pole within the loop changes, resulting in a loop bandwidth variation from 500 kHz to 10 MHz. Consequently, the chopping frequency should be adjusted to match the changing bandwidth. After chopper modulation, a low-pass filter (LPF) is employed to further filter out the high-frequency noise [21], [22], [23]. The LPF is constructed by RC network. In addition, the capacitor in the RC network is also employed to form Miller compensation.

Besides the chopping frequency, MOS switches in the chopper should be designed carefully. First, to minimize the voltage drop caused by the on-resistance, aspect ratios of the MOS switches should be large enough. When the MOS switch turns on, the on-resistance can be expressed as (10).

$$R_{on} = 1/[\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})] \tag{10}$$

To achieve an on-resistance of less than 100 Ω, the aspect ratio of MOS switches in ch1 is designed to be 25, and that of dummy switches is 12.5. However, the aspect ratio of MOS switches in ch2 and ch3 is designed to be 50 in order to further lower the impact on subsequent circuits. Secondly, dummy transistors are added to chopper switches as shown in Fig. 7 (a) and (b), in order to reduce non-ideal effects introduced by MOS switches, such as clock feedthrough and charge injection [22]. The dummy transistor is implemented by a source-drain connected NMOS transistor, and is driven by a clock complementary to the clock driving its serial MOS switch. When the MOS switch turns off, its channel charge will be injected into the dummy transistor on both sides to compensate the channel charge of the dummy transistor, reducing effects of clock feedthrough and charge injection.

C. PASS TRANSISTOR AND FEEDBACK RESISTOR NETWORK DESIGN

The power transistor of the LDO is implemented by a PMOS transistor, which makes the output stage to be a common-source stage and provides an additional gain to the LDO loop, improving the PSRR of the LDO. Due to a small load current requirement of the LDO, which is a few hundred microamperes, a small-sized PMOS is used as the power transistor.

The feedback network includes a series resistor network that divides the LDO's output voltage to obtain a demanded feedback voltage used as an input voltage of the operational amplifier. To determine values of R_A and R_B, noise and power dissipation should be taken into account.

To reduce output noise, small-value feedback resistors should be adopted at the expense of higher power dissipation. Equation (11) provides the feedback resistors' ratio based on the relationship between the LDO's output voltage and the reference voltage, which is equal to 1.2 V.

$$V_{out} = V_{REF}(1 + R_A/R_B) \tag{11}$$

In order to determine the size of the feedback resistor, the quiescent current flowing through the feedback resistor is also considered.

$$I_q = V_{out}/(R_A + R_B) \tag{12}$$

In the design, the output voltage of the LDO is 1.3 V, and the current allocated to flow through the feedback resistor is about 84 μA. Consequently, R_A is 1.21 KΩ and R_B is 14.3 KΩ, according to (11) and (12).

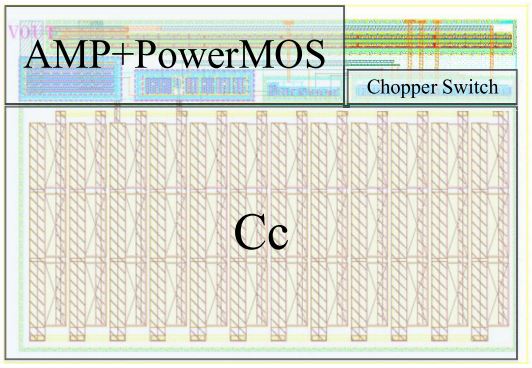

FIGURE 9. Layout of the proposed LDO.

TABLE 2. Integrated noise within GBW with and without use of chopping technique.

CL/GBW	f_{chop}	Integrated noise within GBW (chop off/chop on)	Reduction
1 nF / ~ 7 M	3.5 M	71 μV_{rms} / 55 μV_{rms}	~ 23%
5 nF / ~ 2 M	1 M	55 μV_{rms} / 40 μV_{rms}	~ 27%
10 nF / ~ 1 M	500 k	45 μV_{rms} / 31 μV_{rms}	~ 31%

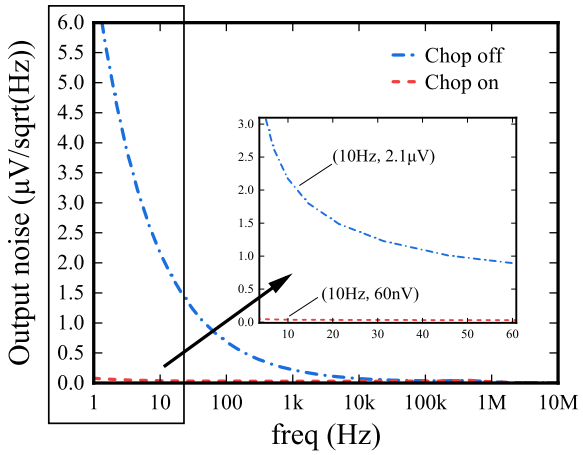

FIGURE 10. Comparison of post-simulated output noise of the LDO with and without use of chopping technique.

VI. SIMULATION RESULTS

The proposed LDO is designed in a 0.18 μm CMOS process. To evaluate its performance, such as output noise, PSRR, stability, load regulation, line regulation and transient response, simulations are performed after extracting the parasitic R, C and CC of all nodes. The LDO layout has a horizontal length of 180 μm and a vertical width of 120 μm, as shown in Fig. 9.

A. OUTPUT NOISE

As it states, f_{chop} changes with GBW. Under the condition that the load capacitance CL is 5 nF and the load current is 1 mA, setting a GBW of approximately 2 MHz, f_{chop} is designed to be 1 MHz. The resulting simulated output noise of the LDO with and without use of chopping technique is shown in Fig. 10. The PSD at 10 Hz of the LDO with and without use of chopping technique is 2.1 μV/sqrt(Hz) and 60 nV/sqrt(Hz) respectively, while the integrated noise within the bandwidth is 55 μV and 40 μV respectively. 27% of integrated noise is reduced by adoption of chopping technique, which proves

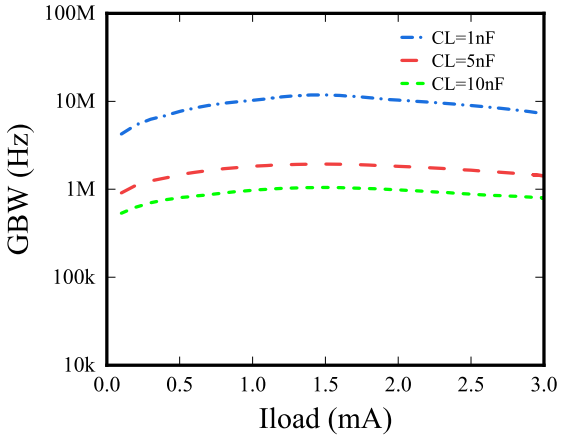

FIGURE 11. Variations of GBW with load current and load capacitances.

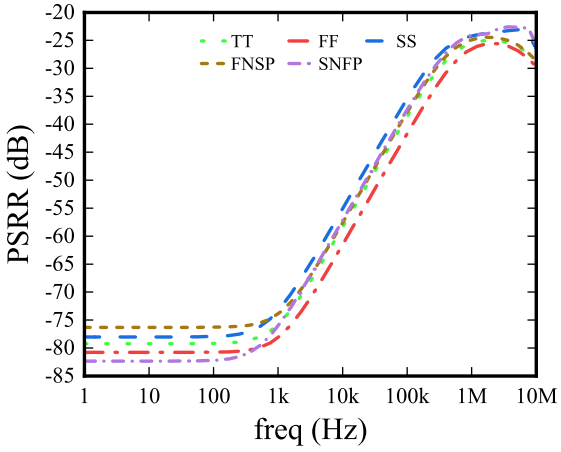

FIGURE 12. PSRR obtained from post-simulation at all corners with a full load current and a load capacitor of 0.5 nF.

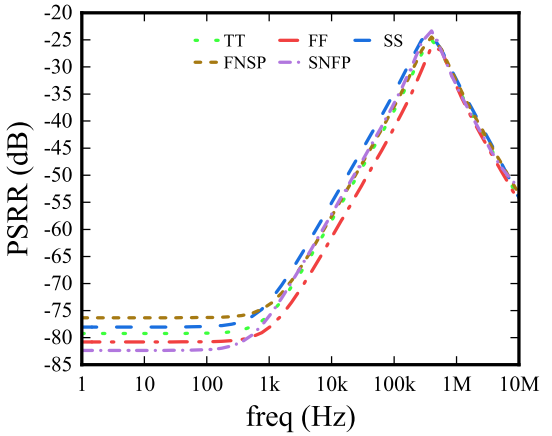

FIGURE 13. PSRR obtained from post-simulation at all corners with a full load current and a load capacitor of 10 nF.

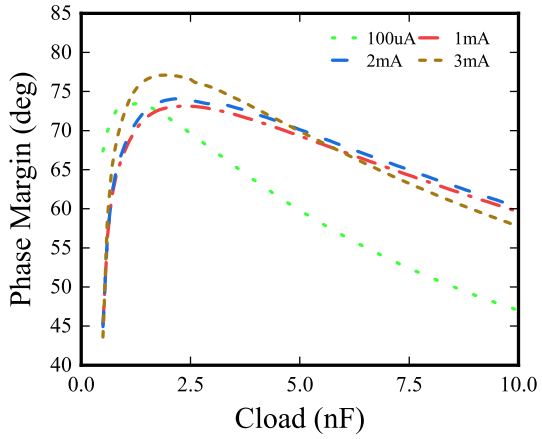

FIGURE 14. Phase margin at various load capacitance and load currents.

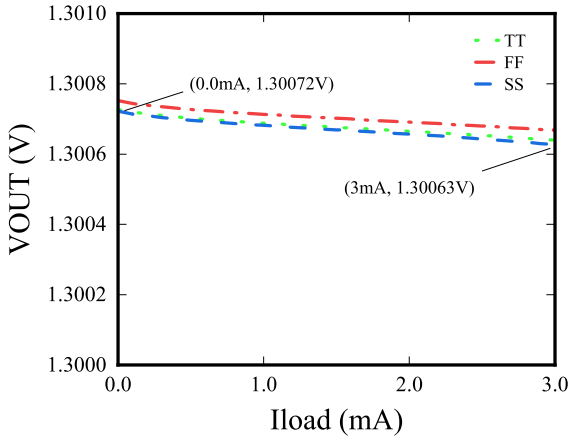

FIGURE 15. Load regulation of the designed LDO through post-simulation.

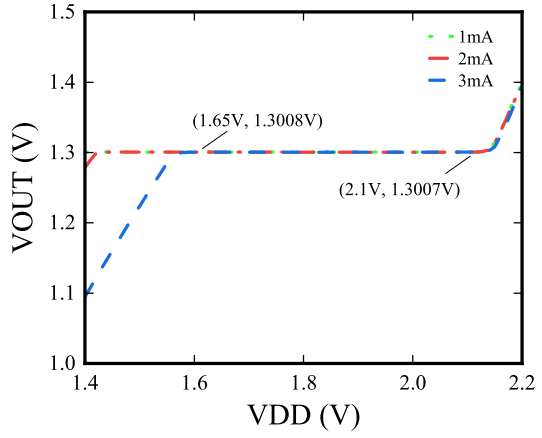

FIGURE 16. Line regulation of the designed LDO through post-simulation.

the feasibility of employing chopping technique to reduce LDO output noise, especially the flicker noise. Fig. 11 depicts the curve of GBW with load current and load capacitances. Table 2 summarizes the integrated noise within GBW with and without use of chopping technique at several typical values of GBW.

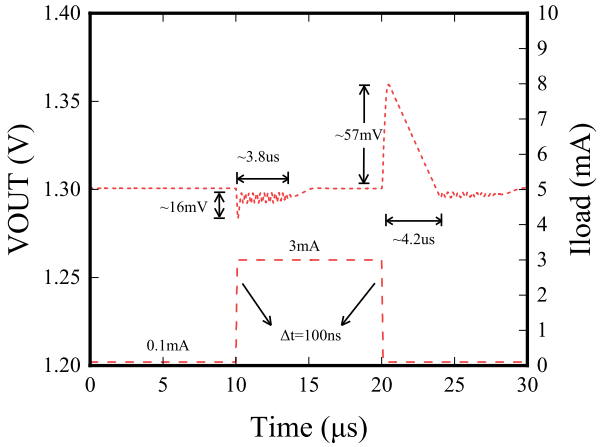

FIGURE 17. Pre-simulation results of the transient response with a load capacitor of 10 nF.

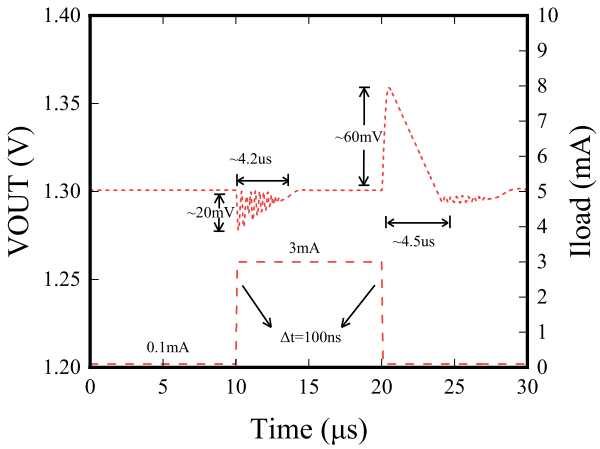

FIGURE 18. Post-simulation results of the transient response with a load capacitor of 10 nF.

B. PSRR

Simulated PSRR of the LDO at all process corners with full load current and load capacitors of 0.5 nF and 10 nF is depicted in Fig. 12 and Fig. 13 respectively. According to the simulation results, the minimum PSRR achieved is −23 dB. Furthermore, PSRR is improved when the load capacitance increases. That hints that a higher PSRR can be achieved for the LDO with larger load capacitors, corresponding to bigger pixel arrays.

C. STABILITY

Stability simulations are performed to verify the stability of the LDO at various load capacitance and load currents. Fig. 14 shows simulated phase margin. It is evident that the phase margin remains above 43° with various load currents as the load capacitance increases from 0.5 nF to 5 nF, and the phase margin still maintains above 46° at 10 nF. This indicates that the LDO achieves excellent stability at various conditions.

D. LOAD REGULATION AND LINE REGULATION

To obtain load regulation and line regulation of the LDO, simulations of output voltages versus load currents, power supple

TABLE 3. Comparison of key specifications among LDOs.

Parameters	This work	[3]	[4]	[9]	[10]
Technology (nm)	180	28	180	250	40
Input voltage (V)	1.8	1.8	1.4	3.5	3.3
Output voltage (V)	1.3	0.9	1.2	1-3.3	1.3-2.6
Quiescent current (μA)	170	/	36	40	30
Output noise [nV/sqrt(Hz)]	60 @10Hz	50 @10k	800 @10Hz	130 @100Hz	2950 @1Hz
Integrated output noise (μV_{rms})	17.5 10 ~ 100k	18.95 10 ~ 100k	/	14.8 10 ~ 100k	7.46 1 ~ 100
Line regulation	0.15%	/	/	/	0.3%
Load regulation	0.023%	8.4%	/	0.38%	1.28%
PSRR (dB)	-58 @10k	-44 @10k	/	-50 @10k	-53.8 @10k
Undershoot (mV)	20	/	5	/	60
Overshoot (mV)	60	/	/	/	320

voltages were performed. The resulting curve of output voltages, obtained by scanning load currents from 0 to 3 mA at a fixed input voltage of 1.8 V, is shown in Fig. 15. As the load current increases, the output voltage of the LDO decreases gradually. The load regulation of the LDO is calculated as 0.023% according to (13). The resulting curve of output voltages for different loads as the supply voltage increases, is shown in Fig. 16. As the supply voltage increases from 1.6 V to 2.1 V, the output voltage of the LDO is stable. The line regulation of the LDO is calculated as 0.15% according to (14).

$$LoadRegulation = \frac{\Delta V_{out}}{V_{out-norm}\Delta I_{load}} \times 100\% \quad (13)$$

$$LineRegulation = \frac{\Delta V_{out}}{V_{outnorm}\Delta V_{in}} \times 100\% \quad (14)$$

E. TRANSIENT RESPONSE

Transient response simulations were performed to verify the ability of the LDO when a load current is switching. Fig. 17 and Fig. 18 show the pre-simulation and post-simulation of the transient response respectively for voltage recovery to 99.7% of the final value. The overshoot and undershoot disappear after 4.5 μs through post-simulation. It can be seen that performance parameters through the post-simulation, such as the overshoot, undershoot and recovery time, are slightly worse than those through the pre-simulation due to a negative impact of parasitic capacitors and resistors.

Table 3 summarizes the post-simulation performance of the proposed LDO and compares it with other LDOs. The proposed LDO exhibits a lowest output noise of 60 nV/$\sqrt{}$Hz at 10 Hz, exceptional line regulation and load regulation of 0.15% and 0.025% respectively, and PSRR of −58 dB at 10 kHz, which are better than those of other LDOs at the expense of a higher quiescent current.

VII. CONCLUSION

In the paper, a low-noise LDO is proposed to provide a low-noise, clamping reference voltage used during CDS operation of CPS dedicated to the application of high-energy physics experiments. The proposed LDO adopts chopper technique for reduction of flicker noise and total output noise. According to the simulation results, the PSD of the LDO's output noise is as low as 60 nV/$\sqrt{}$Hz at 10 Hz and total integrated noise within the bandwidth is 40 μV with a noise reduction of 28%. In addition, the proposed LDO can not only be applied in CPS but also in high-precision electronics, such as micro-sensors that raise stringent requirements of low flicker noise.

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