CMOS Fast Transient Low-Dropout Regulator

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Abstract— **In this paper a fast transient response CFA-based low-dropout regulator (LDO) is introduced. The circuit is stable for 0-100mA output load current and a 1µF output capacitor without any internal compensation. The CFA consists of a voltage follower with output local current-current feedback based on a level-shifted flipped voltage follower (LSFVF) which is instrumental to achieve high regulation and fast transient response. The inverting output buffer stage of the CFA together with current-mirror-based driving of the pass transistor results in high PSRR. Full transistor-level simulation results for an AMS 0.35µm CMOS process design reveal that the proposed LDO dissipates 58µA quiescent current at no-load condition and in worst case conditions has a current efficiency of 99.8%. For a 1µF output capacitor, the maximum output voltage variation to a 0-100mA load transient with rise and fall time of 10 and 100ns is only 2.5mV, and the PSRR is smaller than -58dB over the entire load current range.**

Keywords-fast transient; level-shifted flipped voltage follower; low-dropout

I. INTRODUCTION

Power management circuits are very essential in battery-operated electronic systems like cellular phones and PDAs in order to reduce the standby power consumption and increase the battery life. Low-dropout regulators (LDOs) are widely used alone in many integrated power management circuits but also used as post regulators of switching converters, as they can provide wideband regulated low noise supply voltage for noise-sensitive analog and RF loads. A conventional LDO consists of an error amplifier for detecting the error between the reference and output voltage, a pass transistor controlled by the error amplifier for delivering current to the load, a feedback network, and an output capacitor. Several performance indexes should be carried out when designing an LDO, such as closed-loop stability for a wide range of loads, static regulation in front of input voltage and load variations, and fast rejection of abrupt transient load variations [1, 2]. Different techniques have been proposed up to now for stability, such as pole-zero cancellation method [2] and pole-splitting schemes [3-5]. An internal zero generated through a voltage-controlled current source (VCCS) is used in [6] for frequency response compensation and enhanced stability. Dual-loop feedback in the form of using a current buffer approach in the compensation network is another way to improve transient response and stability, which was proposed in [7-10]. LDOs based on the flipped voltage follower (FVF) were introduced in [11, 12]. Current-mode LDOs have been proposed in [13, 14], in which the pass transistor operates like a voltage-controlled current source. With this method, the LDO dropout is minimized and high power supply ripple rejection (PSRR) can be achieved.

In previously reported LDOs, voltage-mode operational amplifiers are used as error amplifiers, thereby limiting the regulator performance due to their fixed gain-bandwidth product and limited slew rate. These limitations affect the LDO stability and transient response. Complementarily, a strategic design target is to avoid on-chip compensating capacitors, which occupy a large chip area thus achieving the required stability using only external off-chip load capacitance [3]. With regard to the above considerations, in this paper a CMOS fast transient LDO regulator based on a current feedback amplifier (CFA) exhibiting fast transient stable performance is presented. Section II describes the proposed LDO architecture. In section III, the CFA design criteria of the LDO are presented. Finally, transistor-level characterization and conclusions are given in sections IV and V, respectively.

II. PROPOSED LDO ARCHITECTURE

The block diagram of the proposed LDO is shown in Fig. 1. The control mechanism of the pass transistor in the LDO is accomplished by a CFA which is based on the conjunction of an open-loop voltage follower with current copying capability and an inverting output buffer. The output signal is transferred to the inverting input of the CFA (X node, which has very low impedance), through the feedback network, and is compared with the reference voltage. This comparison result is amplified through the transimpedance gain of the CFA thereby controlling the gate of the pass transistor. Very low impedance at the inverting input of the CFA is the key to achieve high regulation and fast transient response. In addition, if the slew rate at the gate of the pass transistor is much slower than the gain-bandwidth product, transient voltage spikes appear at the output voltage node during fast load transient. So, due to the fact that CFAs have excellent performance in terms of bandwidth and slew rate, this issue can be eliminated in the proposed LDO and fast transient response with minimum slew rate limiting can be achieved.

The transistor level schematic of the proposed LDO is shown in Fig. 2. The circuit is composed of a CFA (a class AB voltage follower, M_1-M_{12}, plus an inverting output buffer, M_{13}, M_{14}), a pass transistor M_P, and a feedback network R_1 and R_2. In order to achieve high input impedance, the

Partial funding by projects TEC2007-67988-C02-01, TEC2010-15765, and RUE CSD2009-00046 (Consolider-Ingenio 2010), from the Spanish Ministry of Science and Innovation.

reference voltage V_{ref} is fed to the circuit through a simple unity-gain amplifier, which is not shown in Fig. 2. Also, this ensures that there is no DC current drained from the reference voltage. Since the bias conditions and sizes of transistor pairs M_1-M_3 and M_2-M_4 are equal, it is derived that $V_{SG1}=V_{SG3}$, $V_{GS2}=V_{GS4}$ and hence the generated reference voltage through the unity-gain amplifier appears at the output node. The mechanism of voltage regulation in the event of a load current transient is discussed in the following. In case that the load current increases, the voltage at the output capacitor drops. Thus, the source terminal voltage of M_3 and M_4, and hence their drain terminal voltage will be decreased, this voltage reduction being transferred to the gate voltage of M_7 and M_8 through M_5 and M_6, respectively. This voltage reduction instantaneously increases the current through transistors (M_7, M_9, M_{11}) and decreases the current through (M_8, M_{10}, M_{12}). As a result, the gate voltage of M_{13} increases, which causes the gate voltage of M_P to decrease so that more drain current is sourced to the load as well as to the output capacitor. Therefore, the output voltage will be increased. An analogous mechanism occurs when the load current decreases.

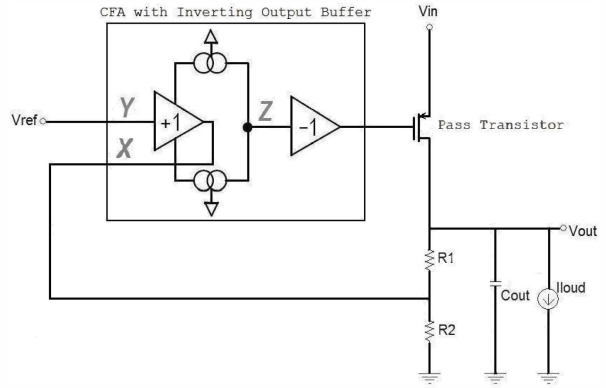


Figure 1. Proposed LDO architecture.

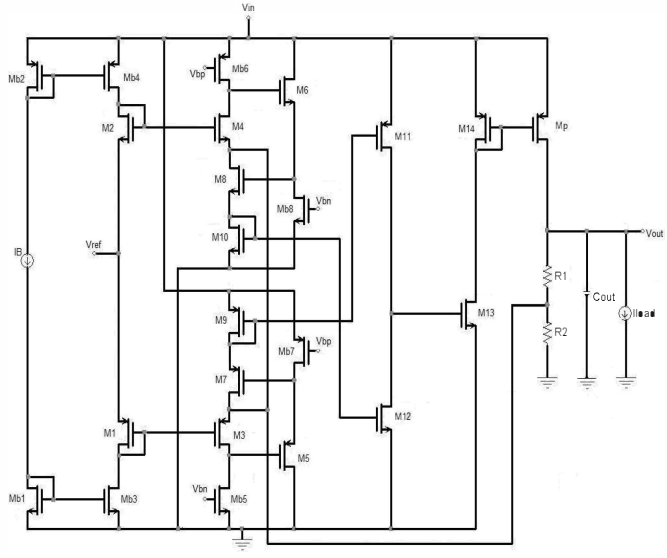


Figure 2. Schematic of the proposed LDO.

III. Design Considerations

The CFA which is used in the proposed LDO consists of an input buffer with current copying capability. Conventional buffers in CMOS processes have output impedances around $1/g_m$, which is in the range of kilo ohms. In this structure, a pre-compensated level shifter flipped voltage follower (LSFVF) with local current-current feedback is used as an input voltage buffer with current copying capability aiming to obtain very low output impedance in the range of ohms, and achieving high regulation and fast transient response. Because of the use of current-current feedback, the output impedance of the LSFVF formed by transistors (M_3, M_5, M_7) and (M_4, M_6, M_8) is given by

$$R_{o,LSFVF}=\frac{1}{g_{m3}g_{m7}r_{ds3}}\|\frac{1}{g_{m4}g_{m8}r_{ds4}} \quad (1)$$

where g_{mi} and r_{dsi} are the transconductance and output impedance of transistor M_i, respectively. The AC output impedance of the input voltage buffer is under 32 ohms, which is a very low value for a MOS technology. Regulation and transient response of the LDO is proportional to its loop-gain, and so by increasing the loop-gain, high regulation and fast transient response can be achieved. The main advantage of using a LSFVF is an increase of the loop-gain ($A\beta$) of the CFA-based LDO, where A is the transimpedance gain of the CFA and β is the feedback factor, which is equal to the transconductance at the inverting input of the CFA (X node). By using local feedback, the feedback factor β will be increased from g_{mi} to $g_{mi}g_{mj}r_{dsi}$, causing an increase in the loop-gain and hence an improvement of the regulation and transient response without stability degradation.

Transistors M_{13} and M_{14} implement the inverting output buffer of the CFA used to generate the negative feedback loop. In addition, transistor M_{14} with pass transistor M_P forms a current-mode control for the gate of pass transistor and so M_P works as a voltage-controlled current source, operating in saturation region. Therefore, its output impedance (r_{dsp}) is high, which is key to obtain high PSRR. In typical LDOs, the power supply ripple to output transfer function is approximated by [15]

$$\frac{\partial V_{out}}{\partial V_{dd}}=[\frac{1-A_p}{A\beta}+\frac{1}{g_{mp}r_{dsp}}\frac{1}{A\beta}] \quad (2)$$

where A_p is the gain from the power supply V_{dd} (V_{in} in Fig. 2) to the gate of the pass transistor, A is the gain from V_{ref} to the gate of pass transistor, g_{mp} and r_{dsp} are the transconductance and the output impedance of the pass transistor, and β is the feedback factor. As it can be seen, one way to improve PSRR is to increase the gain of the CFA. An alternative approach is to design the circuit such that A_p is close to 1. This means that the gate voltage of the pass transistor M_P should be close to the supply voltage and track

the source terminal voltage of M_P, which is connected to the supply voltage. In this design, transistors M_{13} and M_{14} form a subtractor stage. This stage feeds the supply noise directly into the feedback loop and modulates the gate of M_P with respect to its source terminal. Since the output impedance of transistor M_{13}, r_{ds13}, is higher than the diode-connected transistor M_{14}, $1/g_{m14}$, the gate terminal voltage of M_P follows its source terminal. So, the drain current variation of the pass transistor due to the supply voltage noise will be reduced and the output node will be less sensitive to the supply noise.

IV. CIRCUIT CHARACTERIZATION

The proposed LDO topology has been designed and characterized in Cadence in an AMS 0.35µm CMOS process. It does not require any compensation capacitor and is stabilized by an output capacitor in the range of 600nF to 1µF. The LDO is designed to source a nominal output current between 0-100mA and consumes a small quiescent current of 58µA under no-load and 200 µA under full-load condition, which corresponds to a worst case current efficiency of 99.8%. The measured load and line regulations are 22µV/mA and 11.9mV/V, respectively. The power supply ripple to output (PSR) of the LDO and its open-loop AC response with a 1µF output capacitor are shown in Figs. 3 and 4, respectively. The measured PSR is smaller than -58dB over the entire load current range.

Load transient response of the designed LDO with a 1µF output capacitor to the 0-100mA load transient with rise and fall time of 10 and 100ns is shown in Fig. 5. It is apparent that the LDO can react to fast load current changes and is stable over the entire load current with a maximum output voltage variation of only 2.5mV.

Table I provides a performance comparison between the proposed LDO and recently published designs. The figure of merit (FOM= $T_R \times I_q / I_{load,Max}$) used in [11] is adopted here to compare the transient response of different LDOs by evaluating the effect of the quiescent current I_q to the load transient response time (T_R). The T_R of the LDO is given by $T_R = C_{out} \Delta V_{out} / I_{load,Max}$, where ΔV_{out} is the maximum transient output voltage variation.

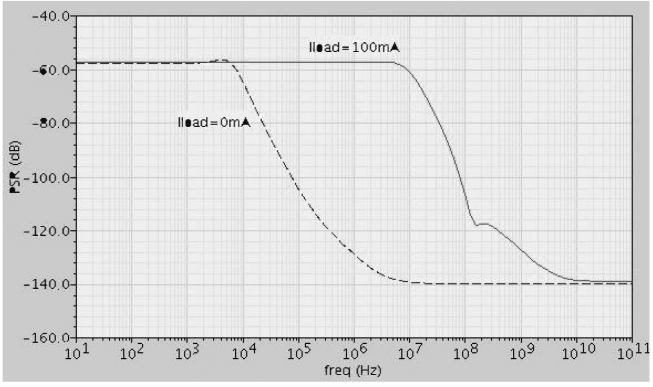


Figure 3. PSR of the proposed LDO with 1µF output capacitor.

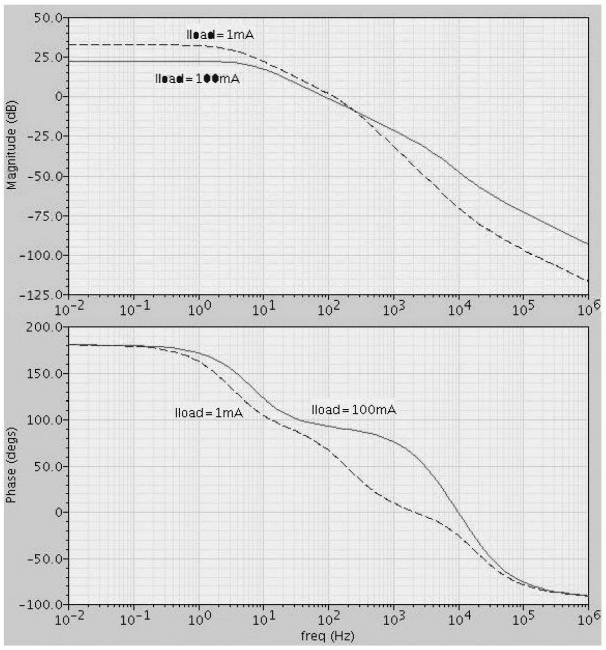
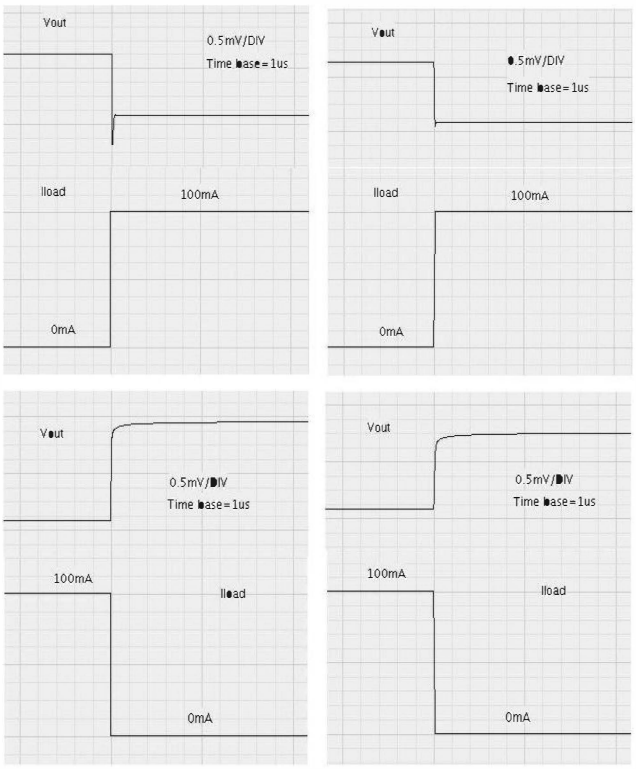


Figure 4. Open-loop AC response with 1µF output capacitor.



(a) (b)

Figure 5. Load transient response with 1µF output capacitor (a) load transient with 10ns rise and fall time (b) load transient with 100ns rise and fall time.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH RECENTLY PUBLISHED WORKS

Parameter	Unit	[6]	[7]	[11]	[12]	[14]	[16]	**This Work**
Technology	µm	0.5	0.35	0.09	0.35	0.35	0.25	**0.35**
$I_{load,Max}$	mA	160	200	100	50	50	50	**100**
V_{in}	V	3.3	2-5.5	1.2	1.2-1.5	1.05-3.5	2-2.5	**3-5**
V_{out}	V	2.8	1.8	0.9	1	0.9	1.5-1.97	**2.8**
Output Capacitor	µF	2.2	1	0.0006	1	1	0.05	**1**
I_{q}	µA	25	20-320	6000	95	4.04-164	100	**58-200**
PSRR	dB	N.A.	>45 (0Hz-20KHz)	N.A.	N.A.	>50 (0Hz-1MHz)	43 @30KHz	**>58**
ΔV_{out}	mV	200	54	90	30	6.6	15	**2.5**
T_R	µs	2.75	0.27	0.00054	0.6	0.132	0.03	**0.025**
FOM	ns	0.43	0.027	0.032	1.14	0.0106	0.06	**0.0145**

A lower FOM implies a better transient response achieved by the LDO. By using a 1µF output capacitor in the proposed LDO, the maximum output voltage variation is 2.5mV and T_R is equal to 0.025µs. Hence, as it can be observed in table I, the FOM of the proposed LDO is very comparable to the design in [14] and smaller than other reported LDOs.

V. CONCLUSION

A current-steering fast transient response CFA-based LDO is presented. The circuit is stable for 0-100mA output load and a 1µF output capacitor without any internal compensation capacitor. The CFA consists of an open-loop voltage follower with output local current-current feedback based on a LSFVF that is the key to achieve good regulation and fast transient response. The inverting output buffer stage of the CFA together with a current-mirror-based driving of the pass transistor results in high PSRR. Simulation results for an AMS 0.35µm CMOS process design reveal that the proposed LDO dissipates 58µA quiescent current at no-load condition and in the worst case has a current efficiency of 99.8%. With a 1µF output capacitor, the maximum output voltage variation to the 0-100mA load transient with rise and fall time of 10 and 100ns is only 2.5mV and the PSRR is smaller than -58dB for all frequencies and over the entire load current range.

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