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Stress Relaxed Multiple Output High Voltage Level Shifter

Vikas Rana, and Rohan Sinha

Abstract—**In this brief, a new positive high voltage level shifter is presented for voltage level shifting over a wide supply range. The proposed level shifter can tolerate voltages up to three times the safe operating limit of the individual MOS transistors. Limitations of conventional high voltage level shifter such as floating nodes and threshold voltage dependency are eliminated in order to guarantee multiple conversion ranges with proper driving capability. The circuit is realized in 110nm triple well HVCMOS technology to convert input signals of 1.8V to output signals of voltages ranging from 4.5V-13.5V. Post layout simulation shows that the proposed level shifter has a static power dissipation of 0.37 nW, and a switching delay of (2.5-8) ns for the different outputs of the level shifter. The total energy per transition is measured as 35.12 pJ for a 10 MHz input pulse with almost equal rise and fall delays.**

***Index Terms*—High voltage complementary metal oxide semiconductor (HVCMOS), Electrically erasable programmable read only memory (EEPROM), Electro static discharge (ESD), Intellectual property (IP), Level shifter (LS), Embedded nonvolatile memory (eNVM)**

I. Introduction

RECENTLY, the growing market for internet of things has pushed the requirement of embedded nonvolatile memories esp. EEPROMs where the memory requirement is very low which are typically up to 10kb [1], [2]. Some notable applications are IP security, radio frequency identification, analog trimming, circuit calibration and ESD protection [1]-[4]. Traditionally, EEPROM cell requires high voltages for performing memory write and erase operations [5], [6] where the signals coming from digital controller or microprocessor are standard low voltage signals and circuits near the memory core are operating at high voltages as depicted in fig.1.

Level shifter (LS) is a circuit which converts the signal level from one voltage to another, thus helping in the interaction of the circuits operating at different supply voltages. There exist various challenges in the design of LS which converts signals from low voltage to high voltage whereas, CMOS inverters are usually adequate to shift a signal level from a positive high voltage to a positive low voltage [7]. Additionally, when dealing with multiple supply systems, the complexity increases when we target to decrease the cost of level conversion between different voltage domains without hampering the robustness and reliability of the design [8].

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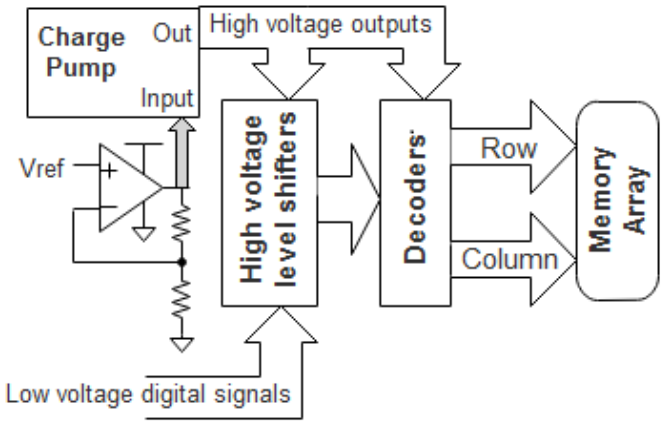

Fig. 1. High voltage decoding system in EEPROM memory

The approaches which basically deal with processing higher voltages than the safe operating limit of individual MOS transistors are: (*i*) to provide high voltage transistors which have higher operating voltage limit in the same process technology, thus requiring additional masks and area, resulting in a more expensive process; (*ii*) to use circuit techniques which ensures that the maximum voltage across the junction of each and every transistor remain below the maximum operating voltage as defined by the technology. This helps in designing a circuit that can tolerate high supply voltage in a standard CMOS process without adding any extra processing steps. The last approach helps in reducing the cost, without affecting the reliability and performance of the whole IP. Therefore, the design of high voltage circuit esp. level shifters in eNVM and other applications using low voltage transistors is a very hot research topic.

In this brief, a new high voltage level shifter has been introduced which can tolerate voltages up to 13.5V where the transistors used are capable of handling a maximum of 4.5V across its junctions. The proposed architecture can also be extended for voltages higher than 13.5V and is very area effective. A brief review of the conventional high voltage level shifters and their limitations are discussed in section II. The proposed circuit is presented in section III. Section IV discusses about the results obtained and finally, conclusions are drawn in section V.

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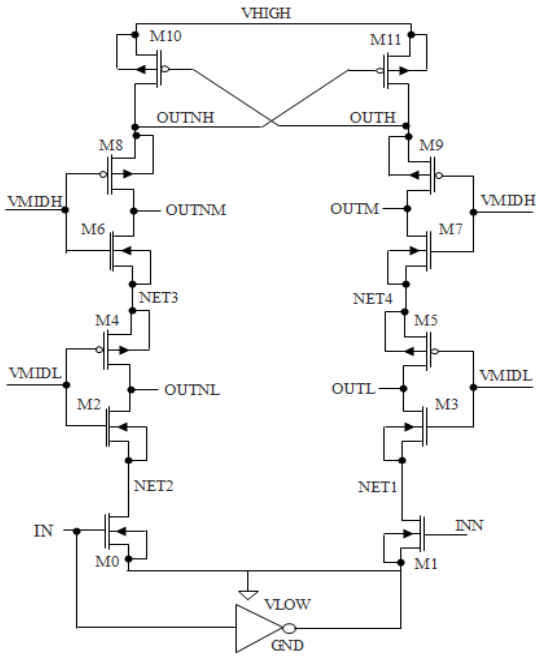

Fig. 2(a). Conventional high voltage level shifter

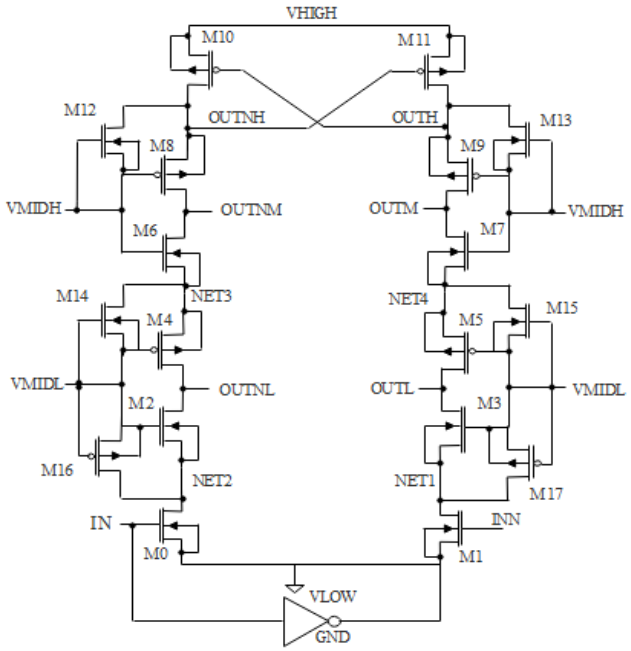

Fig. 2(b). Conventional high voltage level shifter with diode clamping

II. CONVENTIONAL HIGH VOLTAGE LEVEL SHIFTERS

Fig.2(a) shows the conventional high voltage level shifter [9], [10] having four supply voltages namely, VHIGH = 13.5V, VMIDH = 9V, VMIDL = 4.5V and VLOW = 1.8V. VMIDL and VMIDH supplies are used as cascode voltage and VHIGH is the level shift voltage. The signals at nodes IN and INN are digital signals and signal at IN is coming from the digital controller circuit. The level shifter consists of a half latch formed by two PMOS transistors M10 and M11. M10 and M11 provide positive feedback to the circuit and accelerates the settling of the nodes OUTH and OUTNH after they are excited by M0 and M1 driven by signals at inputs IN and INN. In this circuit, the pullup and pulldown strengths of M10 (M11) and M0 (M1) need to be balanced such that the pull down transistors can sufficiently discharge the output nodes overcoming the state of the output which remains latched by the cross coupled PMOS transistors M10 and M11. Transistors M2-M9 are used in cascoded fashion to avoid any kind of voltage stress in the devices.

As evident from Fig. 2(a) and 2(b), the lower side voltages of nodes OUTH (OUTNH), OUTM (OUTNM) settle at $(9V+|V_{tp}|)$ and $(4.5V+|V_{tp}|)$ while OUTL (OUTNL) settle to $(4.5V-V_{tn})$ on the higher side. $|V_{tp}|$ and V_{tn} are the threshold voltages of the PMOS and NMOS transistors, which varies according to the different process corners and temperature. This can cause static power dissipation problem in the succeeding stage, e.g., when OUTH node drives an inverter whose supply and ground rail are VHIGH and VMIDH, it is always conducting considering the NMOS of the inverter will always get a V_{gs} (Gate to Source voltage) of at least one $|V_{tp}|$ [11]. Also, if in case the voltages at one of the output drops due to coupling or charge loss, then there is no circuitry to pull that node to its desired state leading to improper functionality.

Thus, the output voltage levels which are driven by these nodes are not stable and are poorly driven.

To overcome this effect, diode connected transistors are placed in reverse bias fashion as shown in Fig. 2(b) [11], [12], which clamps the output nodes when it lowers or exceeds from a predetermined voltage level that can stress the device junctions. Although this helps in limiting the device stress across the junctions, but is effective only after the output nodes exceeds the device stress limit by one threshold voltage. If the device remains in this stressed condition for a long time, then it can cause oxide degradation leading to increase in leakage current [13] and dielectric breakdown [14].

III. PROPOSED HIGH VOLTAGE LEVEL SHIFTER

Fig.3 shows the proposed high voltage tolerant level shifter that properly drives the different output nodes of the level shifter to specific voltage ranges. VMIDH and VMIDL voltages are also used for cascoding to prevent the devices from stress and helps to isolate the transistors working at higher voltage domain with those working at lower voltage domain. Transistors M2, M3, M6, M7, M10, M11, M14 and M15 are used as cascoded stages. The gate of M2, M3, M6 and M7 are driven by VMIDL supply and the gate of M10, M11, M14 and M15 are driven by VMIDH supply. Transistors M8 and M9 are used to drive the minimum voltage of the OUT3 and OUTN3 node to VMIDL supply voltage. Similarly, M16 and M17 are used to drive the minimum voltage of the OUT5 and OUTN5 node to VMIDH level. PMOS transistors M4, M5, M12, M13, M18 and M19 are used in cross coupled fashion to compare and latch its respective outputs to their desired state when the input is stable at any one logic level.

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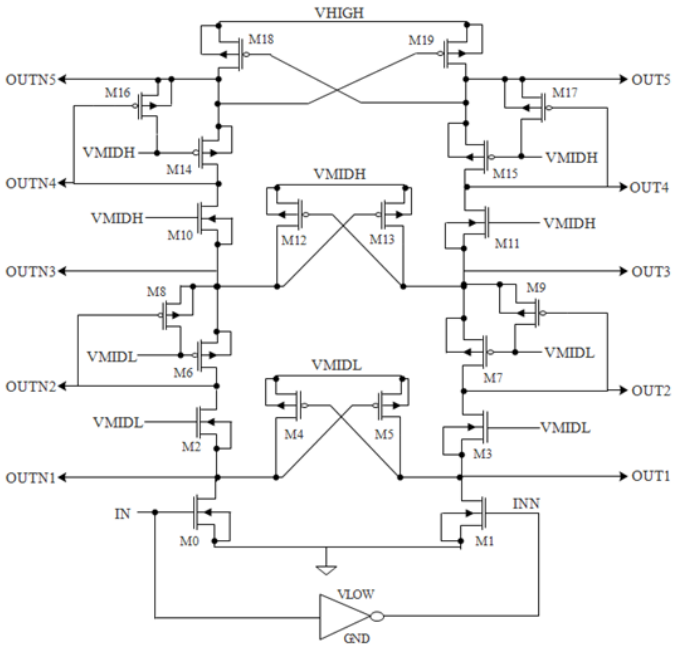

Fig. 3. Proposed high voltage level shifter

A. *Device Sizing Approach*

In this section, the design equations are derived and discussed for the level shifter to properly convert the low voltage input signals to high voltage outputs. $|V_{tp}|$ and V_{tn} are the threshold voltages of PMOS and NMOS devices and are positive quantities. By virtue of symmetry, the half circuit concept [15] is applied and the equations are derived for transistors in the left half. The transistors at the right half are sized in the same way.

The cross coupled transistors M4, M12, M18 and transistors M8, M16 are sized equally. M0 is sized relative to M4, M12 and M18 such that when the gate of M0 switches from 0V to VLOW level, the drain of M4, M12 and M18 are pulled down by at least $|V_{tp}|$ to flip the state of the latch. It can be said that M0 sees M4, M12 and M18 in parallel. Therefore, it is sized such that to overcome the effective pullup strength of PMOS transistors. At the start of switching, M0 is in saturation while M4, M12 and M18 are in deep triode region.

The current equation for these MOS are given by:

$$I_{DM0} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_n (V_{GSM0} - V_{tn})^2 \quad (1)$$

$$I_{DMP} = \mu_p C_{ox}\left(\frac{W}{L}\right)_p (V_{SGMP} - |V_{tp}|)|V_{tp}| \quad (2)$$

$$V_{SGMP} = (VMIDH - VMIDL);\ (VHIGH - VMIDH);\ VMIDL$$

The subscript MP stands collectively for M4, M12 and M18.

For $I_{DM0} = I_{DM4} + I_{DM12} + I_{DM18} = 3I_{DMP}$

$$\frac{\left(\frac{W}{L}\right)_{M0}}{\left(\frac{W}{L}\right)_{MP}} = \frac{6\mu_p(V_{SGMP} - |V_{tp}|)|V_{tp}|}{\mu_n(V_{GSM0} - V_{tn})^2} \quad (3)$$

As M0 pulls down the output nodes by one threshold voltage, M2, M10 turns on and the initial pull down drive is governed by these transistors. However, when the outputs drop significantly, the overdrive of M6 and M14 decreases and makes the pull down path weaker. Hence, the ratio of M2, M6, M10 and M14 with respect to M12, M18 in these conditions is a critical design parameter. For algebraic simplicity, we have solved for the case where,

$V_{SGCP} = V_{SG,M6,M14} = V_{SGMP} - 2|V_{tp}|$

And,

$V_{GSCN} = V_{GS,M2,M10} = 2|V_{tp}|$

$$I_{DM6} = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_{M6} (V_{SGMP} - 2|V_{tp}| - |V_{tp}|)^2 \quad (4)$$

$$I_{DM2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_{M2} (2|V_{tp}| - V_{tn})^2 \quad (5)$$

For $I_{DM6} = I_{DM2} = I_{DM12} + I_{DM18} = 2I_{DMP}$

$$\frac{\left(\frac{W}{L}\right)_{M6}}{\left(\frac{W}{L}\right)_{MP}} = \frac{2(V_{SGMP} - |V_{tp}|)|V_{tp}|}{(V_{SGMP} - 3|V_{tp}|)^2} \quad (6)$$

$$\frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{MP}} = \frac{2\mu_p(V_{SGMP} - |V_{tp}|)|V_{tp}|}{\mu_n(2|V_{tp}| - V_{tn})^2} \quad (7)$$

Similarly,

$I_{DM10} = I_{DM14} = I_{DM18} = I_{DMP}$

$$\frac{\left(\frac{W}{L}\right)_{M10}}{\left(\frac{W}{L}\right)_{MP}} = \frac{\mu_p(V_{SGMP} - |V_{tp}|)|V_{tp}|}{\mu_n(2|V_{tp}| - V_{tn})^2} \quad (8)$$

$$\frac{\left(\frac{W}{L}\right)_{M14}}{\left(\frac{W}{L}\right)_{MP}} = \frac{(V_{SGMP} - |V_{tp}|)|V_{tp}|}{(V_{SGMP} - 3|V_{tp}|)^2} \quad (9)$$

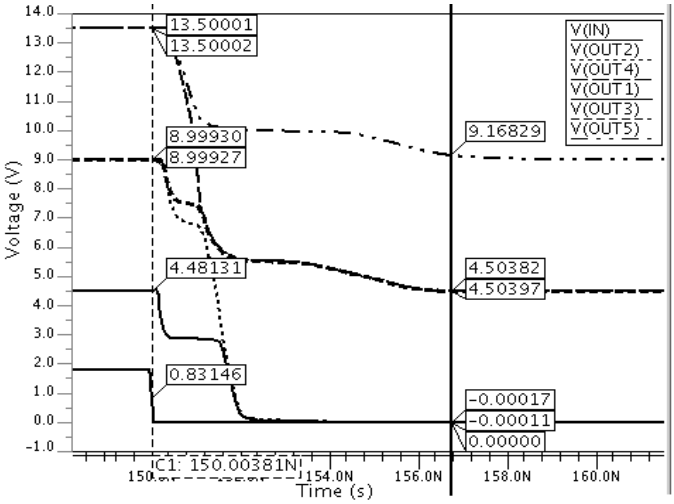

Fig. 4. Transient behavior of the proposed high voltage level shifter

For circuit robustness, the devices are sized for P fast/N slow corner with minimum VLOW and maximum VMIDL, VMIDH and VHIGH. For our case, we have made the pull down path around 2.8-3 times stronger than the pullup path.

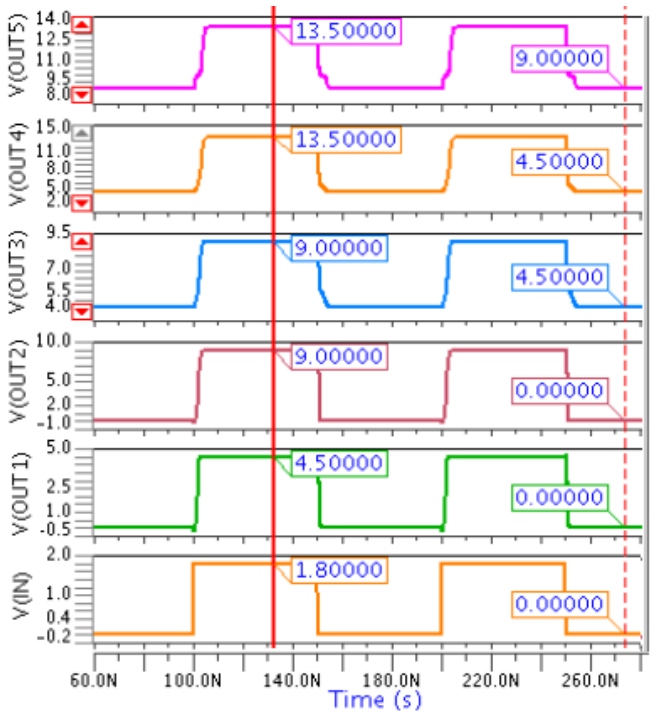

Fig. 5. Transient simulation results of the proposed level shifter.

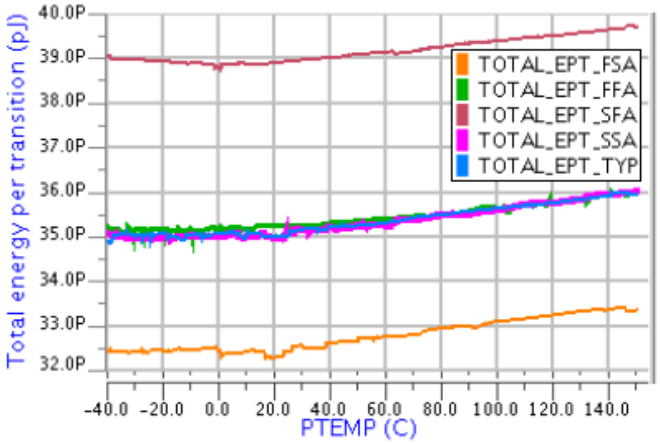

Fig. 6. Total energy per transition graph of the proposed level shifter at all process corners with respect to temperature.

B. Dynamic performance description

Following is the detailed description of the working of the proposed level shifter where the maximum operating voltage of all devices is 4.5V. Input logic signal varies between VLOW (1.8V) to 0V. VMIDL is at 4.5V, VMIDH at 9V and finally, VHIGH is at 13.5V.

When input signal IN is of "0V" level (i.e. logic "0"), OUT1 and OUT2 node is discharged to 0V. OUT3, OUT4 are discharged up to 4.5V and OUT5 is at 9V. Simultaneously, OUTN5 and OUTN4 are charged up to 13.5V. OUTN3 and OUTN2 are settled to 9V level and OUTN1 is at 4.5V.

Now, when the input signal "IN" switches from 0V to 1.8V (logic "0" to logic "1"), OUTN1 starts to discharge from 4.5V to 0v. OUTN3 and OUTN2 start to discharge from 9V through transistor M6 and M2. Similarly, OUTN5 and OUTN4 start discharging their node voltages from 13.5V through transistor

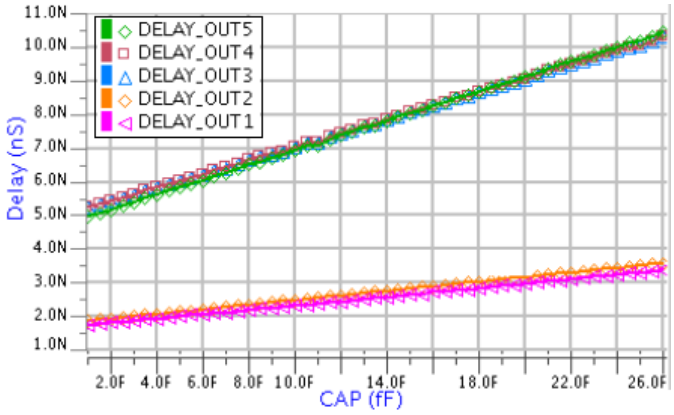

Fig. 7. Switching delay of the proposed level shifter with load capacitance variation.

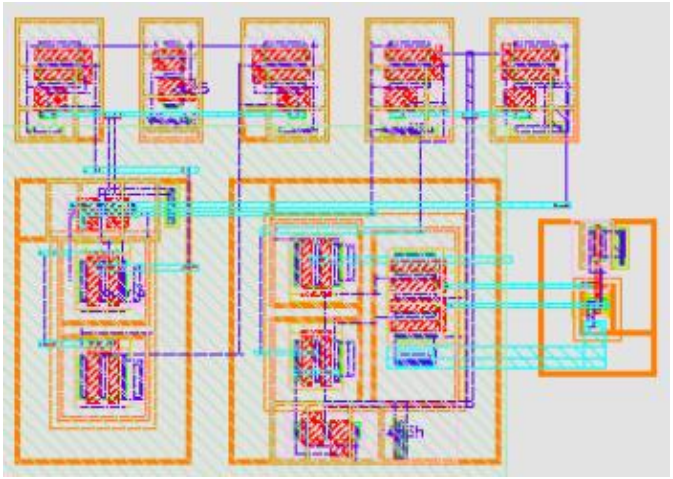

Fig. 8. Layout view of the proposed level shifter (30µm × 29µm)

M14 and M10. So, for a short period of discharge time OUTN5 follows OUTN4 and OUTN3 follows OUTN2.

Now, as OUTN3 discharges up to (4.5V + $|V_{tp}|$) transistor M6 gets into cutoff region and is switched off. OUTN2 still goes on discharging from (4.5V + $|V_{tp}|$) to 0v and as soon as M8 sees a certain $|V_{gs}|$, it will drive OUTN3 to 4.5V. Similar is the case for OUTN5 node where M14 goes to cutoff when OUTN5 is at (9V + $|V_{tp}|$), but OUTN4 still discharges unto 4.5V and M16 will then drive the OUTN5 to 9V.

Simultaneously, since OUTN1 is discharged to 0V which is the gate of M5, so M5 charges node OUT1 to 4.5V which is initially floating since input INN is at 0v and transistor M1 is switched off. OUT2 is a floating node and there is no current path from this node to GND while following OUT1 until it charges up to (4.5V - V_{tn}) until M3 gets off. OUT3 charges up to 9V through M13 whose gate is at 4.5V. OUT2 which is a floating node will follow OUT3 and also charges to 9V. During all this, M9 will try to sink some current from 9V supply to 4.5V supply since its gate is initially at (4.5V - V_{tn}) but will soon be switched off when its gate is charged to 9V. The speed with which the gate of M9 charges to 9V voltage depends on the current driving strength of transistor M7 and the (W/L) ratio of M7 and M9. Same phenomenon occurs for OUT4 and OUT5 node where the respective nodes are charged up to 13.5V voltage level through M19 and M15 transistors.

TABLE I

SUMMARY OF PREVIOUS AND EXISTING WORK

Parameter	[8]	[11]	[16]	[17]	[18]	This Work (Typ.)
Input voltage	0.2 V	3.3 V	0.4V	0.3V	1.8 V	1.8 V
Output voltage	1V	10 V	1.8V	1.2V	(9.8-12.8) V	(4.5-13.5) V
Operating frequency	1 MHz	25 MHz	100 KHz	1 MHz	1.25 MHz	10 MHz
Rise/Fall time	21.8 ns	2.4 ns	31.7 ns	25 ns	45 ns	2.5-8 ns
Output load	100 fF	15 fF	-	-	15 pF	15 fF
EPT	0.074 pJ	-	173 fJ	30.7 fJ	-	35.12 pJ
Process technology	0.09 µm CMOS	0.35 µm HVCMOS	0.18 µm CMOS	0.065 µm CMOS	0.18 µm BCD	0.11 µm HVCMOS

IV. RESULTS AND DISCUSSION

The proposed level shifter has been designed in 110nm triple well HVCMOS technology where the transistors are capable of handling a maximum of 4.5V. The results shown here are post layout simulated results, performed for an input signal frequency of 10MHz, input voltage of 1.8V and input rise and fall time of 1 ns with load capacitance considered as 15fF at all the output nodes of the level shifter, typically.

The worst case corner in terms of switching delay comes for fast PMOS (low $|V_{tp}|$) and slow NMOS (high V_{tn}) and temperature at 150ºC. In this analysis, we have made the input and supply voltages constant to know the dynamics of the level shifter corresponding to process and temperature only.

The transient behavior of the proposed level shifter is presented in Fig.4 where the input is changing its state from 1.8V to 0V. Fig.5 shows the switching of the output nodes with respect to the changes in the input signal. The output voltages are independent of threshold voltages as claimed in section III. The total energy per transition (EPT) is reported in Fig.6 for all the process corners with variation in temperature. Increase in temperature shows an increase in the EPT. This is because even though the peak current decreases with temperature, the switching delay of the circuit increases, which causes the EPT to increase as temperature rises. Also, the maximum EPT is observed for slow PMOS and fast NMOS process corner which is because of the higher overdrive voltage of NMOS compared to PMOS devices.

The proposed level shifter has almost symmetric rise and fall delays where the fall time is higher than the rise time by 0.2ns. The rise time of the level shifter is presented as switching delay in Fig.7. The shift in the delay of the different output nodes are shown as the load capacitance varies. Fig.8 shows the layout cross section of the level shifter which measures 870 um^2. Table I summarizes the performance of the level shifter with existing high voltage level shifters presented in [8], [11], [16], [17] and [18].

V. CONCLUSION

In this brief, a high voltage level shifter is presented which have different outputs nodes switching between different supply ranges. The proposed circuit properly drives the output nodes which is hard to achieve in conventional level shifter topologies without causing any voltage stress to the individual transistors used in the circuit. The circuit also offers almost symmetric rise and fall propagation delays because of the symmetric structure of the level shifter experiencing fully differential input signals.

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