

A Residue-Current-Locked Hybrid Low-Dropout Regulator Supporting Ultralow Dropout of Sub-50 mV With Fast Settling Time Below 10 ns

Young-Ha Hwang^{ID}, Member, IEEE, Jonghyun Oh^{ID}, Member, IEEE, Woo-Seok Choi^{ID}, Member, IEEE, Deog-Kyo Jeong^{ID}, Fellow, IEEE, and Jun-Eun Park^{ID}, Member, IEEE

Abstract—This article proposes a fully integrated hybrid low-dropout regulator (HLDO) that features an ultralow dropout and a highly improved transient response. This HLDO incorporates a residue-current-locked loop (RLL) that realizes joint regulation using a residue-compensating analog LDO (RLDO) and residue-triggered asynchronous digital LDO (DLDO). The RLDO supplements the residual current to compensate for the current quantization error (CQE) of the DLDO, thus eliminating the limit cycle oscillation (LCO) and improving the power supply rejection compared to standalone DLDOs. Moreover, the RLDO uses a bounded residue control (BRC) scheme that achieves sub-50-mV dropout regulation based on the RLL. The RLDO based on a flipped-voltage-follower (FVF) is equipped with a droop-edge injection scheme, and it improves the fast transient response against a heavy load by promptly triggering the self-coded DLDO. Residue-driven DLDO control is realized using asynchronous pointer-shift registers (PoSRs) so that the DLDO can respond rapidly without the use of any high-frequency clock. The prototype implemented using a 65-nm CMOS process achieves a 76-mV voltage droop and an 8.2-ns settling time against a load current step of 80 mA/0.5 ns with a 20-mV dropout voltage. The prototype demonstrates load regulation of 0.06 and less than 0.01 mV/mA with a dropout voltage of 20 and 50 mV, respectively, at a 1-V input.

Index Terms—Fast transient, fully integrated, hybrid, low-dropout regulator (LDO), power management.

I. INTRODUCTION

MANY system-on-chips (SoCs), ranging from low-power microcontrollers to high-performance proces-

Manuscript received July 28, 2021; revised October 14, 2021; accepted November 11, 2021. Date of publication November 30, 2021; date of current version June 29, 2022. This article was approved by Associate Editor Piero Malcovati. This work was supported in part by Chungnam National University and in part by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education under Grant NRF-2019R1I1A1A01058181. (Corresponding author: Jun-Eun Park.)

Young-Ha Hwang is with the John A. Paulson School of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138 USA (e-mail: youngha@g.harvard.edu).

Jonghyun Oh is with the Department of Electrical Engineering, Columbia University, New York, NY 10027 USA (e-mail: jo2686@columbia.edu).

Woo-Seok Choi and Deog-Kyo Jeong are with the Department of Electrical and Computer Engineering and the Inter-University Semiconductor Research Center, Seoul National University, Seoul 08826, South Korea (e-mail: wooseokchoi@snu.ac.kr; dkjeong@snu.ac.kr).

Jun-Eun Park is with the Department of Electronics Engineering, Chungnam National University, Daejeon 34134, South Korea (e-mail: juneun@cnu.ac.kr).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/JSSC.2021.3128815>.

Digital Object Identifier 10.1109/JSSC.2021.3128815

sors, incorporate power management units (PMUs) to achieve an energy-efficient operation [1], [2]. Recently, power management has been realized by using an integrated voltage regulator that combines a high-efficiency switching regulator and a fast-transient low-dropout regulator (LDO). After the switching regulator performs power conversion, the LDO must provide ripple rejection and a fast transient response against steep load current variations. Moreover, the LDO should minimize the dropout voltage, typically, to less than 100 mV, to improve power efficiency. Because LDOs have such stringent requirements, studies have developed digital LDOs (DLDOs) for use in PMUs instead of conventional analog LDOs (ALDOs) [3]–[5].

The DLDO can perform digital control of its power transistor, thereby affording low-voltage, low-dropout operation and ease of process scaling. The digital controller continuously adjusts the number of power transistors to be turned on such that the regulated output voltage is kept as close as possible to a reference voltage; ideally, this is performed independent of the load current at a given moment. DLDOs can be classified into the synchronous type that uses an operating clock and the asynchronous type that operates in an event-driven manner without the use of the clock. The transient response, load regulation, output ripple, and other performance characteristics of synchronous DLDOs can be improved using higher clock frequencies with a tradeoff between speed and power. Some synchronous DLDOs thus utilize a conditionally boosting clock in a time-based approach [6], [7] or select either fast or slow clocks accordingly for coarse-fine tuning [8] to improve the power efficiency. In addition, a binary-search DLDO [9] can reduce the regulation time and quiescent current compared to a baseline linear-search one. Asynchronous DLDOs with an event-driven controller [10]–[17] can overcome the speed-power tradeoff and rapidly recover from voltage droop. This enables scaling down the output capacitor, thereby enabling the realization of a fully integrated LDO without any external capacitor. Even capacitor-less DLDOs [11], [13] demonstrated decent figure-of-merits (FOMs) with a low dropout voltage of sub-50 mV based on their fast transient response owing to their self-coded schemes. A distributed topology of DLDOs [18], [19] showed wide-range load capability at low dropout voltage, which can mitigate the IR drop issue. A DLDO that combines asynchronous binary-searching and synchronous linear-

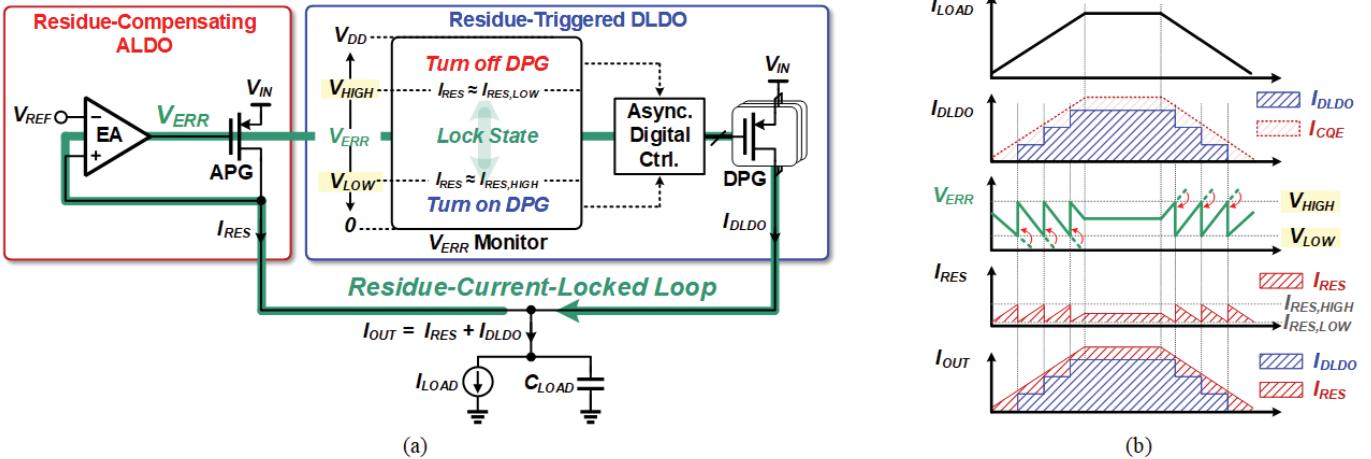


Fig. 1. (a) Conceptual block diagram of the proposed regulation scheme of residue-current-locked loop (RLL). (b) Illustrative load transient response of RLL.

searching schemes [34] showed a wide dynamic load range and achieved a small output voltage ripple. Nevertheless, a current quantization error (CQE) inevitably occurs in DLDOs because of the binary control of the digital pass gate (DPG), resulting in steady-state output ripples and low power-supply rejection (PSR).

To address the above-mentioned limitations of DLDOs, many hybrid LDOs (HLDOs) that combine the benefits of analog and digital control have been proposed [20]–[26], [35]. In [20] and [21], when the load current varied considerably, the digital control loop of an HLDO quickly conducted coarse regulation. Subsequently, once the coarse tuning is done, the HLDO activated an analog loop for performing steady-state fine regulation. However, the HLDO required a clock of hundreds of megahertz for realizing the swift control of the digital loop in response to load variations and an off-chip capacitor for achieving good droop performance. By contrast, in [22], a flipped-voltage-follower (FVF)-based analog loop first responded to load current changes through proportional control. The fast response of the FVF relaxed the speed requirement of the subsequent digital loop despite a smaller load capacitance; however, it was not able to demonstrate a current capacity of the order of tens of milliamperes. In [23], an always-on ALDO activated a clocked DLDO in an event-driven way similar to that in [16]. The HLDO in [23] increased the current capacity up to 500 mA; however, the PSR gradually degraded as the load current increased. In [24], a modular LDO topology enabled PSR programmability with configurable combinations of ALDO and DLDO tiles to satisfy various PSR and power budget requirements with a dropout voltage above 150 mV. In [26], an event-driven LDO based on a charge pump with an ac-coupled feedback was introduced; it demonstrated a superior FOM, although the PSR improvement remained an issue. In [35], a self-coded DLDO utilizes an analog control module to limit the output ripple voltage by reducing the high-frequency component of the ripple.

This article presents a novel residue-current-locked HLDO in which a residue-compensating ALDO (RLDO) and residue-triggered DLDO cooperate for improving the transient response and regulation accuracy. The RLDO and DLDO constitute a residue-current-locked loop (RLL) that forces the

CQE of the DLDO to be compensated by the RLDO. The RLL realizes seamless regulation between fine analog regulation and coarse digital regulation. In the RLDO, a bounded residue control (BRC) scheme is applied to maintain loop gain; it allows a dropout voltage as low as tens of millivolts without the loss of regulation accuracy. Therefore, the HLDO can support an ultralow dropout voltage of sub-50 mV with tight load regulation. In addition, a droop-edge injection scheme is adopted to reduce both the voltage droop and the response time against steep load current variations. The DLDO control is realized using asynchronous pointer-shift registers (PoSRs) that can respond rapidly without a high-frequency operating clock. Consequently, the HLDO achieves a settling time below 10 ns against a load current step of 100 mA/0.5 ns with a 1-V input.

The remainder of this article is organized as follows. Section II describes the overall architecture and operating principles of the proposed HLDO. Section III presents the implementation details and loop analysis. Section IV presents the measurement results and performance comparison. Finally, Section V presents the conclusions of this article.

II. OPERATING PRINCIPLES AND ARCHITECTURE

A. Residue-Current-Locked Loop (RLL)

The proposed HLDO overcomes the limitations of prior DLDOs and HLDOs by incorporating the RLL. Fig. 1(a) shows the conceptual block diagram of the RLL. To compensate for the CQE of the DLDO, the RLDO continuously supplements a residue current I_{RES} . For achieving a fast response to load variations, the RLDO instantly triggers the DLDO to perform coarse regulation as soon as I_{RES} goes outside the compensation range of the RLDO. Because the gate voltage V_{ERR} of the analog pass gate (APG) in the RLDO results from the current difference between the load current I_{LOAD} and the DLDO current I_{DLDO} , I_{RES} corresponds to the CQE of the DLDO. Hence, by sensing V_{ERR} , the RLL can detect whether the residue current is locked into a designed range from $I_{RES,LOW}$ to $I_{RES,HIGH}$. For instance, when the residue current I_{RES} becomes larger than $I_{RES,HIGH}$, the DLDO is triggered in a “residue-driven” manner to increase I_{DLDO} by

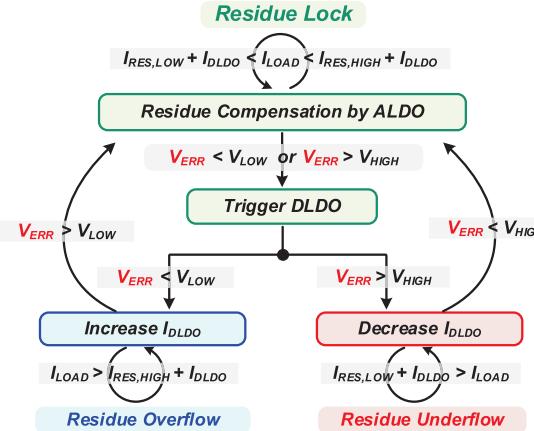


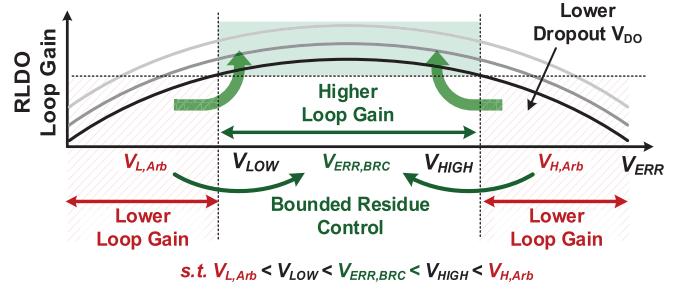
Fig. 2. Flowchart of RLL operation.

turning on the digital pass gate (DPG) so that I_{RES} can be restored within the bounded range, as shown in Fig. 1(b). The digital regulation by the DLDO adaptively continues until both $I_{LOAD} = I_{DLDO} + I_{RES}$ and $I_{RES,LOW} < I_{RES} < I_{RES,HIGH}$ are satisfied.

Fig. 2 shows the flowchart of the RLL operation. When the RLL is in a lock state such that $I_{DLDO} + I_{RES,LOW} < I_{LOAD} < I_{DLDO} + I_{RES,HIGH}$ (*Residue Lock*), the RLDO performs fine regulation by accordingly adjusting I_{RES} without triggering the DLDO. When I_{LOAD} increases and becomes larger than $I_{DLDO} + I_{RES,HIGH}$ (*Residue Overflow*), the DLDO increases I_{DLDO} until $I_{RES,LOW} < I_{LOAD} - I_{DLDO} < I_{RES,HIGH}$ is satisfied. By contrast, when I_{LOAD} decreases and becomes smaller than $I_{DLDO} + I_{RES,LOW}$ (*Residue Underflow*), the DLDO decreases I_{DLDO} until I_{RES} returns to the range. In this way, the RLDO and DLDO cooperatively form a hybrid loop for locking the residue current I_{RES} within the range from $I_{RES,LOW}$ to $I_{RES,HIGH}$. Consequently, the DLDO performs coarse regulation against a heavy load current, whereas the RLDO provides fine regulation to compensate for the residual CQE. Because the DLDO supplies most of the load current at a heavy load condition, a small APG is sufficient for the RLDO to realize fine regulation and cover a light-load range. Furthermore, this facilitates to quickly trigger the DLDO against a heavy load.

B. Bounded Residue Control (BRC)

For achieving higher power efficiency, a lower dropout voltage at the pass gate is desirable. Many DLDOs [9], [11]–[14], [18], [19] can support a dropout voltage of 50 mV. By contrast, HLDOs [20], [24] and ALDOs [27]–[31] cannot easily do so without sacrificing regulation accuracy, mainly because of the reduced gain of an analog regulation loop. The loop gain of an analog loop inevitably decreases at a lower dropout voltage because of the degradation of both the transconductance and output impedance of the APG. Furthermore, as the dropout voltage decreases, the gate voltage range in which the APG operates in the saturation region becomes narrower. In a conventional ALDO structure, if the gate voltage range of the APG is constrained within the range in which the ALDO loop gain is guaranteed to be as high

Fig. 3. Illustrative RLDO loop gain versus V_{ERR} .

as possible for accurate regulation, the load current capability will greatly decrease when the dropout voltage is lowered.

By contrast, the proposed RLL regulation scheme allows the RLDO loop to maintain a large loop gain without concern for the limited load capability. This is because the RLDO always supplies only the residue current, whereas the DLDO covers most of the load current exceeding the residue current range. Hence, the gate voltage can be bounded while keeping a large loop gain without the loss of the entire load capability. Fig. 3 shows the illustrative RLDO loop gain versus the gate voltage V_{ERR} . As V_{ERR} becomes closer to the ground or supply voltage, the RLDO loop gain decreases because both the transconductance of the APG and the gain of the error amplifier decrease. When V_{ERR} is bounded from V_{LOW} to V_{HIGH} , the RLDO loop can maintain a larger loop gain than outside the bounded region, thereby securing the gain of the error amplifier. In this manner, the RLDO can mitigate its loop gain degradation due to the low dropout voltage. Therefore, the BRC scheme is realized by adjusting the trigger voltage levels V_{LOW} and V_{HIGH} for V_{ERR} such that the RLDO loop gain can be sustained.

C. HLDO Regulation Analysis

In steady state, for simplicity, assume that all turn-on DPGs operate in the deep triode region; this is more valid at lower dropout voltages reaching $V_{DS} \ll 2(V_{GS} - V_{TH})$ because the DPGs are fully ON. Then the DPGs can be modeled as a linear resistor with the equivalent ON-resistance R_D , as shown in Fig. 4(a). In a conventional DLDO structure, the DLDO ideally turns on either k or $(k+1)$ DPGs such that

$$V_{OUT,k} = \frac{R_L V_{IN}}{\frac{R_D}{k} + R_L} < V_{REF} < V_{OUT,k+1} = \frac{R_L V_{IN}}{\frac{R_D}{k+1} + R_L} \quad (1)$$

where $V_{OUT,k}$ and $V_{OUT,k+1}$ are the output voltages when k and $(k+1)$ DPGs are ON, respectively, and R_L is the equivalent resistance of a load current I_L . When k DPGs are ON, the regulation error of the DLDO E_{DLDO} is expressed as

$$E_{DLDO} = V_{REF} - \frac{R_L V_{IN}}{\frac{R_D}{k} + R_L}. \quad (2)$$

For a given load current, the output voltage of the DLDO oscillates between $V_{OUT,k}$ and $V_{OUT,k+1}$ because of the CQE, resulting in the limit cycle oscillation (LCO) issue. By contrast, the proposed HLDO eliminates the LCO by compensating for the CQE with the RLDO. Once the DLDO performs coarse regulation with a digitized I_{DLDO} , the RLDO adaptively

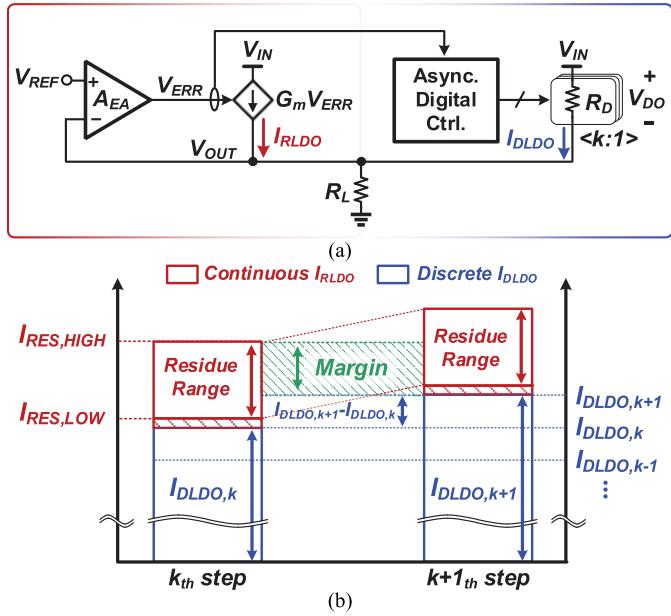


Fig. 4. HLDO regulation analysis. (a) Simplified schematic. (b) Consideration for LCO elimination.

supplies a continuous I_{RLDO} for fine regulation, as shown in Fig. 4(b). To provide seamless regulation between when k - and $(k+1)$ -DPGs are ON for any arbitrary k , the configurable range of I_{RLDO} should satisfy

$$I_{DLDO,k+1} - I_{DLDO,k} = \frac{V_{DO}}{R_D} < I_{RES,HIGH} - I_{RES,LOW} \quad (3)$$

where V_{DO} is the dropout voltage.

To consider the regulation error of the HLDO, the APG of the RLDO is modeled as a voltage-controlled current source with transconductance G_m , as shown in Fig. 4(a). When k DPGs are ON, from Kirchhoff's current law, V_{OUT} is expressed as

$$V_{OUT} = \frac{R_L}{\frac{R_D}{k} + R_L} \left(V_{IN} + \frac{R_D}{k} I_{RLDO} \right) \quad (4)$$

where $I_{RLDO} = G_m A_{EA} (V_{REF} - V_{OUT})$. By substituting I_{RLDO} into (4), V_{OUT} is expressed as

$$V_{OUT} = \frac{1}{1 + A_{RLDO}} \left(\frac{R_L V_{IN}}{\frac{R_D}{k} + R_L} + A_{RLDO} V_{REF} \right) \quad (5)$$

where

$$A_{RLDO} = \left(\frac{R_D}{k} \parallel R_L \right) G_m A_{EA}. \quad (6)$$

From (1), the regulation error of the HLDO E_{HLDO} is expressed as

$$\begin{aligned} E_{HLDO} &= \frac{1}{1 + A_{RLDO}} \left(V_{REF} - \frac{R_L V_{IN}}{\frac{R_D}{k} + R_L} \right) = \frac{E_{DLDO}}{1 + A_{RLDO}} \\ &= \frac{E_{DLDO}}{1 + \left(\frac{R_D}{k} \parallel R_L \right) G_m A_{EA}}. \end{aligned} \quad (7)$$

This indicates that E_{DLDO} is reduced by the RLDO loop gain within the RLL in the HLDO. Hence, the RLL effectively helps the HLDO to eliminate the LCO and perform accurate

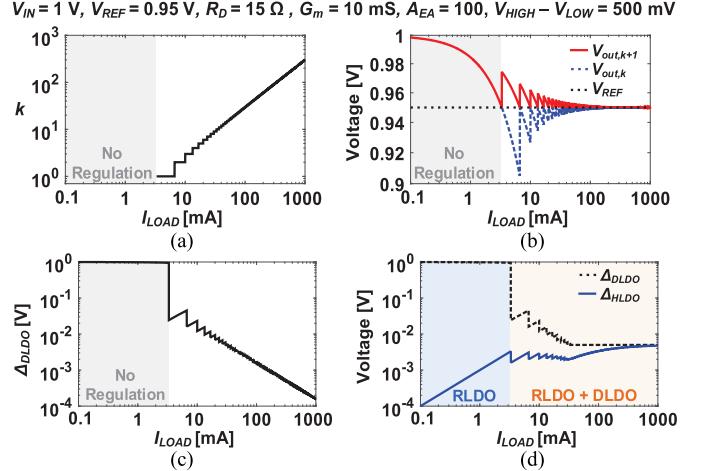


Fig. 5. Simulation results of regulation accuracy of HLDO compared to that of standalone DLDO. (a) Number of turned-on DPGs k in standalone DLDO. (b) Resultant output voltages $V_{OUT,k+1}$ and $V_{OUT,k}$ in standalone DLDO. (c) Regulation accuracy Δ_{DLDO} ($= V_{OUT,k+1} - V_{OUT,k}$) in standalone DLDO. (d) DLDO regulation accuracy Δ_{DLDO} in HLDO and HLDO regulation accuracy Δ_{HLDO} .

regulation by securing both G_m and A_{EA} in conjunction with the BRC scheme.

Fig. 5 shows the simulation results for the regulation accuracy of the HLDO compared to that of a standalone DLDO. Fig. 5(a) and (b) shows the number of turned-on DPGs k and the resultant output voltages $V_{OUT,k}$ and $V_{OUT,k+1}$, respectively, based on (1). We can define the regulation accuracy of the standalone DLDO Δ_{DLDO} by $V_{OUT,k+1} - V_{OUT,k}$, as shown in Fig. 5(c). In the HLDO, because the DLDO is only triggered when the V_{ERR} deviates from (V_{LOW}, V_{HIGH}) , the regulation accuracy is bounded by $(V_{HIGH} - V_{LOW})/A_{EA}$. Fig. 5(d) shows the regulation accuracy of DLDO Δ_{DLDO} and HLDO Δ_{HLDO} . As I_{LOAD} increases, A_{RLDO} decreases owing to the decreasing output impedance as given by (6), and thus, Δ_{HLDO} approaches $(V_{HIGH} - V_{LOW})/A_{EA}$.

D. Overall Architecture

Fig. 6 shows the proposed HLDO architecture. The HLDO consists of the FVF-based RLDO and the DLDO that has 128 unit DPGs (DPG_{Unit}). The RLDO offers a fast response to load variations by deploying an FVF topology with a droop-edge injection scheme. The RLDO has an error amplifier (EA) to obtain a higher DC loop gain. The V_{ERR} monitor implemented using two continuous-time (CT) comparators triggers the DLDO as soon as V_{ERR} deviates from the lock range. The DLDO performs coarse regulation with the asynchronous PoSRs. For instance, when V_{ERR} becomes lower than the lower boundary voltage V_{LOW} , the DLDO is triggered to adjust the number of unit DPGs turned on for increasing I_{DLDO} until V_{ERR} returns to the lock range. Similarly, the DLDO reduces I_{DLDO} when V_{ERR} becomes higher than the upper boundary voltage V_{HIGH} . Simplified up-down control for the unary-weighted DPG array enables the DLDO to be implemented with asynchronous shift registers with relaxed timing constraints. The asynchronous operation of the DLDO can realize a fast response against load current variations and

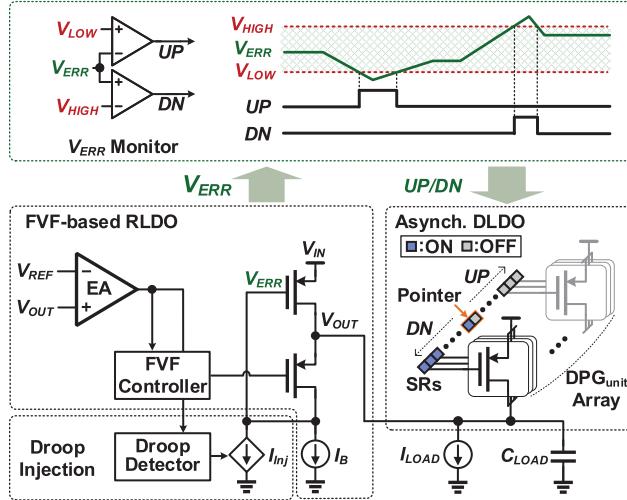


Fig. 6. Overall architecture of the proposed HLDO.

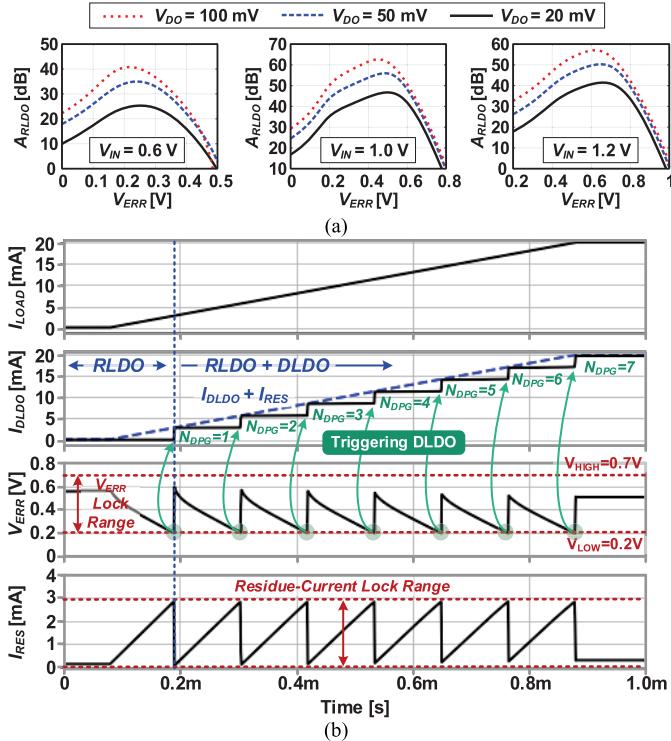


Fig. 7. (a) Simulated RLDO loop gain. (b) Simulated transient operation of RLL hybrid regulation.

reduce voltage droop, thus obviating the need for an off-chip large output capacitor, and a high-frequency clock. In addition, the boundary voltages V_{LOW} and V_{HIGH} used for both realizing the BRC scheme and triggering the DLDO are independent of V_{REF} , and they enable quick reference tracking without involving a multi-bit reference in conventional event-driven structures [15].

Fig. 7(a) shows the simulated A_{RLDO} versus V_{ERR} with respect to the dropout voltage V_{DO} and the supply voltage V_{DD} . Because A_{RLDO} decreases at lower V_{DO} regardless of V_{DD} , the

BRC scheme can effectively secure the loop gain for a wide V_{DD} range. Fig. 7(b) shows the simulated transient response of the RLL hybrid regulation. With a light load current before the activation of the DLDO, the regulation is conducted solely by the RLDO. As I_{LOAD} increases, V_{ERR} decreases to match I_{RES} to I_{LOAD} . When V_{ERR} becomes lower than V_{LOW} , which corresponds to the residue current value of $I_{RES,HIGH}$, the RLDO triggers the DLDO to start its regulation by increasing the number of turned-on DPGs N_{DPG} . Then, I_{RES} is reduced to around $I_{RES,LOW}$, residing in the residue-current-lock range. In this way, the RLDO and DLDO cooperatively minimize the regulation error and provide accurate regulation over the whole load current range.

III. CIRCUIT IMPLEMENTATIONS AND LOOP ANALYSIS

A. FVF-Based RLDO With Droop Injection

The primary role of the RLDO is to supplement a residue current for CQE compensation and to trigger the DLDO for fast recovery from the voltage droop caused by heavy load variations. To achieve both accurate residue regulation and fast responses to load variations, the RLDO is implemented using the FVF topology with the droop-edge injection scheme. Fig. 8(a) shows the circuit implementation of the RLDO with the size information of several critical transistors. It consists of an FVF regulator and its controller, a voltage droop detector, a droop-edge injection stage, and an error amplifier. The bias voltages of p_b and n_b are 0.48 and 0.55 V, respectively. As shown in Fig. 8(b), the RLDO conducts its regulation in three ways: 1) FVF self-feedback regulation; 2) droop-edge injection; and 3) error-feedback regulation. When the load current increases in a narrow edge time, the output V_{OUT} decreases and shows a large voltage droop. Then, the output droop immediately reduces the gate voltage V_{ERR} of the APG M_{RES} through the common-gate configuration of M_{CTRL} . Hence, the FVF regulator offers a fast response to a load variation utilizing the self-feedback structure.

The error amplifier senses the difference between V_{REF} and V_{OUT} . To achieve sufficient DC gain, the error amplifier is implemented using a folded-cascode amplifier with low threshold voltage devices. The output voltage $V_{EA,OUT}$ is used for the droop-edge injection and error-feedback regulation. The droop-edge injection is realized using the voltage-droop detector and the edge-injection stage. The voltage-droop detector senses the falling edge of $V_{EA,OUT}$ caused by V_{OUT} droop. In steady state, both M_{SEN} and M_{GEN} turn off, and the capacitor C_{INJ} is charged to V_{IN} . At the falling edge of $V_{EA,OUT}$ due to V_{OUT} droop, M_{SEN} turns on and starts to inject an instant current from C_{INJ} to the drain/gate nodes of M_{GEN} in proportion to the scale of the undershoot voltage. M_{GEN} mirrors the increased drain current to M_{INJ} and pulls down V_{ERR} depending on the mirrored current. As a result, injection of the falling edge of V_{OUT} droop directly pulls down V_{ERR} , thereby providing fast droop recovery by not only increasing I_{RES} but also immediately triggering the DLDO. As shown in the measured load transient response in Fig. 8(c), the droop-edge injection scheme can improve the voltage droop and response time T_R by 18% and 58%, respectively. After the

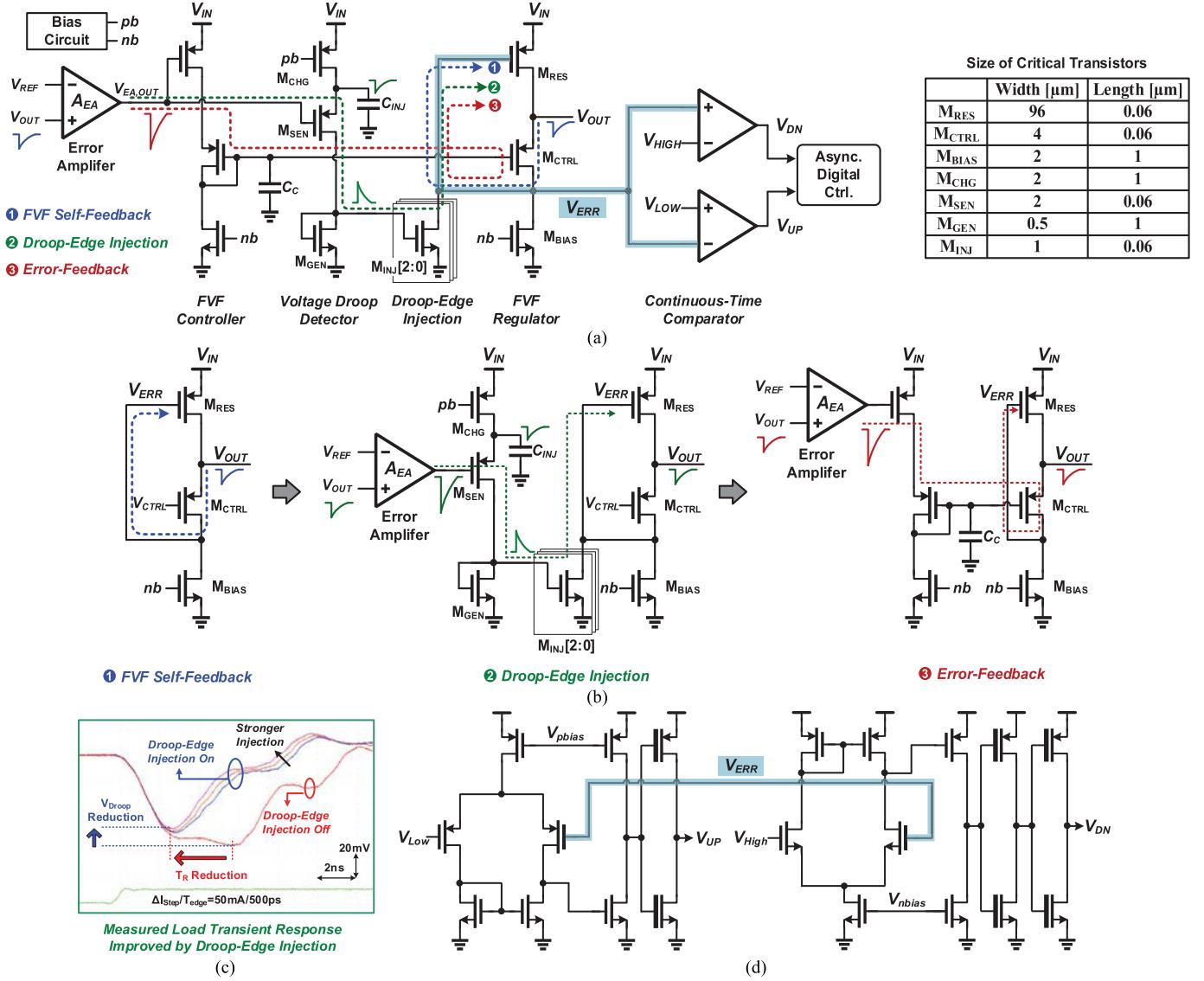


Fig. 8. (a) Schematic of the proposed FVF-based RLDO with size of critical transistors. (b) Procedures of FVF-based regulation in three ways and (c) measured load transient response depending on droop injection. (d) Schematic of continuous-time comparator for monitoring V_{ERR} .

falling edge of the V_{OUT} , C_{INJ} is immediately recharged to V_{IN} by M_{CHG} .

Next, the error feedback loop manages fine regulation. The error-feedback regulation is performed by the error amplifier and FVF controller through the FVF regulator stage. The error amplifier output $V_{EA,OUT}$ is converted to the gate control signal for M_{CTRL} in the FVF controller. The capacitor C_C is added in consideration of the RLDO loop stability. Note that the addition of C_C does not affect the fast regulation by the FVF self-feedback and the droop-edge injection.

The self-triggering of the DLDO is realized by sensing the gate voltage V_{ERR} of M_{RES} . The lower bound voltage V_{LOW} and upper bound voltage V_{HIGH} are compared with V_{ERR} using two CT comparators, as shown in Fig. 8(d). Considering the voltage level of V_{LOW} and V_{HIGH} , a PMOS-input common-source amplifier and an NMOS-input common-source amplifier are used for detecting crossing events over the lower bound and upper bound, respectively.

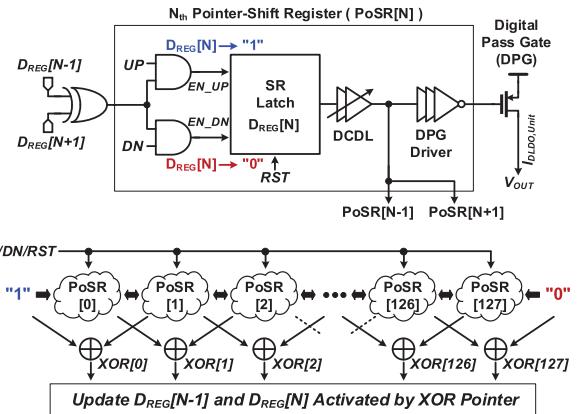


Fig. 9. Block diagram of asynchronous digital LDO.

B. Asynchronous DLDO With Point-Shift Register

Fig. 9 shows the circuit implementation of the residue-driven asynchronous DLDO that consists of 128 b PoSRs

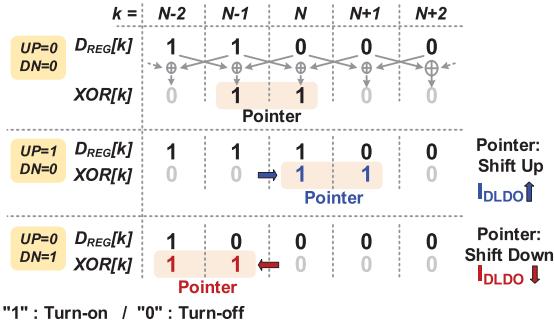


Fig. 10. Operating principle of asynchronous point-shift registers (PoSRs).

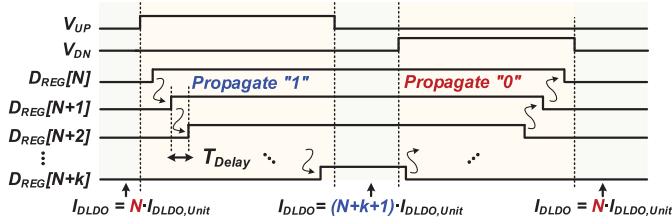


Fig. 11. Timing diagram of asynchronous PoSR.

and a unary-weighted DPG array. When coarse regulation is activated, the DLDO adjusts the number of turn-on pass gates in the DPG array by using the *UP* and *DN* signals generated from the CT comparators. To realize the asynchronous operation of the DLDO, the DLDO controller employs serial point-shifting registers with XOR-based propagation control. Each PoSR comprises two AND gates that determine a propagating direction, an SR latch, a digitally controlled delay line (DCDL) that adjusts a propagation delay to prevent the LCO, and a buffer that drives the corresponding DPG.

Fig. 10 shows the operating principle of the PoSRs. The DPG control signal \$D_{REG}[N]\$ in the *N*th PoSR (*PoSR*[*N*]) is updated if the two adjacent PoSRs' control signals \$D_{REG}[N-1]\$ and \$D_{REG}[N+1]\$ are different from each other. For example, \$D_{REG}[N]\$ is updated to turn-on ("1") or turn-off ("0") depending on the direction signals *UP/DN* only when \$D_{REG}[N-1] = "1"\$ and \$D_{REG}[N+1] = "0.\$" Hence, each PoSR can decide whether to update or hold its control signal based on the XOR operation. Fig. 11 shows the timing diagram for updating the control signal while the *UP* or *DN* signal is activated. When the values of \$D_{REG}[0:N-1]\$ are all "1," the rising event of the *UP* signal triggers to assert \$D_{REG}[N], D_{REG}[N+1], \dots\$, and so on, thereby propagating "1" in the PoSRs until the *UP* signal falls. When the \$D_{REG}[0:N+k+1]\$ values are all "1," the rising event of the *DN* signal operates in the same manner. The propagation delay of \$D_{REG}[N]\$ \$T_{delay}\$ is determined by the sum of the logic delay of the XOR gate, AND gate, latch, DCDL, and buffer. Owing to the DCDL in the PoSR, \$T_{delay}\$ is tunable from 290 ps to 1.65 ns. Thus, the effective clock frequency of the DLDO is higher than 600 MHz, thereby realizing fast regulation of the HLDO.

C. Analysis on Loop Stability

In the proposed HLDO, two cases need to be considered for analyzing the loop stability: 1) only the RLDO governs the

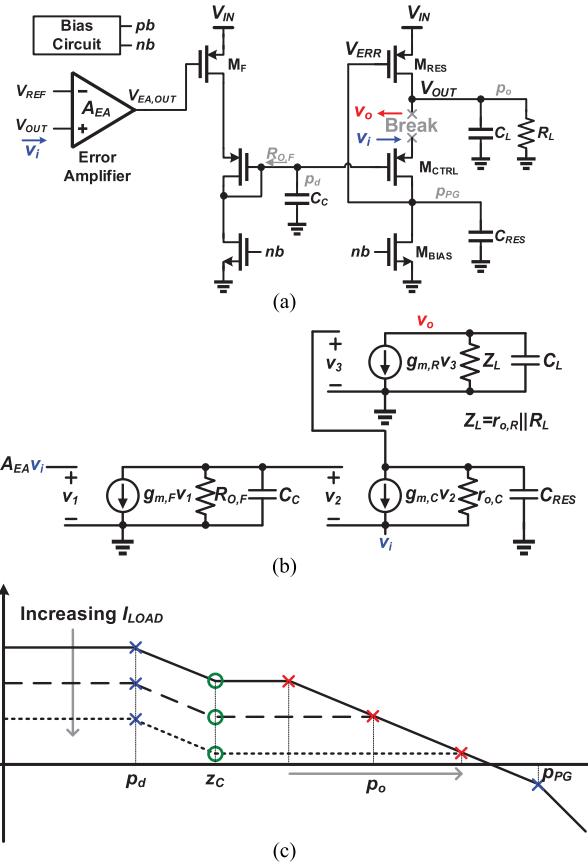


Fig. 12. Loop stability analysis on RLDO. (a) Schematic of loop stability analysis. (b) Small-signal model of overall loop. (c) Overall loop gain.

loop stability at the light load condition and 2) both the RLDO and the DLDO jointly regulate the output at the medium or heavy load condition.

1) *Regulation With RLDO:* For the change of \$I_{LOAD}\$ within a light-load range such that only the RLDO performs regulation, the FVF self-feedback and error-feedback loops mainly determine the loop stability. Fig. 12(a) and (b) shows the RLDO schematic for loop stability analysis and the small-signal model of the overall loop, respectively. Based on the small-signal analysis, the open-loop gain of \$v_o/v_i\$ is expressed as

$$\frac{v_o}{v_i} = A_{DC} \frac{(1 + s/z_c)}{(1 + s/p_d)(1 + s/p_o)(1 + s/p_{PG})} \quad (8)$$

where \$p_d\$ is the dominant pole due to \$C_C\$ in the error-feedback path; \$p_o\$, the output pole; and \$p_{PG}\$, the pole at the gate node of \$M_{RES}\$ due to the gate capacitance. These terms can be expressed using the following equations:

$$A_{DC} = -g_{m,C} r_{o,C} A_{EA} g_{m,F} R_{O,F} g_{m,R} (r_{o,R} || R_L) \quad (9)$$

$$p_d = \frac{1}{R_{O,F} C_C} \quad (10)$$

$$p_o = \frac{1}{(r_{o,R} || R_L) C_L} \quad (11)$$

$$p_{PG} = \frac{1}{r_{o,C} C_{RES}} \quad (12)$$

$$z_C = \frac{A_{EA}g_{m,F}}{C_C} \quad (13)$$

where $g_{m,C}$, $g_{m,F}$, and $g_{m,R}$ are the transconductances of M_{CTRL} , M_F , and M_{RES} , respectively; $r_{o,C}$ and $r_{o,R}$ are the output impedances of M_{CTRL} and M_{RES} , respectively; $R_{O,F}$ is the output impedance of the FVF controller stage; R_L is the equivalent resistance of load current; A_{EA} is the DC gain of the error amplifier; and C_{RES} is the gate capacitance of M_{RES} . Owing to the small size of M_{RES} , the pole p_{PG} at the gate node of M_{PASS} is readily placed at a high frequency of ~ 300 MHz, thereby precluding the use of any buffer to push p_{PG} toward a high frequency for the loop stability of the RLDO. The pole p_o is placed at a frequency of ~ 5 MHz for the minimum I_{LOAD} of $100\ \mu A$. Because the pole p_o moves toward higher frequencies as I_{LOAD} increases, the on-chip capacitor C_C of $20\ pF$ is placed at the gate node of M_{CTRL} to realize a dominant pole p_d of ~ 500 kHz for stability. As a result, the worst case phase margin of the RLDO loop is larger than 50° at the minimum I_{LOAD} . Note that p_d can be placed at a higher frequency if the minimum I_{LOAD} is higher. Fig. 12(c) shows the overall loop gain change to I_{LOAD} . The loop gain decreases as I_{LOAD} increases because of the diminishing impedance at the output node. The DC loop gain values are 44.8 and 44.3 dB at I_{LOAD} of $100\ \mu A$ and $1\ mA$. At I_{LOAD} of $4\ mA$ with the DPG ON, the DC loop gain is 21.1 dB. From (8)–(11) and (13), the unity-gain bandwidth is expressed as

$$UGB = \frac{g_{m,C}r_{o,C}g_{m,R}}{C_L}. \quad (14)$$

The phase margin is improved as I_{LOAD} increases because p_o moves toward high frequencies, which is desirable to trigger the DLDO stably. Even if we take into consideration the pole at the amplifier output node in the error-feedback loop, the phase margin is hardly affected. This is because the pole effect is canceled by another zero in the FVF self-feedback loop, and thus the phase margin is mainly determined by the location of p_o and p_{PG} .

2) Joint Regulation With RLDO and DLDO: As I_{LOAD} increases further, the DLDO takes part in the regulation. One way to stabilize this dual-loop regulation is to make one much faster than the other when both are activated, precluding interactions with each other [24]. The DLDO loop is activated only when V_{ERR} deviates from (V_{LOW}, V_{HIGH}) , whereas the RLDO regulation predominates when V_{ERR} is in (V_{LOW}, V_{HIGH}) . Because the DLDO loop is much faster than the error-feedback path of RLDO loop owing to the asynchronous PoSRs and CT comparators, the RLDO always manages fine regulation once the coarse regulation by the DLDO is completed without any stability issue. Moreover, since V_{OUT} controlled by the DLDO is connected to V_{ERR} directly through the voltage-follower path with high bandwidth P_{PG} , V_{ERR} can settle stably by making settling time of V_{ERR} shorter than the operating period of DLDO. Thus, the DLDO can offer stable operation. In addition, the comparator and shift register delay should be considered for eliminating the LCO, as shown in Fig. 13. $T_{C,Delay,Low}$ and $T_{C,Delay,High}$ are the delay of the comparator output from V_{ERR} crossing over V_{LOW} and V_{HIGH} , respectively. $T_{SR,Delay}$ is the delay of the PoSR shifting.

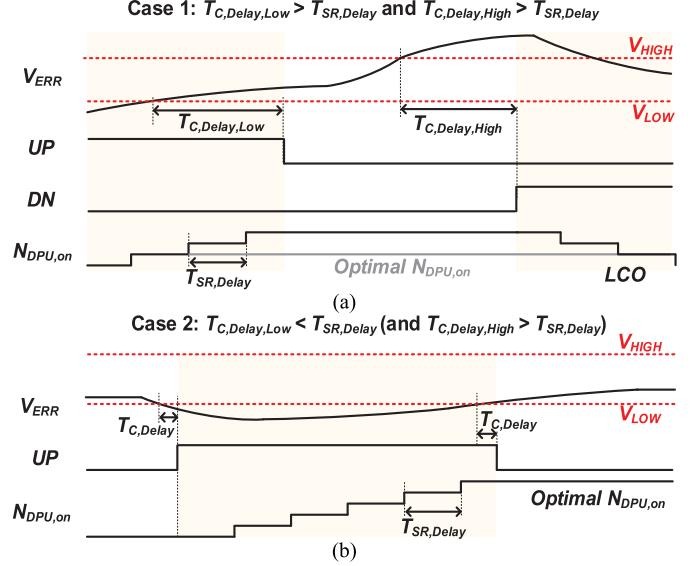


Fig. 13. Consideration of comparator delay $T_{C,Delay}$ and shift register delay $T_{SR,Delay}$ for eliminating LCO. (a) Case 1: $T_{C,Delay,Low} > T_{SR,Delay}$ and $T_{C,Delay,High} > T_{SR,Delay}$. (b) Case 2: $T_{C,Delay,Low} < T_{SR,Delay}$ (and $T_{C,Delay,High} > T_{SR,Delay}$).

If $T_{C,Delay,Low} > T_{SR,Delay}$ and $T_{C,Delay,High} > T_{SR,Delay}$ (Case 1), $N_{DPG,ON}$ always passes by the optimal value and eventually oscillates around it, resulting in LCO. If $T_{C,Delay,Low} < T_{SR,Delay}$ and $T_{C,Delay,High} < T_{SR,Delay}$ (Case 2), $N_{DPG,ON}$ can be settled at the optimal value, and then the RLDO performs regulation with the optimal $N_{DPG,ON}$ of DPGs.

D. PSR Performance

Conventional DLDOs show poor PSR performance in general. The proposed HLDO, however, shows a comparable PSR performance to the analog counterparts for a wide range of I_{LOAD} owing to the RLL. For such a light I_{LOAD} that only the RLDO works for regulation without the aid of the DLDO, the PSR is determined by the RLDO. For a small-signal analysis of PSR, the RLDO can be simplified to the error-feedback amplifier with a gain of A_{EF} and the power transistor with a transconductance of G_m as shown in Fig. 14(a). Assume that only the dominant pole is considered for simplicity. When there is a perturbation in V_{IN} , V_{OUT} is expressed as

$$V_{OUT} = G_m(R_O || R_L)(V_{ERR} - V_{IN}) \\ = -A_P \left(\frac{A_{EF}}{1 + s/p_d} V_{OUT} + V_{IN} \right) \quad (15)$$

where p_d is the dominant pole in the error-feedback path. Then V_{OUT} is expressed by a function of V_{IN} as follows:

$$V_{OUT} = \frac{-A_P V_{IN}}{1 + A_P \frac{A_{EF}}{1+s/p_d}} \approx -\frac{V_{IN}}{A_{EF}} \left(1 + \frac{s}{p_d} \right). \quad (16)$$

Therefore, the PSR performance is determined by

$$\text{PSR} \approx \frac{1}{A_{EF}} \left(1 + \frac{s}{p_d} \right) \quad (17)$$

which is approximately proportional to $1/A_{EF}$ in the frequency range up to the dominant pole of the error-feedback loop.

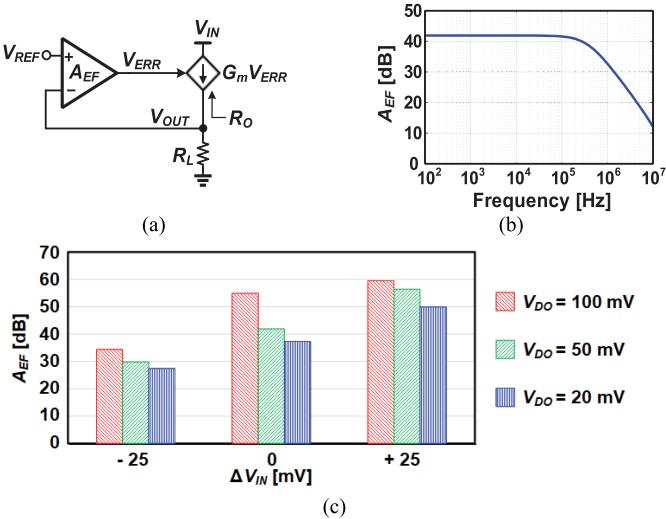


Fig. 14. Analysis on PSR performance. (a) Simplified small-signal model. (b) Simulated A_{EF} at V_{IN} of 1.2 V. (c) A_{EF} with respect to V_{IN} perturbation at V_{IN} of 1.2 V.

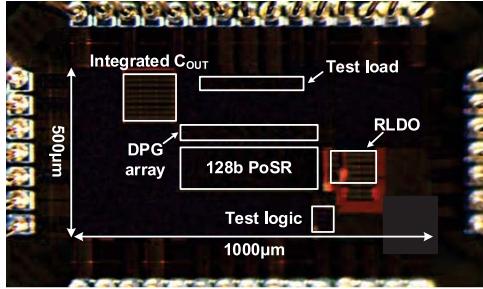


Fig. 15. Die microphotograph.

When both the RLDO and DLDO regulate the input supply (V_{IN}) ripple at a heavy I_{LOAD} , the RLL continuously minimizes the quantization error of DLDO by adjusting the number of turned-on digital pass gates $N_{DPG,ON}$ based on the value of V_{ERR} against the input supply ripple. Hence, for a low-frequency supply ripple, the remaining ripple at the output approximates the static error of load regulation which is bounded by $(V_{HIGH} - V_{LOW})/A_{EF}$. Therefore, A_{EF} dominates the PSR in both cases of the light and heavy load, thus the pole of the error-feedback loop p_d determines the cut-off frequency of PSR. Fig. 14(b) shows the simulated A_{EF} with a pole frequency of about 370 kHz at V_{IN} of 1.2 V. However, with low dropout voltages, a perturbation in the supply voltage can modulate A_{EF} . Fig. 14(c) shows the simulated A_{EF} with respect to the input voltage perturbation ΔV_{IN} at the nominal V_{IN} of 1.2 V. Given this simulation result, the PSR may be degraded to worse than -30 dB against ΔV_{IN} of 50 mV_{pp}. For further PSR improvement, it is important to design the loop gain stage that can sustain high A_{EF} against the supply perturbation.

IV. MEASUREMENT RESULTS

The proposed HLDO is fabricated in a 65-nm CMOS process. Fig. 15 shows the die microphotograph of the prototype that fully integrates an on-chip output capacitor

of 100 pF and a test load. The prototype occupies an active area of 0.079 mm².

Fig. 16 shows the measured transient responses to a load current step. Under a dropout voltage V_{DO} of 20 mV and an input voltage V_{IN} of 1.2 V, the HLDO achieves a voltage droop of 76 mV and a settling time of 8.12 ns when a load current step from 24 to 104 mA was applied within a 500-ps edge time. For V_{DO} of 50 mV and V_{IN} of 1 V, the measured voltage droop was 109 mV and the settling time was 8.72 ns with a load current step of 100 mA/500 ps. The measurement results of a fast settling time below 10 ns were realized by combining the fast-response RLDO and the self-triggered asynchronous DLDO without using any high-frequency clock. Fig. 17(a) and (b) show the measured transient responses to load current step of 50 mA starting from minimum currents of 1 and 5 mA, respectively. At V_{IN} of 1.2 V and V_{DO} of 20 mV, the HLDO achieved a settling time of 19.3 ns and a voltage droop of 116 mV. Also, the HLDO showed a settling time of 34 ns even at a lower V_{IN} of 0.9 V as shown in Fig. 17(b). Under the harsh load condition starting from several mA, the HLDO demonstrated fast transient response and ultralow dropout regulation. Fig. 17(c) and (d) show the measured transient responses with various conditions. The HLDO maintained the ultralow dropout regulation even with a low V_{IN} of 0.6 V as shown in Fig. 17(c). When heavy load current step of 501 mA was applied slowly with an edge time of 40 ns and V_{DO} of 200 mV, as shown in Fig. 17(d), the HLDO accomplished regulation without oscillation issue and achieved improved settling time compared with [23] and [24].

Fig. 18 shows the measured transient response tracking the reference voltage V_{REF} from 1.05 to 1.15 V in the case of dynamic voltage scaling (DVS). The settling time taken for tracking V_{REF} was less than 360 ns at V_{IN} of 1.2 V. The DLDO triggering is related to the gate voltage V_{ERR} of the APG and its upper bound V_{HIGH} and lower bound V_{LOW} ; however, it is independent of the V_{REF} value. For the other works [20], [22] that have a multi-bit reference voltage to control their DLDOs, it is difficult to quickly track the V_{REF} change because the multi-bit reference voltage should also be adjusted accordingly. In contrast, the DLDO in the proposed HLDO is triggered when V_{ERR} moves out of its upper bound V_{HIGH} and lower bound V_{LOW} , regardless of the V_{REF} value itself. Therefore, the DLDO can directly respond to V_{REF} variation and track V_{REF} change for DVS.

Fig. 19 shows the measured regulation error $|V_{OUT} - V_{REF}|$ versus the lower bound voltage V_{LOW} for the BRC scheme at different V_{DO} values. In the case of an undershoot event, the regulation accuracy is mainly determined by V_{LOW} . For an ultralow V_{DO} of 20 mV and a 50-mA load, as shown in Fig. 19(a), V_{LOW} higher than 0.4 V enabled accurate regulation with an error less than 2 mV. With a 50-mV V_{DO} and a 200-mA load, as shown in Fig. 19(b), V_{LOW} higher than 0.25 V guaranteed a regulation error less than 2 mV. This implies that the BRC scheme enables accurate regulation independent of the V_{LOW} variation if V_{LOW} is set higher than certain threshold values such as 0.2 V for a 20-mV dropout and 0.4 V for a 50-mV dropout. Furthermore, we can set V_{LOW} in accordance with the V_{IN} level, indicating that the BRC scheme can be

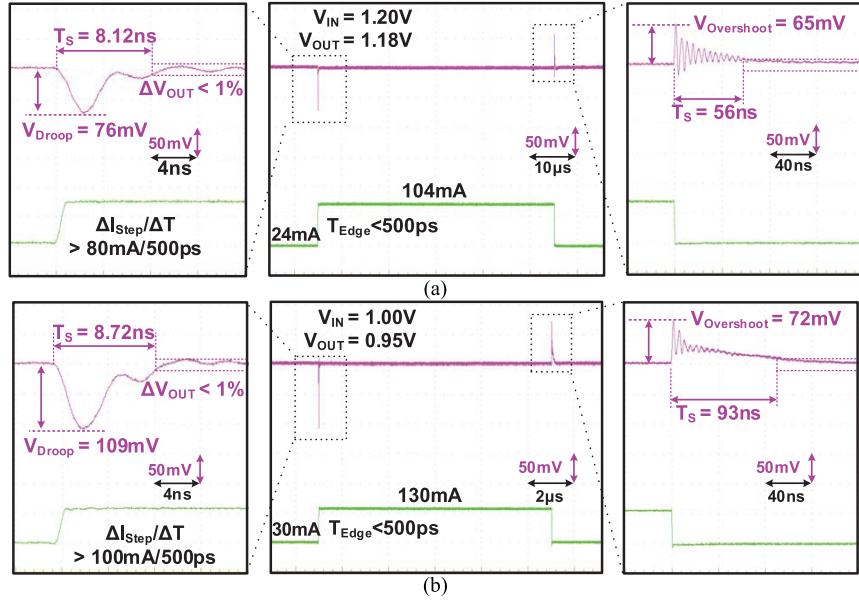


Fig. 16. Measured load transient responses with V_{IN} of (a) 1.2 V and (b) 1 V.

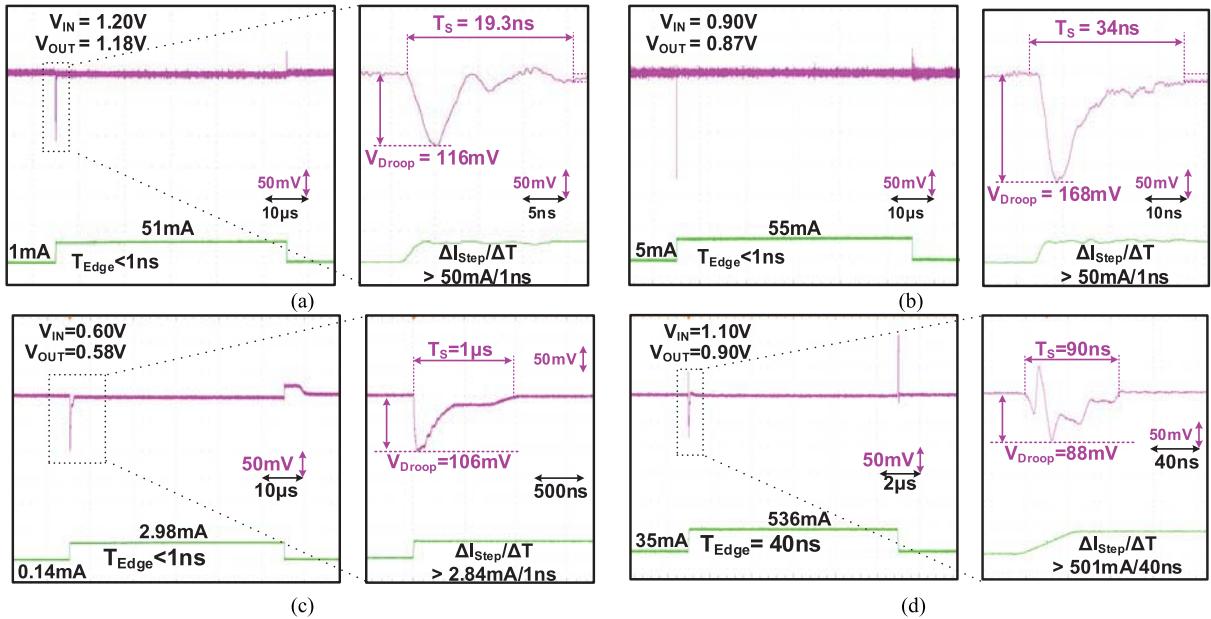
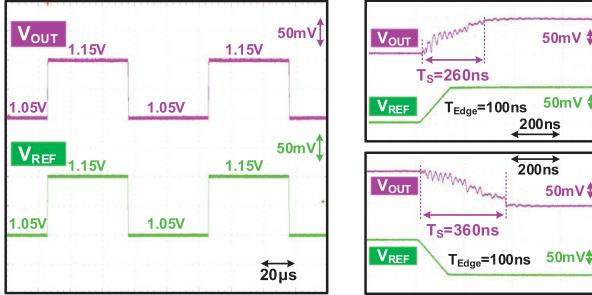
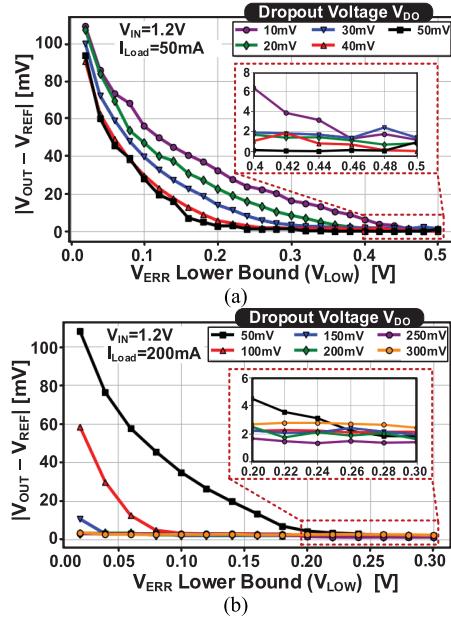
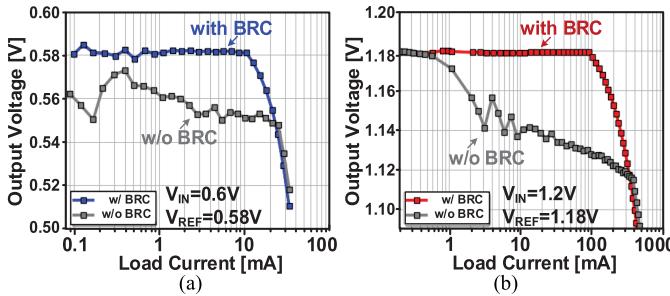


Fig. 17. Measured load transient responses with 50-mA current step (a) starting from 1 mA at V_{IN} of 1.2 V and (b) starting from 5 mA at V_{IN} of 0.9 V. Measured load transient responses (c) at low V_{IN} of 0.6 V and (d) with heavy load current step of 501 mA at V_{DO} of 200 mV and edge time of 40 ns.

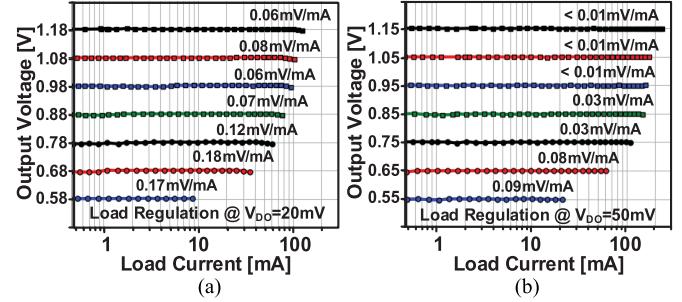
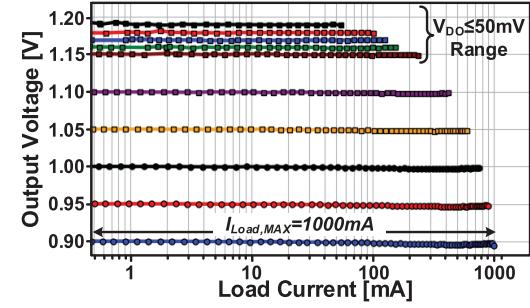
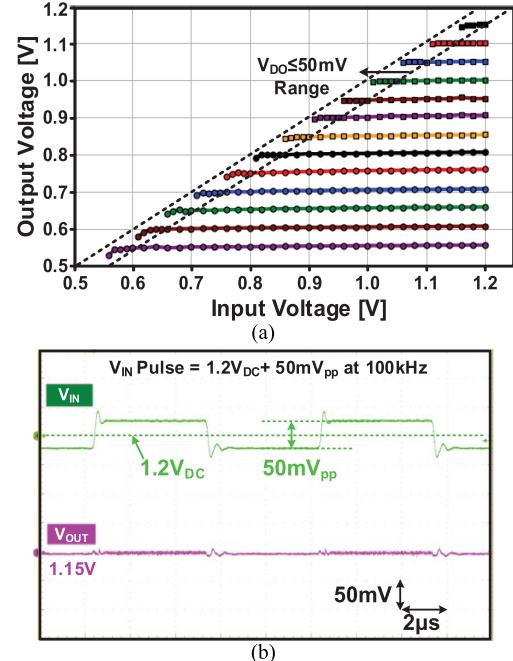
utilized at a low V_{IN} as well. Fig. 20 shows the measured load regulation with V_{DO} of 20 mV at V_{IN} of 0.6 and 1.2 V. Upon adopting the BRC scheme, the HLDO can improve the regulation accuracy regardless of the V_{IN} range even with an ultralow V_{DO} of 20 mV. Fig. 21 shows the measured load regulation within the V_{IN} range of 0.6–1.2 V. When V_{DO} was 20 mV, the HLDO achieved a load regulation of less than 0.2 mV/mA. When V_{DO} was 50 mV, the HLDO achieved the best load regulation of less than 0.01 mV/mA at V_{IN} above 1 V, demonstrating a superior load regulation compared to [23]. Fig. 22 shows the measured load regulation at V_{IN} of 1.2 V with V_{DO} range of 10–300 mV. With V_{DO} of 50 mV,

the HLDO can supply a load current up to 250 mA. With V_{DO} of 200 and 300 mV, the load current capability of the HLDO can be increased to 800 mA and 1 A, respectively. Therefore, the HLDO can be deployed in modern SoCs having various load current and dropout voltage requirements. For instance, the HLDO can replace a heavy-load analog LDO like [32] with a better transient response improved by the RLL and BRC schemes. Fig. 23(a) shows the measured line regulation within the V_{IN} range of 0.6–1.2 V, demonstrating the wide operating range of the HLDO. Fig. 23(b) shows the measured transient response when V_{IN} is scaled dynamically. The HLDO steadily maintains the output voltage despite the

Fig. 18. Measured transient response tracking stepped variation of V_{REF} .Fig. 19. Measured regulation error versus lower bound voltage V_{LOW} for BRC with respect to dropout voltage V_{DO} . (a) V_{DO} of 10–50 mV at I_{Load} of 50 mA. (b) V_{DO} of 50–300 mV at I_{Load} of 200 mA.Fig. 20. Measured load regulations depending on BRC with V_{DO} of 20 mV at V_{IN} of (a) 0.6 V and (b) 1.2 V.

dynamic scaling of V_{IN} . Fig. 24 shows the measured current efficiency of the HLDO when V_{DO} is 50 mV. Within the V_{IN} range of 0.6–1.2 V, the HLDO provided a peak current efficiency exceeding 99.93%.

Fig. 25(a) shows the measured V_{IN} ripple rejection at ripple frequencies of 100 kHz and 1 MHz. At V_{IN} of 1.2 V with V_{DO} of 50 mV, a 55-mV_{pp} ripple was injected into V_{IN} when the load current was 75 mA. The HLDO achieved rejected output

Fig. 21. Measured load regulations with V_{DO} of (a) 20 mV and (b) 50 mV.Fig. 22. Measured load regulation versus V_{DO} of 10–300 mV at 1.2-V V_{IN} .Fig. 23. Measured (a) line regulation and (b) transient response to dynamic voltage scaling of V_{IN} .

ripples of less than 3 and 7 mV_{pp} at 100 kHz and 1 MHz, respectively, even though the 55-mV_{pp} ripple injection reduced V_{DO} below 25 mV. Although prior HLDOs [20], [23], [24] that operate under V_{DO} larger than or equal to 150 mV show a good PSR of up to –43, –30, and –42 dB, respectively, the HLDO achieved ripple rejection under the lowest V_{DO} of 50 mV. To evaluate the PSR performance under a constant V_{DO} , a small-signal ripple was injected into V_{IN} , and the output

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	VLSI'18 [15]	ISSCC'20 [13]	JSSC'20 [26]	JSSC'21 [24]	JSSC'21 [23]	This Work	
Process [nm]	65	28	65	14	65	65	
Architecture	Digital (ED)	Digital (ED)	Hybrid (ED-CP)	Hybrid (ED, Modular)	Hybrid (DA)	Hybrid (ED)	
Clock-Free Operation?	Yes	Yes	No (1MHz)	Yes	No	Yes	
Need Multi-Bit $V_{REF}[N:0]$?	Yes	No	No	No	No	No	
V_{IN} [V]	0.5 – 1	0.5 – 1	0.5 – 1	1 – 1.2	1.2	0.6 – 1.2	
V_{OUT} [V]	0.45 – 0.95	0.45 – 0.95	0.45 – 0.95	0.7 – 0.85	0.6 – 1.15	0.55 – 1.18	
Min. Dropout V_{DO} [mV]	50	50	50	150	50	20	
C_{OUT} / C_{TOTAL} [pF]	100/100	0/4.11 (Cap-free)	0/42 (Cap-free)	4000/4000	250/250	100/120	
Max. I_{LOAD} [mA]	18.5	480	105	530	500	250	
I_Q [μ A]	18.1	7.7 – 241	4.9	31.1 – 53.5	120	15.4 – 152	
Load Regulation [mV/mA] @ V_{DO}, V_{IN}	0.16 @ $V_{DO}=50$ mV, $V_{IN}=1$ V	-	0.09 @ $V_{DO}=50$ mV, $V_{IN}=0.6$ V	0.009 @ $V_{DO}=200$ mV, $V_{IN}=1.05$ V	0.03 @ $V_{DO}=200$ mV, $V_{IN}=1.2$ V	0.06 @ $V_{DO}=20$ mV, $V_{IN}=1.2$ V <0.01 @ $V_{DO}=50$ mV, $V_{IN}=1.2$ V	
Voltage Droop [mV] @ $\Delta I_{Step} / T_{Edge}$ (Current Step: $I_{Step,min} \rightarrow I_{Step,max}$)	49.8 @ 2.3mA/0.1ns (0.07mA → 2.37mA)	112 @ 430mA/2ns (20mA → 450mA)	185 @ 100mA/1ns (5mA → 105mA)	133 @ 508mA/0.5ns (21mA → 530mA)	55 @ 450mA/100ns (50mA → 500mA)	76 @ 80mA/<0.5ns (24mA → 104mA)	116 @ 50mA/<1ns (1mA → 51mA)
Settling Time $T_{Settling}$ [ns] (Undershoot/Overshoot)	26.4 / NA	> 10* / 6000*	62 / 103*	> 300* / > 300*	174 / 220	8.2 / 56	19.3 / 35
¹ FOM ₁ [ps]	17.4	0.561	0.028	0.083	13.3	0.692	2.37
² FOM ₂ [ps]	1.22	11.22	0.14	1.74	665	16.6	2.37
³ FOM ₃ [ps]	14.5	112.1	15.2	662.2	2320	373.9	58.7
PSR [dB] @ V_{DO}, I_{LOAD}	-	-	-	-2 – -21 @ $V_{DO}=200$ mV, $I_{LOAD}=530$ mA	-2 – -21* (1MHz) @ $V_{DO}=200$ mV, $I_{LOAD}=1$ –200mA	-19 (1MHz) @ $V_{DO}=50$ mV, $I_{LOAD}=1$ –150mA	
⁺ Power Efficiency [%]	89.71	94.41	91.66	84.99	83.31	98.27	
Active Area [mm ²]	0.0057	0.049	0.04	0.262	0.36	0.079	

*Estimated from measurement result.

¹FOM₁ = ($C_{TOTAL} \cdot \Delta V_{OUT,Droop} + \Delta I_{Step}/(2 \cdot SR) \cdot (I_Q/\Delta I_{Step})$) [24]. Smaller FOM is better.

²FOM₂ = $\alpha \cdot FOM_1$, $\alpha = (I_{Step,Min}/1mA)$. Smaller FOM is better. ³FOM₃ = $\alpha \cdot T_{Settling,Uncertain} \cdot (I_Q/\Delta I_{Step})$, $\alpha = (I_{Step,Min}/1mA)$ [11][36]. Smaller FOM is better.

⁺Power Efficiency [%] = $(I_{LOAD} \cdot V_{OUT}) / ((I_{LOAD} + I_Q) \cdot V_{IN}) \cdot 100$.

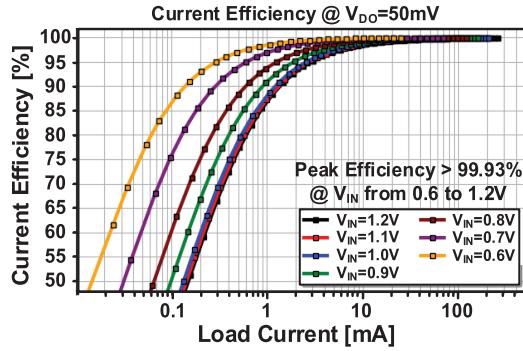


Fig. 24. Measured current efficiency at V_{DO} of 50 mV.

V_{OUT} was measured using a spectrum analyzer, as shown in Fig. 25(b). Fig. 25(c) shows the measured PSR at V_{IN} of 1.2 V and V_{DO} of 50 mV. At a ripple frequency lower than 1 MHz, the HLDO demonstrated a PSR of better than -19 dB.

Fig. 26 shows comparison of the FOM versus V_{DO} with the state-of-the-art works [7], [11]–[14], [16]–[21], [23], [24], [26]–[31], [33]. The FOM suggested in [24] is used to take the slew rate effect of di/dt into consideration. Many HLDOs and DLDOs were seen to achieve V_{DO} of 50 mV or lower with reasonable FOMs; by contrast, the ALDOs achieved V_{DO} of 100 mV or higher with relatively worse FOMs. Table I

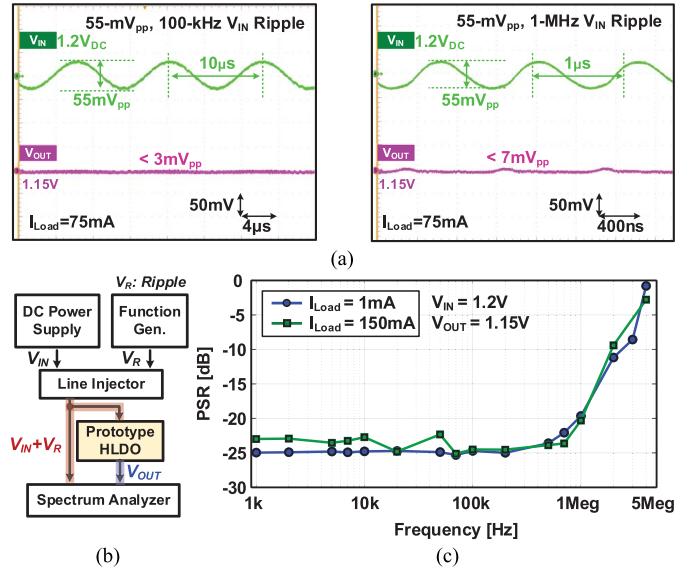


Fig. 25. (a) Measured V_{IN} ripple rejection at 100 kHz and 1 MHz. (b) PSR measurement setup. (c) Measured PSR.

shows the detailed performance comparison. The proposed HLDO achieved clock-free operation and an ultralow dropout as low as 20 mV, showing excellent load regulation of 0.06 and less than 0.01 mV/mA with V_{DO} of 20 and 50 mV, respectively,

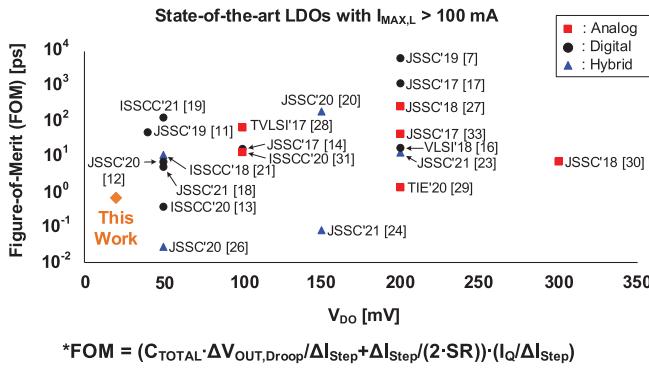


Fig. 26. Figure-of-merit comparison.

at V_{IN} of 1.2 V. Furthermore, the HLDO demonstrated a fast transient response with a settling time below 10 ns. The HLDO maintained a PSR of -19 dB at 1 MHz even with V_{DO} of 50 mV. Finally, the HLDO achieved a power efficiency of 98.27% owing to V_{DO} of 20 mV, outperforming other state-of-the-art LDOs.

V. CONCLUSION

This article proposed a fully integrated HLDO that supports an ultralow dropout voltage with a highly improved transient response. The measurement results demonstrated that this HLDO realizes sub-50-mV dropout regulation by using the RLDO with the BRC scheme based on the RLL in collaboration with the DLDO. The RLDO also compensated for the residual CQE of the DLDO, thus eliminating LCO and improving PSR compared to standalone DLDOs. Furthermore, by utilizing the FVF-based RLDO with the droop injection scheme for promptly triggering the DLDO, the proposed HLDO achieved a settling time below 10 ns against a steep load change of 100 mA/0.5 ps owing to the asynchronous digital control of the PoSRs. Although this article mainly focuses on the LDO design with ultralow dropout, generating a reliable reference voltage is also critical to sustain the merit of the ultralow dropout design.

ACKNOWLEDGMENT

The EDA tool was supported by the IC Design Education Center (IDEC), South Korea.

REFERENCES

- J. Myers *et al.*, “A 12.4pJ/cycle sub-threshold, 16pJ/cycle near-threshold ARM Cortex-M0+MCU with autonomous SRPG/DVFS and temperature tracking clocks,” in *Proc. IEEE VLSI Circuits Symp.*, Jun. 2017, pp. C332–C333.
- S. T. Kim *et al.*, “Enabling wide autonomous DVFS in a 22 nm graphics execution core using a digitally controlled fully integrated voltage regulator,” *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 18–30, Jan. 2016.
- P. Y. Or and K. N. Leung, “An output-capacitorless low-dropout regulator with direct voltage-spike detection,” *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 458–466, Feb. 2010.
- C.-J. Park, M. Onabajo, and J. Silva-Martinez, “External capacitor-less low drop-out regulator with 25 dB superior power supply rejection in the 0.4–4 MHz range,” *IEEE J. Solid-State Circuits*, vol. 49, no. 2, pp. 486–501, Feb. 2014.
- S.-W. Hong and G.-H. Cho, “High-gain wide-bandwidth capacitor-less low-dropout regulator (LDO) for mobile applications utilizing frequency response of multiple feedback loops,” *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 1, pp. 46–57, Jan. 2016.
- S. Gangopadhyay, D. Somasekhar, J. W. Tschanz, and A. Raychowdhury, “A 32 nm embedded, fully-digital, phase-locked low dropout regulator for fine grained power management in digital circuits,” *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2684–2693, Nov. 2014.
- S. Kundu, M. Liu, S.-J. Wen, R. Wong, and C. H. Kim, “A fully integrated digital LDO with built-in adaptive sampling and active voltage positioning using a beat-frequency quantizer,” *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 109–120, Jan. 2019.
- M. Huang, Y. Lu, S.-W. Sin, U. Seng-Pan, and R. P. Martins, “A fully integrated digital LDO with coarse–fine-tuning and burst-mode operation,” *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 7, pp. 683–687, Jul. 2016.
- L. G. Salem, J. Warchall, and P. P. Mercier, “A successive approximation recursive digital low-dropout voltage regulator with PD compensation and sub-LSB duty control,” *IEEE J. Solid-State Circuits*, vol. 53, no. 1, pp. 35–49, Jan. 2018.
- Y. H. Lee *et al.*, “A low quiescent current asynchronous digital-LDO with PLL-modulated fast-DVS power management in 40 nm SoC for MIPS performance improvement,” *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1018–1030, Apr. 2013.
- M. A. Akram, W. Hong, and I. Hwang, “Capacitorless self-coded all-digital low-dropout regulator,” *IEEE J. Solid-State Circuits*, vol. 54, no. 1, pp. 266–276, Jan. 2019.
- K. Z. Ahmed *et al.*, “A variation-adaptive integrated computational digital LDO in 22-nm CMOS with fast transient response,” *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 977–987, Apr. 2020.
- J. Oh, J.-E. Park, Y.-H. Hwang, and D.-K. Jeong, “25.2 A 480 mA output-capacitor-free synthesizable digital LDO using CMP-triggered oscillator and droop detector with 99.99% current efficiency, 1.3ns response time, and 9.8A/mm² current density,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 382–384.
- F. Yang and P. K. T. Mok, “A nanosecond-transient fine-grained digital LDO with multi-step switching scheme and asynchronous adaptive pipeline control,” *IEEE J. Solid-State Circuits*, vol. 52, no. 9, pp. 2463–2474, Sep. 2017.
- D. Kim, S. Kim, M. Seok, H. Ham, and J. Kim, “0.5 V-VIN, 165-mA/mm² fully-integrated digital LDO based on event-driven self-triggering control,” in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018, pp. C109–C110.
- J.-E. Park and D.-K. Jeong, “A fully integrated 700 mA event-driven digital low-dropout regulator with residue-tracking loop for fine-grained power management unit,” in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2018, pp. C231–C232.
- Y.-J. Lee *et al.*, “A 200-mA digital low drop-out regulator with coarse-fine dual loop in mobile application processor,” *IEEE J. Solid-State Circuits*, vol. 52, no. 1, pp. 64–76, Jan. 2017.
- S. J. Kim *et al.*, “0.5-1-V, 90–400-mA, modular, distributed, 3 × 3 digital LDOs based on event-driven control and domino sampling and regulation,” *IEEE J. Solid-State Circuits*, vol. 56, no. 9, pp. 2781–2794, Sep. 2021.
- D.-H. Jung *et al.*, “29.6 A distributed digital LDO with time-multiplexing calibration loop achieving 40A/mm² current density and 1 mA-to-6.4A ultra-wide load range in 5nm FinFET CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2021, pp. 414–416.
- D. Zhou, J. Jiang, Q. Liu, E. G. Soenen, M. Kinyua, and J. Silva-Martinez, “A 245-mA digitally assisted dual-loop low-dropout regulator,” *IEEE J. Solid-State Circuits*, vol. 55, no. 8, pp. 2140–2150, Aug. 2020.
- Y. Lu, F. Yang, F. Chen, and P. K. T. Mok, “A 500 mA analog-assisted digital-LDO-based on-chip distributed power delivery grid with cooperative regulation and IR-drop reduction in 65nm CMOS,” in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 310–312.
- M. Huang, Y. Lu, and R. P. Martins, “An analog-proportional digital-integral multiloop digital LDO with PSR improvement and LCO reduction,” *IEEE J. Solid-State Circuits*, vol. 55, no. 6, pp. 1637–1650, Jun. 2020.
- F. Chen, Y. Lu, and P. K. T. Mok, “A fast-transient 500-mA digitally assisted analog LDO with 30- μ V/mA load regulation and 0.0073-ps FOM in 65-nm CMOS,” *IEEE J. Solid-State Circuits*, vol. 56, no. 2, pp. 511–520, Feb. 2021.

- [24] X. Liu *et al.*, "A universal modular hybrid LDO with fast load transient response and programmable PSRR in 14-nm CMOS featuring dynamic clamp strength tuning," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2402–2415, Aug. 2021.
- [25] X. Ma, Y. Lu, R. P. Martins, and Q. Li, "A 0.4 V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 306–308.
- [26] X. Wang and P. P. Mercier, "A dynamically high-impedance charge-pump-based LDO with digital-LDO-like properties achieving a sub-4-fs FOM," *IEEE J. Solid-State Circuits*, vol. 55, no. 4, pp. 977–987, Apr. 2020.
- [27] J. Jiang, W. Shu, and J. S. Chang, "A 65-nm CMOS low dropout regulator featuring >60-dB PSRR over 10-MHz frequency range and 100-mA load current range," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2331–2342, Aug. 2018.
- [28] Y. Lim *et al.*, "An external capacitor-less ultralow-dropout regulator using a loop-gain stabilizing technique for high power-supply rejection over a wide range of load current," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 25, no. 11, pp. 3006–3018, Nov. 2017.
- [29] J. Park, B. Lee, and S.-W. Hong, "An output capacitorless low-dropout regulator with a low-VDD inverting buffer for the mobile application," *IEEE Trans. Ind. Electron.*, vol. 67, no. 10, pp. 8931–8935, Oct. 2020.
- [30] R. Magod, B. Bakkaloglu, and S. Manandhar, "A $1.24\ \mu$ A quiescent current NMOS low dropout regulator with integrated low-power oscillator-driven charge-pump and switched-capacitor pole tracking compensation," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2356–2367, Aug. 2018.
- [31] J.-E. Park, J. Hwang, J. Oh, and D.-K. Jeong, "32.4 A 0.4-to-1.2 V 0.0057 mm^2 55fs-transient-FoM ring-amplifier-based low-dropout regulator with replica-based PSR enhancement," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2020, pp. 492–494.
- [32] W. Xu, P. Upadhyaya, X. Wang, R. Tsang, and L. Lin, "5.10 A 1A LDO regulator driven by a 0.0013 mm^2 class-D controller," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 104–106.
- [33] Q.-H. Duong *et al.*, "Multiple-loop design technique for high-performance low-dropout regulator," *IEEE J. Solid-State Circuits*, vol. 52, no. 10, pp. 2533–2549, Oct. 2017.
- [34] S. Li and B. H. Calhoun, "14.6 A 745pA hybrid asynchronous binary-searching and synchronous linear-searching digital LDO with 3.8×10^5 dynamic load range, 99.99% current efficiency, and 2 mV output voltage ripple," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2019, pp. 232–234.
- [35] S. S. Kudva, S. Song, J. Poulton, J. Wilson, W. Zhao, and C. T. Gray, "A switching linear regulator based on a fast-self-clocked comparator with very low probability of meta-stability and a parallel analog ripple control module," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Apr. 2018, pp. 1–4.
- [36] Y. Song, J. Oh, S.-Y. Cho, D.-K. Jeong, and J.-E. Park, "A fast droop-recovery event-driven digital LDO with adaptive linear/binary two-step search for voltage regulation in advanced memory," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1189–1194, Feb. 2022.



Young-Ha Hwang (Member, IEEE) received the B.S. (*summa cum laude*) and Ph.D. degrees in electrical and computer engineering from Seoul National University, Seoul, South Korea, in 2014 and 2019, respectively.

In 2019, he was with the Inter-University Semiconductor Research Center, Seoul National University, as a Post-Doctoral Researcher. Since 2020, he has been working as a Post-Doctoral Fellow at Harvard University, Cambridge, MA, USA. His research interests include designing sensor interfaces, data converters, and low-dropout regulators.

Dr. Hwang received the Special Award at the IC Design Education Center Chip Design Contest, International SoC Design Conference, in 2017. He was a co-recipient of the Bronze Prize of HumanTech Paper Award from Samsung Electronics in 2016.



Jonghyun Oh (Member, IEEE) received the B.S. and Ph.D. degrees in electrical and computer engineering from Seoul National University, Seoul, South Korea, in 2015 and 2021, respectively.

In 2021, he was a Post-Doctoral Researcher with the Inter-University Semiconductor Research Center, Seoul National University. Since September 2021, he has been a Post-Doctoral Research Scientist at Columbia University, New York, NY, USA. His main research interests include high-speed interfaces, integrated voltage regulators, synthesizable systems, and neuromorphic hardware design.



Woo-Seok Choi (Member, IEEE) received the B.S. and M.S. degrees in electrical engineering and computer science from Seoul National University, Seoul, South Korea, in 2008 and 2010, respectively, and the Ph.D. degree in electrical and computer engineering from the University of Illinois at Urbana-Champaign, Champaign, IL, USA, in 2017.

From 2018 to 2019, he was a Post-Doctoral Fellow at Harvard University, Cambridge, MA, USA. He is currently an Assistant Professor with the Department of Electrical and Computer Engineering, Seoul National University. His research interests include designing energy-efficient integrated circuits and algorithm/hardware co-design for machine learning applications.

Dr. Choi was a recipient of the IEEE SSCS Predoctoral Achievement Award (2016–2017), the Analog Devices Outstanding Student Designer Award in 2016, and the Provost's Distinguished Graduate Fellowship from Oregon State University (2011–2012). He has served as a Reviewer for various journals, including IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS, and IEEE TRANSACTIONS ON SIGNAL PROCESSING.



Deog-Kyoon Jeong (Fellow, IEEE) received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, South Korea, in 1981 and 1984, respectively, and the Ph.D. degree in electrical engineering and computer sciences from the University of California at Berkeley, Berkeley, CA, USA, in 1989.

From 1989 to 1991, he was with Texas Instruments, Dallas, TX, USA, as a member of the Technical Staff and worked on the modeling and design of BiCMOS gates and the single-chip implementation of the SPARC architecture. Then, he joined the faculty of the Department of Electronics Engineering and the Inter-University Semiconductor Research Center, Seoul National University, where he is currently a Professor. He was one of the cofounders of Silicon Image (now Lattice Semiconductor), Sunnyvale, CA, which specialized in digital interface circuits for video displays, such as DVI and HDMI. His main research interests include the design of high-speed I/O circuits, phase-locked loops, and memory system architecture.

Dr. Jeong was a recipient of the ISSCC Takuo Sugano Award for Outstanding Far-East Paper in 2005.



Jun-Eun Park (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering and computer science from Seoul National University, Seoul, South Korea, in 2011, 2013, and 2017, respectively.

In 2017, he was with the Inter-University Semiconductor Research Center, Seoul National University, as a Post-Doctoral Research Fellow. From 2018 to 2020, he was a BK Assistant Professor at the BK21+ Creative Research Engineer Development for IT, Seoul National University. In 2020, he joined the Department of Electronics Engineering, Chungnam National University, Daejeon, South Korea, where he is currently an Assistant Professor. His research interests include the design of digital low-dropout regulators, sensor interfaces, energy-efficient DNN accelerators, low-power analog-to-digital converters, and design automation of mixed-signal circuits.

Dr. Park was a recipient of the Distinguished M.S. Degree Dissertation Award from the Department of Electrical Engineering and Computer Science, Seoul National University, in 2013; the Doyeon Paper Award from Inter-University Semiconductor Research Center, Seoul National University, in 2016; and the Bronze Prize of HumanTech Paper Award from Samsung Electronics in 2016.