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# A Capacitor-Free Fast-Transient-Response LDO with Dual-Loop Controlled Paths

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***Abstract* — *A capacitor-free fast-transient-response low-dropout voltage regulator (LDO) with dual-loop controlled paths is presented in this paper. This technique can make the transient response to be faster than other LDOs with traditional controlled loop. Especially, the performance of settling time of proposed LDO is excellent without off-chip capacitors. With 1.5V power supply voltage, the output voltage is designed as 1.2V. The prototype of the LDO is fabricated with TSMC 0.35-μm DPQM CMOS processes. The active area is only 360μm x345μm.***

Index Terms: voltage regulator; low dropout voltage regulator; transient response

## I. INTRODUCTION

The power management IC is more and more important in the consumer electronics. Most of proposed LDOs are usually used to isolate the noise from power supply. Since the SoC products are more and more popular recently, it is difficult for integrating analog circuits and digital circuits into a single chip. From the aspect of noise, the digital circuits will generate power bounces [1-4], and transmit noise to the power supply of the analog circuits. Finally, the power bounce influences the performance of analog circuits. Moreover, when the loading current of microprocessor is greater, it responses dynamic voltage dip due to loading variation. Hence, the current would vary severely, and make output voltage to be changed quickly. The power IC must response the loading variation immediately to maintain original output voltage level. Furthermore, the power supply usually has the other noise.

There is another reason which exists in the conscientious circuit for choosing correct power management IC. Indeed, the power supply influences the intensity of the analog signal, and affects the entire system performance finally. The simple way to upgrade the signal-path performance is finding the correct power supply. The important parameter of the signal intensity is the ripple of the power line. The ripple of power supply could couple with the output of the operational amplifier, phase lock loop, voltage-controlled oscillator, or degrade the signal to noise ratio (SNR) of ADC, so the LDO is a better choice which compare with switching-mode power supply. Based on the reasons of above all, the LDO is needed to implement for high-speed application.

In LDO design, there is huge parasitic capacitor existing in the gate terminal of the power transistor. That often makes the unity-gain frequency and slew-rate at the gate drive of the LDO cut down in the low power dissipation condition. To solve this problem, a voltage buffer could be inserted between power transistor and error amplifier, usually. In our structure, we added the operational trans-impendence amplifier in the LDO, and added extra feedback path in the operational trans-impendence amplifier to increase the transient response and make the pole in the gate terminal of the power transistor to be far away. There is another problem of the transditional LDO is the stability. In the transditional LDO, the error amplifier is usually used to improve line and load regulation. If the error amplifier is cascaded the power transistor, the number of the poles is increasing one. O the other hand, the LDO added the off-chip capacitor in the output [5-7]. Because it has the equivalent series resistance (ESR), it could produce a negative zero for stable operation. In our proposed circuit, we have no off-chip capacitor to enhance stability. In this paper, a description of proposed LDO and the simulation results will be included in section II, and the experimental results of proposed LDO are shown in section III. Finally, the conclusion is made in section IV.

## II. CIRCUIT DESCRIPTIONS

The building block of proposed LDO is shown in figure 1. It includes an operational trans-conductor amplifier, an operational trans-impedence amplifier, a current sensing circuit, and a power transistor. From figure 1, there are dual control loops, which are voltage control loop and current control loop separately, in this circuit.

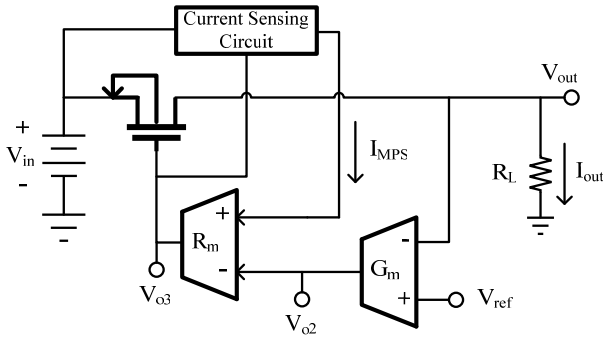


**Figure 1 the building block of proposed LDO**

The voltage control loop is the general case in the LDO. The output voltage is sent into the trans-conductor stage ($G_m$) and compared with reference voltage $V_{ref}$. After that, the output current of the trans-conductor stage and sensing current are connected to the trans-impedence stage. Finally, we complete a closed-loop motion through power transistor. Besides, the feedback path of the current control loop is shorter than voltage control loop, so its transient response is more superior than conventional one, and the feedback current $I_{MPS}$ is proportional to the output current $I_{out}$ for a ratio K, in our circuit, the ratio K is about 2000.

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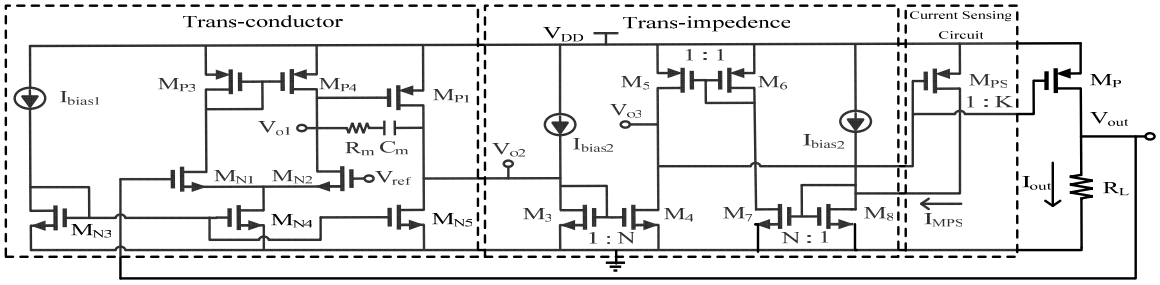



**Figure 2 the circuit of the proposed LDO**

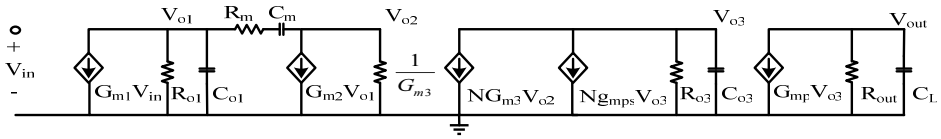



**Figure 3 the small-signal model of proposed LDO**

$$T(s) = A_{OL} \cdot \frac{1}{1+sR_{out}C_L} \cdot \frac{1}{1+\frac{sC_{o3}R_{o3}}{1+Ng_{mps}R_{o3}}} \cdot \frac{sC_m(R_m - \frac{1}{G_{m2}})+1}{s^2C_{o1}R_{o1}C_m(R_m+\frac{1}{G_{m3}})+s\{[(1+\frac{G_{m2}}{G_{m3}})R_{o1}+\frac{1}{G_{m3}}+R_m]C_m+C_{o1}R_{o1}\}+1} \quad (1)$$

$$A_{OL} = \frac{\frac{G_{m2}}{G_{m3}}G_{m1}R_{o1}NG_{m3}R_{o3}G_{mp}R_{out}}{1+Ng_{mps}R_{o3}} \quad (2)$$

The circuit of proposed LDO is shown in figure 2. The first stage is the trans-conductor stage, and it could compare $V_{ref}$ and $V_{out}$. $M_3$~$M_4$ are the current amplifier. It amplifies the current signal for a ratio N, and $M_{PS}$ is current sensing transistor. It senses the current of the power transistor, and feedback to the second stage. Besides, it also amplifies the feedback signal for a ratio N by $M_5$~$M_8$. The feedback signal and the differential input signal compare each other. Eventually, the result is shown in $V_{o3}$. When the output voltage is varying, the feedback signal $I_{MPS}$ has shorter path to revise the output voltage.

In the figure 3, it is the small-signal model for the open loop of proposed LDO. In the equation (1), it is the open loop gain totally, where $G_{m1}$ is the transconductance of the differential pair stage, $R_{o1}$ is the output resistance of the differential pair stage, $G_{m2}$ is the transconductor of $M_{P1}$, $G_{m3}$ is the transconductor of $M_3$, N is the amplification of current amplifier, $R_{o3}$ is the output resistance of the trans-impedence, $g_{mps}$ is the transconductance of $M_{PS}$, $G_{mp}$ is the transconductance of power transistor, $R_{out}$ is the output resistance at the terminal of the LDO, respectively. The $R_{out}$ is the $R_L$ and $r_{dsp}$ of the power transistor which are parallel. In this small-signal model, because $V_{o2}$ is a low impedance node and the equivalent parasitic capacitor is small, we ignore it to be a pole. The equation (2) is the dc gain of the open-loop transfer function, where $R_m$ is the compensated resistance, and $C_m$ is the compensated capacitor which is used to create a new dominant pole, respectively. The $R_m$ is used to compensate $\omega_z$, and it makes the positive zero to be the negative zero. Moreover, $R_m$ must be larger than $1/G_{m2}$. It is shown in the equation (3).

$$\omega_z = \left.\frac{1}{C_m(R_m - \frac{1}{G_{m2}})}\right|_{R_m \geq \frac{1}{G_{m2}}} \quad (3)$$

If $(1+G_{m2}/G_{m3})R_{o1} \fallingdotseq R_{o1} >> (R_m+1/G_{m3})$, $R_m >> 1/G_{m3}$, and $C_m >> C_{o1}$, the equation (1) could be simplified, and shown them in the equation (4).

$$T(s) \cong A_{OL} \cdot \frac{(1+\frac{s}{\omega_z})}{(1+\frac{s}{\omega_{p3}})\cdot(1+\frac{s}{\omega_{p4}})} \cdot \frac{1}{s^2C_{o1}R_{o1}C_mR_m+sR_{o1}C_m+1} \quad (4)$$

,where

$$\omega_{p3} = \frac{1+Ng_{mps}R_{o3}}{C_{o3}R_{o3}} \quad (5)$$

$$\omega_{p4} = \frac{1}{C_LR_{out}} \quad (6)$$

Since the N is a large number, the pole $\omega_{p3}$ is at high frequency. On the other hand, the LDO is capacitor-free, so the output capacitor is zero, and the pole $\omega_{p4}$ is aproaching infinity. If we want to solve the second-order equation in the equation (4), we assume this equation to be zero, as shown in the equation (7).

$$s^2 C_{o1} R_{o1} C_m R_m + s R_{o1} C_m + 1 = 0 \tag{7}$$

We could get two solutions, as shown in the equation (8).

$$s_{1,2} = \frac{-R_{o1}C_m \pm \sqrt{(R_{o1}C_m)^2 - 4C_{o1}R_{o1}C_m R_m}}{2C_{o1}R_{o1}C_m R_m} = \frac{-R_{o1}C_m[1 \pm \sqrt{1 - 4\frac{C_{o1}R_m}{R_{o1}C_m}}]}{2C_{o1}R_{o1}C_m R_m} = \frac{-[1 \pm \sqrt{1 - 4\frac{C_{o1}R_m}{R_{o1}C_m}}]}{2C_{o1}R_m} \tag{8}$$

Based on the previous assumptions ($C_m >> C_{o1}$ and $R_{o1} >> R_m$), we could simplify the equation (8) by using the Taylor series. The $(1-x)^m$ is almost 1-mx, if x is very small. Finally, we got last two poles, $\omega_{p3}$ and $\omega_{p4}$, described as the following equations.

$$s_{1,2} = \frac{-[1 \pm \sqrt{1 - 4\frac{C_{o1}R_m}{R_{o1}C_m}}]}{2C_{o1}R_m} \cong \frac{-[1 \pm (1 - 2\frac{C_{o1}R_m}{R_{o1}C_m})]}{2C_{o1}R_m} \cong \frac{-1}{C_{o1}R_m} or \frac{-1}{C_m R_{o1}} \tag{9}$$

$$\omega_{p1} = \frac{1}{C_m R_{o1}} \tag{10}$$

$$\omega_{p2} = \frac{1}{C_{o1}R_m} \tag{11}$$

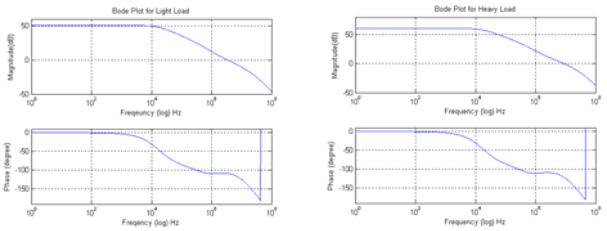
Eventually, the transfer function could be simplified and briefly described the positions of the poles and zero from equation (12) in the figure 3.

$$T(s) \cong A_{OL} \cdot \frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}}) \cdot (1 + \frac{s}{\omega_{p2}})} \tag{12}$$

The equation shows the one zero and two poles, so the phase margin almost achieves 90 degree, as shown in the figures 4(a) and (b). In the figures 4(a) and (b), we show the simulation results of the frequency response for light-loading and heavy-loading current. It display the unity-gain frequency is 2MHz for light-loading and 10MHz for heavy-loading.

## III. EXPERIMENTAL RESULTS

The capacitor-free fast-transient-response low-dropout voltage regulator with dual-loop controlled paths is fabricated with TSMC 0.35μm CMOS DPQM processes. The photography of the proposed LDO is shown in figure 6, and active area is 360μm x 345μm. The maximum output current of proposed LDO is designed as 120mA. All measured results are performed at room temperature.




(a) (b)

**Figure 4 the simulated results of proposed LDO with (a) light-loading current; (b) with 100mA loading current, from top to bottom, the waveforms are Magnitude Response, and Phase Response ( horizontal scale: log scale; vertical scale: 50dB/div, and 50 degree/div, from top to bottom.)**

In figures 6, we show the variation of the output voltage for different loading resistors, including 10ohm, and infinite resistors, and the measured results are 0.05%/V and 0.047%/V for line regulation. In the figure 7, the load regulation is shown for light to heavy loading, and the load regulation of measured results is 13.3ppm/mA. In the figures 8(a) and (b), the output voltage and current for the heavy load and light load are measured. Generally speaking, the transient response is very important in the LDO design, so we present the dynamic response for light to heavy and heavy to light loading in the figures 9(a) and (b). The settling time is only 200ns and 300ns for rising and falling load variation, respectively. The output noise of proposed LDO with light and heavy loading current is shown in figures 10(a) and (b). Finally, we summarize the specifications of LDO in Table I, and show the comparison with the pervious LDO in Table II.

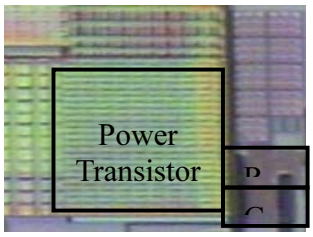
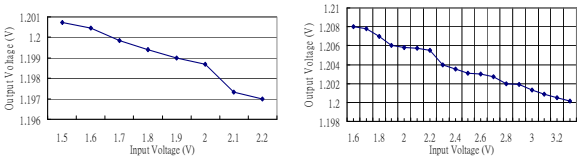



**Figure 5 the photography of proposed LDO**




(a) (b)

**Figure 6 the statistic results of line egulation for (a) $I_{out}$=120 mA and $R_L$=10 ohm; (b) $I_{out}$=0 mA and $R_L$=infinity.**

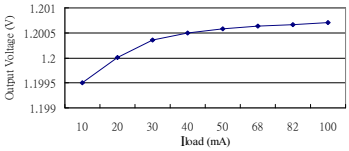
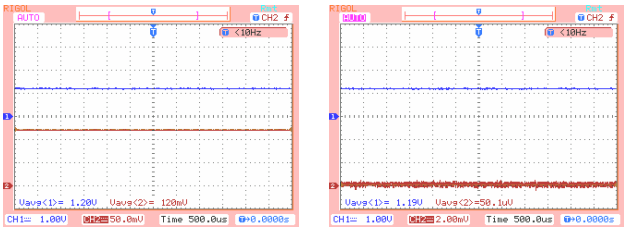



**Figure 7 the experimental results of load regulation for $V_{out}$=1.2 V and $V_{DD}$=1.5 V**



(a) (b)

**Figure 8 the experimental results of proposed LDO; from top to bottom, the waveforms are output voltage $V_{out}$, and output current $I_{out}$ with (a) heavy load( horizontal scale: 500μs/div; vertical scale: 1V/div, and 50mA/div, from top to bottom.); (b) light load ( horizontal scale: 500μs/div; vertical scale: 1V/div, and 2mA/div, from top to bottom.)**

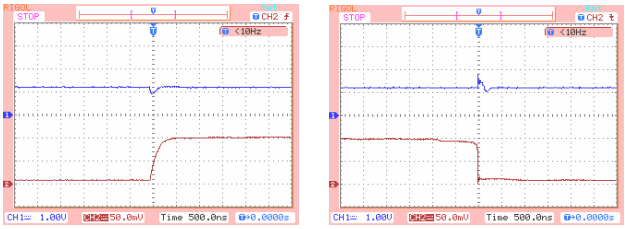
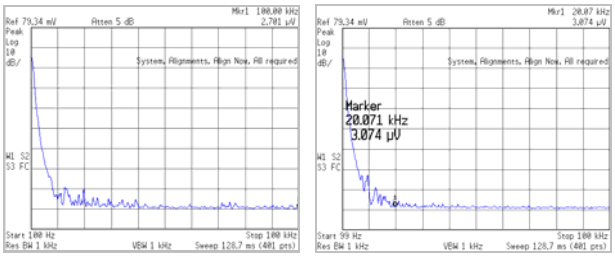


**Figure 9 the experimental results of proposed LDO; from top to bottom, the waveforms are output voltage $V_{out}$, and output current $I_{out}$ (a) from 100mA to 10mA. ( horizontal scale: 500ns/div; vertical scale: 1V/div, and 50mA/div, from top to bottom.) ; (b) from 10mA to 100mA. ( horizontal scale: 500ns/div; vertical scale: 1V/div, and 50mA/div, from top to bottom.)**




(a) (b)

**Figure 10 the experimental results of proposed LDO; (a) the waveforms is the noise density of the output with light loading current; (b) the waveforms is the noise density of the output with 100mA loading current**

**Table I**
**THE SPECIFICATION OF THE PROPOSED LDO**

| | | |
|---|---|---|
| Technology | | TSMC 0.35μm 2P4M |
| Input Voltage Range | | 1.5~4.5V |
| Maximum Power Consumption | | 180mW@ $V_{in}$=1.5V |
| Max Efficiency | | 80%@ $V_{in}$=1.5V & $I_{out}$=120mA |
| Output Voltage | | 1.2V |
| Operation Temperature | | -55℃~130℃ |
| Max Output Current | | 120mA |
| Active Area | | 360μm x 345μm |
| Output Spectral Noise Density | | 2.701μV/sqrt Hz @$I_{out}$=0mA<br>3.074μV/sqrt Hz @$I_{out}$=100mA |
| Load Regulation | | 13.3ppm / mA |
| Line Regulation | | 0.057% / V |
| Settling Time (0.5% error) | $I_{out}$= 100mA to 10mA | 200ns |
| | $I_{out}$= 10mA to 100mA | 300ns |

**Table II**
**PERFORMANCE COMPARISON WITH PREVIOUSLY PUBLISHED LOW-DROPOUT REGULATORS**

| Characteristics | 2004 [8] | 2005 [9] | 2006 [10] | This work |
|---|---|---|---|---|
| Technology | AMS 0.6μm CMOS | TSMC 0.35μm 2P4M | CSMC 0.5μm CMOS 2P2M | TSMC 0.35μm 2P4M |
| Input Voltage (V) | 1.5~4.5 | 2~5 | 1.8-6 | 1.5~4.5 |
| Output Voltage (V) | 1.3 | 1.8 | 1.2-3.5 | 1.2 |
| Max Output Current (mA) | 100 | 150 | 150 | 120 |
| Active Area (μm x μm) | 541 x 555 | 480 x 675 | 960 x 770 | 360 x 345 |
| Load Regulation ( ppm/mA ) | 85 | 56 | 93 | 13.3 |
| Line Regulation (%/V) | 0.123 | 0.127($I_{out}$=0mA)<br>0.165($I_{out}$=150mA) | 0.1 | 0.047 ($I_{out}$=0mA)<br>0.05($I_{out}$=120mA) |
| Settling Time (0.5% error) (light load to heavy load) | < 1μs | 4μs | - | 0.3μs |

## IV CONCLUSIONS

A capacitor-free fast-transient-response low-dropout voltage regulator with dual-loop controlled paths has been designed with TSMC 0.35μm DPQM CMOS processes. The proposed LDO has better dynamic response for the heavy to light loading and light to heavy loading and it provide the excellent settling time for SoC application. Because of its low power supply, it could be used in the portable device, too.

## ACKNOWLEDGEMENT

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