Auto Correction Feedback for Ripple Suppression in a Chopper Amplifier

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***Abstract*—This paper proposes a local feedback, named Auto Correction Feedback (ACFB), for a chopper amplifier to suppress its offset related ripple. It nulls out the amplifier's initial offset in DC domain which would otherwise become modulated ripple at the chopper amplifier's output, instead of filtering the ripple with a post filter. The proposed ACFB has been implemented as a stand alone chopper operational amplifier fabricated in 0.64 mm^2 die area with a 0.35 μm standard CMOS process. It achieves 10 μV maximum input offset voltage and 95 nV/rt(Hz) input voltage noise spectrum density flat down to 0.1 Hz, with a 1.8–5.5 V supply voltage range and 13 μA supply current dissipation. When configured in unity-gain, the typical magnitude of the input referred ripple at the chopping frequency is 9.4 μVrms, as a result of 45 dB ripple attenuation obtained by the ACFB. The analysis, the simulation, and the measurement prove there is no noise penalty due to the addition of ACFB.**

***Index Terms*—Chopper, CMOS operational amplifier, local feedback, low noise, low offset, low power dissipation, ripple suppression, switched capacitor filter.**

I. Introduction

AUTO-ZEROING and chopping are widely used for high precision CMOS amplifiers to achieve low offset, low offset drift, and low $1/f$ noise. They are suitable for a signal sensing application where errors at DC and low frequency are critical. Either topology can realize an operational amplifier with input referred offset voltage in the order of few micro-volt to few tens micro-volt. Furthermore it enables the use of standard inexpensive CMOS process without post trimming, making it cost competitive over trimmed low offset operational amplifiers made on bipolar process.

Unfortunately each topology has its drawback in return for eliminating the amplifier's initial offset. Auto-zeroing increases the noise density in the base band above its original thermal noise floor, due to aliasing of the broad band thermal noise introduced by offset sampling [1]. Chopping offers the same noise density in the base band as its original thermal noise floor, but it has offset related ripple as it modulates the initial offset up to its chopping frequency [1]. As another demand for operational amplifiers, low power dissipation is always desirable after achieving the required level of precision. Therefore, low supply voltage and low supply current dissipation make the operational amplifier more appealing.

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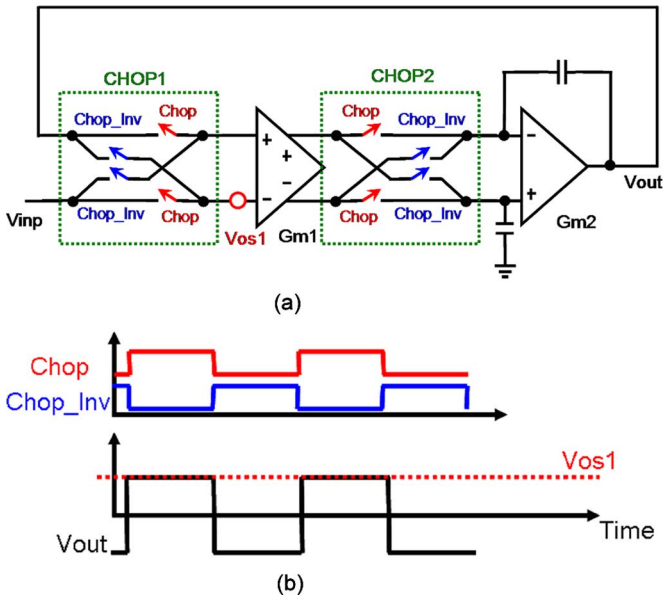

Fig. 1. Conventional chopper amplifier in (a) a unity gain buffer and (b) a timing diagram.

The original thermal noise floor in the amplifier would be primarily determined by the transconductance of the input device, with some contributions from load current sources. The transconductance is linearly scaled with the current dissipation by using the MOSFET in the weak inversion region, which is the best case [2]. Even so, lowering the thermal noise floor painfully increases the required current dissipation. The auto-zeroed amplifier, as stated, has increased noise density in the base band as its original thermal noise floor, while the chopper amplifier does not. For this reason, the auto-zeroed amplifier has to consume more supply current for the input devices, in order to achieve the same resulting noise density in the base band as the chopper amplifier [3]–[5]. It makes the chopping more attractive approach to optimize offset, noise, and power dissipation, if the magnitude of its modulated ripple is successfully reduced to acceptable levels.

II. Background

Fig. 1(a) shows a conventional two stage chopper amplifier put in a unity gain buffer. It consists of an input chopping (CHOP1), a first transconductance amplifier (G_{m1}), an output chopping (CHOP2), and a second transconductance amplifier (G_{m2}). The G_{m1} is chopped by CHOP1 and CHOP2 with a timing diagram shown in Fig. 1(b).

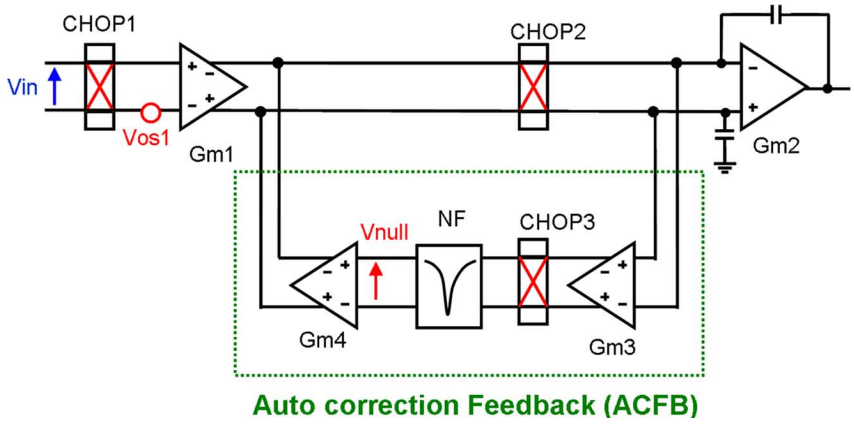

Fig. 2. Ripple suppression method with auto correction feedback.

If we had a desired input signal at the input ($V_{\rm inp}$), it is modulated by CHOP1 and then demodulated by CHOP2. The reconstructed desired signal appears at the output with no difference compared with a non-chopper amplifier.

Next we assume an unwanted initial input offset voltage ($V_{\rm os1}$) associated with G_{m1} to see how chopping works. The $V_{\rm os1}$ is modulated only by CHOP2 and appears at the output ($V_{\rm out}$) as the modulated ripple as shown in Fig. 1(b). Because of the feedback operation, the magnitude of the ripple in RMS value is the same as that of $V_{\rm os1}$, which could be about 10 mV with a typical CMOS process [5]. The ripple can be attenuated by an off chip post low pass filter at the cost of reducing the bandwidth available for the signal. Furthermore, it requires additional components, area for its implementation, and cost.

There have been many papers reported that show on-chip ripple reduction techniques. One method is to employ both autozeroing and chopping [6]. The drawback for this topology is that there're two input stages required with ping-pong operation to use it in a continuous time appreciation, requiring more power and chip area for the input stages. Another method is to employ a switched-capacitor filter in its signal path to filter the ripple out [3], [4], [7], [8]. However, having the sampling circuit in the signal path still introduces the noise penalty due to aliasing, and requires complicated design for compensation network [5]. Moreover it relies on the accuracy of the clock and the capacitor's matching in the notch filter, in order to achieve the required filter characteristics. More recently, instrumentation amplifiers employing AC-coupled ripple reduction loop have been reported [5], [9]. It senses the modulated ripple at its output, and forms a local feedback loop to null out the initial offset. Though this method is good for instrumentation amplifiers, additional considerations and difficulties come up to use this method for the stand alone operational amplifiers, which can be used wide range of output load and of closed-loop gain.

III. Proposed Ripple Suppression Method

A. Approach

From the observation in the previous section, the ripple occurs as the initial offset associated with G_{m1}. We propose to null the initial offset of G_{m1} out before it is modulated by CHOP2, instead of filtering the modulated ripple out by a post filter.

B. Auto Correction Feedback

The proposed method is shown in Fig. 2. In addition to the conventional two stage chopper amplifier, it has a local feedback named Auto Correction Feedback (ACFB). The ACFB tries to eliminate the initial offset of G_{m1} ($V_{\rm os1}$) in the following way. A third transconductance amplifier (G_{m3}), coupled to the output of CHOP2, would sense the modulated ripple. The sensed component is demodulated down to DC by a third chopping (CHOP3), which operates with the same clock as the CHOP2. The demodulated DC component passes a switched capacitor notch filter (NF) and creates a null voltage ($V_{\rm null}$) at the output of NF. It forms a feedback through a fourth transconductance amplifier (G_{m4}), coupled to the output of G_{m1}. By the feedback operation, any DC offset current from G_{m1} is nulled out by G_{m4}, which would otherwise appear as ripple at the output of CHOP2 and at the output of G_{m2}. The null voltage is then proportional to the initial offset voltage such that $V_{\rm null} = (G_{m4}/G_{m1}) * V_{\rm os1}$. Because this method senses the modulated ripple at the input of G_{m2} instead of the output of amplifier, the characteristics such as the loop gain of ACFB is independent of the output load or the closed-loop gain for the amplifier. It makes this method applicable to a stand alone operational amplifier.

C. Signal Selection by Notch Filter

The NF has a function to selectively suppress the undesired offset related ripple, without disturbing a desired input signal from overall input. Here we assume the desired DC input signal ($V_{\rm in}$) at the overall input terminal in Fig. 2. This causes a DC signal at the input of Gm3, unlike the modulated ripple which was the case with the undesired $V_{\rm os1}$. Then the DC signal is modulated by CHOP3 and is filtered out by NF, which is designed to have the notch at the chopping frequency as discussed later.

D. Switched Capacitor Notch Filter (NF)

Fig. 3(a) shows the switched capacitor Notch Filter (NF) presented in [7], following to G_{m3} and CHOP3. The NF is a pseudo-differential sampling network. The positive signal path from the input ($V_{\rm nf\_inp}$) to the output ($V_{\rm nf\_outp}$) contains two sampling capacitors ($C_{\rm nf1}$ and $C_{\rm nf2}$) driven by the complementary timings (NF and NF_INV) followed by a load capacitor

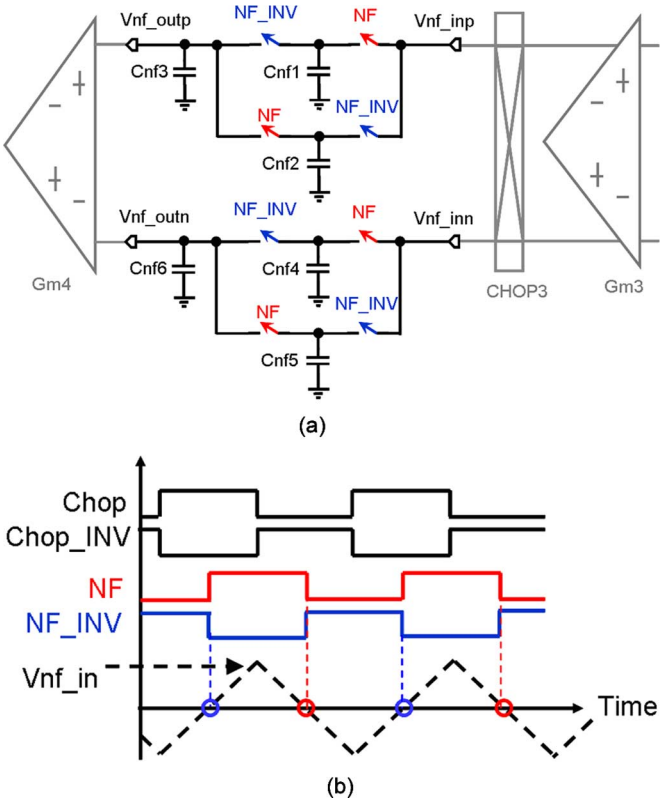

Fig. 3. (a) Switched capacitor notch filter and (b) timing diagram.

($C_{\rm nf3}$). The timings are synchronized and orthogonal relative to the chopping clock as shown in Fig. 3(b).

The filter operation should be analyzed including G_{m3} and CHOP3 as follows. The DC voltage at the input of G_{m3}, coming from the desired DC input signal, becomes modulated currents flowing into the input terminals of NF, $V_{\rm nf\_inp}$ and $V_{\rm nf\_inn}$. Those currents are integrated with the sampling capacitors connected to those terminals, and create a triangular voltage waveform ($V_{\rm nf\_in}$) where $V_{\rm nf\_in}$ is the differential input voltage ($V_{\rm nf\_inp} - V_{\rm nf\_inn}$). Then the waveform is sampled every time it crosses zero as shown in Fig. 3(b), because of the orthogonal relationship between the chopping and the NF sampling clocks. Thus, when the sampled voltage is transferred to the load capacitors coupled to the input of G_{m4} in the next phase, any modulated component such as DC input signal and offset of Gm3 from CHOP3 is filtered out.

IV. Overall Amplifier Design

A. Design Target

Here we discuss the overall design that implements the proposed ACFB in a stand alone chopper operational amplifier. It is targeting low frequency signals especially around DC -10 Hz with high precision, very low power dissipation, and small die size. It offers a single supply voltage ranging from 1.8 V to 5.5 V, temperature range from -40 C to 125 C, and rail-to-rail input common mode range. It is designed with a 0.35 μm DPTM CMOS process with 5 V devices used to accommodate up to 5.5 V I/O. It should also be stable in a unity gain or in any closed-loop gain with up to 100 pF external load capacitance, as well as other typical industrial operational amplifiers.

B. Block Diagram

Fig. 4 shows the full block diagram for the proposed chopper amplifier. It has on chip clock generator providing the chopping and the NF timings. The amplifier contains a high DC gain path and a high frequency path in parallel [3], [10]. The high DC gain path, dominating DC performance, is based on the circuit shown in Fig. 2 with the addition of a fifth transconductance amplifier (G_{m5}) as an output buffer to drive external load. The high frequency path contains a sixth transconductance amplifier (G_{m6}) followed by G_{m5}, to bypass phase shift introduced by ACFB at the center frequency of NF, and to make the overall amplifier's loop stable. The phase compensation is done by capacitors (C_1, C_2, and C_3). The gain and the phase of the overall amplifier are dominated by the high DC gain path where the frequency is well below the NF's center frequency. The gain of the high DC gain path significantly drops around the NF's center frequency, and then the high frequency path starts dominating the overall gain. It still maintains the overall gain dropping with -20 dB/dec slope. The unity gain frequency of the open loop becomes $G_{m6}/(2\pi C_1)$, which is designed to be 100 kHz and is greater than the NF's center frequency. The transconductance of G_{m6} is designed same as the one of G_{m1} to avoid a pole-zero doublet [3], [10].

C. ACFB Loop Gain

Here we figure out the loop gain of ACFB ($A_{\rm ACFB}$) in the proposed chopper amplifier shown in Fig. 4. The loop gain can be analyzed by breaking the loop at the output of NF, and decomposing it into two parts.

The first part is the gain from the breaking point to the output of CHOP2 ($A_{\rm ACFB1}$), which can be evaluated by putting the test voltage at the breaking point ($V_{t,i}$) while putting no voltage at the input of G_{m1}. Because the voltage at the breaking point is modulated by CHOP2, we should take the impedance at the chopping frequency rather than at DC to calculate the impedance at the output of CHOP2. In such frequency, the impedances at the output of CHOP2 and at the output of G_{m2} are dominated by capacitors. The loop can be made to apply Kirchhoff's voltage law from the input of G_{m5} to the input of G_{m2}, through C_1 and C_2, leading to

$$\frac{G_{m2}}{2\pi j f_{\rm chop} C_1} V_{t,\rm CHOP2} - \frac{G_{m4}}{2\pi j f_{\rm chop} C_2} V_{t,i} + V_{t,\rm CHOP2} \approx 0. \tag{1}$$

Here $V_{t,\rm CHOP2}$ is the output voltage of CHOP2 responding to the test voltage. The input voltage of G_{m5} is assumed as virtual ground as its transconductance is quite larger than the others. The gain can be expressed after superposition, as shown in (2):

$$\begin{aligned} A_{\rm ACFB1} &\equiv \frac{V_{t,\rm CHOP2}}{V_{t,i}} \\ &\approx G_{m4}\left(\frac{1}{C_2} \bullet \frac{C_1}{G_{m2}}\right) \bullet \frac{1}{1 + 2\pi j f_{\rm chop} C_1 / G_{m2}} \\ &\approx G_{m4}\left(\frac{1}{C_2} \bullet \frac{C_1}{G_{m2}}\right). \end{aligned} \tag{2}$$

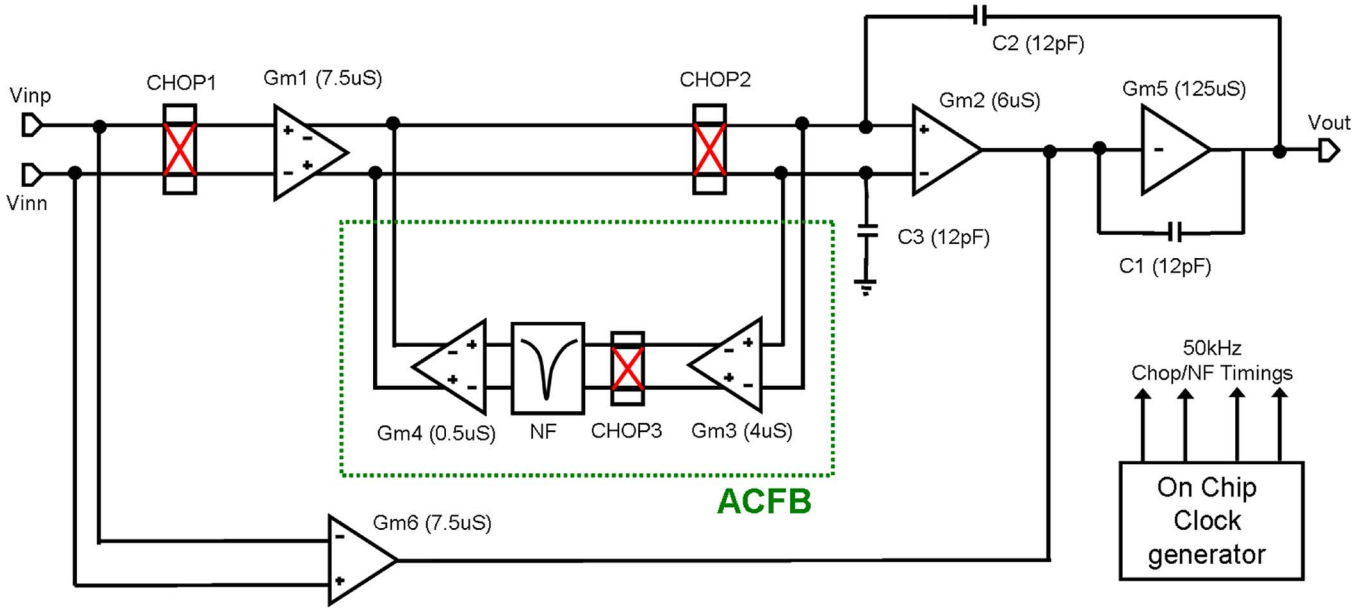

Fig. 4. Full block diagram of the proposed chopper amplifier.

The pole (C_1/G_{m2}) is located above the chopping frequency and is neglected.

The second part is the gain from the output of CHOP2 to the breaking point (A_{ACFB2}). The NF can be considered as the combination of an integrator and a sinc filter. The characteristic of the sinc filter is described in [1], and the combined gain is shown in (3):

$$A_{\mathrm{ACFB2}} \approx \frac{G_{m3}}{2\pi j f(C_{\mathrm{nf1}}+C_{\mathrm{nf2}}+C_{\mathrm{nf3}})} \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_{\mathrm{chop}}}\right)}{\frac{\pi}{2}\frac{f}{f_{\mathrm{chop}}}} \tag{3}$$

where $C_{\mathrm{nf1}}, C_{\mathrm{nf2}}$, and C_{nf3} are the capacitors in NF shown in Fig. 3(a). The DC gain of A_{ACFB2} is limited by the output resistance of G_{m3}. The cascode topology is essential to make it large enough to suppress the residual ripple. In addition care needs to be taken not to have much capacitance at the output of G_{m3} as it creates the conductance together with CHOP3.

The overall loop gain of ACFB is

$$A_{\mathrm{ACFB}} = A_{\mathrm{ACFB1}} \bullet A_{\mathrm{ACFB2}} \approx \left(\frac{G_{m4}}{G_{m2}}\frac{C_1}{C_2}\right) \times \frac{G_{m3}}{2\pi j f(C_{\mathrm{nf1}}+C_{\mathrm{nf2}}+C_{\mathrm{nf3}})} \frac{\sin\left(\frac{\pi}{2}\frac{f}{f_{\mathrm{chop}}}\right)}{\frac{\pi}{2}\frac{f}{f_{\mathrm{chop}}}}. \tag{4}$$

As the sinc filter creates significant phase shift at the chopping frequency, the unity gain frequency must occur well below the chopping frequency to make the loop stable. The capacitors at the NF are sized at $C_{\mathrm{nf1}} = C_{\mathrm{nf2}} = C_{\mathrm{nf4}} = C_{\mathrm{nf5}} = 7$ pF and $C_{\mathrm{nf3}} = C_{\mathrm{nf6}} = 14$ pF, which sets the unity gain frequency at 1.9 kHz. The clock frequency of the chopping and NF is set to 50 kHz. The calculated equation of the loop gain is shown in Fig. 5 with the simulated one. The simulation has been done with Periodic AC analysis (PAC) provided by Spectre RF, which includes the effect of the dynamic characteristics of the chopping and NF [11]. The simulated DC gain is 41 dB and the unity gain frequency is 1.22 kHz.

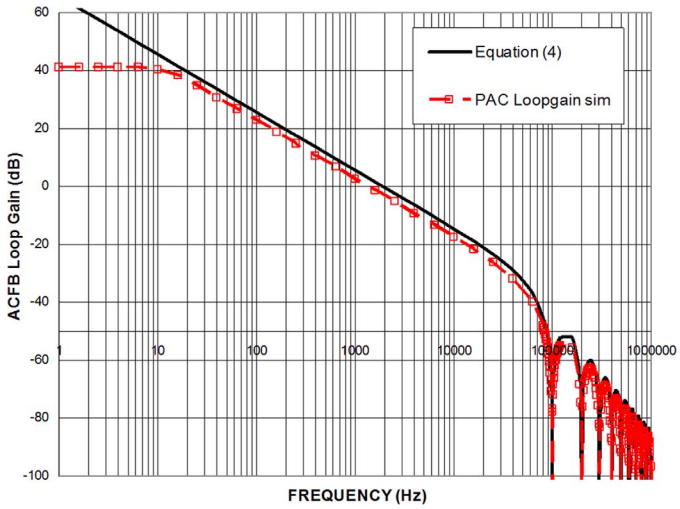

Fig. 5. Calculated and simulated loop gain of ACFB.

D. Detail Design

The circuit diagram of G_{m1}, G_{m2} and G_{m4} is shown in Fig. 6 with CHOP1 and CHOP2. The G_{m1} employs both n-channel input pair (M_{n1} and M_{n2}) and p-channel input pair (M_{p1} andM_{p2}), followed by a folded cascode output stage. Their tail bias current are controlled depending on the input common mode voltage, such that $I_{\mathrm{p1}} + I_{\mathrm{n1}} = 0.48\ \mu$A. The G_{m4} is realized in the folded cascode stage of G_{m1} with $M_{\mathrm{p7}}, M_{\mathrm{p8}}$, and R_1, which avoids consuming extra bias current. The transconductance of G_{m4} is determined by R_1, as the R_1 is 4 MΩ and much larger than the inverse of transconductance of M_{p7} and M_{p8}. Most of the current signal from the n-channel input pair does not flow into R_1 because of its larger value.

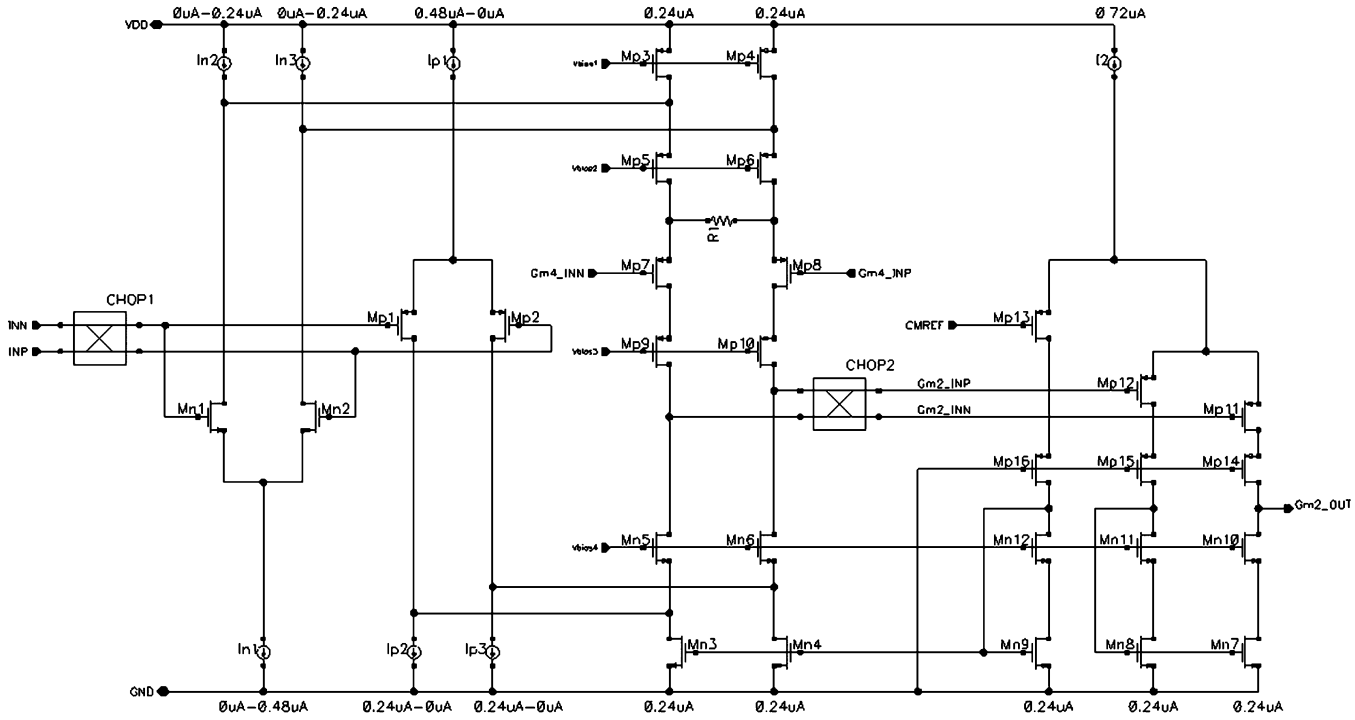

Fig. 6. Circuit diagram of G_{m1}, G_{m2}, and G_{m4}.

TABLE I
BUDGET OF SUPPLY CURRENT FOR EACH CIRCUIT

	Supply current	Transconductance
G_{m1}	0.83μA	7.5μS
G_{m2}	0.48μA	6.0μS
G_{m3}	0.60μA	4.0μS
G_{m4}	0.48μA	0.5μS
G_{m5}	6.63μA	125.0μS
G_{m6}	0.71μA	7.5μS
Bias	1.30μA	N/A
Clock generator	1.92μA	N/A
Chip Total	12.95μA	N/A

Larger R_1 also makes its noise contribution smaller and the sensitivity from the error at NF smaller. $M_{\rm p11}, M_{\rm p12}$, and $M_{\rm p13}$ have same device size, and it realizes the input pair of G_{m2} and common mode feedback for G_{m1}. The differential voltage at node of $G_{m2\_\rm INP}$ and $G_{m2\_\rm INN}$ is amplified by $M_{\rm p11}$ and $M_{\rm p12}$, and it becomes the output current signal of G_{m2} at node of $G_{m2\_\rm OUT}$. The common mode voltage at node of $G_{M2\_\rm INP}$ and $G_{M2\_\rm INN}$ is compared with a reference voltage of CMREF, and it is fed back to the G_{m1} through a current mirror with $M_{\rm n3}, M_{\rm n4}$, and $M_{\rm n9}$. The input pairs for G_{m1}, G_{m2} and G_{m4} ($M_{\rm n1}, M_{\rm n2}, M_{\rm p1}, M_{\rm p2}, M_{\rm p7}, M_{\rm p8}, M_{\rm p11}, M_{\rm p12}$, and $M_{\rm p13}$) are biased in the weak inversion region, to get larger transconductance for a given bias current [2]. The required amount of G_{m1}'s transconductance is primarily driven by the targeted noise density in the base band, as it is dominated by the thermal noise floor of G_{m1}. The transconductance of G_{m2} is set large enough to locate the pole above the chopping frequency in (2). It is also set large enough to suppress the offset contribution from G_{m6} as discussed later. The transconductance of G_{m5} has to be large enough to drive an external load capacitor of 100 pF without introducing excess phase shift, dominating the overall supply current dissipation. As the ACFB needs gain only at DC, the transconductance for G_{m3} does not have to be very large. The amount of current dissipation and transconductance in each transconductance amplifier are shown in Table I. The error from NF can be also suppressed by making their capacitors large, making the sensitivity low from the charge injection error. As the non-linearity of the capacitors does not affect the overall performance in the main loop, high density MOS capacitors can be used here.

V. RESIDUAL ERROR ANALYSIS

A. Residual Ripple

Here we conduct residual error analysis for the proposed chopper amplifier shown in Fig. 4 including the non-idealities of the circuit. The amount of ripple suppression is determined by the loop gain of ACFB. With finite DC gain of ACFB, the null voltage ($V_{\rm null}$) contains a residual DC error voltage ($V_{\rm err}$) at the input of G_{m4} as shown in (5) and (6):

$$V_{\rm null} = \frac{G_{m1}}{G_{m4}} V_{\rm os1} + V_{\rm os4} + V_{\rm err} \tag{5}$$

$$V_{\rm err} \approx -\frac{1}{1 + A_{\rm ACFB}} \left(\frac{G_{m1}}{G_{m4}} V_{\rm os1} + V_{\rm os4} + V_{NF,\rm sample} \right). \tag{6}$$

$V_{\rm os1}$ and $V_{\rm os4}$ are input referred initial offset voltages of G_{m1} and G_{m4} respectively. The last term ($V_{\rm NF,sample}$) is the error voltage arising in NF due to the charge injection during sampling process, which is also suppressed by the loop gain of ACFB. The $V_{\rm err}$ creates a DC error current at the output of G_{m1}, which becomes modulated ripple at the overall output through

CHOP2. The magnitude of the ripple voltage ($V_{\mathrm{out,rip}}$) in RMS value is expressed as

$$V_{\mathrm{out,rip}} \approx \left|\frac{G_{m4}}{G_{m1}}V_{\mathrm{err}}\right| \approx \frac{1}{1+A_{\mathrm{ACFB}}} \times \left(V_{\mathrm{os1}} + \frac{G_{m1}}{G_{m4}}\left(V_{\mathrm{os4}} + V_{\mathrm{NF,sample}}\right)\right). \quad (7)$$

As well as the initial offset of G_{m1}, any error in the ACFB causes modulated ripple rather than critical DC error. The total magnitude of the ripple would be dominated by the initial offset of G_{m1}, as the contribution from the other error sources can be suppressed by making G_{m4} smaller relative to G_{m1}.

B. Residual Offset

The input offset voltages of G_{m2} and G_{m6} (V_{os2} and V_{os6}) appear at the input of G_{m2}, and contribute to residual input offset voltage ($V_{\mathrm{os,res}}$) if the DC gain of G_{m1} (A_1) is not large enough as shown in (8):

$$V_{\mathrm{os,res}} \approx \frac{1}{A_1}\left(V_{\mathrm{os2}} + \frac{G_{m6}}{G_{m2}}V_{\mathrm{os6}}\right). \quad (8)$$

The initial input offset of G_{m3} is modulated by CHOP3 and is filtered out by NF, in the same manner as the desired input signal at the overall input is. So the initial offset of G_{m3} does not cause any error.

The transient simulation with the initial offset has been conducted to see the residual ripple and the residual offset. The amplifier shown in Fig. 4 is put in a unity gain feedback. The initial offsets are put at the input of $G_{m1}, G_{m2}, G_{m3}, G_{m4}$, and G_{m6}. To take the worst case, their magnitude are set to 4.5-sigma extracted from the device characterization data on this CMOS process. The resulting output waveform is shown in Fig. 7 with the timing diagram. It is not exact square waveform like the one in Fig. 1(b), due to not large enough bandwidth of the overall amplifier relative to the chopping frequency. The residual ripple of 41.7 $\mu\mathrm{V_{rms}}$ is seen synchronized with the chopping clock, in addition to the residual offset of 8.11 μV.

Table II shows the sensitivity from each initial offset voltage source to the residual ripple and to the residual offset voltage. The simulation is done with the same setup as for Fig. 7, except that only one offset source at a particular transconductance stage is added in a simulation to see its sensitivity. Moreover the mismatch errors are added at the NF, while all the transconductance stages have the initial offset. A 1% mismatch is added on the sampling capacitors in one simulation, and a 1% phase error between the chopping and NF clock is added in the other simulation. The amount of residual error increase due to those mismatches turns out to be minimal. The result indicates the achieved ripple attenuation of 43 dB by calculating the ratio between the magnitude of the residual ripple and the initial offset of G_{m1}. The amount of the ripple attenuation is determined by the DC loop gain of ACFB shown in Fig. 5.

C. Errors Due to Charge Injections

The charge injections at the chopping and at NF are be demodulated back to the input of amplifier, and it can contribute to the residual ripple and to the residual offset. The charge injection error comes from mismatch among the switches in the chopping and NF, as it creates different amount of coupling capacitor between the clock line and the signal line. The amount of the mismatch depends on the process parameter and the layout design, and it would be hard to be predicted. However it is still worth it conducting the simulation in order to see the sensitivity from each source of the charge injection. A 1fF coupling capacitor is added to causes the mismatch in each circuit, and the residual ripple and the residual offset are simulated as shown in Table III. The sensitivity from CHOP3 and NF are less than those from CHOP1 and CHOP2, which already exists in conventional chopper amplifiers. Such result is achieved by designing the transconductance of G_{m4} smaller than that of G_{m1} as discussed. The resulting capacitor's mismatch in the actual amplifier is quite less than the level assumed here, as the measured residual offset and ripple are close to the values simulated with the initial offset of transconductance amplifiers as discussed later.

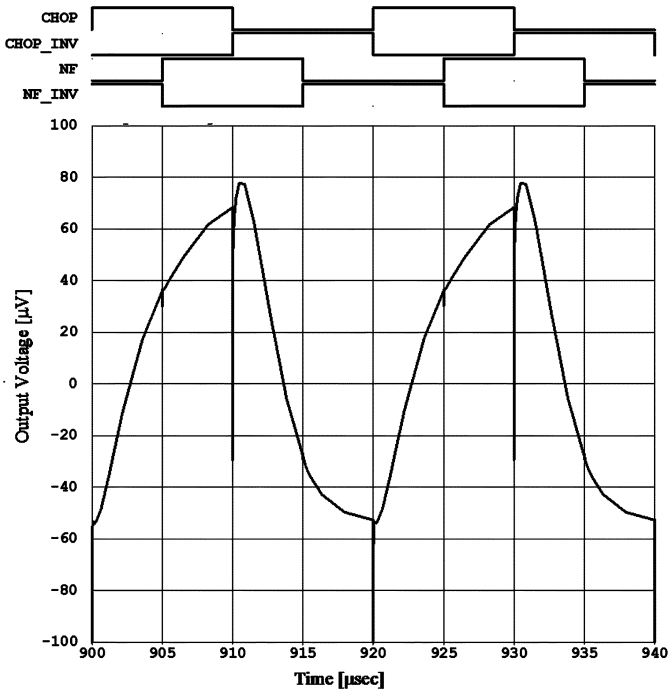

Fig. 7. Transient waveform of the proposed chopper amplifier.

TABLE II
SENSITIVITY FROM EACH INITIAL OFFSET

Initial offset location	Initial offset magnitude	Residual ripple	Residual offset
V_{os1}	6.1mV	36.0μV_{rms}	0.17μV
V_{os2}	7.0mV	1.6μV_{rms}	3.09μV
V_{os3}	5.5mV	1.0μV_{rms}	0.03μV
V_{os4}	5.8mV	3.4μV_{rms}	0.00μV
V_{os6}	6.5mV	2.6μV_{rms}	5.15μV
Total	N/A	41.7μV_{rms}	8.11μV
(Add NF cap error)	N/A	41.8μV_{rms}	8.11μV
(Add NF clock error)	N/A	41.7μV_{rms}	8.28μV

TABLE III
SENSITIVITY FROM CHARGE INJECTION ERROR

Error source location	Residual ripple	Residual offset
(No error)	$0.2\mu V_{rms}$	$0.00\mu V$
CHOP1	$3.4\mu V_{rms}$	$1.8\mu V$
CHOP2	$12.3\mu V_{rms}$	$17.7\mu V$
CHOP3	$2.3\mu V_{rms}$	$0.09\mu V$
NF	$2.0\mu V_{rms}$	$0.09\mu V$

D. Noise

The input referred voltage noise density in the base band is essentially dominated by the thermal noise floor of G_{m1} because of the principle of the chopping [1]. The output current noise of G_{m4} contributes in the same manner as G_{m1}. The noise contribution from G_{m4} can be reduced by making its transconductance smaller, designed to be 0.07 relative to that of G_{m1}. The equation for the resulting input voltage noise density in the base band $(V_{\mathrm{n,B.B}})$ is

$$V_{n,B.B} = \sqrt{8\,kT\frac{1}{G_{m1}}\left(1+\alpha+\frac{G_{m4}}{G_{m1}}\right)} \approx 87\ \mathrm{nV_{rms}}/\sqrt{\mathrm{Hz}}. \quad (9)$$

Here α is noise contribution from load current sources relative to the input devices in G_{m1}, designed to be 0.63.

The simulated total noise and the contribution from G_{m1}, G_{m3}, and G_{m4} are plotted in Fig. 8 with linear frequency scale. The simulation here is conducted by Periodic Noise analysis provided by Spectre RF. Similar to the PAC analysis conducted for Fig. 5, it computes the noise spectrum density including the effect of dynamic characteristics of the chopping and NF [11]. The base band noise below 50 kHz is dominated by the thermal noise of G_{m1} with little contribution from G_{m4} as expected. The sampled noise at NF is modulated by CHOP2 and creates a peak noise spectral density around the chopping frequency at 50 kHz, in the same manner as the residual ripple expressed in (7). The total sampled noise power can be calculated by considering the noise bandwidth of ACFB $(f_{u,\mathrm{ACFB}})$ as in (10):

$$V_{n,\mathrm{sampled}} \approx 82.2\ \mathrm{nV_{rms}}/\sqrt{\mathrm{Hz}} \bullet \sqrt{2\frac{\pi}{2}f_{u,\mathrm{ACFB}}} \approx 5.08\ \mu V_{\mathrm{rms}}. \quad (10)$$

The total power spectrum around the chopping frequency is expressed in (11) by combining the modulated sampled noise and the residual ripple:

$$V_{n,\mathrm{spectrum}} = \sqrt{V_{n,\mathrm{sampled}}^2 + V_{\mathrm{out,rip}}^2} \approx \sqrt{5.08\ \mu V_{\mathrm{rms}}^2 + (\sigma \bullet 9.3\ \mu V_{\mathrm{rms}})^2}. \quad (11)$$

Here the magnitude of the second term becomes 9.3 μV_{rms} with $\sigma = 1$ as typical case, and becomes 41.7 μV_{rms} with $\sigma = 4.5$ as the worst case. Such distribution over the units of the amplifier occurs, because the initial offset also has the distribution over the units due to random mismatches.

This sampled noise includes the contribution not only from G_{m3}, but also from the thermal noise of the switches in NF. The peak noise density contributed by those switches is less than 0.5 $\mathrm{nV_{rms}}$/rt(Hz) and it is negligible compared to the one from G_{m3}. This is because the inverse of the transconductance of G_{m3} is quite larger than the on-resistance of those switches in NF.

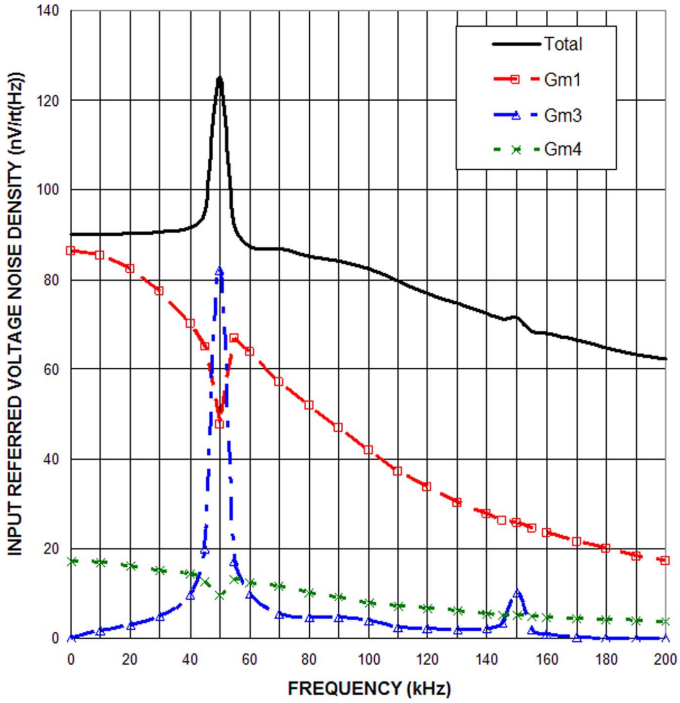

Fig. 8. Simulated noise contribution from each G_m by Spectre RF.

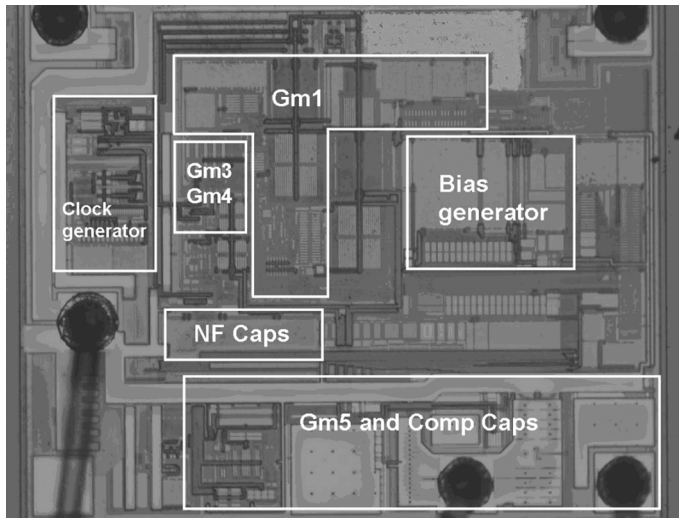

Fig. 9. Die photo of the proposed chopper amplifier (740 μm × 860 μm).

VI. MEASURED RESULT

The proposed chopper amplifier has been fabricated in a 740 μm × 860 μm active die area which is shown in Fig. 9. The added ACFB including G_{m3}, G_{m4}, and NF occupies about 15% of the total area.

Fig. 10 shows the histogram of the input referred offset voltage, corresponding to the magnitude of the residual offset in Table II.

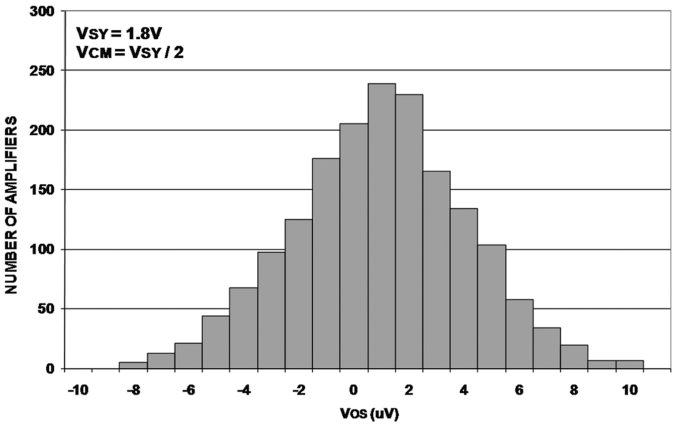

Fig. 10. Histogram of the input referred offset voltage.

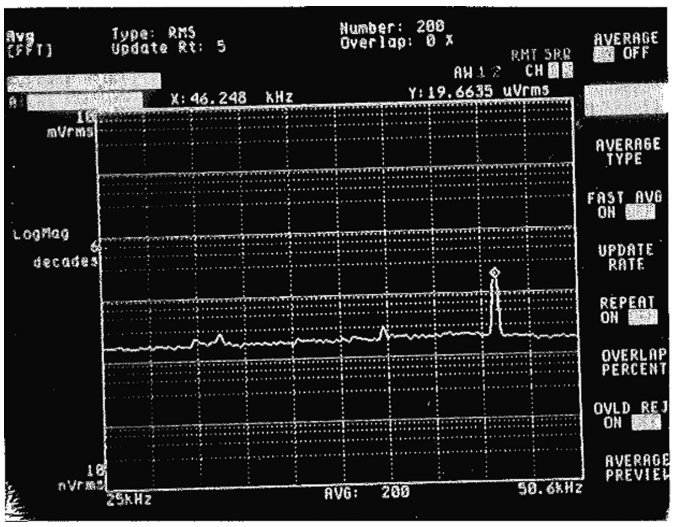

Fig. 11. Peak spectrum around chopping frequency.

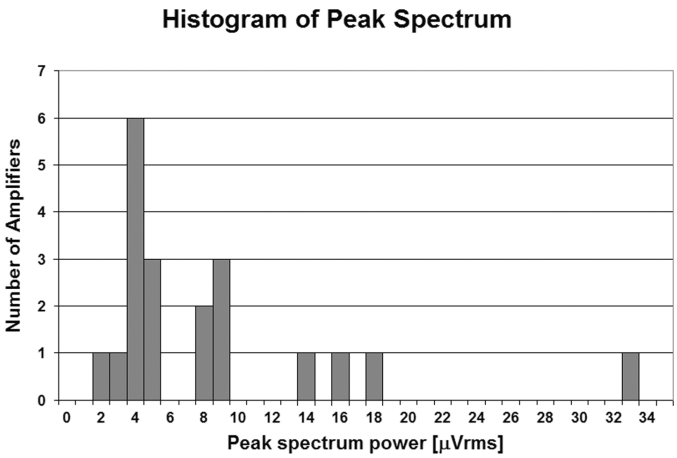

Fig. 12. Histogram of the magnitude of the peak spectrum.

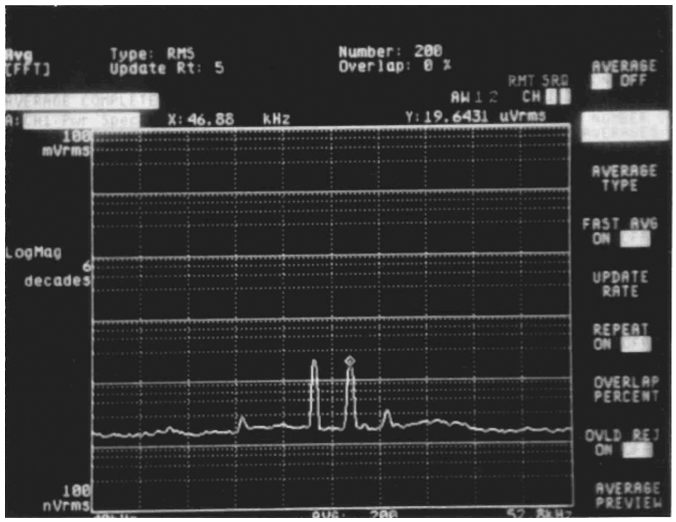

Fig. 13. Inter-modulation with 1 kHz–1 V_{rms} sinusoid input voltage.

The spectrum around the chopping frequency is shown in Fig. 11. The amplifier is put in a unity gain buffer and measured by the dynamic signal analyzer, HP35670A. Peak spectrum of 19.7 μV_{rms} is observed at 46.2 kHz as the residual ripple with this particular unit. The histogram over 20 units is shown in Fig. 12, indicating the magnitude of the peak spectrum is 9.4 μV_{rms} at 1-sigma and becomes 34.7 μV_{rms} at the worst. As in the simulation result, the ripple attenuation by ACFB is regarded as the ratio between the magnitude of the ripple and the initial offset of G_{m1}, which is 45 dB.

Inter-modulation test result is shown in Fig. 13, to see modulation effect between input signal and chopping clock. A 1 kHz sinusoid voltage with 1 V_{rms} magnitude is put at the input of unity gain buffer amplifier. The result shows 19.6 μV_{rms} peak spectrum at the frequency of $f_{chop} - f_{in}$ and $f_{chop} + f_{in}$, where f_{in} is the input signal frequency. It indicates -94 dB of inter-modulation effect by taking the ratio of the magnitude of resulting ripple and input signal.

Fig. 14 shows four plots of the input referred voltage noise spectral density by AC noise simulation, Periodic Noise simulation (PNoise), and two measurements. The AC noise simulation computes the noise spectral density at a fixed bias condition, so that the effect of the chopping and the NF are not included. It shows $1/f$ noise with 183 Hz corner frequency as a usual non-chopper amplifier does. The PNoise simulation shows a flat noise spectral density of 86 nV_{rms}/rt(Hz) down to 10 Hz, which is matched to the thermal noise floor by an AC noise simulation as expected. At lower frequencies, the simulation shows slightly increased spectrum at 0.01 Hz, which is 91 nV_{rms}/rt(Hz). To conduct the measurements, a non-inverting amplifier with a gain of 10 is followed by the dynamic signal analyzer. While one measurement is done with the chopping and ACFB disabled, and the other is done with the chopping and ACFB enabled. By enabling the chopping and the ACFB, a flat 95 nV_{rms}/rt(Hz) noise spectrum density down to 10 Hz is observed. A high side cutoff frequency of 10 kHz because of the non-inverting gain configured. In order to investigate the noise characteristic below 10 Hz, the noise waveform after a 6th order 0.1–10 Hz band pass filter with a gain of 10 000 is shown in Fig. 15. The input referred peak-to-peak voltage noise is 1.94 $\mu V_{p\text{-}p}$ as shown. Dividing by the noise bandwidth and by 6.6-sigma, this corresponds to 93.4 nV_{rms}/rt(Hz) of input voltage noise spectral density. As this is very close to the measured noise spectral density at 10 Hz, the noise spectrum density is regarded to be flat down to 0.1 Hz by combining two different noise measurements.

Fig. 16 is the measured open-loop gain and phase, showing 100 kHz unity gain frequency and 45 degree phase margin.

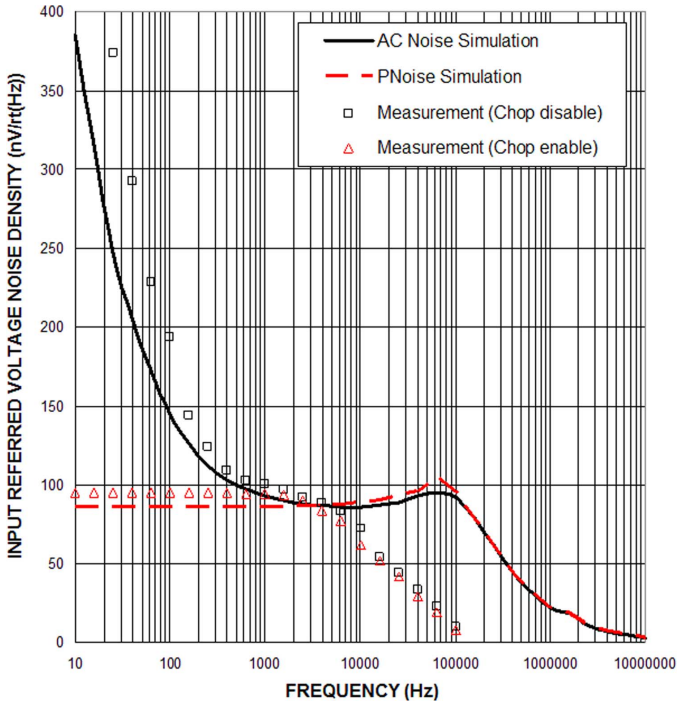

Fig. 14. Simulated and measured noise spectrum density.

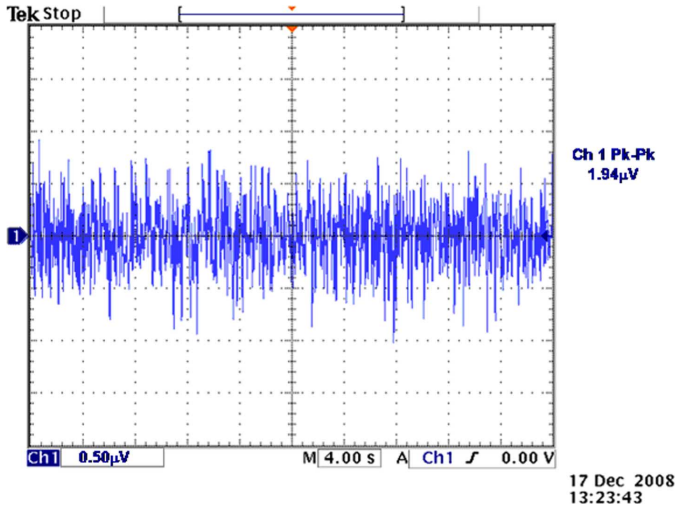

Fig. 15. Input referred voltage noise waveform with 0.1–10 Hz bandwidth.

There is also a bump for the gain and the phase around 50 kHz, which is at the chopping and at the NF's center frequency. Though it is due to phase shift introduced by ACFB, it does not degrade the stability thanks to the high frequency path added. As a result, the amplifier shows stable closed-loop gain characteristics as shown in Fig. 17. The stability can be also seen by looking at the small-signal step response as shown in Fig. 18.

Table IV summarizes the performance of the proposed chopper amplifier, achieved with 1.8 V supply voltage. The input bias current comes from the mismatch of the charge injections of the four switches in CHOP1. The competitive result is achieved by careful layout design to avoid any mismatch between MOS switches, differential input lines, and chopping clock lines.

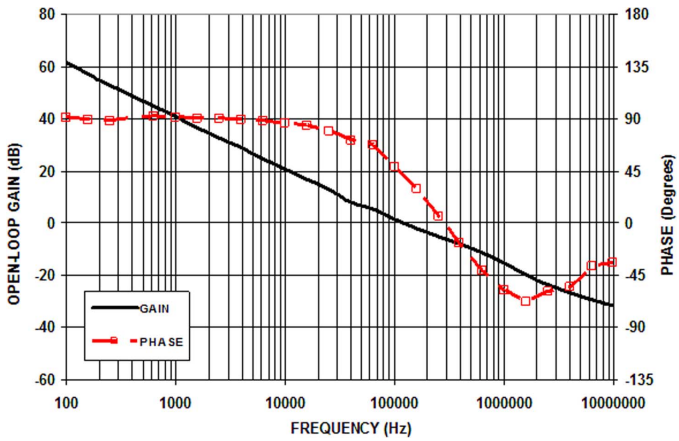

Fig. 16. Open-loop gain and phase.

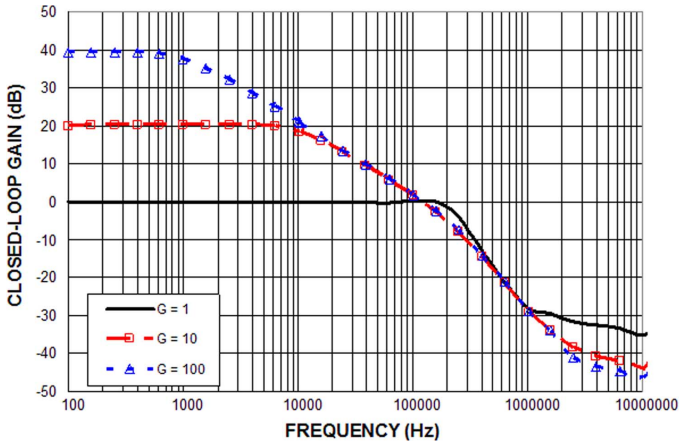

Fig. 17. Closed-loop gain.

TABLE IV
PERFORMANCE SUMMARY OF THE CHOPPER AMPLIFIER

	Typical	Worst
Input offset voltage	1.3µV	10µV
Offset drift	0.02µV/C	
CMRR (from 0 to supply rail)	125dB	105dB
PSRR (from 1.8 to 5.5V)	135dB	110dB
Input bias current	5pA	50pA
Voltage noise density	95nV/rt(Hz)	
0.1-10Hz peak-peak noise	1.94µV$_{P-P}$	
Spectrum at chop frequency	9.4µV$_{rms}$	34.7µV$_{rms}$
Open loop DC gain	130dB	106dB
Unity gain frequency	100kHz	
Supply current dissipation	13µA	17µA

VII. CONCLUSION

Auto correction feedback (ACFB) is presented as a method to suppress the ripple in a chopper amplifier. The proposed chopper amplifier with ACFB achieves 45 dB ripple suppression compared to a conventional chopper amplifier without introducing major performance degradations such as noise. The ripple attenuation in the chopper amplifier eliminates or relaxes the requirement for a post filter. It increases the power dissipation by 8% and the die area by 5% to implement the ACFB in the chopper amplifier. The comparison with previous published work is provided in Table V. Two figures of merit

TABLE V
PERFORMANCE COMPARISON WITH PREVIOUS WORK

	This work	[4]	[3]	[6]
Year published	2010	2007	2006	2002
Chopping frequency	50kHz	16kHz	125kHz	15kHz
Input offset voltage	1.3μV	1.5μV	3.0μV	3.0μV
Input bias current	5pA	Not shown	70pA	40pA
Voltage noise density (en)	95nV/rt(Hz)	150nV/rt(Hz)	55nV/rt(Hz)	20nV/rt(Hz)
Unity gain frequency (GBW)	100kHz	1.3MHz	350kHz	2.5MHz
Current dissipation (Iq)	13μA	700μA	17μA	800μA
Die area	0.64mm^2	3.6mm^2	0.7mm^2	0.67mm^2
en^2 x Iq (nV/rt(Hz)*mA) Figure of merit	117	15750	51	320
GBW/Iq (kHz/μA) Figure of merit	8	2	21	3

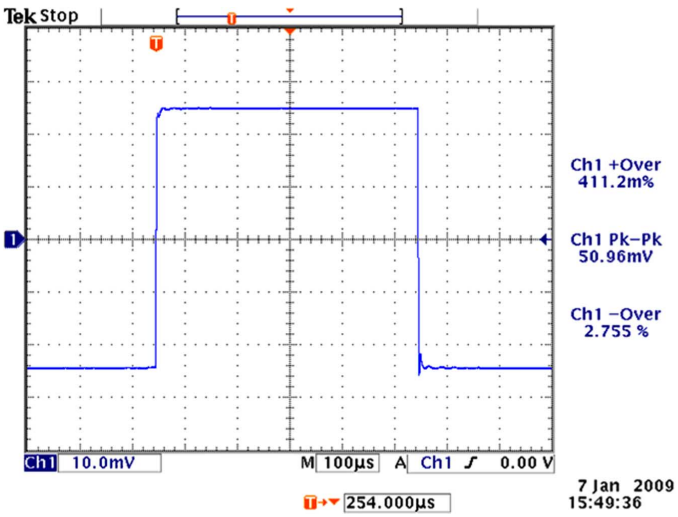

Fig. 18. Small-signal step response.

used in [3] are employed here to compare the noise and the speed per given current dissipation.

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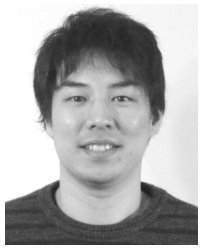

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