Frequency Compensation Techniques for Op-Amps and LDOs: A Tutorial Overview

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***Abstract*— Today's op-amp is not just a stand-alone IC, rather it is more custom and complex, catering the needs of highly integrated SoC. Tighter line and load regulation, low quiescent current operation, capacitor-free and wide-range output capacitor specifications are some of the contradicting requirements in an LDO, which drive newer topologies and newer frequency compensation techniques. The objective of this paper is to provide a tutorial treatment of some of the basics and recent advances in frequency compensation. Transistor level implementation of efficient LHP zero techniques and design examples are detailed.**

I. Introduction

Several op-amp and LDO architectures have evolved, from a simple two-stage topology using Miller compensation with nulling resistor to a complex multi-stage op-amp with feed-forward and nested/reverse-nested feedback paths which utilize active capacitance multiplication techniques. This tutorial attempts to highlight some of the recent advances in compensation techniques after revisiting with some basics.

Rest of the paper is organized a follows: In Section II, a simple two-stage LDO is analyzed, focusing on the necessity to compensate an LDO. Section III details various topologies for frequency compensation, starting from basic Miller's theorem to advanced inverting current buffer using current mirror and impedance degeneration techniques. Several efficient LHP zero techniques are detailed.

II. Necessity of Frequency Compensation in LDOs

Consider the schematic of a two-stage low dropout voltage regulator (LDO), shown in Fig. 1. The circuit consists of a PMOS pass transistor M_{pass}, a sampling network formed by R_{f1} and R_{f2}, a single-stage error amplifier g_{mEA}, an output capacitor C_{OUT} with equivalent series resistance (ESR) R_{ESR}.

The small signal equivalent of Fig. 1 (using Miller compensation capacitor C_m and a nulling resistor R_m between nodes V_{EA} and V_{OUT}) is shown in Fig. 2. After solving the Kirchhoff's current law nodal equations, the locations of poles and zeros are given by

Closed Loop DC Gain: $A_{DC} = \beta g_{mEA} R_{EA} g_{mP} R_{OUT}$

First Pole: $\omega_{P1} \approx -\frac{1}{R_{EA} C_m g_{mP} R_{OUT}}$

Output Pole: $\omega_{POUT} = -\frac{g_{mP} C_m}{C_{EA} C_m + C_m C_{OUT} + C_{OUT} C_{EA}}$

Parasitic RHP Zero: $\omega_{Z,Cgd} = +\frac{g_{mP}}{C_{gd,pass}}$

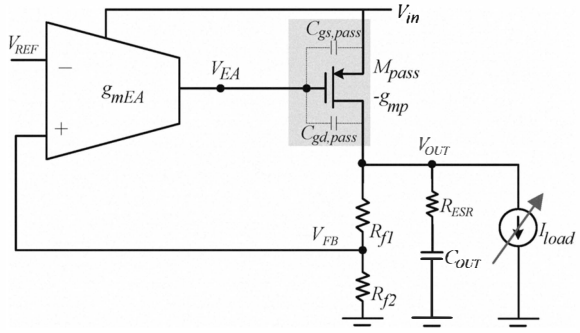

Fig. 1. Schematic of a simple two-stage LDO (compensation network not shown).

LHP Zero due to ESR: $\omega_{Z,ESR} = -\frac{1}{R_{ESR} C_{OUT}}$

LHP Zero due to Compensation Capacitor C_m:

$\omega_{Z,C} = +\frac{g_{mP}}{C_m}; for R_m = 0$

$\omega_{Z,C} \approx -\frac{1}{R_m C_m}; for R_m \gg \frac{1}{g_{mP}}$

Output Impedance: $R_{OUT} = r_{opass} || (R_{f1} + R_{f2})$

Feedback Factor: $\beta = R_{f2} / (R_{f1} + R_{f2})$

A. External Compensation using Output Capacitor and ESR

In the case of external compensation with an output capacitor, the output pole ω_{POUT} is dominant and $\omega_{Z,ESR}$ compensates the LDO [1], [2].

B. Internal Compensation using Capacitance Multiplication

In the case of an output capacitor-free LDO architecture with internal compensation, the dominant pole is $\omega_{P,EA}$, created internally at the output of error amplifier [3].

Often op-amps are designed to operate for a particular loading condition and hence the location of poles are fixed. In case of an LDO, the output load current is designed to vary and the location of the poles of LDO $\omega_{P,EA}$ and $\omega_{P,OUT}$ move, as illustrated in Fig. 3.

For an internally-compensated LDO, at low load currents, the non-dominant output pole moves to lower frequencies since $r_{o,pass}$ of the PMOS pass transistor is inversely proportional to the load current, given by

$$r_{o,pass} = \frac{1}{\lambda I_{LOAD}} \quad (1)$$

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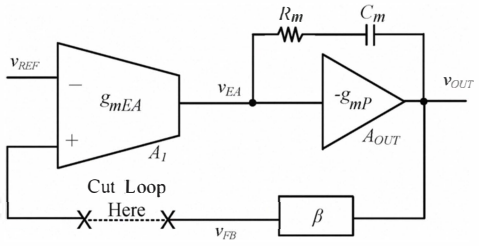
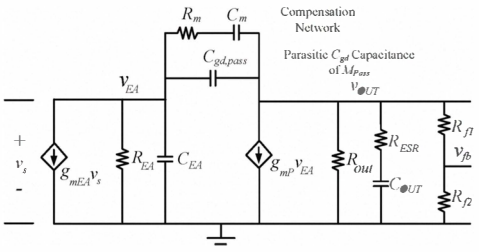


(a)



(b)

Fig. 2. (a) Simplified block diagram representation and (b) small signal equivalent model of the LDO of Fig. 1.

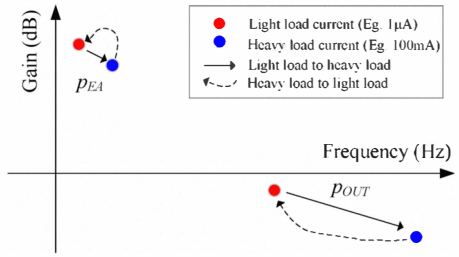


Fig. 3. Movement in the location of poles at different loading conditions.

The movement of the output pole below the unity-gain frequency jeopardizes stability of the closed-loop amplifier. Hence, proper compensation is required to ensure stability over a wide range of loading conditions.

III. Overview of Frequency Compensation Techniques

A. Miller's Theorem

If an impedance Z_C is connected between its input and output nodes of an ideal voltage amplifier of gain $-A_v$, Miller's theorem [4] states that the input and output impedances of the circuit, of Fig. 4, are given by

$$Z_{IN} = \frac{Z_C}{1+A_v} \approx \frac{Z_C}{A_v}$$
$$Z_{OUT} = \frac{Z_C}{1+1/A_v} \approx Z_C \quad (2)$$

If the impedance Z_C is replaced by a capacitor $Z_C = 1/sC_C$, then the input capacitance $C_{IN} \approx A_v C_C$ gets multiplied by the gain of the op-amp and feels "big". The output capacitance $C_{OUT} \approx C_C$, implying that the Miller capacitance loads the output. On the contrary, if Z_C is replaced by a resistor R_C, the input resistance gets divided by the gain.

B. Miller RHP Zero

Fig. 5(a) shows a Miller compensation capacitor, used to split the poles associated with nodes X and Y. In addition to pole splitting, the Miller capacitor C_m forms a feedforward path resulting in an RHP zero, located at [5], [6]

$$\omega_Z = +\frac{g_{mY}}{C_m}. \quad (3)$$

C. Shifting the Miller zero from RHP to LHP

The Miller RHP zero can either be cancelled or shifted to the LHP by choosing an appropriate value for the series nulling resistor R_m shown in Fig. 5(b). The equation for ω_Z becomes:

$$\omega_Z = \frac{1}{C_m\left(\frac{1}{g_{mY}} - R_m\right)} \quad (4)$$

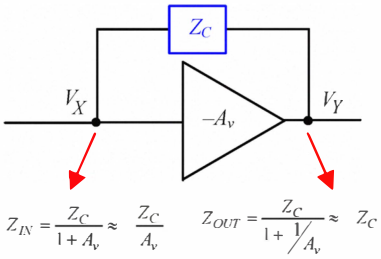


Fig. 4. Illustration of the Miller's theorem.

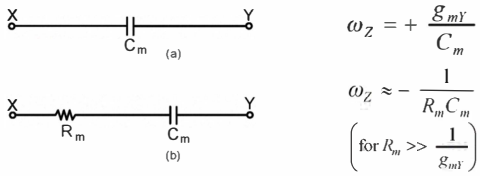


Fig. 5. (a) Miller compensation (b) Miller compensation with nulling resistor.

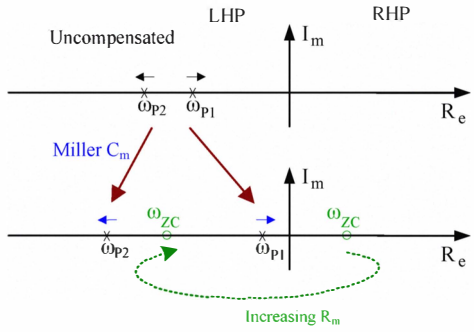


Fig. 6. Pole-Zero diagram showing movement of Zero for various values of nulling resistor R_m.

When $R_m = 1/g_{mY}$, the RHP zero gets cancelled. For $R_m \gg 1/g_{mY}$, the zero shifts to LHP and is approximately located at

$$\omega_Z \approx -\frac{1}{R_m C_m} \quad (5)$$

as shown in Fig. 6. Similarly a voltage or current buffer can be placed in series with the Miller capacitor in order to move the RHP zero to the LHP [7], as described below.

D. Miller Compensation using Current Buffers

Current buffers can be loosely classified as non-inverting or inverting.

1) Cascode Compensation: As shown in Fig. 7, a non-inverting current buffer, implemented with a common-gate amplifier transistor g_{mCG}, can be used to obviate the feedforward path [5], [6], [8], [9] and introduce a LHP zero at

$$\omega_Z = -\frac{g_{mCG}}{C_C} \tag{6}$$

This cascode compensation topology is popularly known as Ahuja compensation. A cascode transistor M_{CG} inherent in a folded-cascode or a telescopic op-amp introduces an LHP zero without additional bias circuitry or quiescent current [9], [10].

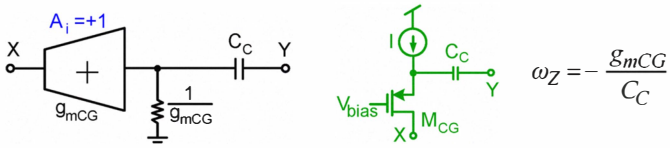


Fig. 7. Illustration of Ahuja cascode compensation.

2) Compensation using a Current Mirror: A current mirror is an ubiquitous component, and is inherent in a differential, folded-cascode and telescopic op-amps. A simple, yet efficient Miller compensation network can be formed with a current mirror of unity current gain, as shown in Fig. 8 [10]–[12]. This inverting current buffer can be used in series with compensation capacitor to introduce an LHP zero at

$$\omega_Z = -\frac{g_{m,BU}}{C_C} \tag{7}$$

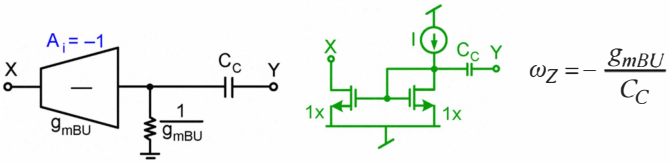


Fig. 8. Miller compensation using inverting current buffer topology.

E. Effective Placement of LHP Zeros

Often LHP zeros are used to cancel poles and improve phase response. To make the LHP zero more dominant, either the value of the transconductance (of Eqns. 6 or 7), or the compensation capacitance C_C has to be modified. However changing these values for a given design significantly affects other small signal and large signal parameters and may not form a feasible solution.

A simple and effective solution for accurately placing the LHP zero is to place a resistor R_C in series with the current buffers as shown in Fig. 9 [10], [13]. The new location of the LHP zero is given by

$$\omega_{Z,CB} = -\frac{1}{C_C\,(1/g_{mCB} + R_C)} \approx -\frac{1}{R_C C_C} \tag{8}$$

Equation 8 illustrates the new location of the LHP zero, independent of transconductance, giving an additional degree of freedom with the choice in value of resistor R_C.

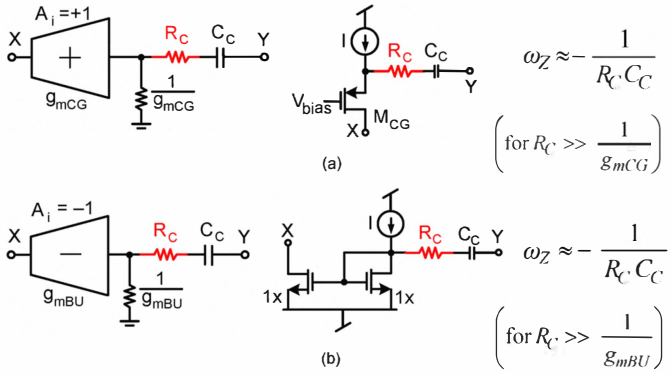


Fig. 9. (a) Modified Ahuja cascode compensation (b) Resistor R_C in series with current mirror.

The significance of adding resistor R_C is illustrated in Fig. 10, in which the zero moves to lower frequencies as the value of R_C increases.

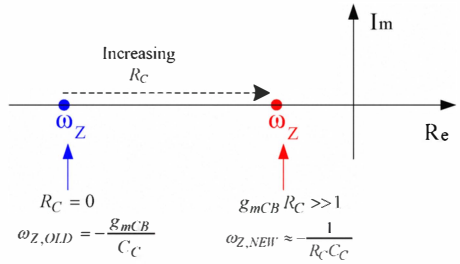


Fig. 10. Significance R_C: Diagram illustrating the movement of the current buffer zero as a function of R_C [13].

Fig. 12 shows a design example of LDO of [10] and Fig. 11 shows the corresponding small signal diagram. In this circuit, two LHP zeros are formed by positive and inverting current buffers in a reverse nested Miller compensation implementation.

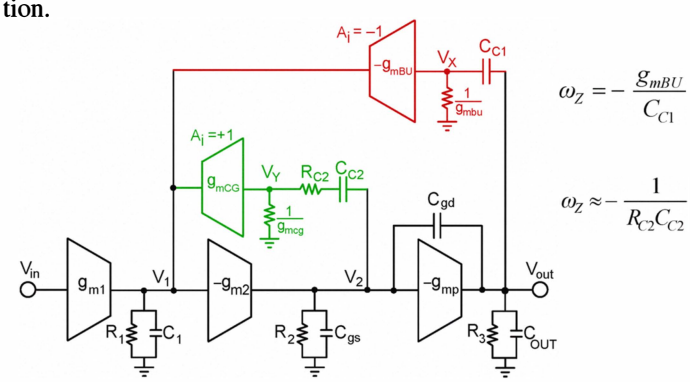


Fig. 11. Small signal diagram of reverse nested Miller Compensation scheme using current buffers implemented in the LDO.

F. Passive LHP zero at Internal Node

Similar to the LHP zero of an output capacitor with ESR, a LHP zero can be introduced with small on-chip capacitance C_i and series resistance R_i as shown in Fig. 13.

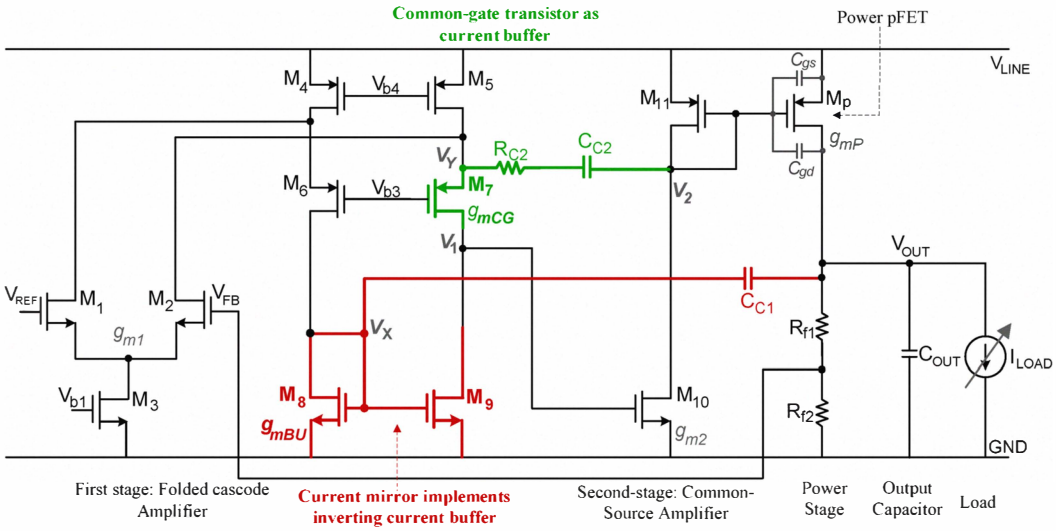


Fig. 12. Schematic of LDO, based on [10] highlighting inverting current buffer and modified cascode compensation.

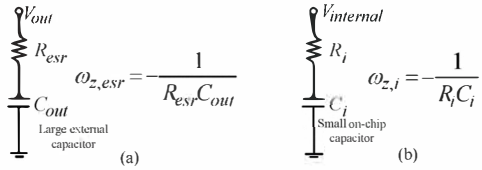


Fig. 13. LHP zero with (a) ESR (b) internal capacitor and series resistance.

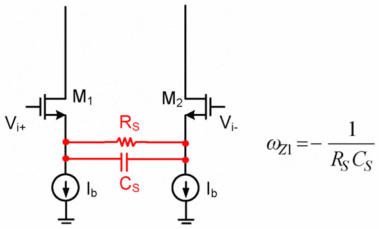


Fig. 14. Impedance degeneration differential pair creating LHP zero.

G. LHP Zero from Source Impedance Degeneration

The combination of source degeneration resistor R_S and capacitor C_S in Fig. 14 introduces a LHP zero at

$$\omega_{Z1} = -\frac{1}{R_S C_S} \tag{9}$$

This impedance degeneration technique is utilized in [14] to obtain a high power supply rejection response in an LDO.

IV. Summary

Several LHP zero techniques for op-amps and LDOs are elucidated. Current buffers embedded in the op-amp can be utilized to implement the compensation network, obviating the need for additional circuitry and power consumption.

Acknowledgments

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