An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection

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***Abstract*—An output-capacitorless low-dropout regulator (LDO) with a direct voltage-spike detection circuit is presented in this paper. The proposed voltage-spike detection is based on capacitive coupling. The detection circuit makes use of the rapid transient voltage at the LDO output to increase the bias current momentarily. Hence, the transient response of the LDO is significantly enhanced due to the improvement of the slew rate at the gate of the power transistor.**

The proposed voltage-spike detection circuit is applied to an output-capacitorless LDO implemented in a standard 0.35-μm CMOS technology (where $V_{\rm THN} \approx 0.5$ V and $V_{\rm THP} \approx -0.65$ V). Experimental results show that the LDO consumes 19 μA only. It regulates the output at 0.8 V from a 1-V supply, with dropout voltage of 200 mV at the maximum output current of 66.7 mA. The voltage spike and the recovery time of the LDO with the proposed voltage-spike detection circuit are reduced to about 70 mV and 3 μs, respectively, whereas they are more than 420 mV and 30 μs for the LDO without the proposed detection circuit.

***Index Terms*—Capacitive coupling, low-dropout regulator, voltage spike.**

I. Introduction

TRANSIENT response is a critical dynamic specification in low-dropout regulator (LDO) design. Both the amplitude of the voltage spike and the recovery time of the regulated output voltage $(V_{\rm O})$ affect its overall accuracy, which indirectly impacts the performance of the circuits supplied by the LDO. In fact, the transient response of a LDO is related to different design parameters such as the closed-loop stability, the loop bandwidth $(BW_{\rm L})$ and the slew rate at the gate of the power transistor (SR_G) [1]–[5]. The closed-loop stability and $BW_{\rm L}$ are small-signal parameters related to the positions of the poles and the zeros in the feedback system, while SR_G is a large-signal parameter that depends heavily on the magnitude of the bias current [6]. Undoubtedly, typical measures to optimize the transient response of a LDO are to increase the output capacitance, use a low equivalent-series-resistance (ESR) capacitor, and increase the bias current of the error amplifier/voltage buffer [1]. However, in the SoC design, it is expected to place an on-chip output-capacitorless LDO adjacent to individual circuit blocks, so that the power supply of each circuit block can be optimized independently (i.e. accuracy, magnitude, power-supply rejection and noise) to improve the overall performance of the system [7]. The regulated power supplies are generated inside the SoC chip. Under this circumstance, in the SoC design, the generic approach using external capacitors is no longer useful to effectively reduce the voltage spike due to the non-zero bondwire inductance and the long power-line routings (i.e. RC delay). Therefore, more power is needed to increase both $BW_{\rm L}$ and SR_G of the LDO to suppress the voltage spike and reduce the recovery time.

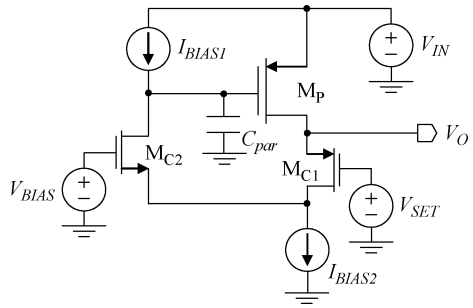

Fig. 1. An output-capacitorless LDO reported in [8]–[10].

Fig. 1 shows one reported LDO structure used in [8]–[10] to enable output capacitorless LDO. The LDO structure is basically based on the flipped voltage follower [11], which is a modified structure of the super source follower [6]. $V_{\rm IN}$ is the unregulated input voltage of the LDO. $\rm M_P$ is the power transistor, while $\rm M_{C1}$ and $\rm M_{C2}$ form a folded error amplifier in the common-gate configuration [10]. The source of $\rm M_{C1}$ detects the LDO output for comparing with a control voltage $(V_{\rm SET})$ defined at the gate of $\rm M_{C1}$. An error signal is then generated at the gate of the power transistor to achieve closed-loop voltage regulation by the negative feedback. The output impedance of the LDO is reduced drastically by the loop gain of the shunt feedback [6]. Since there is no large output capacitor in an output-capacitorless LDO, the shunt feedback can push the pole created at the LDO output away from $BW_{\rm L}$ (it is noted that the parasitic capacitance from the power line does not affect the closed-loop stability, as its value is, in general, in the order of pF or nF at most) [10]. Generally, $BW_{\rm L}$ is wide, as the dominant pole is a function of the gate capacitance of the power transistor $(C_{\rm par})$, which is much smaller than the value of the output capacitance typically in the order of μF [8]–[10]. Thus, the transient response of the LDO shown in Fig. 1 is dominated by the SR_G limit.

There are several reported approaches to solve the problem. Hazucha *et al.* proposed to use heavy bias current of 6 mA,

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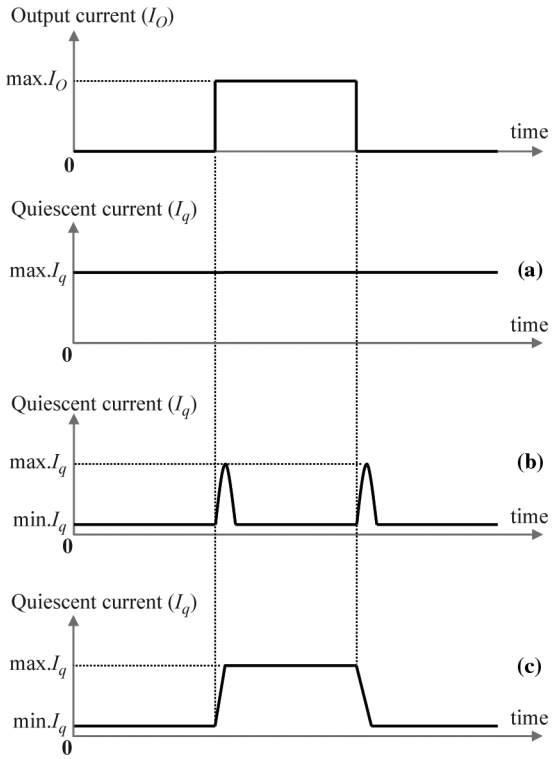

Fig. 2. Relationship between the output current and the quiescent current of the LDO (a) constant biasing [8] (b) dynamic biasing [9] (c) current-efficient current buffer [1], [12].

where the bias current is independent of the output current as shown in Fig. 2(a), and connect a 600-pF on-chip output capacitor to their LDO, implemented in CMOS 90-nm technology, to deliver a maximum output current of 100 mA [8]. However, this approach is not always applicable to the power-saving, chip-area-limited SoC designs implemented in inexpensive technologies. In [9], Man *et al.* reported to use dynamic biasing, so more bias current is used only at the transient instant when the output current is changed, as shown in Fig. 2(b). The error amplifier has a push-pull output stage to inject and withdraw more current for charging and discharging $C_{\rm par}$ during the transient instant. The push-pull output stage is activated by a differential-input common-gate amplifier. This approach enables higher bias current to solve the SR_G-limit problem. However, the differential common-gate amplifier has limited input common-mode range and, most importantly, limited bandwidth. The fast changing voltage spike cannot be detected effectively by the differential common-gate amplifier. As a result, more power applied to the amplifier is needed in order to achieve significant improvement of the transient response. In addition, this approach is not applicable when $V_{\rm O}$ is a small value. This situation happens when providing an adaptive supply for a power-saving SoC design. Another approach is to increase the bias current according to the magnitude of the output current [1], [12], as shown in Fig. 2(c). This method is not as good as the adaptive-biasing technique reported in [9], as the bias current remains high in the steady state when the output current does not reach the minimum.

According to the brief review, it is obvious that the extra bias current is only needed during the transient instant to solve the SR_G-limit problem. It is not necessary to keep the bias current high in the steady state. The adaptive biasing technique reported in [9] enables this important advantage, but it suffers from the slow response and the limited input range of the differential common-gate input stage. To solve this problem, a simple and effective voltage-spike detection circuit applied to the LDO structure shown in Fig. 1 is proposed in this paper. The proposed voltage-spike detection is based on capacitive coupling. The detection circuit makes use of the rapid transient voltage at the LDO output to increase the bias current momentarily. Hence, the transient response of the LDO can be significantly enhanced due to the improvement of SR_G. Moreover, the small-signal response is also improved by the capacitive-coupling feature.

In this paper, Section II presents the small-signal and large-signal responses of the output-capacitorless LDO. Section III introduces the proposed voltage-spike detection circuit and its design details. Experimental results are presented in Section IV. Finally, the conclusion of this paper is given.

II. Small-Signal and Large-Signal Responses of the Output-Capacitorless LDO

Referring to the output-capacitorless LDO shown in Fig. 1, when the output current of the LDO ($I_{\rm O}$) suddenly increases (or decreases), the LDO cannot respond to the change for decreasing (or increasing) the gate voltage of $\rm M_P$ to increase (or decrease) its drain current instantaneously due to the finite $BW_{\rm L}$ of the LDO [1]–[5]. When the LDO is able to respond, the decrease (or increase) of the gate voltage of MP is then constrained by the limited SR_G. Since an output-capacitorless LDO does not have a large off-chip output capacitor to provide charges to the load circuit (or accept the excess current from $\rm M_P$) at the transient instant, $V_{\rm O}$ drops (or increases) dramatically and a large voltage spike is generated.

In fact, the closed-loop small-signal response of the output-capacitorless LDO is mainly determined by $\rm M_{C1}$, since $\Delta V_{\rm O}$ changes its $V_{\rm SG}$ to generate a small-signal current for voltage regulation. As a result, the transconductance of $\rm M_{C1}$ should be large in order to improve the small-signal response. This implies that more power is needed to apply to the LDO to achieve faster small-signal response.

The output-capacitorless LDO undergoes large-signal response when there is rapid and large change of $I_{\rm O}$. Fig. 3(a) and (b) shows the large-signal responses of the LDO when $I_{\rm O}$ suddenly increases and decreases, respectively. When $I_{\rm O}$ rapidly increases, the LDO cannot change $V_{\rm SG}$ of $\rm M_P$ instantaneously to provide current due to the large $C_{\rm par}$, and this situation causes $V_{\rm O}$ to drop. The drop of $V_{\rm O}$ reduces $V_{\rm SG}$ of $\rm M_{C1}$, and it causes $\rm M_{C1}$ to cut off momentarily. Thus, $I_{\rm BIAS2} - I_{\rm BIAS1}$ is the discharging current of $C_{\rm par}$.

Similarly, when $I_{\rm O}$ suddenly decreases, the LDO cannot reduce $V_{\rm SG}$ of $\rm M_P$ immediately and it makes $V_{\rm O}$ rise. The increase of $V_{\rm O}$ causes the drain voltage of $\rm M_{C1}$ to increase due to the property of the common-gate amplifier. Since the source terminal of $\rm M_{C2}$ has low resistance ($\sim 1/g_m$), the increase of the drain voltage of $\rm M_{C1}$ is nearly the same as the increase of $V_{\rm O}$. This causes $\rm M_{C2}$ to cut off momentarily. Therefore, the charging current of $C_{\rm par}$ is $I_{\rm BIAS1}$.

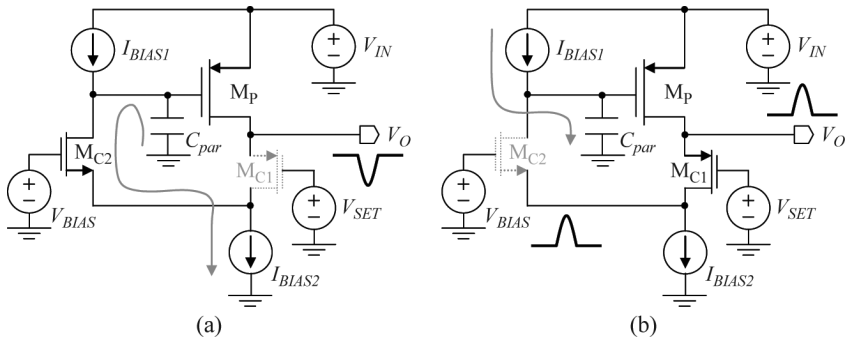

Fig. 3. Large-signal response of the output-capacitorless LDO (a) undershoot (b) overshoot.

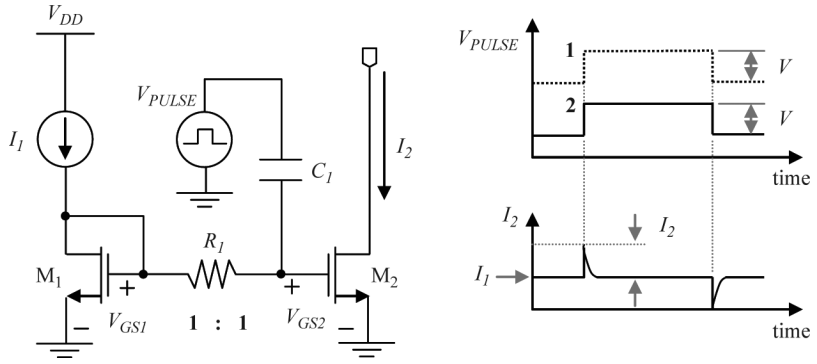

Fig. 4. Current mirror with high-pass RC-network to momentarily increase the bias current.

From the above analysis, both $I_{\rm BIAS1}$ and $I_{\rm BIAS2}$ determine SR_G. Higher bias current does enhance the transient response of the LDO, but this approach consumes unnecessary power since there is no charge/discharge mechanism of $C_{\rm par}$ in the steady state. Moreover, the discharging current of $C_{\rm par}$ is $I_{\rm BIAS2} - I_{\rm BIAS1}$. Therefore, the discharging capability of $C_{\rm par}$ cannot be fully utilized by solely increasing $I_{\rm BIAS2}$. Finally, the transistor size of $\rm M_P$ is very critical, since it determines the value of $C_{\rm par}$ or, in another point of view, the required amount of the bias current to solve the SR_G-limit problem. In 1-V or even sub-1V operation without low threshold-voltage devices, a larger transistor size is needed to compensate the low $V_{\rm IN}$ (the maximum allowable $V_{\rm SG}$ of $\rm M_P$) for delivering a large $I_{\rm O}$. Low and steady quiescent current is not possible to achieve fast transient response of the sub-1-V LDO since $C_{\rm par}$ is extremely large.

III. LDO With the Proposed Voltage-Spike Detection Circuit

The proposed voltage-spike detection circuit will be introduced in this section. The design and operation of the LDO with the proposed circuit will be discussed in detail.

A. Structure and Principle of Operation of the Proposed Voltage-Spike Detection Circuit

Fig. 4 illustrates the concept of the proposed direct voltage-spike detection circuit. The main idea of the circuit is to momentarily increase the bias current of the control circuit of the LDO when voltage spikes appear at the LDO output in order to overcome the problem of the SR_G limit due to the large $C_{\rm par}$ of $\rm M_P$. The circuit, in fact, is a simple current mirror formed by $\rm M_1$ and $\rm M_2$, where I_1 and I_2 are the input current and the output current of the current mirror, respectively. The major modification to this current mirror is the addition of two passive components, R_1 and C_1 [13]. The voltage source V_{PULSE} is used to demonstrate the voltage spike for investigating the effect to the change of I_2.

In the steady state, V_{PULSE} remains constant, and so $V_{\rm GS2}$ is defined by $V_{\rm GS1}$ to give $I_2 = I_1$. However, as shown by the timing diagrams in Fig. 3, when the amplitude of V_{PULSE} changes from low to high (ΔV) instantaneously, the rapid voltage change of V_{PULSE} is coupled to the gate of $\rm M_2$ directly due to the high-pass property of C_1. In addition, R_1 is chosen to be large for better isolation between $\rm M_1$ and $\rm M_2$ during the change of V_{PULSE}. As a result, when C_1 is chosen to be larger than $C_{gs1}+C_{gs2}$, the gate voltage of $\rm M_2$ is dominated by the coupled signal from C_1 in this instant, instead of the DC voltage provided by R_1. Thus, $V_{\rm GS2}$ is increased momentarily to increase I_2. The extra current (ΔI_2) can be found from

$$\begin{aligned} I_2+\Delta I_2 &= \frac{\mu_n C_{\rm OX}}{2}\cdot\left(\frac{W}{L}\right)_{\rm M2}\cdot(V_{\rm GS2}+\Delta V-V_{\rm TH})^2 \\ &= \frac{\mu_n C_{\rm OX}}{2}\cdot\left(\frac{W}{L}\right)_{\rm M2}\cdot\left[(V_{\rm GS2}-V_{\rm TH})^2+\Delta V^2\right. \\ &\qquad \left.+2\Delta V(V_{\rm GS2}-V_{\rm TH})\right] \quad (1) \end{aligned}$$

From (1), the magnitude of ΔI_2 is extracted and is given by

$$\Delta I_2 \approx \mu_n C_{\rm OX}\cdot\left(\frac{W}{L}\right)_{\rm M2}\cdot\left(V_{\rm GS2}+\frac{\Delta V}{2}-V_{\rm TH}\right)\Delta V \quad (2)$$

From (2), it is found that a larger W/L aspect ratio of the current mirror helps to increase ΔI_2 for injecting more transient current.

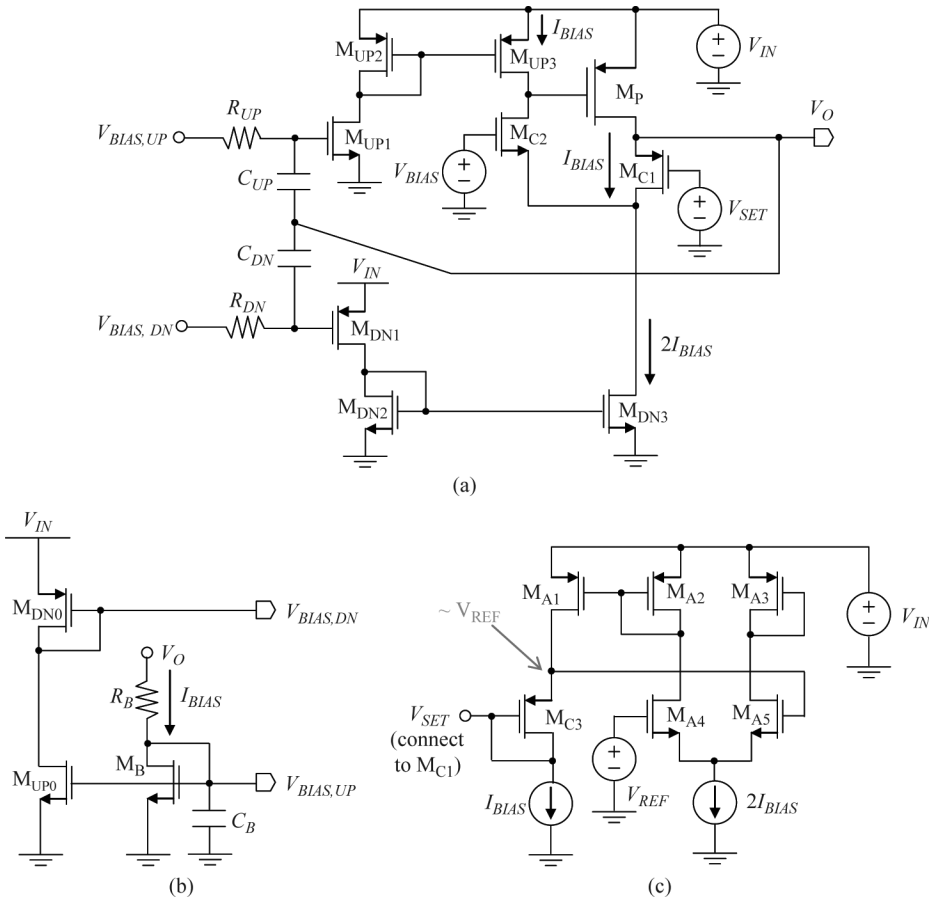

Fig. 5. Full circuit diagram of the LDO with the proposed voltage-spike detection circuit (a) LDO core (b) bias-current generator (c) control-voltage generator.

When V_{PULSE} stays at a constant voltage level (i.e. the steady state), C_1 is open-circuited and R_1 dominates. Thus, $V_{\rm GS2}$ is defined by $V_{\rm GS1}$ in the steady state to make $I_2 = I_1$ once again. Similarly, when V_{PULSE} changes from high to low, the rapid ΔV is coupled through C_1 to the gate of $\rm M_2$ and the coupled voltage signal decreases $V_{\rm GS2}$ to generate a smaller I_2. From the above analysis, the proposed direct voltage-spike detection circuit can provide auto shutdown of the bias-current boosting.

Finally, the coupling effect is independent of the DC value (but is limited by the breakdown voltage of the transistors) of V_{PULSE} (Curves 1 and 2 in Fig. 4) due to the high-pass characteristic of the capacitor. Therefore, the proposed detection method is suitable for detecting any output voltage level of the LDO.

B. LDO With the Proposed Voltage-Spike Detection Circuit

The LDO presented in this paper is formed by the proposed voltage-spike detection circuit, a bias-current generator and a control-voltage generator [10]. Their circuit implementations are shown in Fig. 5. Fig. 5(a) shows the modified LDO structure based on the LDO shown in Fig. 1. $\rm M_{UP1}$, $\rm M_{UP2}$ and $\rm M_{UP3}$ provide $I_{\rm BIAS1}$ to the LDO shown in Fig. 1, while $\rm M_{DN1}$, $\rm M_{DN2}$ and $\rm M_{DN3}$ give $I_{\rm BIAS2}$. The coupling capacitors, $C_{\rm UP}$ and $C_{\rm DN}$, as well as two resistors, $R_{\rm UP}$ and $R_{\rm DN}$, are included to the LDO to form the proposed voltage-spike detection circuit illustrated in Fig. 4. One of the two terminals of both $C_{\rm UP}$ and $C_{\rm DN}$ are connected to $V_{\rm O}$ to achieve direct detection of the voltage spikes created at the transient instant. Moreover, the voltage source $V_{\rm SET}$ is generated by the control-voltage generation circuit in Fig. 5(c).

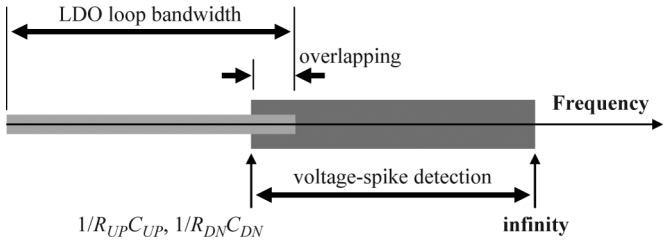

Fig. 6. Frequency range of operation of the LDO and the proposed voltage-spike detection circuit.

The bias-current generator shown in Fig. 5(b) provides two bias voltages, $V_{\rm BIAS,UP}$ and $V_{\rm BIAS,DN}$. To make the bias-current generator independent of the supply voltage, the regulated output voltage of the LDO is used for the bias-current generation. As shown in Fig. 5(b), $I_{\rm BIAS}$ is formed by R_B, $\rm M_B$ and $V_{\rm O}$, so that $I_{\rm BIAS} = (V_{\rm O} - V_{\rm SG,B})/R_B$ where $V_{\rm SG,B}$ is the source-to-gate voltage of $\rm M_B$. Since $V_{\rm O}$ is regulated, $I_{\rm BIAS}$ is supply-independent as $V_{\rm SG.B}$ is a constant when $I_{\rm BIAS}$ is once defined. A decoupling capacitor (C_B) is used to stabilize $I_{\rm BIAS}$. The accuracy of C_B is not important and it is 2 pF only in this design, since the value of $I_{\rm BIAS}$ is small and is about 1 μA in the LDO design.

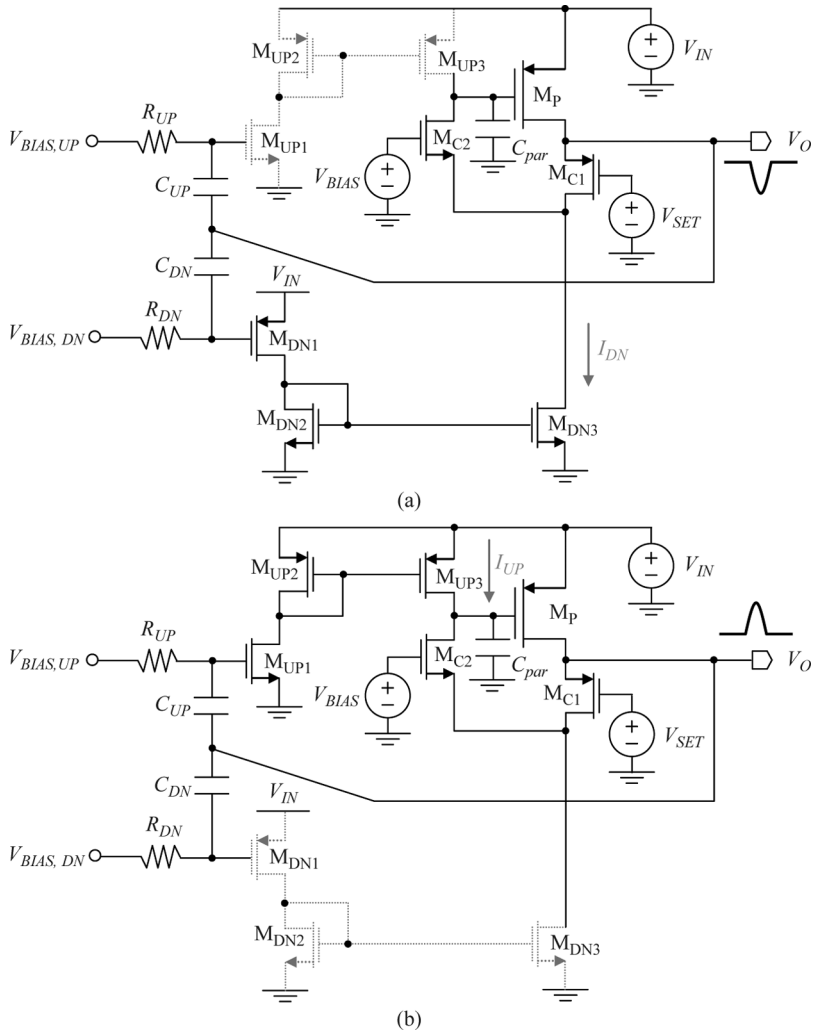

Fig. 7. Principle of operation of the proposed voltage-spike detection circuit. (a) Undershoot. (b) Overshoot.

The control-voltage generator shown in Fig. 5(c) is basically an amplifier with negative feedback. It occupies nearly the same chip area as the error amplifier inside a generic LDO. A temperature- and supply-independent reference voltage ($V_{\rm REF}$) is provided by a voltage-reference circuit. The source-to-gate voltage of $\rm M_{C1}$ ($V_{\rm SG,C1}$) is connected at the output of the LDO, so that $V_{\rm O} = V_{\rm SET} + V_{\rm SG,C1}$. Since $V_{\rm SET} = V_{\rm REF} - V_{\rm SG,C3}$ where $V_{\rm SG,C3}$ is the source-to-gate voltage of $\rm M_{C3}$, $V_{\rm SG,C1} = V_{\rm SG,C3}$ is needed to achieve $V_{\rm O} = V_{\rm REF}$. As a result, the transistor sizes of $\rm M_{C1}$ and $\rm M_{C3}$ are the same and the current flowing through $\rm M_{C1}$ and $\rm M_{C3}$ are designed to be $I_{\rm BIAS}$.

C. Principle of Operation of the LDO With the Proposed Voltage-Spike Detection Circuit

This section includes the small-signal and large-signal analysis, as well as the design details of the LDO with the proposed voltage-spike detection circuit.

1) Small-Signal Response: For the output-capacitorless LDO with the proposed voltage-spike detection circuit shown in Fig. 5, the insertion of $C_{\rm UP}$ and $C_{\rm DN}$ (high-pass components) provides two quick paths and skip $\rm M_{C1}$ (a low-pass and bandwidth-limited component) to detect $\Delta V_{\rm O}$. The drop (or increase) of $V_{\rm O}$ is detected by $C_{\rm UP}$ to decrease (or increase) the gate voltage of $\rm M_{UP1}$ and subsequently decrease (or increase) the gate voltage of $\rm M_P$ through the signal path formed by $\rm M_{UP2}$ and $\rm M_{UP3}$. Similarly, $C_{\rm DN}$ also senses the drop (or increase) of $V_{\rm O}$ to decrease (or increase) the gate voltage of $\rm M_{DN1}$ and finally decreases (or increase) the gate voltage of $\rm M_P$ via the signal path formed by $\rm M_{DN2}$, $\rm M_{DN3}$ and $\rm M_{C2}$.

The selection of the values of $C_{\rm UP}$ and $C_{\rm DN}$, as well as $R_{\rm UP}$ and $R_{\rm DN}$ can be done by investigating their corner frequencies and $BW_{\rm L}$ of the LDO. Fig. 6 shows a simple figure to illustrate the relationship. Since $BW_{\rm L}$ of the LDO is low-pass and limited while $C_{\rm UP}$ & $R_{\rm UP}$ and $C_{\rm DN}$ & $R_{\rm DN}$ are high-pass with the corner frequencies equal to $1/C_{\rm UP}R_{\rm UP}$ and $1/C_{\rm DN}R_{\rm DN}$, it is designed to make the corner frequencies lower than $BW_{\rm L}$. This approach does virtually extend the loop-bandwidth of the LDO, and it makes sure that either the LDO itself or the proposed voltage-spike detection circuit responds to the small-signal changes of $V_{\rm O}$. The typical $BW_{\rm L}$ of a LDO with 100-mA output capability is about 200 kHz to 1 MHz [1]–[5]. Assuming the corner frequency is set to be 100 kHz, the required $C_{\rm UP}$ ($C_{\rm DN}$) and $R_{\rm UP}$ ($R_{\rm DN}$) are 3 pF and 530 kΩ, respectively. The accuracy and the matching of the values are not important,

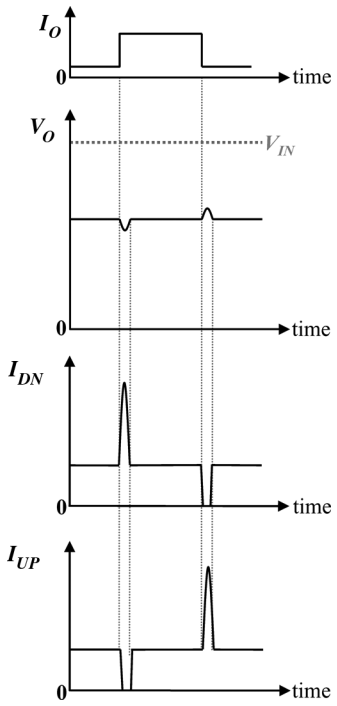

Fig. 8. Drain-current change of $\mathrm{M_{UP3}}$ and $\mathrm{M_{DN3}}$ during the load transient response.

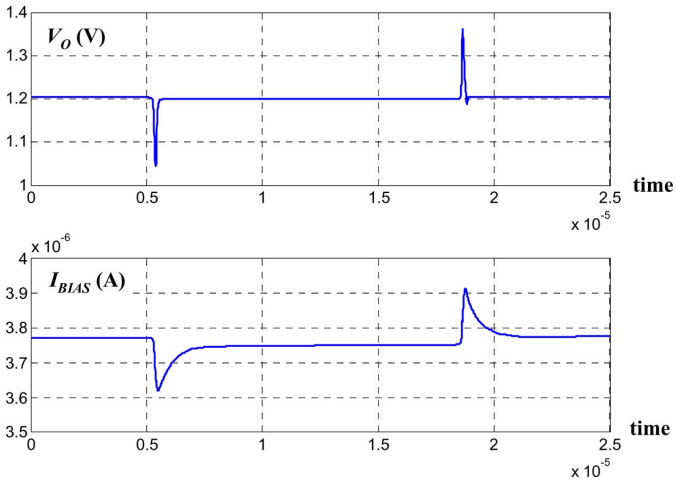

Fig. 9. Simulated change of I_{BIAS} under the change of V_{O}.

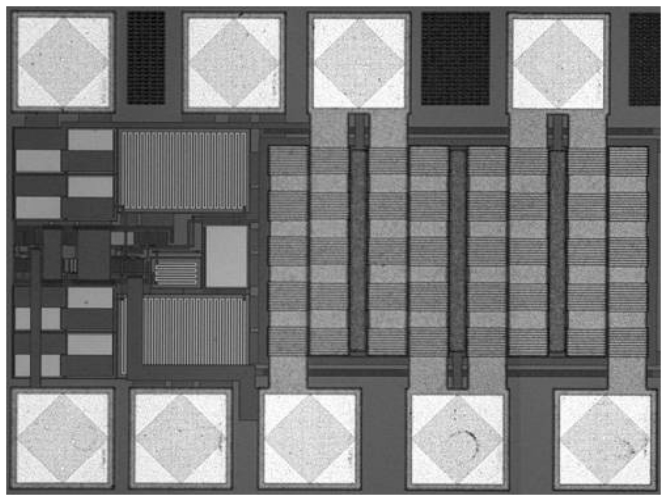

Fig. 10. Micrograph of the LDO with the proposed voltage-spike detection circuit.

and so C_{UP} and C_{DN} are implemented by poly-poly capacitor and they can be implemented by MOS capacitors to reduce chip area in triple-well technologies. R_{UP} and R_{DN} can be implemented by MOSFET or NWELL-resistor to reduce the chip area.

2) Large-Signal Response: The large-signal response is illustrated in Fig. 7, and the corresponding transient responses of the drain current of $\mathrm{M_{UP3}}$ and $\mathrm{M_{DN3}}$ are shown in Fig. 8. In Fig. 7(a), when I_{O} increases suddenly, V_{O} drops rapidly. The change is then sensed by C_{UP} and C_{DN}, and is coupled to the gates of $\mathrm{M_{UP1}}$ and $\mathrm{M_{DN1}}$. Due to coupling effect of C_{UP}, V_{GS} of $\mathrm{M_{UP1}}$ decreases, and thus the current of $\mathrm{M_{UP3}}$ is reduced. At the same time, C_{DN} passes the change to the gate of $\mathrm{M_{DN1}}$. It leads to a drastically and momentarily increase of V_{SG} of $\mathrm{M_{DN1}}$ to make I_{DN} increase. Therefore, a push-pull output stage is formed by $\mathrm{M_{UP3}}$ and $\mathrm{M_{DN3}}$ to discharge C_{par}. When V_{O} is regulated back to the nominal value, the bias condition of the circuit returns to the normal. This shows the auto-shutdown feature of the proposed bias-current boosting.

Similarly, as shown in Fig. 7(b), when I_{O} suddenly decreases, V_{O} increases. This change is coupled through C_{UP} and C_{DN} again to increase V_{GS} of $\mathrm{M_{UP1}}$ and reduce V_{SG} of $\mathrm{M_{DN1}}$ simultaneously. Therefore, a push-pull output stage is formed momentarily, since $\mathrm{M_{UP3}}$ provides more drain current while $\mathrm{M_{DN3}}$ gives less drain current. C_{par} is charged up to reduce the current provided by $\mathrm{M_P}$ to the load. The operation is automatically shut down again when V_{O} returns to the steady state.

Finally, as mentioned previously, C_B in Fig. 5(c) is used to maintain the bias current during large-signal response. In Fig. 9, a simulation shows the change of V_{O} not affecting I_{BIAS} much.

IV. Experimental Results

The proposed voltage-spike detection circuit has been applied to a LDO design in Fig. 5 fabricated by austriamicrosystems (AMS) 0.35-μm CMOS process. The applications of the proposed LDO are for the analogue and RF parts in a SoC system. In order to make a fair comparison on the transient performance, a LDO without the proposed voltage-spike detection circuit is also implemented. The only difference is that both C_{UP} and C_{DN} are removed to disable the detection circuit, while the circuit structure, all transistor sizes and the bias current of both LDO designs remain the same. Fig. 10 shows the micrograph of the LDO with the proposed detection circuit. Table I summarizes the key information. The threshold voltages of the nMOSFET and pMOSFET are about 0.5 V and -0.65 V, respectively. Since the threshold voltage of the pMOSFET is -0.65 V, the overdrive voltage is not high when the supply voltage is low (e.g., 1 V). Therefore, the required transistor size of $\mathrm{M_P}$ is 30000 μm/0.35 μm to provide high I_{O}. The chip area is 597 μm $\times$ 260 μm, excluding the test pads. The chip area occupied by the control-voltage generator is less than 2% of the overall chip area. The transient responses of both LDOs

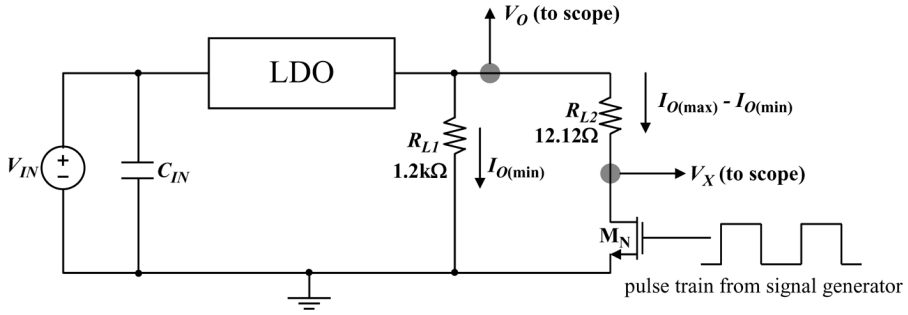

Fig. 11. Measurement setup to investigate the load-transient response.

TABLE I
SUMMARY OF THE DESIGN PARAMETERS

Technology	AMS CMOS 0.35-μm 2P4M
V_{THN}	~ 0.5 V
V_{THP}	~ -0.65 V
Power-transistor size	30000 μm / 0.35 μm
Chip area	597 μm × 260 μm (excluding the test pads)
Output capacitor	Not required Stable even connected with a 100-pF or 1-nF capacitor

are measured. Both LDOs do not need an off-chip capacitor to achieve stability. It is also found that the LDOs are stable when the output parasitic capacitance due to the power line, which is located at the output of the LDO, is non-zero (two cases are tested: 100 pF and 1 nF).

Fig. 11 shows the experimental setup to measure the load-transient response of both LDOs. The minimum output current ($I_{\mathrm{O(min)}}$) is defined by R_{L1} connected between the LDO output and the ground, and so $I_{\mathrm{O(min)}} = V_{\mathrm{O}}/R_{\mathrm{L1}}$. To define the maximum output current ($I_{\mathrm{O(max)}}$), R_{L2} and an integrated nMOSFET ($\mathrm{M_N}$) are used. The purpose to integrate $\mathrm{M_N}$ on the chip for the measurement is to minimize the associated parasitic capacitance and resistance for obtaining more accurate transient results in the range of micro- or nano-second. The gate of $\mathrm{M_N}$ is driven by a signal generator with a periodic square wave, so that $\mathrm{M_N}$ is turned on and off alternatively. By applying a large gate voltage to $\mathrm{M_N}$ (3.3 V is used in the measurement), the on-resistance of $\mathrm{M_N}$ is 55 mΩ, which is much smaller than R_{L2} (12.12 Ω), and thus the effect from $\mathrm{M_N}$ can be ignored. Thus, the value of the current flowing through R_{L2} is $I_{\mathrm{O(max)}} - I_{\mathrm{O(min)}} = V_{\mathrm{O}}/R_{\mathrm{L2}}$. From Fig. 11, V_{O} is directly extracted and monitored by the scope, while I_{O} is obtained indirectly from the node voltage V_X. Since $V_X = V_{\mathrm{O}} - I_{\mathrm{O}}R_{\mathrm{L2}}$, $V_X \propto -I_{\mathrm{O}}$. Therefore, the extracted V_X is scaled and inverted by the scope to illustrate the transient change of I_{O}.

Different combinations of the input voltage, the output voltage and the output current are tested. The measurement results are shown in Figs. 12, 13, and 14. The test cases are:

1) $V_{\mathrm{IN}} = 1.4$ V, $V_{\mathrm{O}} = 1.2$ V and $I_{\mathrm{O(max)}} = 100$ mA (Fig. 12);
2) $V_{\mathrm{IN}} = 1\,\mathrm{V}, V_{\mathrm{O}} = 0.8\,\mathrm{V}$ and $I_{\mathrm{O(max)}} = 66.7\,\mathrm{mA}$ (Fig. 13);
3) $V_{\mathrm{IN}} = 0.95$ V, $V_{\mathrm{O}} = 0.7$ V and $I_{\mathrm{O(max)}} = 58.3$ mA (Fig. 14).

The quiescent current and the current efficiency of each case is shown in Table II. The reason for the difference of $I_{\mathrm{O(max)}}$

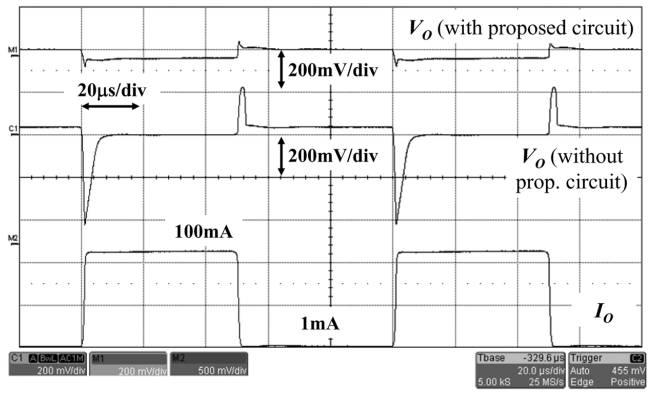

Fig. 12. Comparison of two LDOs with and without the proposed voltage-spike detection circuit, where $V_{\mathrm{IN}} = 1.4$ V, $V_{\mathrm{O}} = 1.2$ V, $d\mathrm{I_O}/\mathrm{d}t = 99$ mA/1 μs.

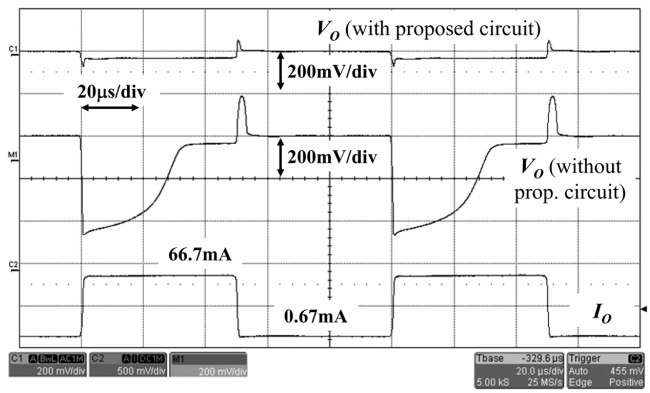

Fig. 13. Comparison of two LDOs with and without the proposed voltage-spike detection circuit, where $V_{\mathrm{IN}} = 1\,\mathrm{V}, V_{\mathrm{O}} = 0.8\,\mathrm{V}, \mathrm{d}I_{\mathrm{O}}/\mathrm{d}t = 66\,\mathrm{mA}/1\,\mu\mathrm{s}$.

at different V_{IN} and V_{O} is that the values of R_{L1} and R_{L2} are fixed in the measurement (as shown in Fig. 11). In fact, when the size of $\mathrm{M_P}$ is fixed, $I_{\mathrm{O(max)}}$ is limited by V_{IN} (due to the maximum allowable V_{SG} of $\mathrm{M_P}$) and it is also constrained by the dropout voltage $(V_{\mathrm{IN}} - V_{\mathrm{O}})$. Therefore, at $V_{\mathrm{IN}} = 0.95\,\mathrm{V}$, the value of $I_{\mathrm{O(max)}}$ is the lowest and the required dropout voltage is 0.25 V. Moreover, Fig. 5(c) shows that the quiescent current of the LDOs is a function of V_{O}. Therefore, the quiescent current at $V_{\mathrm{O}} = 0.7$ V is the lowest among the three test cases. There is only 14 μA to drive the large C_{par} of $\mathrm{M_P}$ with size of 30000 μm/0.35 μm. This implies the SR_G limit becomes more serious when V_{O} is lower. The above results demonstrate the impact of the lower quiescent current to the transient response

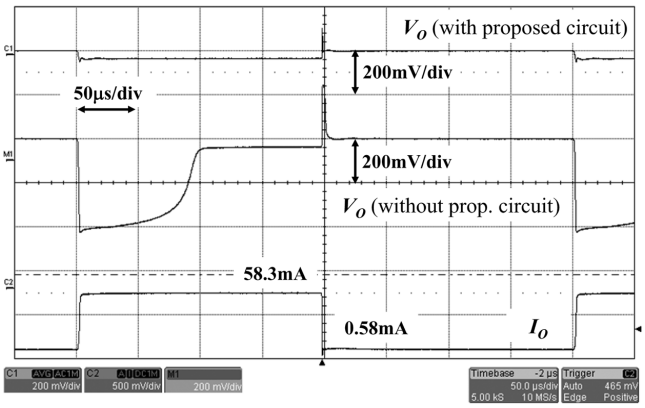

Fig. 14. Comparison of two LDOs with and without the proposed voltage-spike detection circuit, where $V_{\rm IN} = 0.95$ V, $V_{\rm O} = 0.7$ V, $\mathrm{d}I_{\rm O}/\mathrm{d}t = 57.7$ mA/1 μs.

TABLE II
SUMMARY OF THE MEASUREMENT CONDITIONS OF THE LDO WITH THE PROPOSED VOLTAGE-SPIKE DETECTION CIRCUIT

Input voltage V_{IN}	Output voltage V_O	Max. output current $I_{O(max)}$	Quiescent current I_Q	Current efficiency $I_O/(I_O+I_Q)$
1.4 V	1.2 V	100 mA	43 µA	99.957%
1 V	0.8 V	66.7 mA	19 µA	99.972%
0.95 V	0.7 V	58.3 mA	14 µA	99.976%

of the LDOs with and without the proposed voltage-spike detection circuit.

In Figs. 12, 13 and 14, the measurement results of the LDO with and without the proposed direct voltage-spike detection circuit at different $V_{\rm IN}$, $V_{\rm O}$ and $I_{\rm O(max)}$ are shown. There are three waveforms in each figure:

1) $V_{\rm O}$ of the LDO with the proposed voltage-spike detection circuit (top);
2) $V_{\rm O}$ of the LDO without the proposed voltage-spike detection circuit (middle);
3) $I_{\rm O}$ of both LDOs (bottom).

In all cases, $I_{\rm O}$ switches between the maximum and the minimum in 1 μs.

In Fig. 12, the measurement condition is $V_{\rm IN} = 1.4$ V, $V_{\rm O} = 1.2$ V and $I_{\rm O(max)} = 100$ mA. The quiescent current is 43 μA. The undershoot, the overshoot and the recovery time of the LDO without the proposed detection circuit are about 420 mV, 200 mV and 10 μs, respectively, while those of the LDO with the proposed circuit are about 70 mV, 70 mV and 3 μs only, respectively.

Similarly, in Fig. 13 ($V_{\rm IN} = 1$ V, $V_{\rm O} = 0.8$ V and $I_{\rm O(max)} = 66.7$ mA) and Fig. 14 ($V_{\rm IN} = 0.95$ V, $V_{\rm O} = 0.7$ V and $I_{\rm O(max)} = 58.3$ mA), the quiescent current in both cases is reduced to 19 μA and 14 μA, respectively. The SR_G-limit problem of the LDO without the proposed detection circuit becomes more obvious. The undershoot of $V_{\rm O}$ is about 420 mV, and the recovery time is more than 30 μs (Fig. 13) and about 100 μs (Fig. 14). However, the LDO with the proposed detection circuit at different conditions has no significant difference in the transient response.

V. CONCLUSION

This paper presented a direct voltage-spike detection circuit to improve the transient response of the output-capacitorless LDO. The proposed detection circuit consists of two high-pass coupling capacitors, which are able to detect the fast-changing voltage spikes at the LDO output and adjust the bias current of the control circuit momentarily to improve both the small-signal and large-signal responses. The proposed circuit does not increase the quiescent current in the steady state, and it solves the narrow loop bandwidth and the slew-rate limit problems of the conventional LDO by applying a simple and effective modification to the LDO circuit. Moreover, the accuracy of the values of the added components is not important.

The measurement results have proven that the overshoot, the undershoot and the recovery time of the LDO have been improved significantly by the proposed voltage-spike detection circuit. Even though the threshold voltage of the power transistor is high, the input voltage of the LDO is lower than 1 V and the quiescent current is low.

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