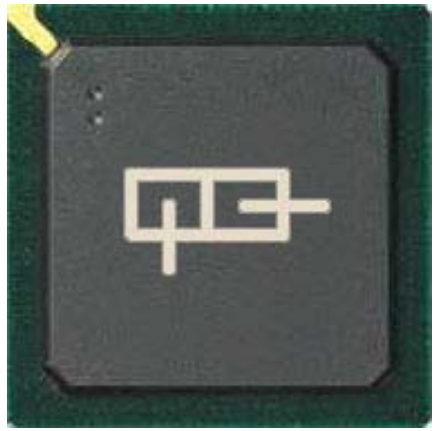
# The CADR2 Project



## Reimplementing CADR on an FPGA

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# Project Constraints

- Three people
- Limited time
- Limited VHDL design experience
- No funding

We need to save time and set a goal that can actually be reached.

# Choosing an architecture

Designing a new architecture does take too much time, so we decided to reimplement a classic design.

This remplementation of a classic design will then be usable as a starting point for change.

# Architectural Options

- CADR – Open Source, least sophisticated
- TI Explorer II – Well researched, legal status questionable
- Symbolics 3600 – Loads of documentation, but much of that only in scanned form, legal status: We can´t do it.
- Xerox – Almost nothing is known, even though there is an emulator.

# The choice

Given this, CADR is the natural choice for a research project that will be run in the public.

All system code including the microcode and a software simulator for the hardware is available.

The project team can concentrate on getting the hardware done.  Design discussions are left for later.

# Performance

- The original TTL implementation ran at less than 5 Mhz
- We expect to be able to run the machine at 50 Mhz

Compiled LISP on Ghz systems with modern compilers will be faster.  But our system will draw only 2 Watts

# Target hardware configuration

We target the hardware that the team members have available. Thus, the basic setup will be:

Target: Spartan-3/Virtex4 FPGA

Memory: DDR SDRAM

Disk: Compact-Flash

Ethernet, VGA, PS/2 Keyboard

# Reimplementing the hardware

- The original hardware will be emulated so that the original drivers can be used
- The simulator code will function as part of the documentation

# Project setup and Timeframe

We will work off a subversion repository located at svn://cadr2.bknr.net/

The core team will communicate through a mailing list that will be archived.

The project´s home page will be at http://cadr2.bknr.net/

We expect to have the basic system running by October 2006.

Hold your thumbs!