



- Notes:
1. This schematic is not finished yet
 2. DET_IN_TRIG signal is -10 uSec
 3. Mega328p ADC:
 - Sample & Hold 1.25 uSec
 - Full 10-bit sample time: 50 uSec @ 250 kHz ADC clock
 - Full 8-bit sample time: 10 uSec @ 2 MHz ADC clock - fast mode
 4. Mega328p interrupt response time: 4 cycles + -16 cycles ISR preamble - -3 uSec until ADC conversion starts
 5. Potentially replaceable with Mega4809 for 0.5 uSec DET_IN_TRIG response

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