Compact Modeling of TFTs for Flexible and Large Area Electronics

Benjamin Iñiguez

Department of Electronic Engineering (DEEEA), Universitat Rovira i Virgili, Tarragona, Catalonia, Spain.

E-mail: benjamin.iniguez@urv.cat

Goals

- Review of compact modeling issues affecting different types of TFTs: a-Si, poly-Si, nc-Si, oxide, organic, polymer TFT
- Presentation of universal modeling and parameter extraction techniques for all types of TFTs

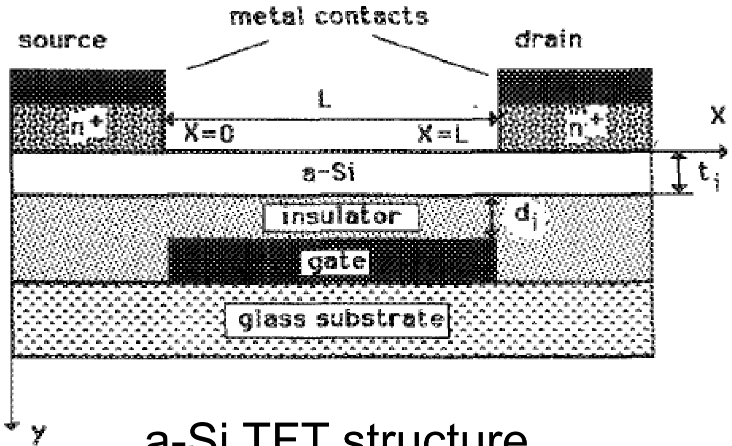
Outline

- Introduction
- TFT modeling issues
  - Amorphous TFT
  - Polycristalline TFT
  - Nanocrystalline TFT
  - Organic TFT
  - Oxide TFT
- Unified TFT modeling and parameter extraction techniques
- Results
- Conclusions

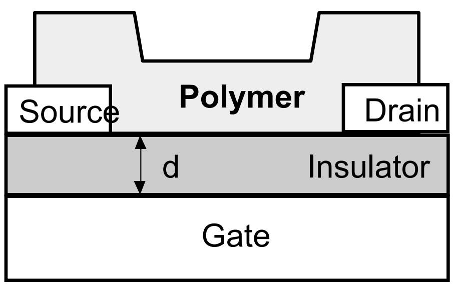
Introduction

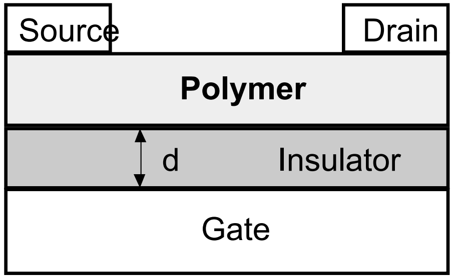
- TFTs are the essential devices in large area low cost circuits (drivers of AMLCDs, transistors for flexible electronics,...)
- **a-Si TFTs** are the most commonly used TFTs
  - **Advantages**: Possibility for deposition over large surfaces at a relatively low temperature.
  - **Disadvantages**: Low mobility, and degradation under illumination and bias stress.
- **Poly-Si TFTs** do not present the disadvantages of a-Si TFTs, and have higher mobility.
  - **Disadvantages**: High temperatures are used for the crystallization of the a-Si:H material.

Introduction



a-Si TFT structure





organic TFT structures

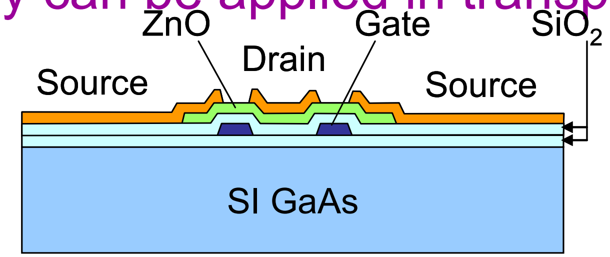
Introduction

- An alternative to both a-Si and poly-Si TFTs are **nanocrystalline Si** TFTs (nc-Si TFTs), which can obtained at low substrate temperatures and over large areas
  - nc-Si films consist of small Si crystallites, embedded in amorphous silicon. Therefore, properties of nc-Si TFTs lay between those of a-Si and poly-Si TFTs

- **Organic TFTs** have emerged as potential challengers to a-Si TFTs, because of their low power consumption and cost, compatibility with flexible substrates and printing processes
  - They combine the electrical properties of inorganic semiconductors with the simple technological processing of plastics
    - They allow flexible, light and low cost applications in large areas

Introduction

- Another alternative: oxide semiconductor TFTs, such as ZnO TFTs, GIZO and HIZO TFTs:
  - They can be amorphous, nanocrystalline or polycrystalline
  - They can be deposited over large and flexible substrates at low temperatures, and also can be printed
  - They can be applied in transparent electronics



Introduction

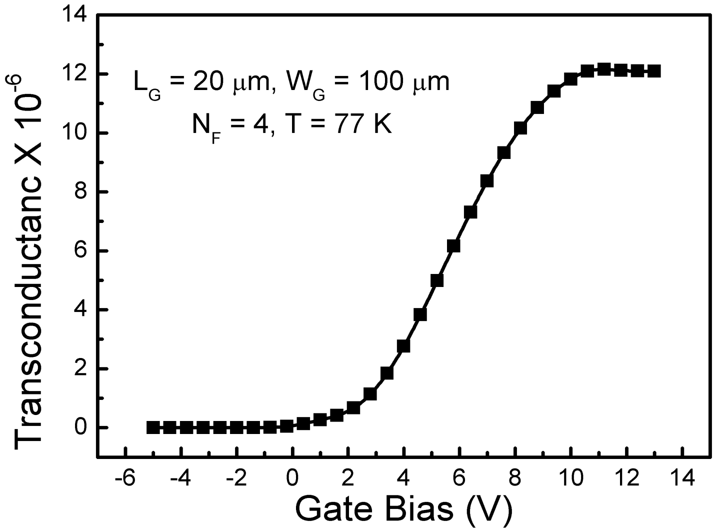
- **The huge increase of the applications of Thin-Film Transistors (TFTs) for large-area and flexible electronics makes it necessary to have accurate compact models of these devices**

- However, accurate TFT modeling is a quite complex task:
  - presence of many special physical phenomena
  - bias and geometry dependence of many parameters

Introduction

- **Examples of special effects**
  - Voltage drop at the series resistance
  - Nonlinear contact effects
  - Bias-dependences of several key parameters
    - Field-effect mobility
    - Threshold voltage
    - Series resistance
  - Frequency dispersion

Introduction



Mobility discussion first requires on accurate extraction method.

Difference with SOI: large gap between V_T and g_m peak!

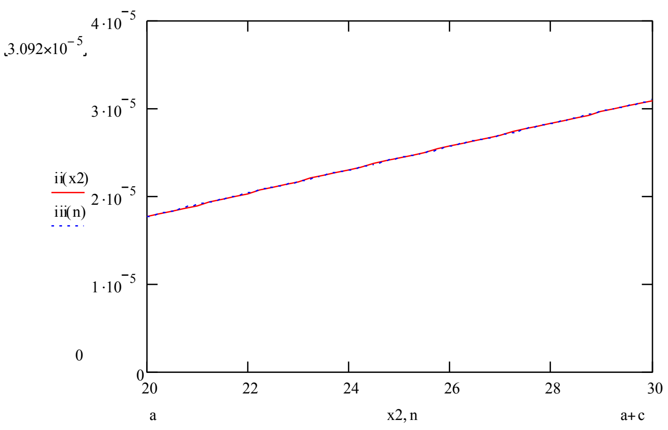
Mobility expression in SOI cannot explain this gap

$$\mu_{eff} = \frac{2\mu_0}{1+\theta(V_G - V_T)}, \qquad Y = \sqrt{\frac{W}{L} C_o x V_D \mu_0} \left(V_G - V_T\right)$$

The Y-function, $Y = I_D / \sqrt{g_m}$, cannot be applied as in SOI!

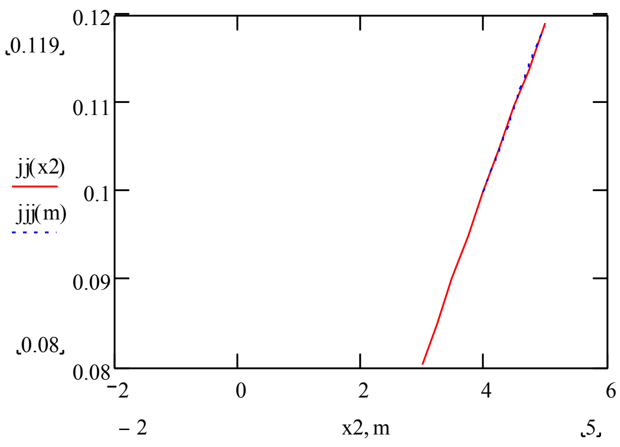
Introduction

- Example: **TFT field effect mobility is a power law of V_{gs}-V_T**



a-Si TFT above threshold

$$ii\left(V_{gs}\right) = I^{1/(\gamma+1)}$$



a-Si TFT below threshold

$$jj\left(V_{gs}\right) = I^{1/(\gamma_b+1)}$$

Poly-Si TFT

- Conduction mechanisms in poly-Si TFTs: **drift-diffusion in the grains**, and **thermionic emission in the grain boundaries**
- Effective medium approach: in order to derive a charge control model, in Poisson's equation the non-uniform poly-Si sample can be treated as some uniform effective medium with effective material properties
- Poly-Si TFT modeling is developed using a drift-diffusion formulation, in which the effect of the grain boundary potential barrier is included in the expression of the field-effect mobility

Poly-Si TFT

- In the subthreshold regime, diffusion dominates:

$$I_{sub} = \mu_s C_{ox} \frac{W}{L} (\eta V_{th})^2 \exp\left(\frac{V_{gs} - V_T}{\eta V_{th}}\right)\left[1 - \exp\left(\frac{-V_{ds}}{\eta V_{th}}\right)\right]$$

- Above threshold there is a significant number of free carriers and the drain current is given by an expression similar to that used for crystalline MOSFETs.

$$I_a = \mu_{FET} C_{ox} \frac{W}{L}\left(V_{gt} - \frac{V_{dse}}{2\alpha_{sat}}\right) V_{dse}$$

- where μ_{FET} is the gate voltage dependent field-effect mobility that includes the effects of the trap states, α_{sat} is the body effect parameter. It increases with the gate voltage until it saturates.
- The leakage well below threshold is due to thermionic field emission through the grain boundary trap sites and is modeled using an additional term

Poly-Si TFT

$$\frac{1}{\mu_{eff}} = \frac{1}{k(V_G - V_T)^m} + \frac{1}{\mu_0}$$

Two limiting mechanisms: potential barriers + regular transport

The model also accounts for mobility degradation at high field

$$\frac{1}{\mu_{eff}} = \left[\frac{1}{k(V_G - V_T)^m} + \frac{1}{\mu 0}\right]\left[1 + \theta(V_G - V_T)\right]$$

$$\frac{1}{I_D} = \frac{1}{\left(\frac{C_{ox} W V_D}{L}\right)\mu_{eff}(V_G - V_T)}$$

$$\left.\begin{array}{r} k : low - field\ mobility\ \text{constant} \\ m : low - field\ mobility\ power\ \text{law exponent} \end{array}\right\} : \text{related to grain boundaries barriers}$$

$\mu_0 : low - field\ mobility$ (as in SOI)

Θ accounts for high field mobility degradation (surface roughness scattering)

Poly-Si TFT

- We use a unified expresion of the drain current valid from subthreshold to above threshold (***RPI model***):

$$I_d = \frac{g_{ch} V_{ds}\left(1 + \lambda V_{ds}\right)}{\left[1 + \left(g_{ch} V_{ds} / I_{sat}\right)^m\right]^{1/m}}$$

- where

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}\left(R_s + R_d\right)} \qquad g_{chi} = q n_s \mu_{eff}\left(W / L\right)$$

- n_s is a unified expression of the sheet carrier density at the source end of the channel

Poly-Si TFT

- The expression of the saturation current I_{sat} is derived using an appropriate velocity-field relationship.
- The DIBL effect is included in the threshold voltage expression.
- λ accounts for channel length modulation
- The impact ionization is modeled by an additional term to the drain current:

$$I_D = I_d + \Delta I_{kink} = I_d(1+M)$$

$$M = \left(\frac{L_{kink}}{L}\right)^{m_{kink}} \left(\frac{V_{ds} - V_{dse}}{V_{kink}}\right) \exp\left(\frac{-V_{kink}}{V_{ds} - V_{dse}}\right)$$

a-Si TFT

- **Conduction** a-Si TFTs is due to the **drift of the induced free charge**
- As the gate voltage is increased, both trapped and free charge are induced.
- The field-effect mobility is proportional to the fraction of free charge, $n_{free}/(n_{free}+n_{trapped})$, and has the form, above threshold:

$$\mu_{FET} = \mu_n \left(\frac{V_{gs} - V_{T0}}{V_{AA}} \right)^{\gamma}$$

a-Si TFT

- Above threshold, the current is written as:

$$I_a = \mu_{FET} C_{ox} \frac{W}{L} \left(V_{gs} - V_{T0} - \alpha_{SAT} V_{dse} \right) V_{dse}$$

Below threshold, the current is a power law of V_{gs}-V_{fb} :

$$I_{sub} \propto \left(V_{gs} - V_{fb} \right)^{1+\gamma_b}$$

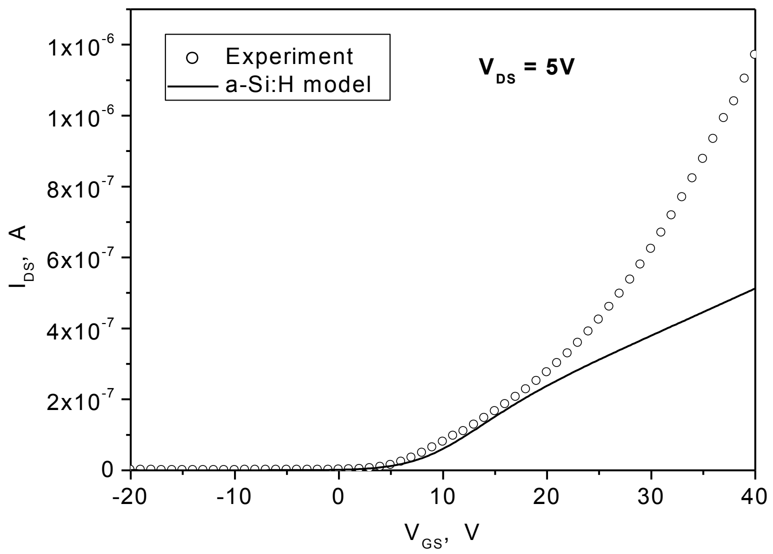
$$\mu_{FET}\left(V_{GS}, V_T\right) = \frac{\mu_{oo}}{V_{aa}^{\gamma_a}} \cdot (V_{GS} - V_T)^{\gamma_a}$$

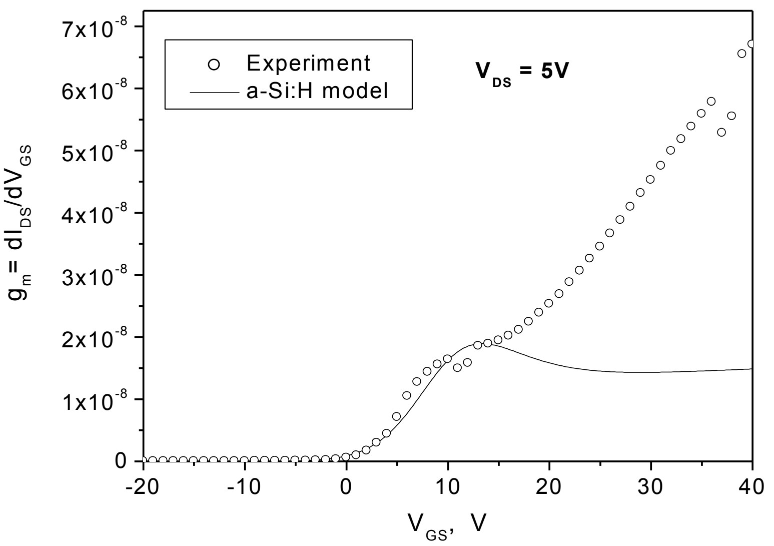
At large negative gate bias, a hole-induced drain leakage current caused by thermionic diffusion at the contacts, is accounted for

nc-Si TFT

- Modeling of nc-Si TFTs is based on the a-Si:H TFT modeling
- Using the a-Si:H TFT model, The modeled good agreement with the experimental curve up to a certain high voltage.
- Above a certain value of V_{GS} we observe a dramatic increase on the experimental drain current and transconductance, which are not reproduced by the model

nc-Si TFT





Experimental and modeled transfer and transconductance characteristics using the a-Si:H TFT model

nc-Si TFT

- This high V_{GS} regime is called the transitional (to crystalline behaviour) regime the traps are almost completely filled, $n_{trapped}$ remains constant and n_{free} increases with increasing V_{GS} similarly to crystalline MOSFET
- As a consequence, the field-effect mobility μ_{fet} will increase linearly with increasing V_{GS}
- In nc-Si:H the DOS is lower than in a-Si:H because of the higher internal atomic order, and we can expect that the transition to crystalline-like regime occurs at significantly lower gate voltages than in a-Si TFTs

nc-Si TFT

- To model this regime, added to the a-Si:H TFT model an above-threshold drain current term, I_{tr}, to account for the transitional regime.

$$V_{Gtre} = V_{th} \cdot \left[1 + \frac{V_{Gtr}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{Gtr}}{2V_{th}} - 1 \right)^2} \right]$$

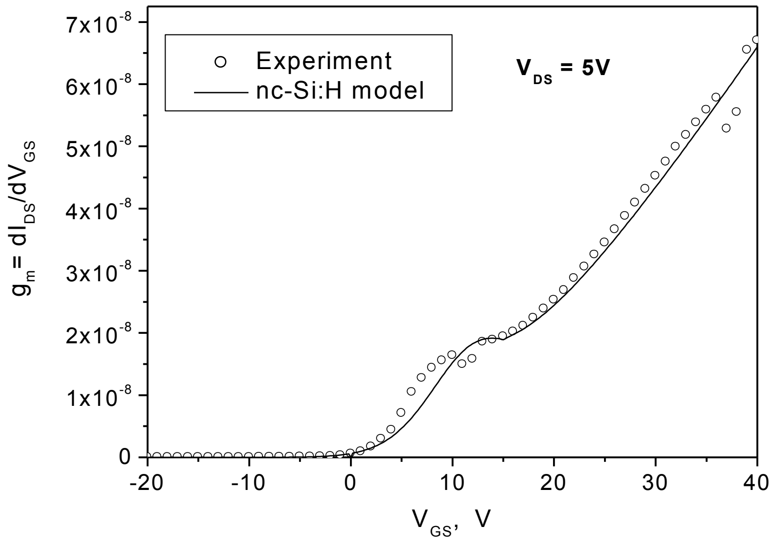
$$I_{tr} = \frac{1}{2} \mu_n C_i \frac{W}{L} V_{DSe} \left(1 + \lambda V_{DS} \right) \cdot M \cdot V_{Gtre}^{2+D}$$

  - where V_{Gtr}=V_{GS}-V_{tr}, V_{th} is thermal voltage and δ is a transition width parameter which ensures the good behavior of V_{Gtre}.

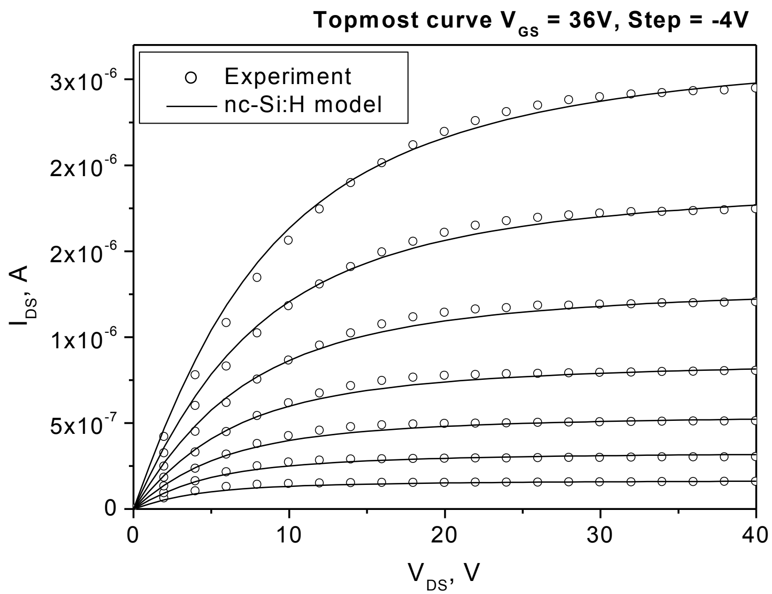
- We use the following unified expression of the channel current:

$$I_{DS} = I_{leak} + \left(\frac{1}{I_{sub}} + \frac{1}{I_{abv} + I_{tr}} \right)^{-1}$$

nc-Si TFT



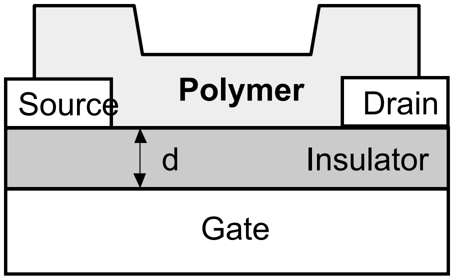
7x10^-8
6x10^-8
5x10^-8
4x10^-8
3x10^-8
2x10^-8
1x10^-8
0
-20
-10
0
10
20
30
40
Experiment
nc-Si:H model
V_DS = 5V
g_m = dI_DS/dV_GS
V_GS, V

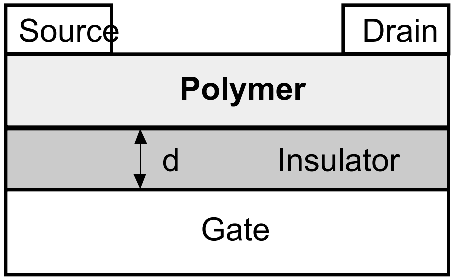


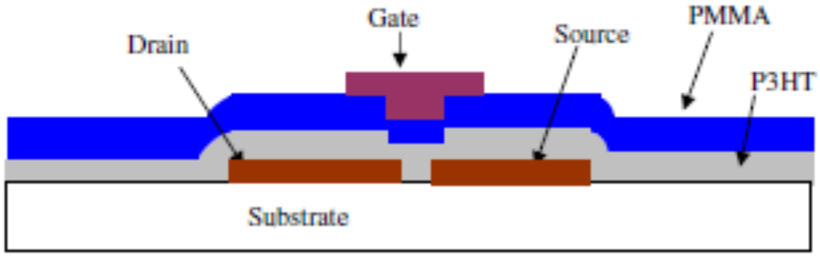
Topmost curve V_GS = 36V, Step = -4V
Experiment
nc-Si:H model
3x10^-6
2x10^-6
2x10^-6
1x10^-6
5x10^-7
0
0
10
20
30
40
I_DS, A
V_DS, V

Organic TFT

- Organic and polymer TFTs will probably become essential devices in niche applications, related to flexible, printed or large ara electronics: electronic tags, drivers in AMLCDs, sensors
- Organic and polymer electronics allow flexible and low-cost substrates for large-area applications by relatively simple and low-temperature fabrication for disposable electronics







Organic TFT

- In organic TFTs transport is due to **hopping** between localized states
- An analytical solution is possible assuming an exponential DOS and neglecting dopants and free charge
- With these assumptions, well above threshold (linear regime), we obtain:

$$I_{DS} = \frac{W}{L} \cdot C_{diel} \frac{T}{2T_0} \mu_0 \cdot \left[\left(V_{GS} - V_{FB} \right)^{2T_0/T} - \left(V_{GS} - V_{DS} - V_{FB} \right)^{2T_0/T} \right]$$

- This expression has the same form as the current in a-Si:H TFT, although the assumed transport mechanism is different.
- It is equivalent to use a crystalline MOSFET model with a field-effect mobility:

$$\mu_{FET} = \mu_0 \left[\frac{\left(V_{GS} - V_{FB} \right)}{V_{aa}} \right]^{2T_0/T-2} = \mu_{FETo} \cdot (V_{GS} - V_{FB})^{2T_0/T-2}$$

Organic TFT

- The current expression can be written in a more general way:

$$I_{DS} = \frac{W}{L} \cdot C_{diel} \frac{\mu_{FET} \cdot (V_{GS} - V_T)}{\left(1 + R \frac{W}{L} \cdot C_{diel} \mu_{FET} \cdot (V_{GS} - V_T)\right)} \frac{V_{DS}(1 + \lambda \cdot V_{DS})}{\left[1 + \left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{\frac{1}{m}}} + I_o$$

- where $V_{DSsat} = \alpha_S (V_{GS} - V_T)$ *R* is source plus drain resistance, I_0 is the leakage current and *m* and λ are adjustment parameters related to the sharpness of the knee region and to the channel length modulation respectively, and α_S is the non-ideal saturation parameter

Organic TFT

- The localized charge in the organic semiconductor in above threshold was considered to be much larger than the free charge, as it is done for inorganic amorphous TFTs in the subthreshold region:

$$I_{DS} = \beta(T,To)\cdot C_i \cdot \frac{W}{L}\cdot\frac{T}{2T_0}\cdot\left[\left(V_{GS}-V_{FB}\right)^{\frac{2To}{T}} - \left(V_{GS}-V_{DS}-V_{FB}\right)^{\frac{2To}{T}}\right]$$

$$\beta(T,To) = \frac{\sigma o}{\left[Bc\cdot\left(2\alpha_o\right)^3\right]^{\frac{To}{T}}}\cdot\left(\frac{k_b T}{\left(1-\frac{T}{To}\right)}\right)\cdot\left[\frac{\sin(\pi T/To)}{2\cdot k_b To}\right]^{\frac{To}{T}}\cdot\frac{\left(C_i\right)^{\left(\frac{2To}{T}-2\right)}}{\left(\varepsilon_S\right)^{\left(\frac{To}{T}-1\right)}}$$

- We can identify OTFT parameters with those of a-Si TFTs

Organic TFT

- In a-Si TFTs above threshold:

$$I_{DS} = P(T,To)\cdot C_i \cdot \frac{W}{L}\cdot\frac{T}{2To}\cdot\left[\left(V_{GS}-V_{FB}\right)^{\frac{2To}{T}} - \left(V_{GS}-V_{FB}-V_{DS}\right)^{\frac{2To}{T}}\right]$$

$$P(T,To) = P'(T,To)\cdot\frac{C_i^{\left(\frac{2To}{T}-2\right)}}{\left(\varepsilon_S\right)^{\left(\frac{To}{T}-1\right)}} \qquad P'(T,To) = \frac{q\cdot k_b T\cdot N_V\cdot\exp\left[-\frac{E_{Fo}-E_V}{k_b T}\right]}{\left[\pi q\cdot k_b T\cdot g_{do}\cdot\exp\left(-\frac{E_{Fo}-E_V}{k_b To}\right)\right]^{\frac{To}{T}}}\cdot\frac{To}{T}\cdot\left[\frac{\sin(\pi T/To)}{2k_b To}\right]^{\frac{To}{T}}$$

- Where an exponential DOS was assumed:

$$g_d(E) = g_{do}\exp\left(-\frac{E}{k_b To}\right)$$

- $\beta(T,To)$ turns to be equal to $P(T,To)$.

Organic TFT

- The field-effect mobility in organic TFTs can be related to the parameters of the exponential DOS:

$$\mu_{FET} = P'(T,To)\cdot\frac{C_i^{\left(\frac{2To}{T}-2\right)}}{\left(\varepsilon_S\right)^{\left(\frac{To}{T}-1\right)}}\left(V_{GS}-V_{FB}\right)^{\frac{2To}{T}-2}$$

$$\mu_{FET} = \frac{1}{\left(V_{aa}^{'}\right)^{\gamma}}\cdot\left(V_{GS}-V_{FB}\right)^{\gamma}$$

$$\frac{1}{\left(V_{aa}^{'}\right)^{\gamma}} = P'(T,To)\cdot\frac{C_i^{\left(\frac{2To}{T}-2\right)}}{\cdot\left(\varepsilon_S\right)^{\left(\frac{To}{T}-1\right)}} \qquad \gamma = \frac{2To}{T}-2$$

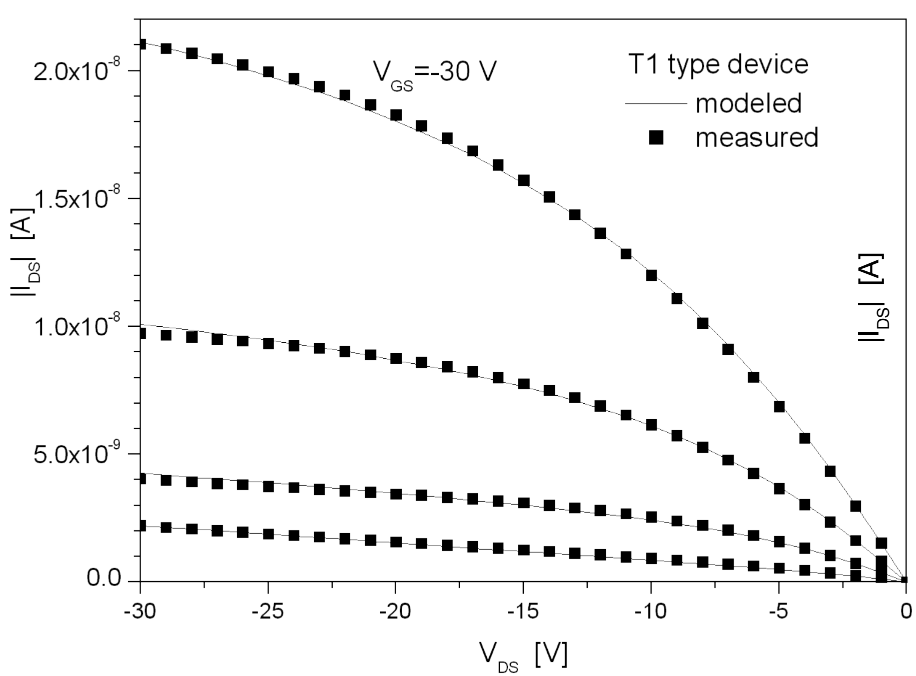
Organic TFT

- **Subthreshold regime**

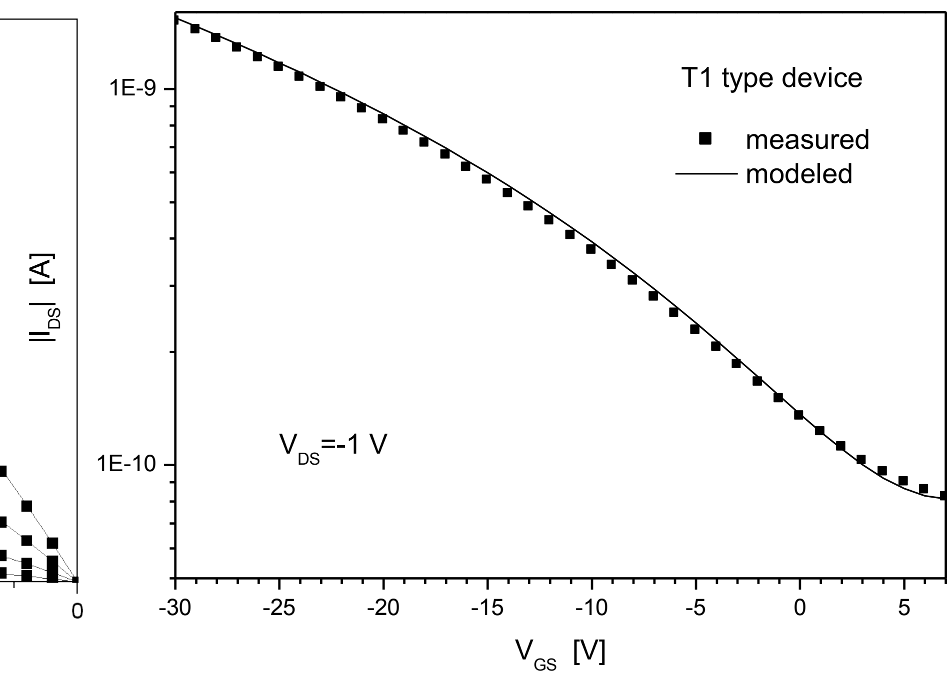
To model the subthreshold region of devices with high on/off ratio in subthreshold, the drain current can be represented as an exponential function of the gate voltage as:

$$I_S = I_o + I_{DS}(V_{sub}, V_{DS}) \cdot e^{\frac{2.3}{S}(V_{GS} - V_T)},$$

Organic TFT

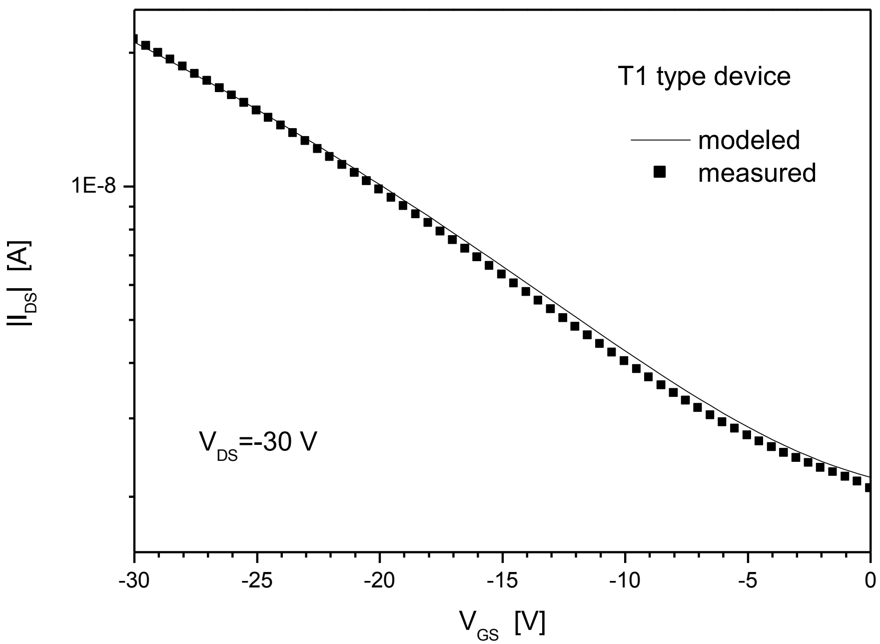


T1 type device
modeled
measured
V_{GS}=-30 V
$|I_{DS}|$ [A]
V_{DS} [V]
2.0x10^{-8}
1.5x10^{-8}
1.0x10^{-8}
5.0x10^{-9}
0.0
-30
-25
-20
-15
-10
-5
0

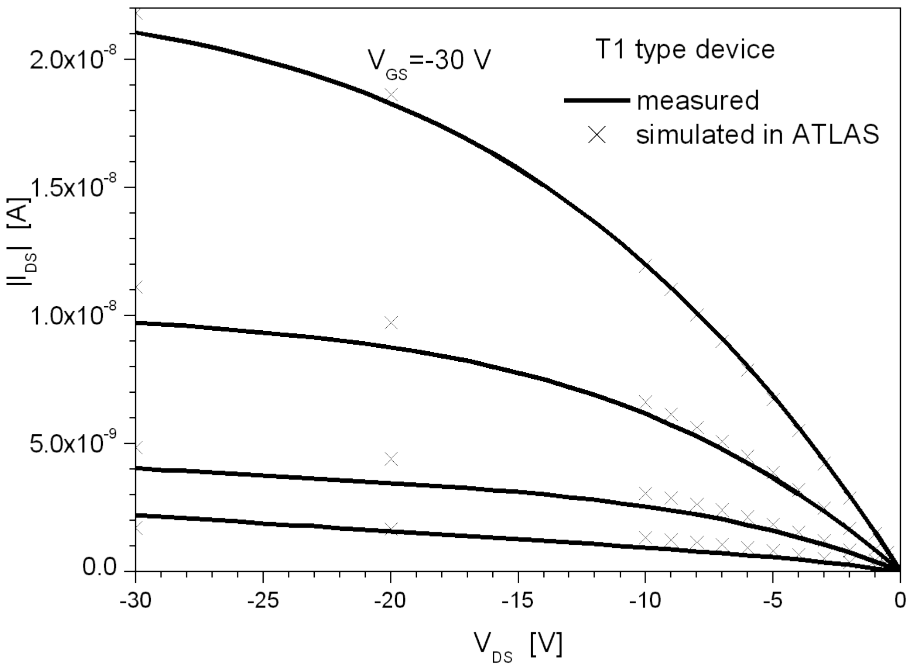


T1 type device
measured
modeled
V_{DS}=-1 V
$|I_{DS}|$ [A]
V_{GS} [V]
1E-9
1E-10
-30
-25
-20
-15
-10
-5
0
5

Organic TFT



T1 type device
modeled
measured
1E-8
$|I_{DS}|$ [A]
V_{DS}=-30 V
-30
-25
-20
-15
-10
-5
0
V_{GS} [V]



V_{GS}=-30 V
T1 type device
measured
simulated in ATLAS
$2.0x10^{-8}$
$1.5x10^{-8}$
$1.0x10^{-8}$
$5.0x10^{-9}$
0.0
$|I_{DS}|$ [A]
-30
-25
-20
-15
-10
-5
0
V_{DS} [V]

Amorphous Oxide TFT

Distribution of acceptor type traps

Conduction band energy

$$g_a = g_{at0} \exp\left(- \frac{E_C - E}{kT_1} \right) + g_{ad0} \exp\left(- \frac{E_C - E}{kT_2} \right)$$

$$T_1 = \frac{(\gamma a + 2)}{2} T$$

Tail acceptor density of states

Deep acceptor density of states

$$T_2 = \frac{(\gamma b + 2)}{2} T$$

The V_{GS} variation in subthreshold modifies the population of the deep states.

The V_{GS} variation above threshold modifies the population of the tail states.

Amorphous Oxide TFT

ABOVE THRESHOLD

Channel length modulation

$$I_{ab}(V_{GS},V_{DS}) = \frac{W}{L} C_i \mu_{FET} \frac{(V_{GS}-V_T)(1+\lambda|V_{DS}|)V_{DS}}{\left(1+R\frac{W}{L}C_i\mu_{FET}(V_{GS}-V_T)\right)\left(1+\left(\frac{V_{DS}}{\alpha(V_{GS}-V_T)}\right)^m\right)^{1/m}}$$

Saturation parameter

Sharpness of the knee region

where

Empirical parameters defining the variation of mobility with Vgs above threshold

$$\mu_{FET} = \frac{\mu_0 (V_{GS}-V_T)^{\gamma a}}{Vaa^{\gamma a}}$$

Amorphous Oxide TFT

To model the subthreshold region of devices, the drain current can be described as:

SUBTHRESHOLD

$$I_{bt}(V_{GS},V_{DS1}) = K\frac{(V_{GS}-V_{FB})^{1+\gamma_b}}{V_{bb}{}^{\gamma_b}}V_{DS1}$$

γ_b depends on the temperature *T* and on the characteristic temperature of the deep states distribution (T_2)

$$\gamma b = \frac{2T_2}{T} - 2$$

Amorphous Oxide TFT

DEEP SUBTHRESHOLD

Well below V_T, in deep subthreshold regime, diffusion becomes the predominant charge transport mechanism and the current shows an exponential dependence with the gate voltage for V_{GS} which can be expressed as:

$$I_{s1} = I_{bt}(V_{GS}, V_{DS1})e^{\frac{V_{GS}-(V_{FB}+V_1)}{S1}2.3}$$

The region where a hump may be present in stressed devices corresponds to a part of the deep subthreshold region where the slope is different due to the presence of the back interface charges, can be represented by another exponential behavior with an inverse slope S_2

$$I_{s2} = I_{bt}(V_{FB}+V_2, V_{DS1})e^{\frac{V_{GS}-(V_{FB}+V_2)}{S2}2.3}$$

where (V_{FB} + V_2) is the gate voltage below V_T where the **hump starts.**

Unified TFT Model Parameter Extraction

- Since a universal model formulation is possible for most types of TFTs, a unified extraction procedure can be applied to extract most parameters

Unified TFT Model Parameter Extraction

- Unified formulation of the drain current model above threshold

$$I = \frac{g_{ch} V_{ds} \left(1 + \lambda V_{ds}\right)}{\left(1 + \left(\frac{g_{ch} V_{ds}}{\left(1 + \lambda V_{ds}\right) I_{sat}}\right)^{m}\right)^{1/m}}$$

$$g_{ch} = \frac{\beta \left(V_{gt} / V_{aa}\right)^{\gamma+1}}{1 + \beta \left(R_s + R_d\right)\left(V_{gt} / V_{aa}\right)^{\gamma}} \qquad I_{sat} = \frac{\beta V_{gt}^{2}}{1 + \beta R_s V_{gt} + \sqrt{1 + 2\beta R_s V_{gt} + \left(\frac{V_{gt}}{V_L}\right)^{2}}}$$

- **Basic parameters**:

$$m, V_T, \gamma, \lambda, \beta / V_{aa}{}^{\gamma+1} = \frac{W}{L} C_{ox} \mu / V_{aa}{}^{\gamma+1}, V_L = v_s L / \mu, R_s, R_d$$

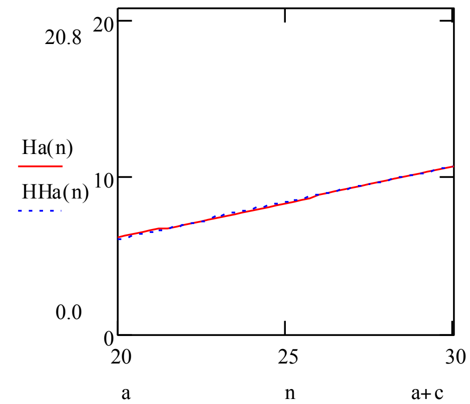
$$V_{GS} = V_{gs} - I R_s$$

$$V_{DS} = V_{ds} - I\left(R_s + R_d\right)$$

Unified TFT Model Parameter Extraction

- Simple extraction methods are used for the basic model parameters
- The threshold voltage and γ are extracted using the integral operator:

$$H(V_{gs}) = \frac{\int_{V_T}^{V_{gs}} I(V_{gs})\,dV_{gs}}{I(V_{gs})} = \frac{V_{gs} - V_T}{\gamma + 2}$$



Ha(n): $H(V_{gs})$ from a-Si TFT measurements

HHa(n): fitted $H(V_{gs})$

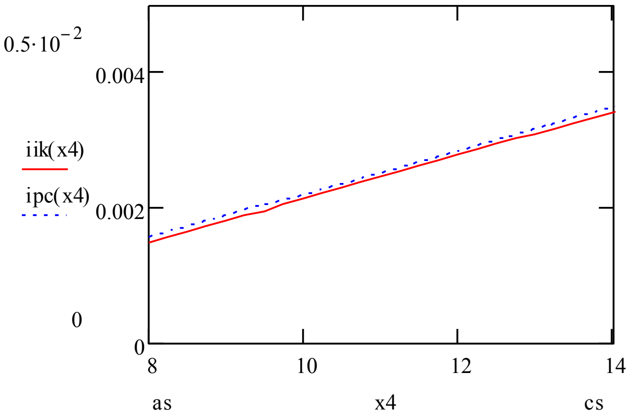
- This method is independent of the mobility

Unified TFT Model Parameter Extraction

- The rest of parameters are obtained from specific equations of each type of device
- Subthreshold
  - In a-Si TFT, $I_{sub} \propto \left(V_{GS} - V_{fb}\right)^{1+\gamma_b}$
    - Using the integral operator we extract V_{fb} and γ_b
  - In poly-Si TFT $I_{sub} \propto e^{V_{gt}/\eta V_{th}}$
    - From a log(I) vs V_{gt} plot we extract η

Unified TFT Model Parameter Extraction

- Saturation threshold voltage (with the DIBL effect)



iik(x4): H(V_{gs}) from measurements
ipc(x4): fitted H(Vgs)

$$H(V_{gs}) = \frac{\int_{V_T}^{V_{gs}} I_{sat}(V_{gs})dV_{gs}}{I_{sat}(V_{gs})} = \frac{V_{gs} - V_{Ts}}{\gamma + 3}$$

$$V_T \approx V_{To} + K_{VT} \times V_{ds}$$

- Current dependent resistance:

$$R_{si} = R_{so} + \frac{R_{sio}}{\frac{I}{I_o} + \alpha_{Rs}}$$

- Kink effect (in short-channel poly-Si TFTs)

Unified TFT Model Parameter Extraction

- **After extracting all the parameters, we complete the final basic compact model formulation:**

$$I = \frac{g_{ch} V_{ds}\left(1 + \lambda V_{ds}\right)}{\left(1 + \left(\frac{g_{ch} V_{ds}}{\left(1 + \lambda V_{ds}\right) I_{sat}}\right)^{m}\right)^{1/m}}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}\left(R_s + R_d\right)} \qquad g_{chi} = \frac{W}{L} \mu q n_s$$

The unified expression of n_s, valid from below to above threshold, depends on the type of device

Poly-Si TFT

$$n_s = 2 n_o \ln\left[1 + \frac{1}{2}\exp\left(\frac{V_{gt}}{\eta V_{th}}\right)\right]$$

a-Si TFT

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = C_{ox} V_{gt}^{\gamma + 1} / V_{aa}^{\gamma}$$

$$n_{sb} = C_{ox}\left(V_{gs} - V_{fb}\right)^{1 + \gamma_b} / V_{bb}^{\gamma_b}$$

Unified TFT Model Parameter Extraction

- **In a-Si:H and amorphous oxide TFTs, the subthreshold current is also a power law of the gate voltage overdrive:**

$$I_{bt}(V_{GS}, V_{DS1}) = K \frac{(V_{GS} - V_{FB})^{1+\gamma_b}}{V_{bb}{}^{\gamma_b}} V_{DS1}$$

V_{FB} is obtained by applying the H operator

γ_b is obtained using the H operator and it depends on the temperature T and on the characteristic temperature of the deep states distribution (T_2)

$$\Rightarrow \quad \gamma b = \frac{2T_2}{T} - 2$$

Unified TFT Model Parameter Extraction

Above threshold

$$I_{DS} = \frac{W}{L}\cdot C_i \cdot \mu_{FET}\cdot \frac{(V_{GS}-V_T)\cdot V_{DS}\cdot(1+\lambda\cdot V_{DS})}{\left[1+R\cdot\frac{W}{L}\cdot C_i\cdot\mu_{FET}\cdot(V_{GS}-V_T)\right]\cdot\left[1+\left[\frac{V_{DS}}{\alpha_S\cdot(V_{GS}-V_T)}\right]^m\right]^{\frac{1}{m}}}$$

$$m = \frac{\log 2}{\log\left[\dfrac{\frac{W}{L}\cdot C_i\cdot\left(\frac{\mu_o}{V_{AA}^{\gamma}}\right)\cdot\alpha_S\cdot(V_{DSsat1})^{2+\gamma}}{I_{DSsat1}(V_{DSsat1})\cdot\left[1+R\frac{W}{L}\cdot C_i\cdot\left(\frac{\mu_o}{V_{AA}^{\gamma}}\right)\cdot\left(\frac{V_{Dsat1}}{\alpha_S}\right)^{1+\gamma}\right]}\right]}$$

m is calculated from this equation for $V_{DSsat1}=\alpha_S(V_{GS1}-V_T)$ at V_{GS1} equal or near V_{GSmax}, considering $\lambda=0$.

Unified TFT Model Parameter Extraction

$$\lambda = \frac{\left[\dfrac{I_{DS2}}{V_{DS2}^{2}}\right]\cdot\left[1 + R\dfrac{W}{L}\cdot C_i\cdot\left(\dfrac{\mu_o}{V_{AA}^{\gamma}}\right)\cdot\left(V_{GS1} - V_T\right)^{1+\gamma}\right]\cdot\left[1 + \left(\dfrac{V_{DS2}}{\alpha_s\cdot\left(V_{GS1} - V_T\right)}\right)^{m}\right]^{\frac{1}{m}}}{\dfrac{W}{L}\cdot C_i\cdot\left(\dfrac{\mu_o}{V_{AA}^{\gamma}}\right)\cdot\left(V_{GS1} - V_T\right)^{1+\gamma}} - \frac{1}{V_{DS2}}$$

λ is evaluated using the same expression, for the same value V_{GS1} and a value of V_{DS2} near the maximum value measured. I_{DS2} is the current measured at V_{DS2}.

Unified TFT Model Parameter Extraction

Deep subthreshold regime in organic and amorphous oxide TFTs:

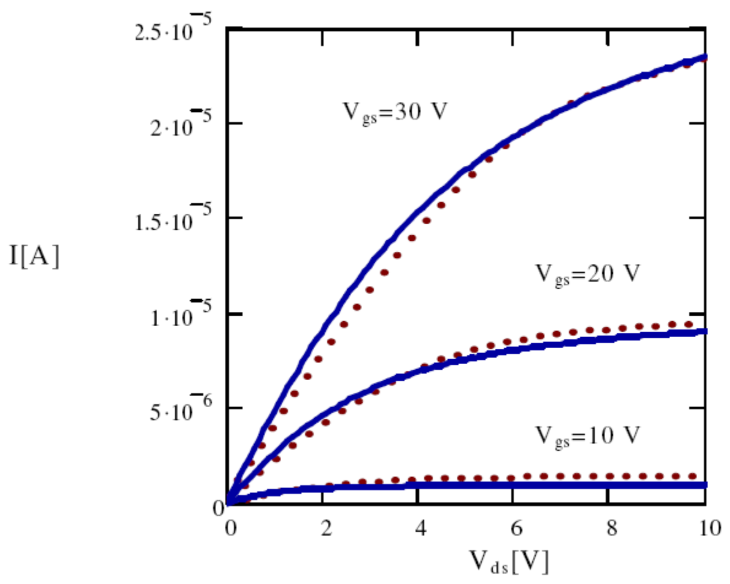
$$I_S = Io + I_{DS}(V_T + DV, V_{DS}) \cdot e^{\left(\frac{V_{GS} - V_T}{S}\right) \cdot 2.3}$$

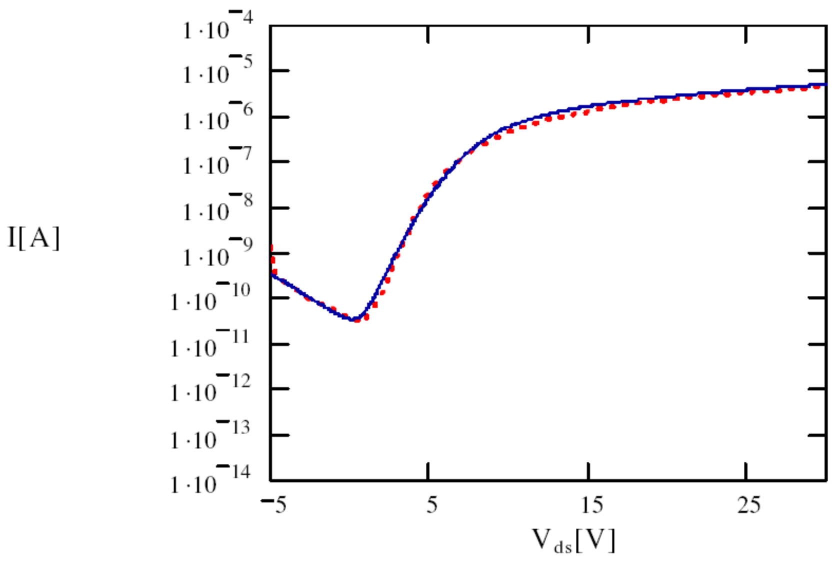
S is extracted from the slope of $\log(I_S)$ vs $(V_{GS}-V_T)$.

The total drain current is the sum of the two components, in above and below threshold regimes. The tahh function is used to sew both terms.

$$I_{DSt} = I_s \cdot \frac{1 - \tanh(V_{GS} - (V_T + DV) \cdot Q)}{2} + I_{DS} \cdot \frac{1 + \tanh(V_{GS} - (V_T + DV) \cdot Q)}{2}$$

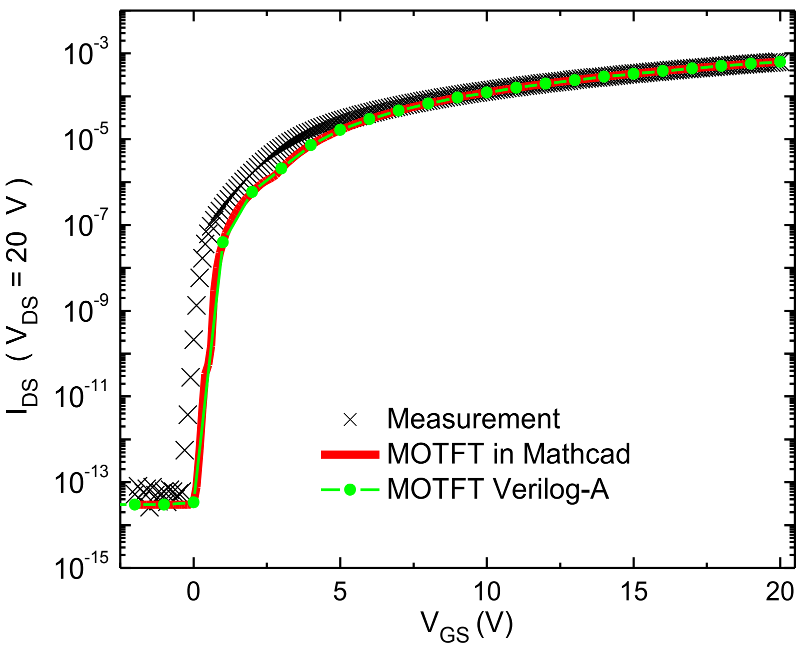
Results

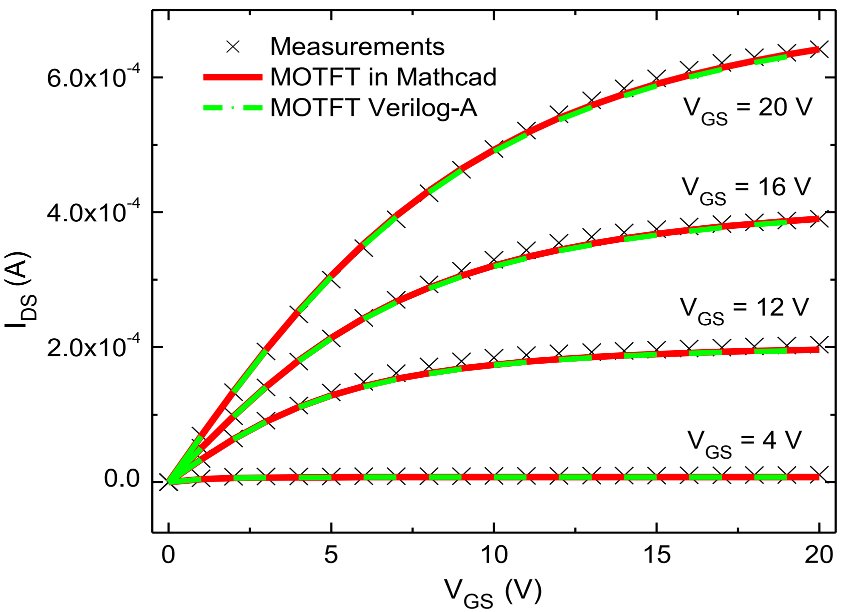




Measured (dots) and calculated (solid lines) characteristics of a-Si TFT
TFTs

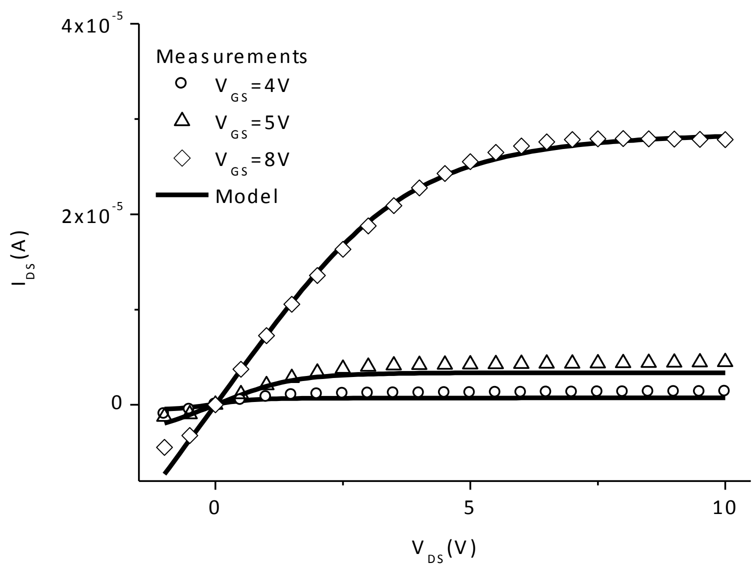
Results

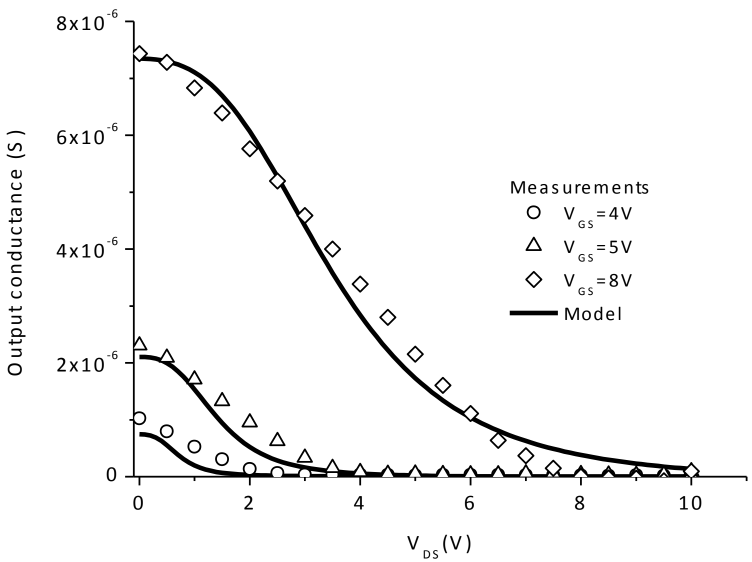




GIZO TFT W=160 μm L=20 μm Vds=20 V

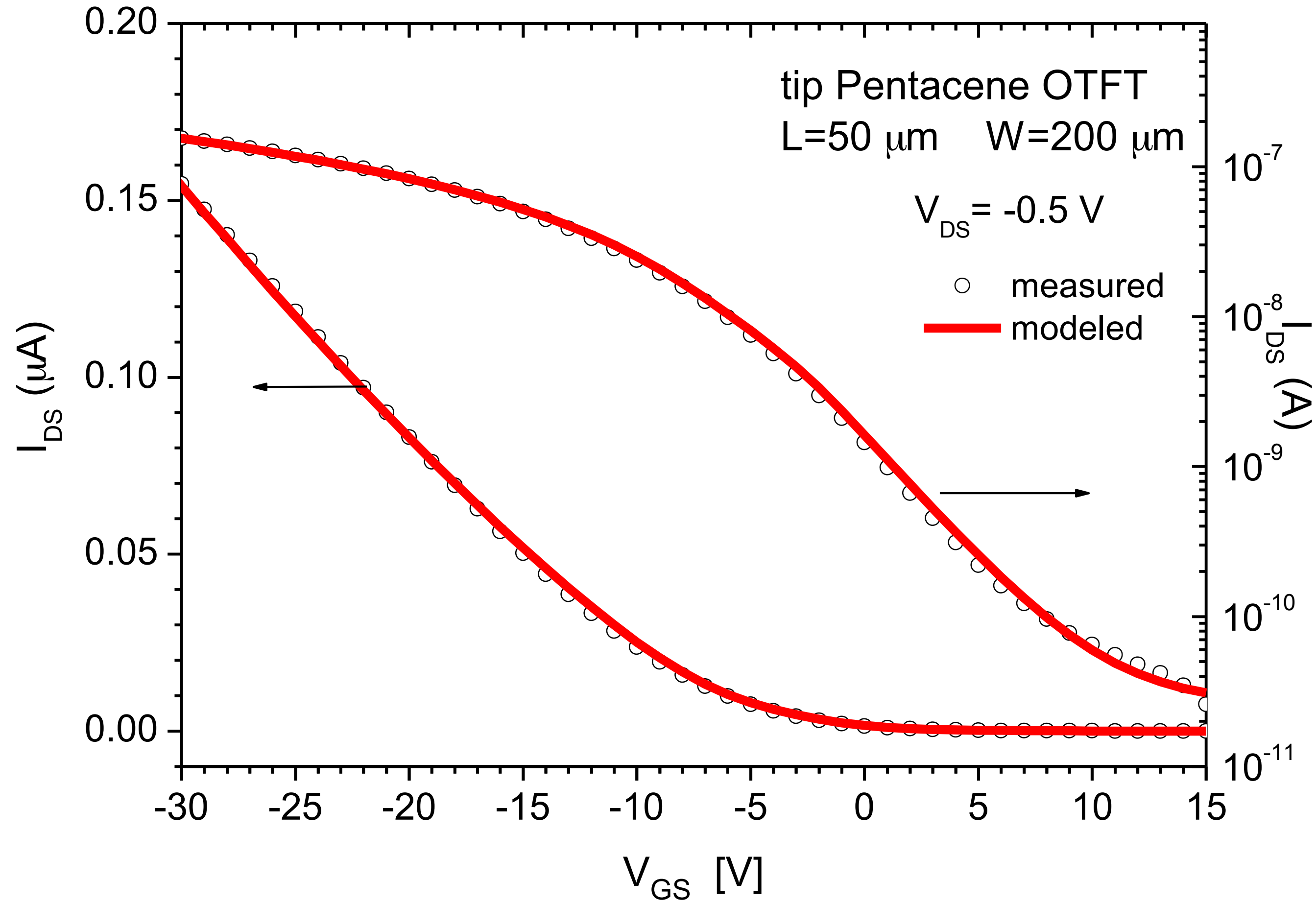
Results





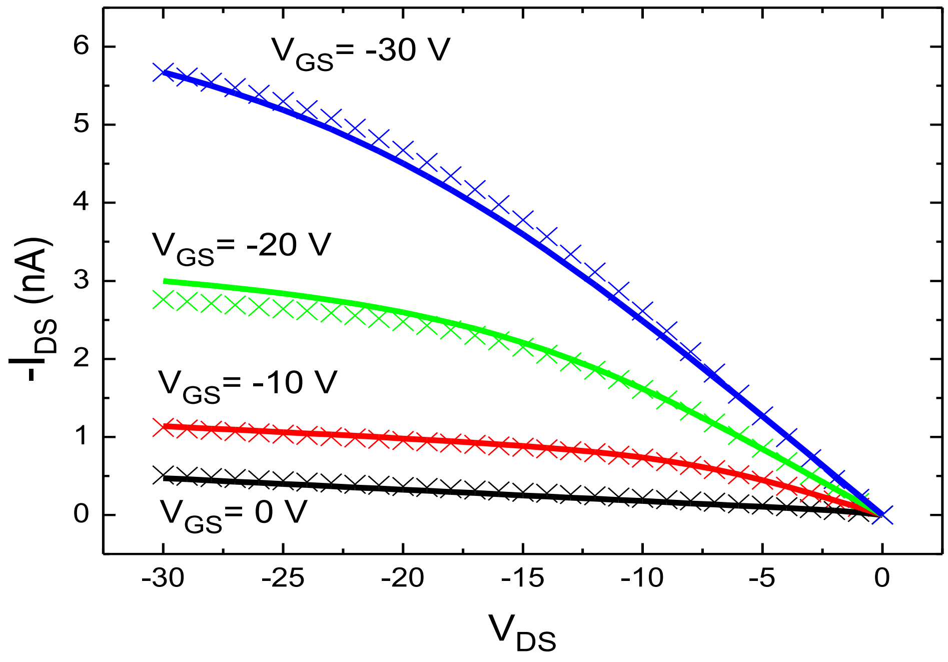
GIZO TFT W=160 μm L=20 μm

Results



tip Pentacene OTFT
L=50 μm W=200 μm
V_DS= -0.5 V
measured
modeled
I_DS (μA)
I_DS (A)
V_GS [V]
0.20
0.15
0.10
0.05
0.00
10^-7
10^-8
10^-9
10^-10
10^-11
-30
-25
-20
-15
-10
-5
0
5
10
15

Results



Experimental (simbols) and modeled (straight lines) I-V characteristics of the PMMA/P3HT OTFT with insulator thickness di_{PMMA}=330 nm and ds_{P3HT}=80 nm.

Quasi-static capacitance modeling

- A quasi-static (QS) charge model is developed by integrating the mobile charge sheet density (per unit area) over the channel

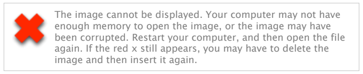
$$Q_{CH} = \frac{-W^2 Ci^2}{I_{DS}} \mu_0 \left[\frac{(V_{GS} - V_T - V_{DS})^{3+\gamma} - (V_{GS} - V_T)^{3+\gamma}}{3+\gamma} \right]$$

- The QS capacitances are obtained by differentiating the total charges with respect to the applied voltages

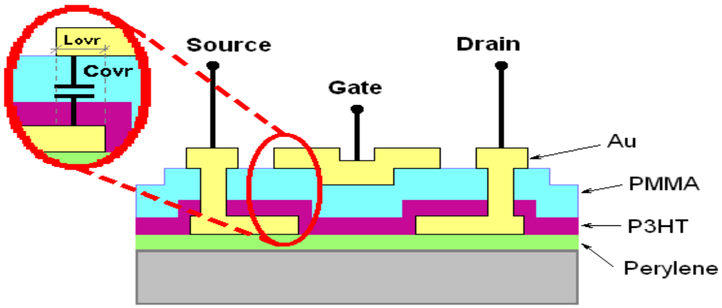
$$C_{GG} = \frac{\partial Q_G}{\partial V_{GS}} = -\frac{\partial Q_{CH}}{\partial V_{GS}}$$

Quasi-static capacitance modeling

- The extrinsic capacitance effect due to the overlap of the gate with the source and drain regions (C_{OVR}) is added to the calculated intrinsic capacitance above:



- L_{OVR} is the overlapping length between gate and drain contacts and between gate and source ones.
- The total gate-to-channel capacitance in accumulation regime and below threshold close to accumulation is:
- $$C_{GGa} = C_{GG} + 2 \cdot C_{OVR}$$



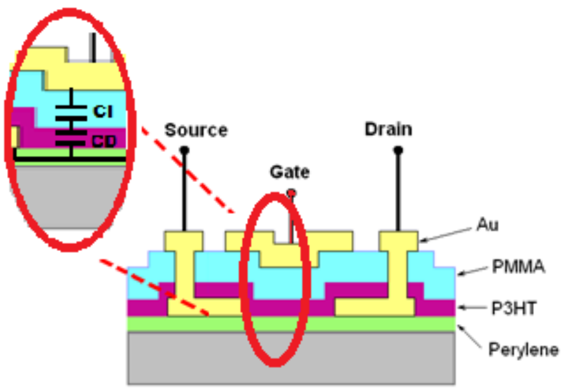
Quasi-static capacitance modeling

- The equivalent capacitance in depletion regime is obtained then from the sum of the series arrange of C_i and the depletion capacitance CD.

$$C_{Deq} = \frac{CD \cdot Ci}{CD + Ci} \qquad CD = \frac{\varepsilon s \cdot W \cdot L}{W_D}$$

- Where, in **partial depletion** conditions:

$$W_D = \sqrt{\frac{2 \cdot \varepsilon_s \cdot \psi s(V_{GS})}{q \cdot NB}} \qquad \psi s(V_{GS}) = \frac{\left[-\sqrt{2 \cdot \varepsilon_s \cdot q \cdot NB} + \sqrt{2 \cdot \varepsilon_s \cdot q \cdot NB + 4 \cdot Ci^2 \cdot (V_{GS} - V_T)}\right]^2}{4 \cdot Ci^2}$$



Quasi-static capacitance modeling

$$C_{Deq} = \frac{CD \cdot Ci}{CD + Ci} \qquad CD = \frac{\varepsilon s \cdot W \cdot L}{W_D}$$

- In conditions of **full depletion**, the organic layer thickness replaces W_D
- The unified expression of the capacitance is:

$$C_{GG} = C_{Deq} \cdot \frac{1 - tanh[(V_{GS} - V_T + \Delta_T) \cdot Q2]}{2} + C_{GG_a} \cdot \frac{1 + tanh[(V_{GS} - V_T + \Delta_T) \cdot Q2]}{2}$$

where Δ_T is the shift of the threshold voltage of the C-V characteristic at different frequencies, and *Q2* is a transition parameter of the *tanh* function

Improved capacitance modeling

Frequency dependence

In OTFTs, it has been observed that the value of the capacitance in accumulation condition is affected as the **frequency** of the applied AC signal increases.

As similarly done in [*] for modeling the MIS capacitor, but assuming that the interface traps are negligible, we applied the empirical formula proposed by Cole and Cole ** to represent the variation of the dielectric constant for a considerable number of liquids and solids:

$$\varepsilon_i = \varepsilon_{i\infty} + \frac{\left(\varepsilon_{i0} - \varepsilon_{i\infty}\right)}{\left[1 + j\omega\tau\right]^p}$$

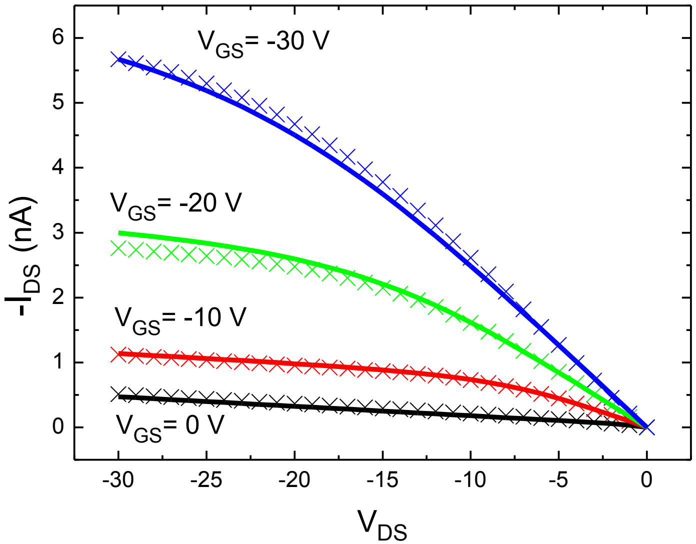
where ε_{i0} and $\varepsilon_{i\infty}$ are the permittivity at very low and very high frequencies, respectively.

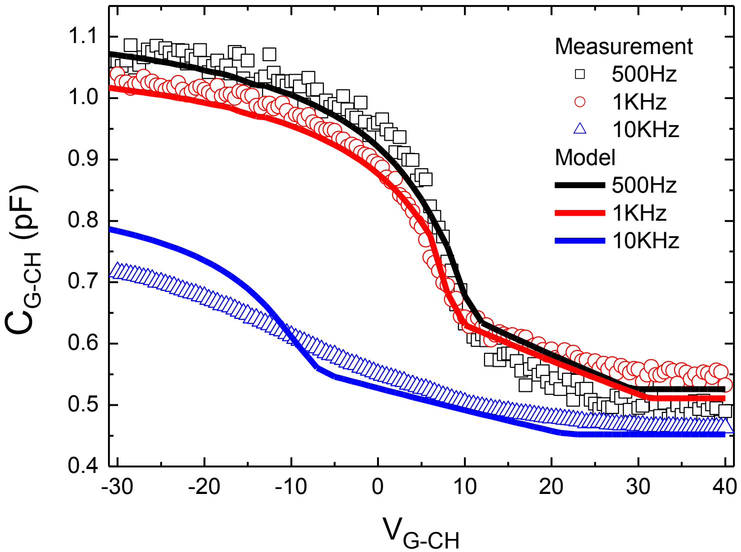
τ is the relaxation time and 1>p>0.

[*] M. Estrada, F. Ulloa, M. Avila, A. Cerdeira, A. Castro-Carranza, B. Iñiguez, L. Marsal, J. Pallarés, "Frequency and voltage dependence of the capacitance of MIS structures fabricated with polymeric materials" *IEEE Trans. Electron. Dev* (in press)

** *J. Chem. Phys.,* vol, 9, no. 4 pp. 341–352, Apr. 1941.

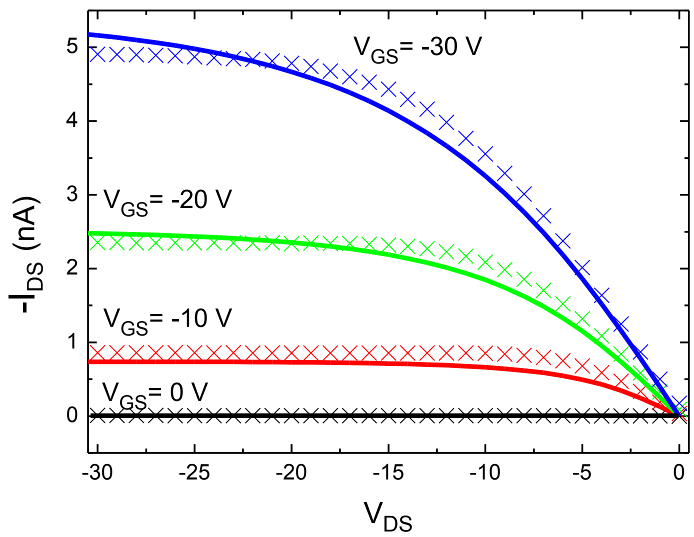
Improved capacitance modeling

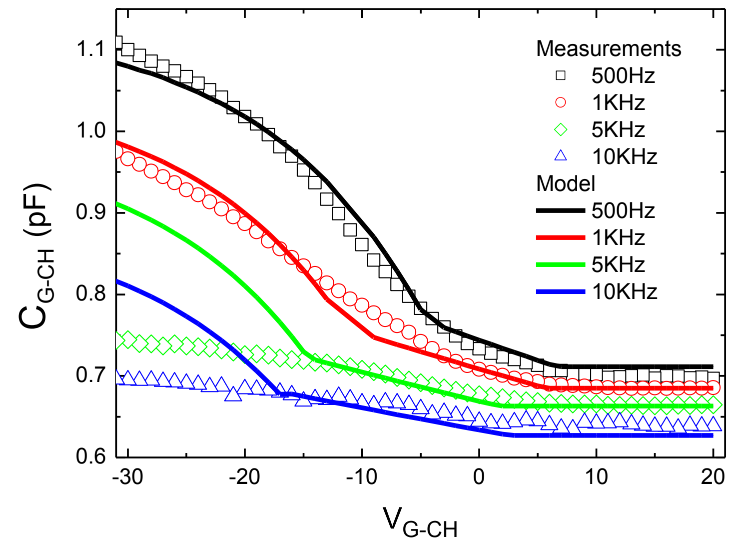




Experimental (simbols) and modeled (straight lines) I-V and C-V characteristics of the PMMA/P3HT OTFT with insulator thickness di_{PMMA}=330 nm and ds_{P3HT}=80 nm.

Improved capacitance modeling





Experimental (simbols) and modeled (straight lines) I-V and C-V characteristics of the PMMA/PCDTBT OTFT with insulator thickness di_{PMMA}=390 nm and ds_{PCDTBT}=50 nm.

Frequency dispersion effects

- The capacitance of polymeric MIS structures fabricated with polymers as dielectric and semiconductor layers can behave quite different as function of frequency, depending not only on the characteristics of the polymers, the thickness of the semiconductor layer but also on the properties of its interface with the insulator and with the metal contact.

- The dielectric constant ki of polymeric insulators can vary with frequency at relatively low frequencies, even below 1 MHz. This effect reduces the accumulation capacitance as the frequency increases, so CV curves shift down.

- The effect of the non depleted part of the polymeric layer introduces a frequency dependent impedance that reduces additionally the measured capacitance, specially, in accumulation. This effect is more important as the active layer is thicker or its resistivity is higher

Frequency dispersion effects

The presence of the high density of interface states can shift and deform the CV curves. Both positively and negatively charged interface states can be observed, depending on the polymers used as dielectric and semiconductor.

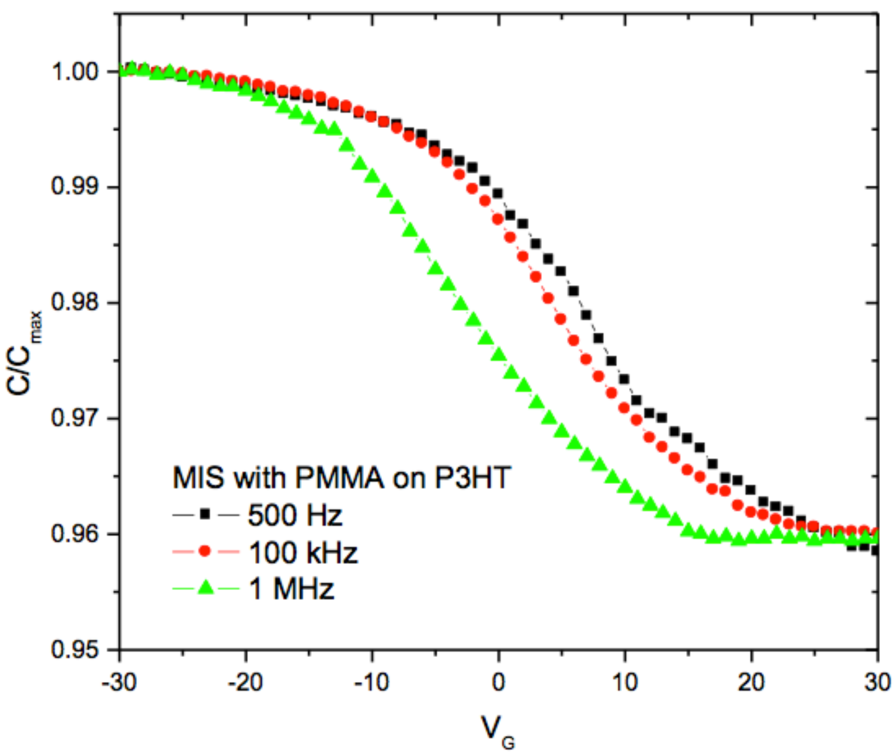
As frequency increases, interface traps will no longer be able of changing their charge with the measurement frequency so the shift they produce is lower

Although polymers have high density of bulk states, their effect was only observed at high frequencies and in MIS structures where the density of interface states was sufficiently small

The presence of a non-linear contact resistance related to the barrier formed at the polymer-metal contact due to the energy difference between the polymer HOMO and metal contact workfunction, can significantly modify the form of the CV curves.

Frequency dispersion effects

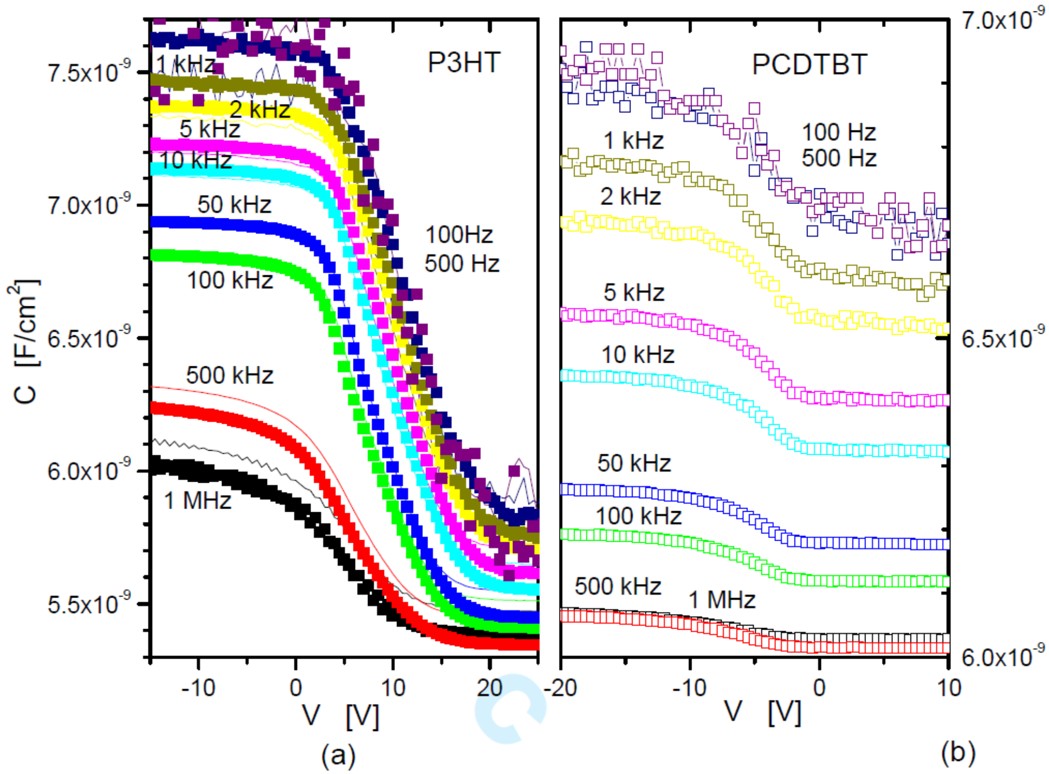
- Study of MIS structures with different materials using CV measurements at different frequencies. 2 main behaviors are observed [1]:



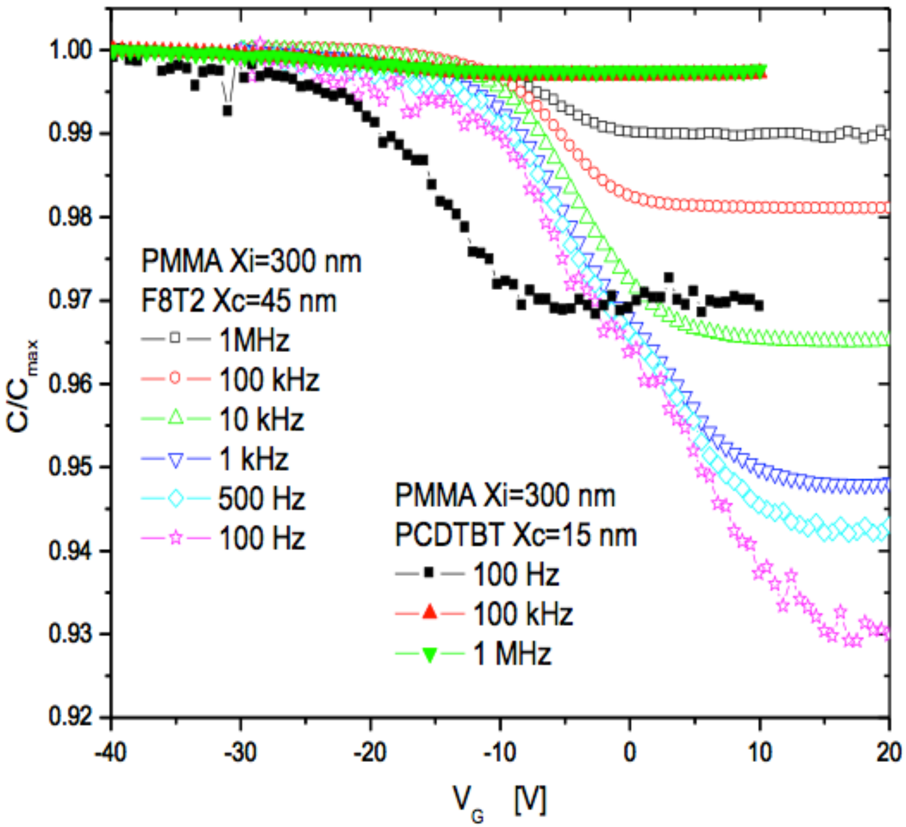
1. C_{min}/C_{max} is constant, and the increase in capacitance was due to the increase of the dielectric constant of the dielectric used

The main properties of the materials used in the MIS structures can be determined even at relatively high frequencies, eg. 1 MHz used in MOSFETs

Frequency dispersion effects



Frequency dispersion effects



2. Cmin/Cmax reduces as the frequency increases, producing a deformation of the CV curve

only low frequency measurements can be used to determine the properties of the materials used

[1] M. Estrada, F. Ulloa, J. Sanchez, A. Cerdeira, B. Iñiguez, "Differences on the frequency dependence of capacitance in MIS structures with different organic materials", ICOE 2012, invited presentation

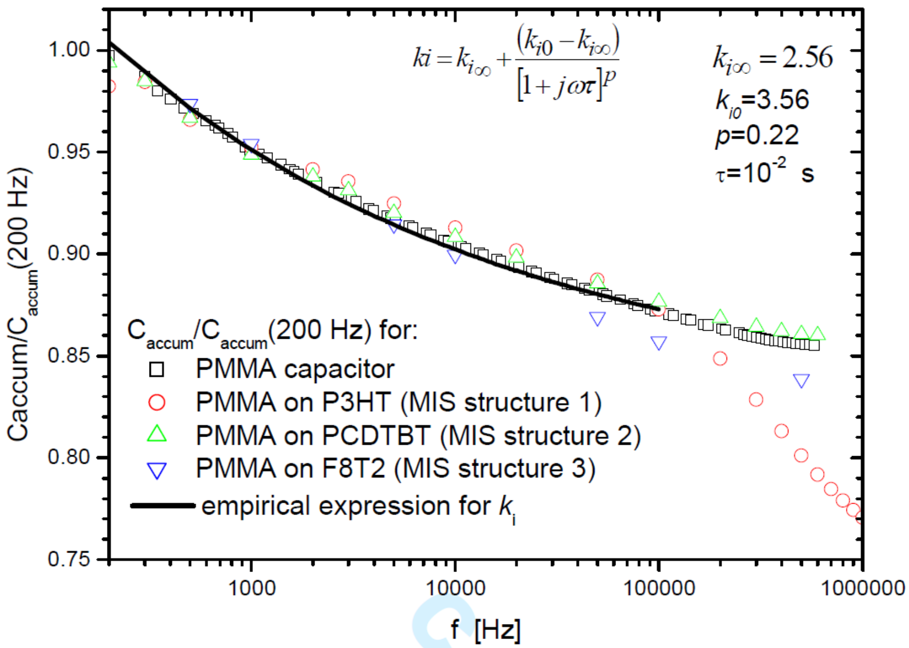
Frequency dispersion effects

Frequency and voltage dependence of the capacitance of MIS structures fabricated with polymeric materials

3 structures are considered:

- Structure 1: 395 nm of PMMA and 95 nm of P3HT layer
- Structure 2: 437 nm of PMMA on top of 30 nm thick PCDTBT layer
- Structure 3: 332 nm of PMMA on top of 22 nm of F8T2 layer

Frequency dispersion effects



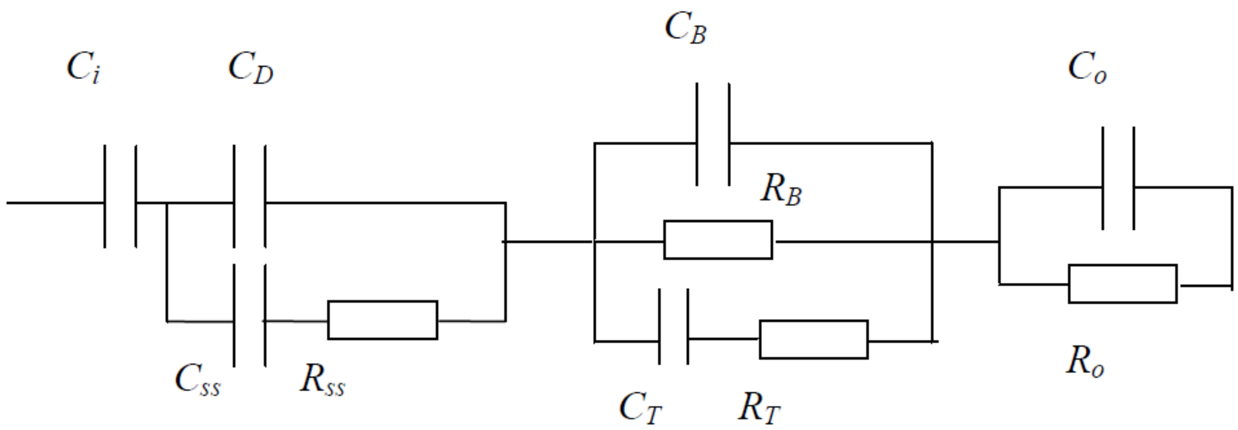
The reduction of C_{accum} is due to the reduction in the dielectric constant

Structure 1: for f > 100 KHz, C_{aacum} decreases more rapidly IF only the variation of k_i *vs. f* is considered

Structure 3: the same behavior starts at f > 80 KHz

Frequency dispersion effects

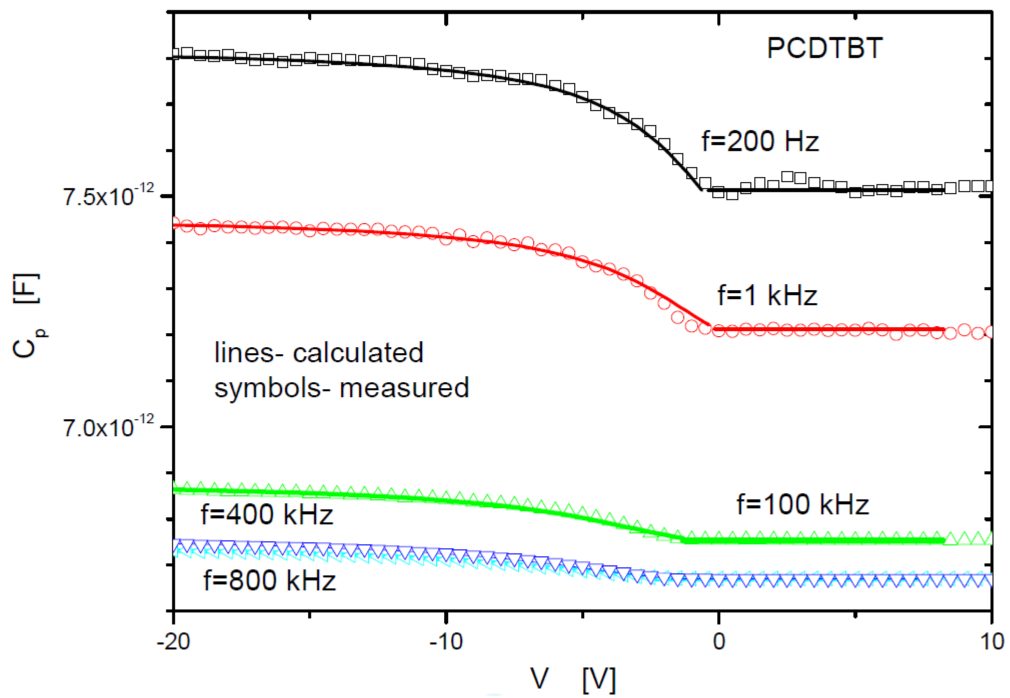
An equivalent circuit, based on a RC network, has been developed to model the capacitances at different frequencies



C_I – the capacitance of the dielectric
C_D – the capacitance of the depleted layer
R_B – resistance of the not yet depleted polymer
C_B – capacitance associated with the non depleted layer

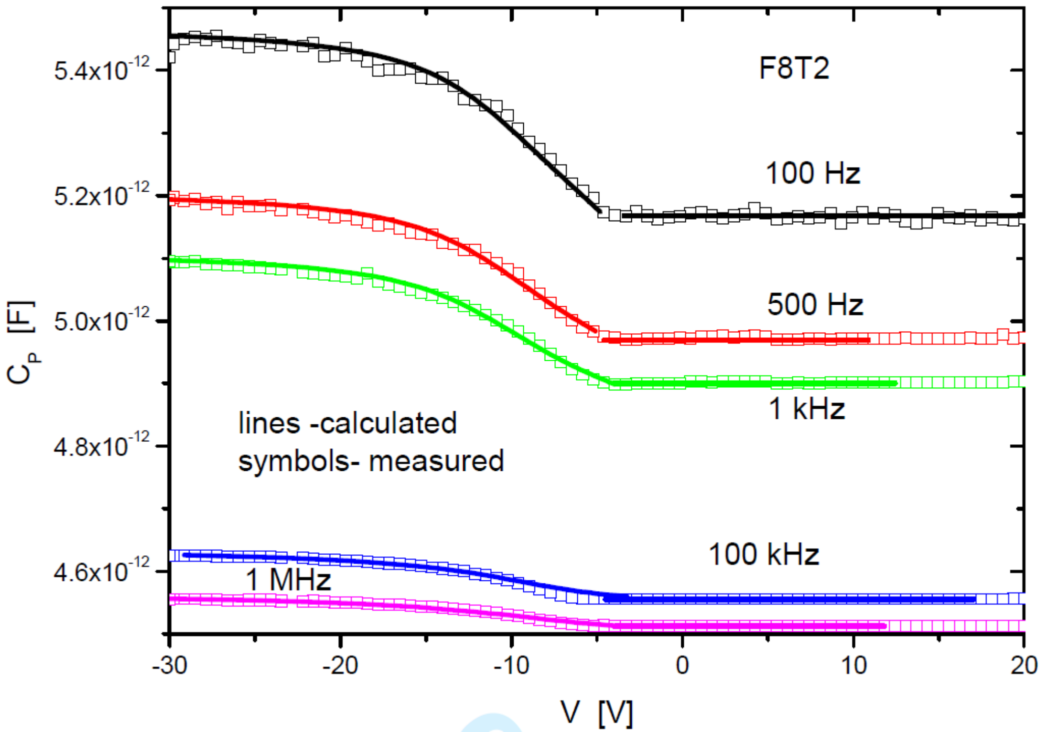
C_{SS} / R_{SS} – effect of the interface states
C_T / R_T – effect of the bulk traps in the semiconductor layer
R_0 / C_0 – effect of the contact resistance between the polymer and the back metal contact

Frequency dispersion effects



Measured and calculated C-V characteristics for a MIS with 437 nm of PMMA on top of 30 nm thick PCDTBT layer

Frequency dispersion effects



Measured and calculated C-V characteristics for a MIS with 332 nm of PMMA on top of 22 nm thick F8T2 layer

Conclusions

- We have reviewed compact modeling issues for the different types of TFTs: amorphous, polycristalline, nanocrystalline, oxide and organic TFTs

- We have presented unified TFT modeling and parameter extraction techniques
- The parameters of the basic model formulation can be obtained from I-V measurements using an extraction method valid for all TFT types
- Direct extraction techniques are possible for the rest of parameters, including those who are specitic to certain TFT types

- Good agreement with measurements have been found for different types of TFTs

Acknowledgements

This research is supported in the last years by contract "Thin Oxide TFT SPICE Model", with Silvaco Inc., and by the FlexNet Network of Excellence (7th Framework Programme of the European Union)