MOSFET's Negative Transconductance at Room Temperature

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***Abstract*—Negative transconductance is reported for the first time at $T = 300$ K for NMOS transistors fabricated with different technologies and oxide thickness in the 3–20 nm range. The effects of drain bias, channel length, oxide thickness as well as substrate doping and bias on the phenomenon are investigated. The results are interpreted in terms of surface-roughness limited mobility, and parameters for mobility modeling at high effective fields are extracted.**

***Index Terms*—Effective mobility, MOSFET, negative transconductance, room temperature.**

I. Introduction

MOSFET's negative transconductance has been already reported at low temperature and high transverse electric field [1]–[5]. The phenomenon has been explained in terms of effective mobility ($\mu_{\rm eff}$) degradation due to surface roughness scattering [1], which at high effective fields and low temperature is the dominant scattering mechanism in electron inversion layers.

In fact, since in the linear region of operation the drain current is given by

$$I_D = (W/L)V_{\rm DS}\mu_{\rm eff}qN_{\rm inv} \tag{1}$$

where W and L are the channel width and length, respectively, $V_{\rm DS}$ is the drain bias and $qN_{\rm inv}$ is the total inversion layer charge per unit area, the device transconductance (g_M) becomes negative when $\mu_{\rm eff}$ decreases with increased gate bias ($V_{\rm GS}$) as $N_{\rm inv}^{-n}$ with $n > 1$.

This occurs at cryogenic temperature in electron inversion layers, where recent results [6] show that mobility at high transverse electric field is roughly proportional to $E_{\rm eff}^{-2}$, where $E_{\rm eff} = q(0.5N_{\rm inv} + N_{\rm depl})/\varepsilon_{\rm Si}$ is the effective electric field, $qN_{\rm depl}$ the total depletion layer charge per unit area and $\varepsilon_{\rm Si}$ the silicon permittivity.

However, at $T = 300$ K the confinement of mobile carriers in the transversal direction is weaker than that at 77 K (and so is also surface roughness scattering), and prior to this work no negative transconductance has been observed at room temperature, even at an oxide field as high as 9 MV/cm [3].

In this paper we report for the first time MOSFET's negative transconductance at room temperature and discuss the dependence of the phenomenon on the main technological parameters and device bias, explaining also why it is not commonly found in conventional transistors.

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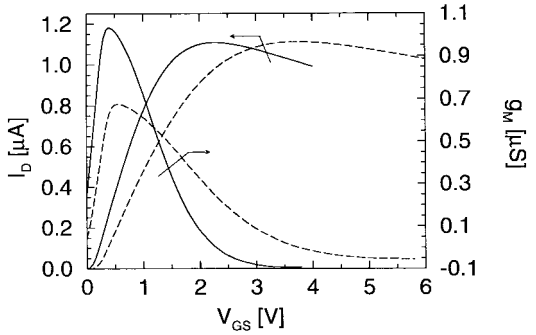

Fig. 1. Measured I_D and g_M versus $V_{\rm GS}$ characteristics with $V_{\rm DS} = 10$ mV for two devices of SET1 featuring $T_{\rm OX} = 3$ (solid line) and 5 nm (dashed line), $N_{\rm Si} = 10^{17}$ cm^{-3}, $L = 20$ μm and $W = 5$ μm.

The paper is organized as follows. In Section II we present experimental data obtained with devices fabricated with different technologies, showing that the phenomenon is a property of all thermally grown oxides. We also identify $\mu_{\rm eff}$ degradation at high $E_{\rm eff}$ as the main mechanism responsible for the observed results.

Section III provides the experimental characterization of the dependence of the negative transconductance on drain bias, channel length, oxide thickness ($T_{\rm OX}$), as well as substrate bias ($V_{\rm SB}$) and doping ($N_{\rm Si}$). In Section IV, a theoretical explanation of the observed results is provided in terms of mobility degradation due to surface roughness, and an extensive discussion of the experimental findings is provided. Finally, in Section V, parameters suitable for mobility modeling at high $E_{\rm eff}$ are extracted.

II. Device and Experiments

Accurate measurements of transconductance have been performed using two sets of LDD NMOS transistors, each fabricated with a different, advanced process by two companies with leading position in the field of deep submicron CMOS technologies.

All devices features n^+ polysilicon gates, while $N_{\rm Si}$ and $T_{\rm OX}$ range from 10^{17} to 10^{18} cm^{-3} and 3 to 5 nm, respectively, for the first set (SET1), and 3 10^{16} to 10^{17} cm^{-3} and 19 to 20 nm, respectively, for the other set (SET2).

All the measurements are performed with the Precision Semiconductor Parameter Analyzer HP4156A at wafer level, with the source terminal grounded. Figs. 1 and 2 show typical

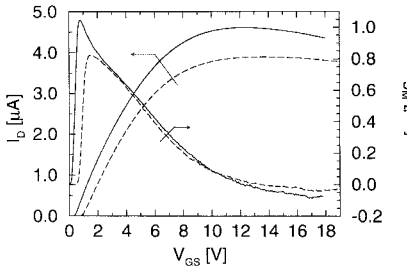

Fig. 2. Measured I_D and g_M versus $V_{\rm GS}$ characteristics with $V_{\rm DS} = 10$ mV for two devices of SET2. Solid line: $T_{\rm OX} = 19$ nm, $N_{\rm Si} = 3\ 10^{16}$ cm^{-3}, $L = W = 25$ μm. Dashed line: $T_{\rm OX} = 20$ nm, $N_{\rm Si} = 10^{17}$ cm^{-3}, $L = W = 10$ μm.

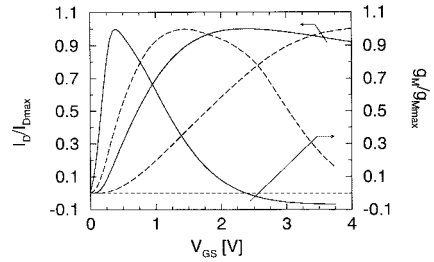

Fig. 3. Measured normalized I_D and g_M versus $V_{\rm GS}$ characteristics for $V_{\rm DS} = 0.1$ (solid line) and 2 V (dashed line).

results obtained with devices of SET1 and SET2, respectively, where negative transconductance is obtained at high gate bias.

A number of possible causes for the observed negative transconductance, different from mobility degradation due to surface roughness scattering, are ruled out for the following reasons.

1) Thermal effects are negligible due to the device low power consumption; moreover, as shown in Section III, negative transconductance tends to disappear for high $V_{\rm DS}$ values (leading to increased power dissipation).
2) The electrons tunneling from the device channel toward the gate do not contribute to the I_D drop at high $V_{\rm GS}$ values, because gate current (I_G) is negligible with respect to I_D (for the maximum $V_{\rm GS}$ considered, I_G is always below the 5% of I_D for all devices investigated in this study).
3) Oxide degradation with consequent threshold voltage $(V_{\rm TH})$ shift, possibly occuring during the sweep of the gate bias, is negligible, as the results are independent of sweep direction and measurement integration time.
4) Large parasitic resistances (not present in our devices) can explain the saturation of I_D but not its drop off, as will be discussed in Section IV.

Therefore, as for $T = 77$ K, the negative transconductance exhibited by the devices at high effective field seems the result of $\mu_{\rm eff}$ degradation due to surface roughness scattering [7].

III. Essential Dependencies

In this section we will describe the bias and technology dependence of the negative transconductance, focusing on devices of SET1, for which a variety of combinations of $N_{\rm Si}$ and $T_{\rm OX}$ values is available. All the samples considered in this and the following sections feature $W = 5$ μm.

A. Drain Bias Dependence

Fig. 3 shows the measured I_D and g_M (normalized to their maximum values $I_{D\max}$ and $g_{M\max}$, respectively) versus $V_{\rm GS}$ for the device featuring $T_{\rm OX} = 3$ nm, $L = 1$ μm and $N_{\rm Si} = 10^{17}$ cm^{-3}. As can be seen, the negative transconductance tends to disappear with increasing $V_{\rm DS}$.

The phenomenon has been already observed at 77 K [3], and confirms that thermal effects are not responsible for the found negative transconductance.

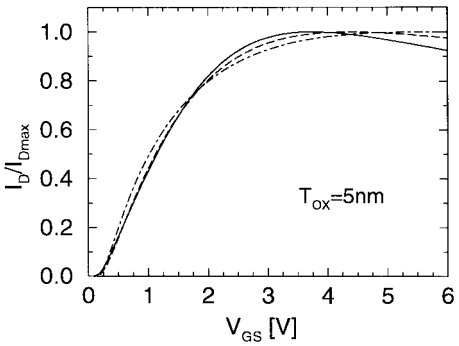

Fig. 4. Measured normalized I_D versus $V_{\rm GS}$ characteristics with $V_{\rm DS} = 10$ mV. Solid, dashed, and dot-dashed lines correspond to $L = 20$, 1, and 0.5 μm, respectively.

B. Channel Length Dependence

Fig. 4 shows the measured normalized I_D versus $V_{\rm GS}$ characteristics of the device featuring $N_{\rm Si} = 10^{17}$ cm^{-3} for three different values of channel length.

As can be seen, the gate overdrive at which $g_M = 0$ $(V_{\rm GTmax})$ increases as channel length decreases, and the 0.5 μm device does not exhibit negative transconductance up to $V_{\rm GS} = 6$ V. This phenomenon has been already observed at 77 K [4], but no clear explanation was provided.

To avoid such a channel length dependence to affect the results regarding the effects of $T_{\rm OX}$ and $N_{\rm Si}$ on the negative transconductance, in the experiments to be described in the rest of this section we will always consider long channel ($L = 20$ μm) devices.

C. Oxide Thickness Dependence

Fig. 1 shows that $V_{\rm GTmax}$ increases almost linearly with $T_{\rm OX}$, when the same $N_{\rm Si} = 10^{17}$ cm^{-3} is considered. Therefore, the oxide field at which $g_M = 0$ occurs is essentially independent of $T_{\rm OX}$, contrary to the results reported in [3] for $T = 77$ K, and can be estimated as $F_{\rm OXmax} \approx V_{\rm GTmax}/T_{\rm OX} = 7$ MV/cm.

D. Substrate Doping and Bias Dependence

Fig. 5(a) shows that as $N_{\rm Si}$ increases the drop in the drain current and $V_{\rm GTmax}$ decreases and increases, respectively, when the same $T_{\rm OX}$ is considered. For $V_{\rm DS} = 2$ V [Fig. 5(b)] only the device with $N_{\rm Si} = 10^{17}$ cm^{-3} still exhibits negative transconductance at $V_{\rm GTmax} = 4.9$ V.

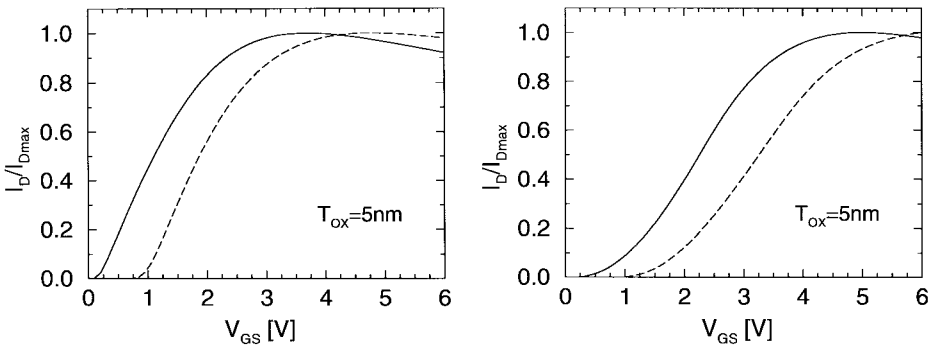

Fig. 5. Measured normalized I_D versus $V_{\rm GS}$ characteristics for $N_{\rm Si} = 10^{17}$ (solid line) and 10^{18} cm^{-3} (dashed line). (A) $V_{\rm DS} = 10$ mV, (B) $V_{\rm DS} = 2$ V.

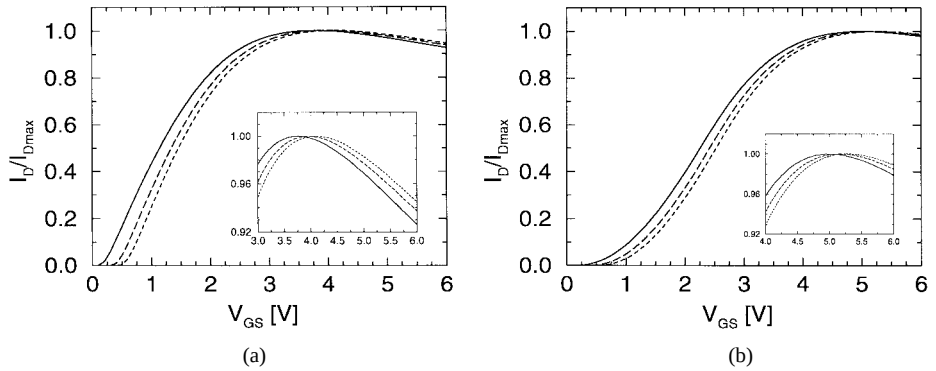

Fig. 6. Measured normalized I_D versus $V_{\rm GS}$ characteristics for $V_{\rm SB} = 0$ (solid line), 2.5 (dashed line) and 5 V (dotted line). (a) $V_{\rm DS} = 10$ mV, (b) $V_{\rm DS} = 2$ V.

Fig. 6(a) shows the normalized I_D versus $V_{\rm GS}$ characteristics obtained for the device featuring $T_{\rm OX} = 5$ nm and $N_{\rm Si} = 10^{17}$ cm^{-3} for different values of $V_{\rm SB}$. As for the $N_{\rm Si}$ dependence, with increasing $V_{\rm SB}$ the drop in the drain current and the value of $V_{\rm GTmax}$ decreases and increases, respectively. For $V_{\rm DS} = 2$ V [Fig. 6(b)] negative transconductance is still obtained for any $V_{\rm SB}$ considered, but at higher values of $V_{\rm GTmax}$.

IV. Discussion

In this Section, we will show that assuming surface roughness scattering to be responsible for the observed negative transconductance, $\mu_{\rm eff}$ degradation at high $E_{\rm eff}$ can be successfully modeled and the essential features of the experiments of Section III can be explained.

In order to experimentally extract $\mu_{\rm eff}$, first the values of $qN_{\rm inv}$ and $E_{\rm eff}$ have been determined as a function of $V_{\rm GS}$ by fitting the experimental gate-to-channel capacitance $(C_{\rm GC})$ with simulations taking into account quantum mechanical and polysilicon depletion effects [8], [9]. Details of the numerical algorithms used to calculate the subband structure and $C_{\rm GC}$ can be found in [8]–[11]. The simulations included the presence of a fixed negative interface charge of $2.5\ 10^{11}$ cm^{-2}, in agreement with charge pumping measurements showing an interface state density in the order of a few 10^{11} cm^{-2} eV^{-1}.

Experimental I_D characteristics have then been measured for long channel devices ($L = 20$ μm), so that the effects of series resistances are negligible, and at low drain bias ($V_{\rm DS} = 10$ mV), so that no correction factor is needed to accurately evaluate inversion layer charge [12]. Finally, experimental mobility has been extracted with the usual formula: $\mu_{\rm eff} = LI_D/WV_{\rm DS}qN_{\rm inv}$.

Starting from the self-consistent subband structure results, $\mu_{\rm eff}$ has been numerically calculated within the relaxation time approximation as described in [13]. However, to improve the model capabilities of [13], we have used different expressions for the rates of the main scattering mechanisms occuring in the two-dimensional (2-D) inversion layer. In particular, phonon scattering rates, both elastic intravalley and inelastic intervalley processes, have been modeled as in [14] with the set of parameters given in [15] for silicon, considering all the possible intersubband transitions (ten subbands per valley have been considered in our simulations).

Coulombic and surface roughness scattering rates have been modeled as in [14], but assuming that the roughness of the interface is exponentially correlated [16], [17]. To agree with experimental data, the root mean square height and the correlation length of the roughness are assumed to be 0.5 and 1 nm, respectively, values similar to those reported in the literature [7], [16], [17]. Two approximations have been introduced in order to simplify the calculations of coulombic and surface roughness scattering rates.

1) Intersubband transitions have been neglected, due to the reduced overlap factors in the transition matrix element with respect to intrasubband scattering rate [18].
2) Static screening in each valley has been approximated with a 2-D screening length given by the sum of the

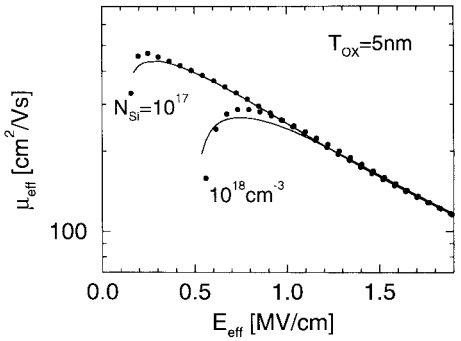

Fig. 7. Experimental (filled circles) and simulated (solid lines) $\mu_{\rm eff}$ versus $E_{\rm eff}$ characteristics.

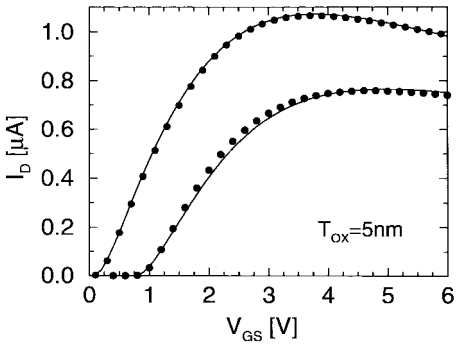

Fig. 8. Experimental (filled circles) and simulated (solid lines) I_D versus $V_{\rm GS}$ characteristics with $V_{\rm DS} = 10$ mV for the two devices of Fig. 7.

screening parameters of each individual subband of that valley (for which we have used the expression given by (59) in [19]).

In spite of these approximations, Fig. 7 clearly shows that an excellent agreement is achieved in the high $E_{\rm eff}$ region between experimental and numerical results, confirming that surface roughness scattering can successfully explain the strong mobility degradation observed in our devices.

The agreement is worse in the low $E_{\rm eff}$ region, where, however, experimental results are subject to larger extraction error [20], [21], whereas numerical results require an accurate description of the energy dependence of the density of interface states [22], [23]. In any case, as shown in Fig. 8, this region affects mainly the subthreshold device characteristics, while a good agreement between experimental and numerical I_D is achieved over the whole $V_{\rm GS}$ range of interest.

As for the main dependences of the negative transconductance presented in the previous section, the mobility modeling introduced above provides the following essential explanations.

The results shown in Fig. 3 can be consistently attributed to the dependence on $V_{\rm DS}$ of the inversion layer charge distribution within the channel. In fact, with increasing $V_{\rm DS}$ the average transverse electric field confining electrons at the interface decreases along the channel and, at the same time, the energy gain from the parallel electric field increases, making more electrons able to populate higher subbands characterized by a larger spatial extension into the bulk. Therefore, electron

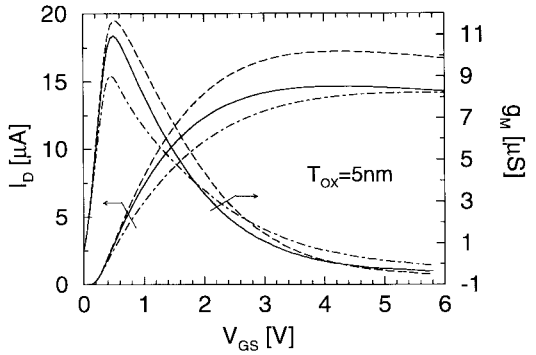

Fig. 9. Measured I_D and g_M versus $V_{\rm GS}$ characteristics for $V_{\rm DS} = 10$ mV for a device featuring $L = 1$ μm and $N_{\rm Si} = 10^{17}$ cm^{-3}with (solid line) an external resistance ($R_{\rm SDext}$) intentionally added in series to the drain terminal and without (dashed line) such a resistance. The dot-dashed line represent the case where $R_{\rm SDext}$ of (2) is numerically added to the measured device total resistance $R_{\rm TOT}$.

confinement at the interface is weaker, and so is surface roughness scattering.

For the long channel devices of Figs. 5(b) and 6(b), instead, the drain bias $V_{\rm DS} = 2$ V is not sufficient to produce significant heating of the carriers flowing in the channel. However, the lower transverse electric field determines the observed increase of $V_{\rm GTmax}$.

The channel length dependence shown in Fig. 4 can be explained in terms of device series resistances ($R_{\rm SD}$), which, at small L, become a larger fraction of the total resistance ($R_{\rm TOT}$) and cannot be neglected when modeling I_D versus $V_{\rm GS}$ characteristics.

In fact, assuming a bias independent $R_{\rm SD}$, when $g_M < 0$ the voltage drop across $R_{\rm SD}$ decreases with increasing $V_{\rm GS}$ (because of the decreasing I_D): thus, the voltage across the intrinsic device increases and this contrasts the effects of mobility degradation, leading to a lower absolute value of the negative transconductance. In addition, if $R_{\rm SD}$ is assumed to decrease with $V_{\rm GS}$, in the negative transconductance region the decrease in $R_{\rm SD}$ can compensate the increase in the resistance of the intrinsic device, so that no negative transconductance can be observed (as is the case for the 0.5 μm device of Fig. 4).

At this regard, Fig. 9 shows an example of the effects on I_D and g_M versus $V_{\rm GS}$ characteristics of an external series resistance ($R_{\rm SDext}$) intentionally added to the device drain terminal. When a constant $R_{\rm SDext} = 100$ Ω (equal to about 18% of $R_{\rm TOT}$) is experimentally added, the absolute value of g_M is reduced in the whole range of $V_{\rm GS}$ and $V_{\rm GTmax}$ does not change significantly. On the contrary, if $R_{\rm SDext}$ is made to depend on $V_{\rm GS}$, to simulate the gate bias dependence of the series resistance in LDD structures, according to the expression [24]

$$R_{\rm SDext} = R_F + \frac{1}{B(V_{\rm GS} - V_{Tn-})} \tag{2}$$

for the set of parameters $R_F = 30$ Ω, $B = 2$ 10^{-3} V^{-1} Ω^{-1} and $V_{Tn-} = -0.4$ V, no negative transconductance is observed for $V_{\rm GS}$ up to 6 V.

This can explain the results of Fig. 4: for long channel transistors the series resistances are negligible with respect

TABLE I
EXPERIMENTAL RESULTS ON $T_{\rm OX}$ AND $N_{\rm Si}$ DEPENDENCE

N_{Si} $[cm^{-3}]$	T_{OX} $[nm]$	E^M_{eff} $[MV/cm]$	V_{GTmax} $[V]$
10^{17}	3	1.2	2.12
	5	1.2	3.52
10^{18}	3	1.7	2.27
	5	1.7	3.85

to $R_{\rm TOT}$ and do not significantly affect the I_D versus $V_{\rm GS}$ characteristics. On the contrary, for short channel transistors, $R_{\rm SD}$ is comparable with $R_{\rm TOT}$ and its bias dependence significantly distorts the I_D versus $V_{\rm GS}$ characteristics, tending to eliminate the negative g_M region.

As for the dependence of the negative transconductance on $T_{\rm OX}$, $N_{\rm Si}$ and $V_{\rm SB}$, it is a direct consequence of the universal mobility behavior featured by our samples in the high $E_{\rm eff}$ region (Fig. 7). In fact, from (1), I_D can be expressed in terms of $E_{\rm eff}$ as

$$I_D = 2(W/L)V_{\rm DS}\mu_{\rm eff}(\epsilon_{\rm Si}E_{\rm eff} - qN_{\rm depl}) \tag{3}$$

hence

$$g_M = \frac{\partial I_D}{\partial V_{\rm GS}} = \frac{\partial E_{\rm eff}}{\partial V_{\rm GS}}\frac{\partial I_D}{\partial E_{\rm eff}} = \frac{1}{2T_{\rm OX}}\frac{\epsilon_{\rm OX}}{\epsilon_{\rm Si}}\frac{\partial I_D}{\partial E_{\rm eff}} \tag{4}$$

where $\epsilon_{\rm OX}$ is the oxide permittivity and we have assumed for the inversion layer charge the approximate expression [21], [25]

$$qN_{\rm inv} = \frac{\epsilon_{\rm OX}}{T_{\rm OX}} \cdot V_{\rm GT}. \tag{5}$$

For a fixed $N_{\rm Si}$, (3) indicates that I_D versus $E_{\rm eff}$ characteristics are independent of $T_{\rm OX}$, while (4) shows that g_M versus $E_{\rm eff}$ characteristics scale linearly with $T_{\rm OX}^{-1}$. However, the value of the effective field $(E^M_{\rm eff})$ at which $g_M = 0$, i.e., that satisfying the equation

$$\frac{\partial I_D}{\partial E_{\rm eff}} = 0 \tag{6}$$

is independent of $T_{\rm OX}$ (see also Table I). Substituting (3) into (6), we have

$$\frac{qN_{\rm inv}}{2}\frac{\partial \mu_{\rm eff}}{\partial E_{\rm eff}} + \mu_{\rm eff}\epsilon_{\rm Si} = 0 \tag{7}$$

from which it is readily obtained

$$\frac{\partial}{\partial E_{\rm eff}}(\log \mu_{\rm eff}) = \frac{-2\epsilon_{\rm Si}}{qN_{\rm inv}}. \tag{8}$$

Finally, substituting (5) into (8), we obtain

$$V_{\rm GTmax} = -2\frac{\epsilon_{\rm Si}}{\epsilon_{\rm OX}}\frac{T_{\rm OX}}{\frac{\partial}{\partial E_{\rm eff}}(\log \mu_{\rm eff})} \tag{9}$$

which confirms the linear dependence of $V_{\rm GTmax}$ on $T_{\rm OX}$ shown in Table I.

Regarding the $N_{\rm Si}$ dependence, the l.h.s. of (8) is independent of substrate doping for any fixed value of $E_{\rm eff}$, whereas the absolute value of the r.h.s. increases with $N_{\rm Si}$. Hence, $E^M_{\rm eff}$ moves at higher effective field values for higher substrate doping, as shown in Table I. This explains the lower drop of I_D and the increase of $V_{\rm GTmax}$ shown in Fig. 5(a) and Table I.

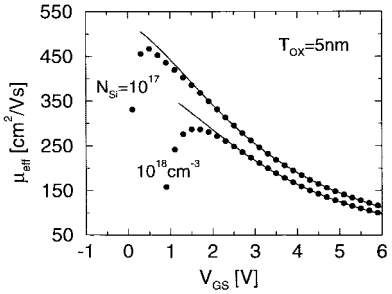

Fig. 10. Comparison between measured (filled circles) and best-fit results of model equation (10) (solid line) $\mu_{\rm eff}$ versus $V_{\rm GS}$ characteristics.

The $V_{\rm SB}$ dependence of Figs. 6(a) and (b) can be explained in the same way as the dependence on $N_{\rm Si}$: with increasing $V_{\rm SB}$ the point at which $g_M = 0$ occurs shifts toward higher values of effective field because of the lower $N_{\rm inv}$ corresponding to the same $E_{\rm eff}$.

In summary, our analysis suggests some considerations on the experimental conditions producing significative values of negative transconductance. Even for relatively low $N_{\rm Si}$ values, the phenomenon occurs at oxide fields as high as 7 MV/cm, much greater than the (critical) field normally assumed for device operation (4 MV/cm) [26]. Furthermore, also at the fields at which negative transconductance is expected to occur, only devices with long channel and small form factor exhibit the phenomenon, because they minimize the effects of series resistance. Since, however, gate and drain currents exhibit different dependences on the device geometry, in that I_G and I_D are proportional to gate area (WL) and device form factor (W/L), respectively, if L increases I_G increases with respect to I_D and can contribute significantly to the I_D drop in the negative transconductance region.

In our opinion, this is the main reason why in [3] (where long channel devices with relatively high form factors $W/L \approx 4$ have been used) no negative transconductance has been found at $T = 300$ K for oxide fields as high as 9 MV/cm.

In conclusion, the essential conditions in order to observe negative transconductance are:

1) oxide fields higher than about 7 MV/cm;
2) devices with long channel and $W/L \leq 1$;
3) gate area small to make I_G negligible with respect to I_D.

V. MOBILITY MODELING AT HIGH EFFECTIVE FIELDS

In order to accurately reproduce the strong mobility degradation at high $E_{\rm eff}$ observed in our samples within the compact models for electrical level simulation, an extra parameter β must be introduced in the gate overdrive dependence of the effective mobility, according to [3], [4]

$$\mu_{\rm eff} = \frac{\mu_0}{1 + \alpha V_{\rm GT} + \beta V_{\rm GT}^2}. \tag{10}$$

With this expression, the universal part of $\mu_{\rm eff}$ versus $V_{\rm GS}$ characteristics can be accurately modeled, as shown in Fig. 10, with the parameters values given in Table II, while the device threshold voltage ($V_{\rm TH} = 0.2$ and 0.95 V for $N_{\rm Si} = 10^{17}$ and 10^{18} cm^{-3}, respectively), has been extracted with the usual linear extrapolation technique from I_D versus $V_{\rm GS}$ data.

TABLE II
BEST-FIT PARAMETERS FOR V_{GT} MOBILITY DEPENDENCE

N_{Si} $[cm^{-3}]$	μ_0 $[cm^2/Vs]$	α $[V^{-1}]$	β $[V^{-2}]$
10^{17}	512	0.13	0.083
10^{18}	362	0.18	0.071

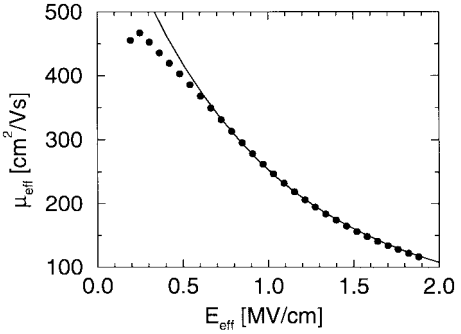

Fig. 11. Comparison between experimental results of Fig. 7 (filled circles) and the model of (11) (solid line) $\mu_{\rm eff}$ versus $E_{\rm eff}$ characteristics.

The parameters μ_0, α and β are, in general, dependent on $T_{\rm OX}$ and $N_{\rm Si}$, and need to be accurately extracted for each individual device, for example with the methods proposed in [4], [27].

From the point of view of numerical device simulation, we have considered the physically based nonlocal effective mobilty model of [28], where the universal part of $\mu_{\rm eff}$ at room temperature is given by

$$\mu_{\rm eff} = \left(\frac{1}{\mu_B} \left[1 + \left(\frac{E_{\rm eff}}{E_0} \right)^{\gamma} \right] + \frac{E_{\rm eff}^2}{\delta} \right)^{-1} \qquad (11)$$

where $\mu_B = 1470$ cm^2/Vs is the phonon limited bulk mobility, while $E_0 = 0.07$ MV/cm, $\gamma(300\ {\rm K}) = 0.2$ and $\delta(300\ {\rm K}) = 6.14\ 10^{14}$ V/s are the fitting parameters values at room temperature [28], [29].

Fig. 11 shows that an excellent agreement is achieved between experimental results and the model of (11), where the only parameter γ (=0.33) has been changed to a value more consistent with the experimental $E_{\rm eff}$ dependence of phonon limited mobility observed at room temperature [6].

Therefore, the conventional $E_{\rm eff}^2$ dependence used to model surface roughness limited mobility is able to reproduce the strong mobility degradation responsible for the negative transconductance observed in our samples at $T = 300$ K.

VI. CONCLUSION

MOSFET's negative transconductance has been reported for the first time at room temperature. Effects of drain bias, channel length, oxide thickness, substrate doping and substrate bias have been analyzed and explained in terms of mobility degradation due to surface roughness scattering.

The analysis shows that the oxide field at which the phenomenon occurs is independent of $T_{\rm OX}$ (provided series resistance effects and interface roughness are independent of oxide thickness [30]), and increases with $N_{\rm Si}$. However, since this value, also for substrate doping as low as 10^{17} cm^{-3}, is far above the oxide critical field for the normal device operation, the phenomenon is not expected to be of concern for future scaled CMOS technologies.

Mobility parameters at high effective fields have been accurately extracted both for electrical level and numerical device simulation purposes.

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