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Design and implementation of four-color conjecture circuit based on memristor neural network

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ABSTRACT

The four-color conjecture is one of the three major mathematical problems in modern times. Aiming at the complicated derivation of four-color conjecture theory and the difficult realization of hardware circuit, a four-color conjecture circuit based on memristor neural network is designed in this paper. The designed circuit mainly includes input module, judgment module, retained module and correction module. The input module can convert digital signals into analog signals, and the judgment module can judge whether the coloring situation conforms to the four-color theory. The retained module can screen out the coloring results that meet the four-color conjecture, while the correction module can converge the cases to four cases that meet the four-color conjecture. The realization of the four-color conjecture circuit based on memristor neural network shows that memristor neural network can design more complex circuits, which provides reference for the further development of more complex neural network circuits.

1. Introduction

In 1971, professor Chua of the university for California at Berkeley predicted the existence of fourth basic circuit element, memristor, from the perspective of symmetry [1]. Memristor is a new type of double-ended passive circuit element, which is different from resistor, inductor or capacitor and has the characteristic of memory [2–10]. In 2008, researchers at Hewlett–Packard (HP) laboratory realized a real memristor during the experiment of small circuits, and the results are published in Nature [11]. Thomas's team at the university of Bielefeld developed memristor with the learning ability in 2012, and analyzed how to turn natural phenomena into technical systems using computers that mimic the nervous system [12]. Memristor can realize storage and computation of the same physical device, which is suitable for realizing efficient bionic neural network on hardware [13–22]. A general three-dimensional discrete memristor-based map model is proposed by [23], which is used for auxiliary classifier generative adversarial nets for greatly improving the identification accuracy. Biological synapses are composed of simple neural networks by connecting neurons, and neural networks complete specific tasks by updating the synaptic weights [24–32]. A discrete memristive Rulkov neuron model is proposed by [33], which can well describe the actual firing activities in biological neurons.

As one of the three major problems in the history of modern mathematics, the four-color conjecture (4CC) was put forward in 1852 by Grace [34]. 4CC is also known as the four-color theorem and four-color problem, which means that on any map, these four colors can be used to draw different colors for neighboring countries. If each area is marked with numbers "1", "2", "3", "4", then the same number cannot appear in adjacent areas. The appearance of high speed calculator provides equipment support for the verification of 4CC. The four-color conjecture problem was proved in 1976 by professor Haakon and professor Appel using three high-speed electronic computers after more than 1200 h [35]. Although the 4CC problem has been verified by the computer, it still has a unique charm to attract the majority of scholars continue to study. As for the 4CC, many scholars have studied the problem based on the mathematical method, but the problem of realizing the 4CC based on the hardware circuit is seldom discussed [36–40].

To solve the problem that the hardware circuit of 4CC is difficult to realize, a 4CC circuit based on memristor neural network is designed in this work. This work builds a 4CC circuit based on memristor neural network by constructing the input module circuit, the judgment module circuit, the retained module circuit and the correction module circuit. The digital input signal is converted into analog signal by the input

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module, and the coloring condition is judged by the judging module to conform to the four-color theory. The retained module will retain the results conforming to the 4CC, and the correction module will converge the other results to the 4CC.

Compared with the existing studies [36–40], the advantages of this work are as follows: firstly, the circuit realizes four colors for five regions, which solves the problem that 4CC is difficult to be realized by hardware circuit. Secondly, the correction module designed in this paper can converge the non-ideal results to the results of the 4CC, ensuring the accuracy of the 4CC. Thirdly, the memristor neural network with variable structure can flexibly configure the circuit structure according to the task requirements, providing ideas for constructing more complex circuits.

This work is presented as follows: in Section 2, the model of memristor is introduced. In Section 3, the input module and the judgment module are designed. The rationed module and correction module are designed in Section 4. In Section 5, a four-color conjecture circuit based on memristor neural network is designed. Circuit simulation results and analysis are in Section 6. Finally, some conclusions are drawn in Section 7.

2. Memristor model

Since the first memristor model appeared in 2008, various memristor models have been developed successively [41–50]. A threshold memristor model based on AgInSbTe (AIST) is used in this paper [51]. The model is described as

$$M(t) = R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right) \tag{1}$$

$M(t)$ is the memristance, $w(t)$ is the width of the high doped region, D is the full thickness of memristive material. R_{ON} and R_{OFF} are resistance when the memristor is fully high doped and low doped, respectively. The derivative of the state variable $w(t)$ is

$$\frac{dw(t)}{dt} = \begin{cases} \mu_v \dfrac{R_{ON}}{D}\dfrac{i_{off}}{i(t) - i_0} f(w(t)), & v(t) > V_{T+} > 0 \\ 0, & V_{T-} \leqslant v(t) \leqslant V_{T+} \\ \mu_v \dfrac{R_{ON}}{D}\dfrac{i(t)}{i_{on}} f(w(t)), & v(t) < V_{T-} < 0 \end{cases} \tag{2}$$

μ_v represents the average ion mobility, i_0, i_{on} and i_{off} are constants. V_{T+} and V_{T-} are positive and negative threshold voltages, respectively. The memristance changes only when the voltage is greater than V_{T+} or less than V_{T-}. $f(w(t))$ as a window function is shown in the following formula. The window function in this paper is the Biolek function, which can avoid the boundary effect.

$$f(w(t)) = 1 - \left(\frac{w(t)}{D} - sgn(-i)\right)^{2p} \tag{3}$$

where p is a positive integer. The sgn is the sign function defined as

$$sgn(x) = \begin{cases} 1, & x > 0 \\ 0, & x = 0 \\ -1, & x < 0 \end{cases} \tag{4}$$

Two memristors are employed in the following circuit design, and their values are cited in [52]. These parameters of the memristors are shown in Table 1. The memristor parameter M_1 in Table 1 is used when the memristors are used to construct AND gates, OR gates. The memristor parameter M_2 is used in the memristor neural network.

3. Input module and the judgment module

There are many five-region structures in each map, so a 4CC circuits is designed for five regions in this work. As shown in Fig. 1, the five-region structure composed of the five neighboring provinces of Xinjiang, Xizang, Qinghai, Gansu and Sichuan in China is represented by the first region-fifth region, respectively. Assume that the four colors of a certain region are red, yellow, blue and green, and different voltage levels are used to represent the four colors. The $1V$ voltage is set to represent red, and the $2V$, $3V$, and $4V$ voltages are yellow, blue, and green, respectively. The input module is designed to convert random digital logic signals into required analog signals, expressed as $1V$-$4V$ analog voltage signals in this work.

Table 1
Parameters of threshold voltage memristor model.

Parameters	M_1	M_2
$R_{on}(\Omega)$	$1k$	100
$R_{off}(\Omega)$	$800k$	$1k$
$V_{TH+}(v)$	0.19	0.19
$V_{TH-}(v)$	−0.37	−0.37
$D(nm)$	3	3
$\mu_v(m^2 s^{-1}\Omega^{-1})$	$1.6e-15$	$1.6e-15$
$i_{off}(A)$	$1.0e-5$	$1.0e-5$
$i_0(A)$	$1.0e-3$	$1.0e-3$
p	10	10

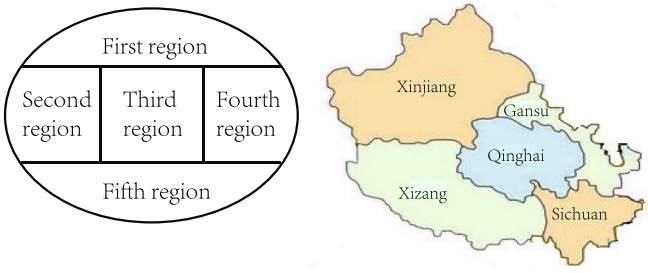

Fig. 1. Schematic diagram of five regions.

The input module converts the logic signal to $1V$-$4V$ voltage, which more intuitively distinguishes the four colors. The circuit diagram of the input module is shown in Fig. 2, which is mainly composed of five signal processing units. Each signal processing unit consists of two inverters, four three-input And gates, four switches, four resistors of the same resistance value, and three summing elements. In the first signal processing unit, switches K_1-K_4 can only be conducted under the action of a positive voltage on the left positive electrode. The signal of output for the signal processing unit is obtained by summing the outputs of the four switches. In the signal processing unit, the output signals of A_1A_0 have four cases, such as “00”, “01”, “10” and “11”, and the output of port Q is always high voltage. When A_1A_0 is “00”, the output signal of AND_1 is high voltage, and the output signal of O_1 is $1V$, and the region is colored in red. When A_1A_0 is “01”, the output signal of AND_2 is high voltage, and the output signal of O_1 is $2V$, and the region is colored yellow. When A_1A_0 is “10”, the output signal of AND_3 is high voltage, the output signal of O_1 is $3V$, and the region is colored blue. When A_1A_0 is “11”, the output signal of AND_4 is high voltage, the output signal of O_1 is $4V$, and the region is colored green.

In the five-region coloring problem, the numbers 1–4 represent the coloring situation. In the process of coloring, the adjacent regions will occur the phenomenon of coloring repetition. 4CC requires that the same coloration cannot occur in adjacent regions. In order to satisfy the requirement of the 4CC, it is necessary to judge the coloring situation of the region. The principle of judgment is to compare the adjacent output signals. If two adjacent colors are the same, the 4CC is not satisfied, and the output of the module is judged to be low voltage. If two adjacent colors meet the 4CC, the module output is judged to be high voltage. The

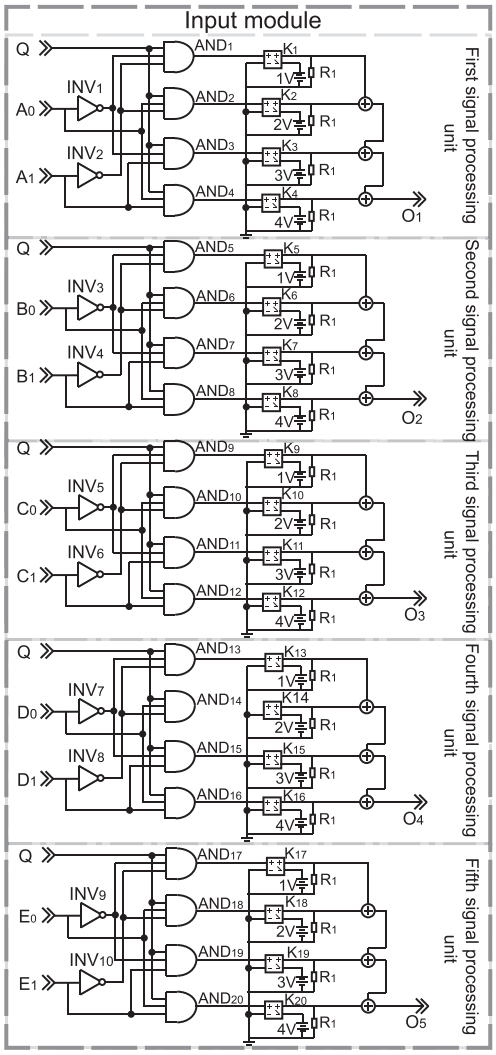

Fig. 2. Circuit diagram of input module. In signal processing unit one, A_0,A_1 and Q are input signals and O_1 is the signal of output. INV_1-INV_2 are inverters, AND_1-AND_4 are four three-input AND gates, K_1-K_4 are switches, and R_1 is a resistor.

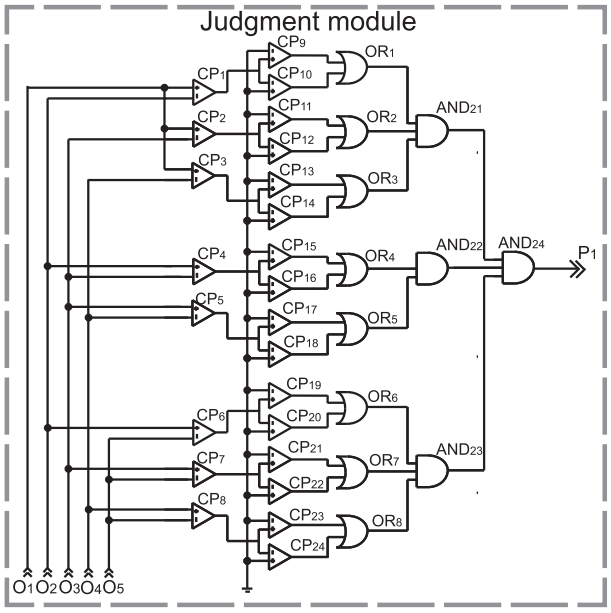

Fig. 3. Circuit diagram of judgment module. O_1-O_5 are input signals and P_1 is output signal. CP_1-CP_{24} are comparators, OR_1-OR_8 are OR gates, and AND_{21}-AND_{24} are And gates.

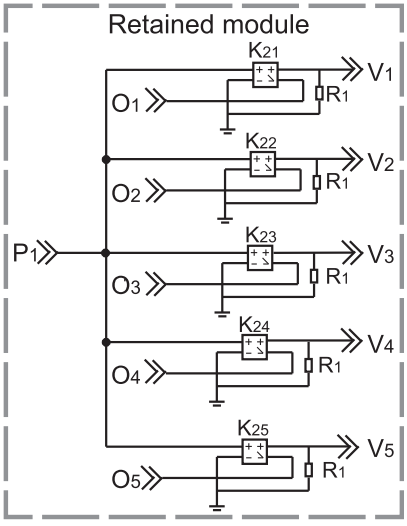

Fig. 4. Circuit diagram of retained module. O_1-O_5 and P_1 are input signals and the output signals are V_1-V_5. K_{21}-K_{25} are switches, and R_1 is a resistor.

circuit diagram of the judgment module is shown in Fig. 3. The input signal of the judgment module is the output signal of the input module, and the output signal of the judgment module is represented by P_1. The judgment module consists of twenty-four comparators and eight OR gates and four AND gates. If the output signal P_1 is high voltage, it indicates that the adjacent regions have not been repeatedly colored. If the output signal P_1 is low voltage, it indicates that the adjacent regions are repeatedly colored.

4. Retained module and correction module

The circuit of the retained module is shown in Fig. 4, which can screen out the results satisfying the 4CC. The signals of input for the retained module are O_1-O_5 and P_1, and the signals of output are V_1-V_5. The realization of the judgment module is the basis of designing the retained module. When P_1 is high voltage and the 4CC is satisfied, the signal of original can be retained, and the signals of output V_1-V_5 are the same as the signals of input O_1-O_5. When P_1 is low voltage, the signals of output V_1-V_5 are $0V$.

When the five-region map is colored, if each region is marked with numbers 1–4, there are only 72 situations satisfying the 4CC, and most of the cases do not satisfy the 4CC. The design of the correction module is to modify the situation that does not meet the requirements of the 4CC, so that these situations can meet the 4CC after correction. The circuit diagram of the correction module is shown in Fig. 5, its input signals are O_1-O_5 and output signals are V_6-V_{10}. The correction module is mainly composed of five switches, ten resistors, one memristor array, five amplifiers, five inverters and five buffers. In order to ensure that switches K_{26}-K_{30} are always "ON", their left positive poles are always connected to the $5V$ power supply, and the left negative poles are uniformly grounded. The right positive poles of K_{26}-K_{30} are connected to the memristor array, and the right negative poles are connected to the signals of input O_1-O_5. The signals of output for the memristor array are connected to the amplifiers AM_1-AM_5, respectively, and the negative poles of the amplifiers are grounded. The signals of output for the amplifiers are connected to the inverters INV_{11}-INV_{15}, respectively, and the signals of output for the inverters are connected to the endpoints of input for the buffers BUF_1-BUF_5, and the output signals of the buffers are

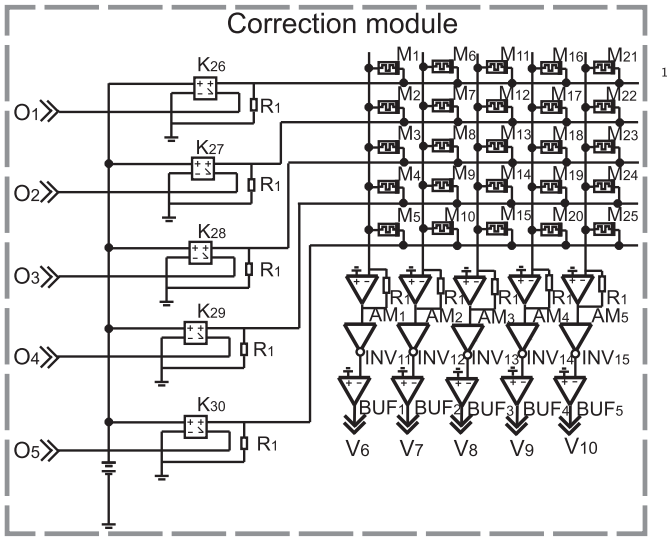

Fig. 5. Circuit diagram of correction module. O_1-O_5 are signals of input and the signals of output are V_6-V_{10}. K_{26}-K_{30} are switches, M_1-M_{25} are memristors, INV_{11}-INV_{15} are inverters, AM_1-AM_5 are amplifiers, BUF_1-BUF_5 are buffers and R_1 is a resistor.

V_6-V_{10}.

In the correction module, the threshold voltage of BUF_1 is $2.05V$. The output result of V_6 is $4V$, when the output voltage of INV_{11} is greater than $2.05V$. The output result of V_6 is $1V$, when the output voltage of INV_{11} is less than $2.05V$. The threshold voltages of BUF_2 and BUF_4 are $0.8V$. When the input signals of BUF_2 and BUF_4 are greater than $0.8V$, the output signals of V_7 and V_9 are $2V$, otherwise, they are $0V$. When the input signal of BUF_3 is greater than $0.8V$, and the output signal of V_8 is $3V$, otherwise $0V$. The threshold voltage of BUF_5 is $1.55V$, and when the output voltage of INV_{15} is greater than $1.55V$, the output signal of V_{10} is $4V$. When the output voltage of INV_{15} is less than $1.55V$, the output signal of V_{10} is $1V$. In the correction module, a 5×5 memristor array, five amplifiers, five inverters and five buffers together create a neuromorphic circuit. The function expression is given as follows

$$X(N) = \begin{cases} High \quad voltage, & N > 0 \\ Low \quad voltage, & N < 0 \end{cases} \tag{5}$$

where $X(N)$ represents the window function and N represents a variable, then the circuit can be expressed as

$$\begin{bmatrix} V_6 \\ V_7 \\ V_8 \\ V_9 \\ V_{10} \end{bmatrix} = X \left(\begin{bmatrix} \frac{R_1}{M_1} & \frac{R_1}{M_6} & \frac{R_1}{M_{11}} & \frac{R_1}{M_{16}} & \frac{R_1}{M_{21}} \\ \frac{R_1}{M_2} & \frac{R_1}{M_7} & \frac{R_1}{M_{12}} & \frac{R_1}{M_{17}} & \frac{R_1}{M_{22}} \\ \frac{R_1}{M_3} & \frac{R_1}{M_8} & \frac{R_1}{M_{13}} & \frac{R_1}{M_{18}} & \frac{R_1}{M_{23}} \\ \frac{R_1}{M_4} & \frac{R_1}{M_9} & \frac{R_1}{M_{14}} & \frac{R_1}{M_{19}} & \frac{R_1}{M_{24}} \\ \frac{R_1}{M_5} & \frac{R_1}{M_{10}} & \frac{R_1}{M_{15}} & \frac{R_1}{M_{20}} & \frac{R_1}{M_{25}} \end{bmatrix} * \begin{bmatrix} O_1 \\ O_2 \\ O_3 \\ O_4 \\ O_5 \end{bmatrix} - \begin{bmatrix} V_{T1} \\ V_{T2} \\ V_{T3} \\ V_{T4} \\ V_{T5} \end{bmatrix} \right) \tag{6}$$

where V_{T1}-V_{T5} represent the threshold voltages of BUF_1-BUF_5, respectively. The memristor resistance value shown in formula (7) is the weight of the memristor neural network. In this study, due to the small amount of data and simple relationship, linear regression method is adopted to train weights in Python. The resistance is $1K\Omega$, and the resistance matrix of memristor array is

$$M = \begin{bmatrix} 10K & 10K & 10K & 10K & 10K \\ 5K & 5K & 5K & 5K & 5K \\ 5K & 3.3K & 5K & 5K & 5K \\ 3.3K & 3.3K & 3.3K & 3.3K & 10K \\ 10K & 10K & 10K & 10K & 10K \end{bmatrix} \tag{7}$$

Substituting the value of formula (7) into formula (6), we can get

$$\begin{bmatrix} V_6 \\ V_7 \\ V_8 \\ V_9 \\ V_{10} \end{bmatrix} \approx X \left(\begin{bmatrix} 0.1 & 0.1 & 0.1 & 0.1 & 0.1 \\ 0.2 & 0.2 & 0.2 & 0.2 & 0.2 \\ 0.2 & 0.3 & 0.2 & 0.2 & 0.2 \\ 0.3 & 0.3 & 0.3 & 0.3 & 0.1 \\ 0.1 & 0.1 & 0.1 & 0.1 & 0.1 \end{bmatrix} * \begin{bmatrix} O_1 \\ O_2 \\ O_3 \\ O_4 \\ O_5 \end{bmatrix} - \begin{bmatrix} 2.05 \\ 0.8 \\ 0.8 \\ 0.8 \\ 1.55 \end{bmatrix} \right) \tag{8}$$

The correction module circuit designed in this work can use the memristor neuromorphic circuit to converge the error for the coloring condition that satisfies the 4CC.

5. Four color conjecture circuit based on memristor neural network

The complete circuit of 4CC based on memristor neural network is shown in Fig. 6. The input signals of the complete circuit are the input signals of the input module, and the output signals are V_1-V_{10}. The input signals are first converted from digital signal to analog signal through the input module. Each signal processing unit can obtain the voltage of $1V$-$4V$ to represent the four colors of red, yellow, blue and green, respectively. When the output signal is high voltage, it conforms to the 4CC. When the output signal is low voltage, the 4CC is not met. The input signal of the retained module is connected to the output signal of the judgment module. When the output signal of the judgment module is high voltage, the retained module retains the original output signal of the input module. When the output signal of the module is judged to be low voltage, the output signals of the retained module are all zero. The correction module can convert all the input signals into the correct condition of the 4CC.

6. Simulation results and analyses

6.1. Results of simulation

The logic signals of the input module have a total of $2^2 * 2^2 * 2^2 * 2^2 * 2^2 = 1024$ cases, which cannot be enumerated in this work, only part of the cases is enumerated in the simulation. The signals of input for the input module are shown in Fig. 7, and each second represents one input situation. In Fig. 7, Q is always high voltage, and $A_1A_0, B_1B_0, C_1C_0, D_1D_0$ and E_1E_0 are the logical input signals to control the coloring of the five regions, respectively. For example, when 0–1s, the input signal of A_1A_0 is "00", then the output signal of the first signal processing unit is predicted to be $1V$, and the color of the first region is red. When the input signal of B_1B_0 is "01", the output signal of the second processing unit is predicted to be $2V$, and the color of the second region is yellow. When the input signal of C_1C_0 is "10", the output signal of the third processing unit is predicted to be $3V$, and the color of the third region is blue. When the input signal of D_1D_0 is "01", the output signal of the fourth processing unit is predicted to be $2V$, and the color of the fourth region is yellow. When the input signal of E_1E_0 is "11", the output signal of the fifth processing unit is predicted to be $4V$, and the color of the fifth region is green. At 1–36s, the principle is similar to that of 0–1s.

Fig. 8 is the simulation diagram of the input module, with a total of 36 cases in 0–36s. At 0–1s, the output signal of O_1 is $1V$, indicating that the first region is colored red. The output signal of O_2 is $2V$, indicating that the second region is colored yellow. The output signal of O_3 is $3V$, indicating that the third region is colored blue. The output signal of O_4 is $2V$, indicating that the fourth region is colored yellow. The output signal of O_5 is $4V$, indicating that the fifth region is colored green. Therefore,

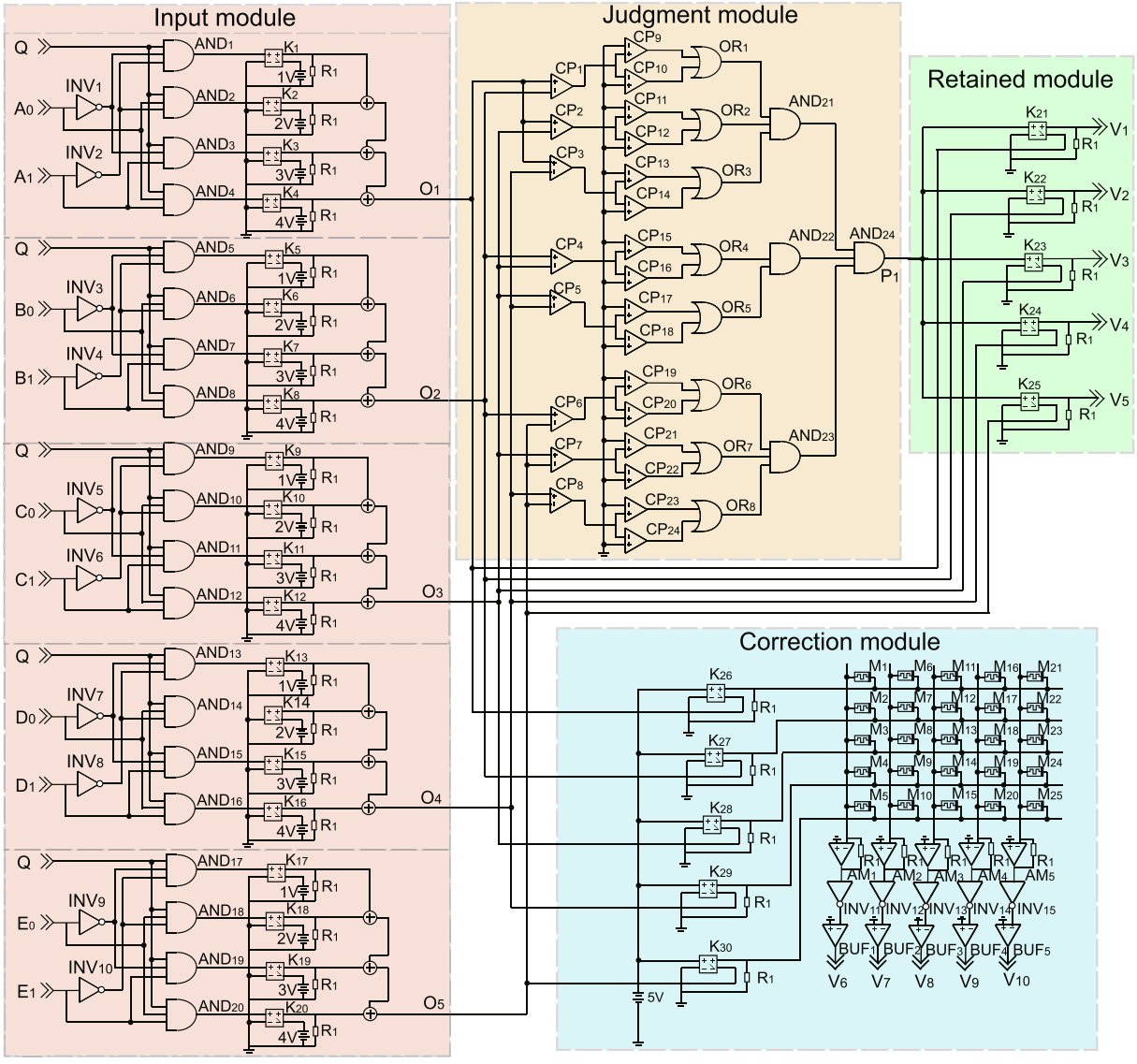

Fig. 6. Schematic diagram of 4CC circuit based on memristor neural network.

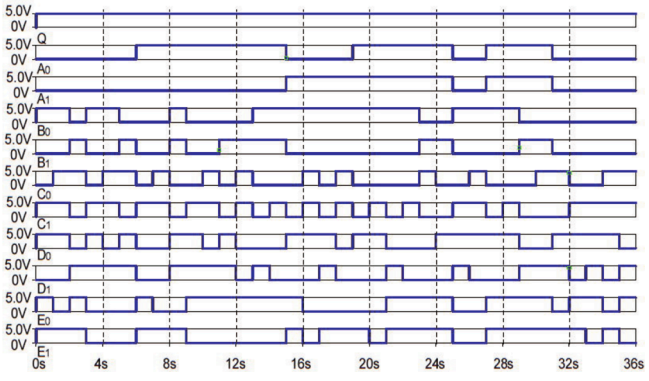

Fig. 7. Simulation diagram of the input signal.

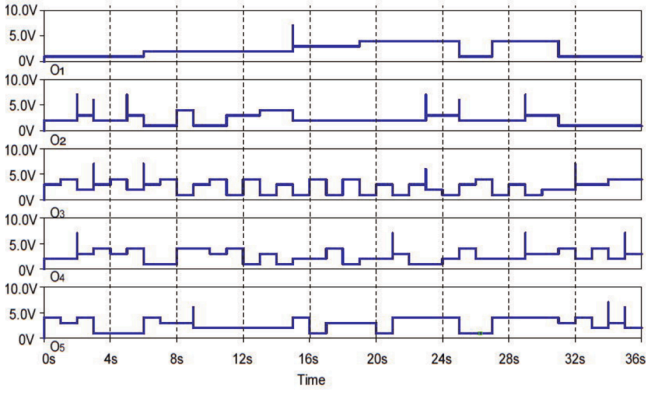

Fig. 8. Simulation diagram of the input module.

during 0–1*s*, the five regions are colored as red, yellow, blue, yellow, and green, respectively, which is the same as the predicted result and meets the 4CC. At 1–36*s*, there are 35 cases in total, and the analysis principle is similar to the above.

The simulation of the judgment module and the retained module are shown in Fig. 9, where P_1 is the output signal of the judgment module. The simulation results show that at 0–31*s*, the output signal of P_1 is always high voltage, indicating that the input conditions of 0–31*s* all meet the 4CC. At 31–36*s*, the output signal of P_1 is always low voltage,

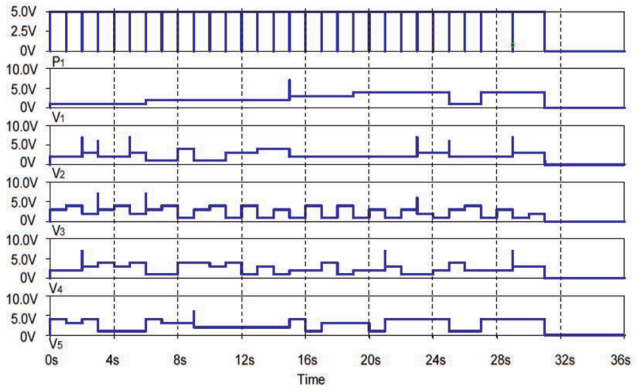

Fig. 9. Simulation diagram of the judgment module and the retained module.

indicating that the input conditions of 31–36*s* do not satisfy the 4CC. The simulation results of the retained module are shown as the output signals of V_1-V_5. The simulation results indicate that when the output signal has a voltage value at 0–31*s*, the output analog voltage satisfying the 4CC is retained. At 31–36*s*, the output signals are all zero, indicating that the retained module does not retain the output analog voltage that does not meet the 4CC.

The simulation results of the correction module are shown in Fig. 10. There are only 72 cases satisfying the 4CC due to the many input cases of five-region coloring. In order to correct these cases which do not satisfy the 4CC, a correction module is designed in this work. The simulation results of the correction module show that there is voltage output from 0*s* to 36*s*, and it is converged to four results: "42324", "42321", "12324" and "12321". For example, the results of 0–6*s*, 8–15*s*, 16–19*s*, 20–26*s*, 28–31*s* and 35–36*s* all converge to "42324", that is, the five regions are colored as "green, yellow, blue, yellow, green", respectively. In 6–7*s*, 15–16*s*, 19–20*s* and 32–33*s*, the results all converge to "12321", that is, the five regions are colored as "red, yellow, blue, yellow, red", respectively. In 7–8*s*, 26–28*s* and 34–35*s*, the results all converge to "12324", that is, the five regions are colored as "red, yellow, blue, yellow, green", respectively. At 31–32*s* and 33–34*s*, the results all converge to "42321", that is, the five regions are colored as "green, yellow, blue, yellow, red", respectively. The above four cases are consistent with the 4CC.

6.2. Circuit analyses

Compared with the traditional digital CMOS electronics, the memristor array designed by Dalgaty's team consumes five orders of magnitude less energy(100,000 times) [53]. The circuit of the 4CC can be further simplified, and the input module and the judgment module can be designed more simply. In order to reduce the volume and area of the circuit, AND and OR logic gates in the original circuit can be replaced by AND and OR logic gates based on memristor. Implementing

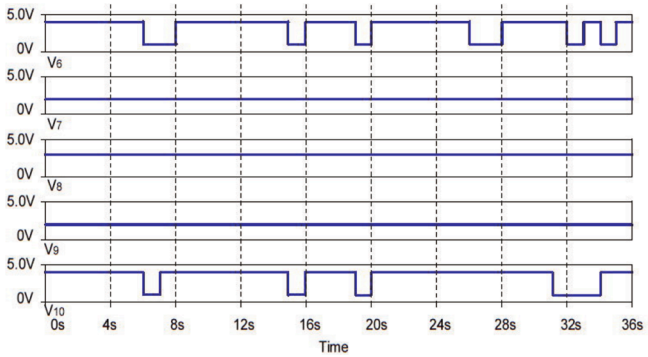

Fig. 10. Simulation diagram of the correction module.

a three-input AND logic gate requires three memristors, and implementing a two-input AND logic gate and OR gate requires two memristors. The circuit size of digital circuit components is much larger than that of memristor. Memristor also has some advantages by replacing it with CMOS device of smaller size and area. The comparison diagram is shown in Fig. 11.

In Fig. 11, six CMOS elements are needed to implement the two-input AND gate and OR gate based on CMOS, and eight CMOS elements are needed to implement the three-input AND gate. Since the number of memristor elements is less and the volume is smaller than that of CMOS elements, the circuit design based on memristor has some advantages in area and volume. In the 4CC circuit based on memristor, the input module has twenty-three-input AND gates, and the judgment module has eight two-input OR gates, one two-input AND gate and three three-input AND gates. Therefore, the number of memristors used for input module and judgment module based on memristors is $(20+3)*3+(8+1)*2=87$. In contrast, the number of CMOS components used in the CMOS implementation input module and judgment module is $(20+3)*8+(8+1)*6=238$. The number of components used in the input module and judgment module based on CMOS is significantly higher than that of memristor, which proves that the 4CC circuit based on memristor has certain advantages in area. In addition, the convergence module uses memristor array to build memristor neural network. Compared with the traditional hardware circuit, it can change the weight without changing the component, which is powerful and smaller in size. To sum up, the 4CC circuit designed in this chapter has the characteristics of smaller volume, flexible construction and stronger functionality, so it has advantages over the traditional circuit.

7. Conclusion

A 4CC circuit based on memristor neural network is constructed by bond memristor neural network with combination circuit for the 4CC problem of five regions. This work solves the problem that 4CC is difficult to be realized by hardware circuit, and aims to further understand the research of 4CC. The circuit is composed of input module, judgment module, retained module and correction module. The input module converts the logical signal into an analog voltage to interpret the coloring of each region. The judgment module plays a role in determining whether the coloration of the five regions conforms to the 4CC. The ratained module can distinguish whether the signal conforms to the 4CC. The correction module realizes the convergence of the cases to the correct results, and greatly improves the results which is not conforming to the 4CC. The design of this circuit has proved that memristor neural network has great compatibility, and can flexibly build circuits to meet

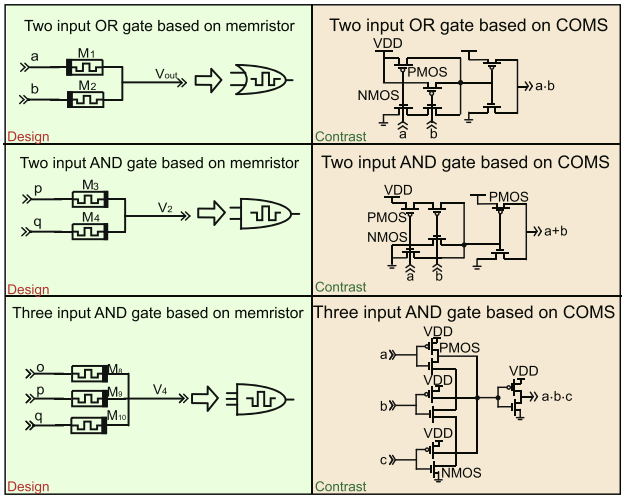

Fig. 11. Schematic diagram of memristor circuit and CMOS circuit comparison.

the task requirements, which provides a reference for more complex circuit design and the application of memristor neural network.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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