



CNT-MOSFET modeling based on artificial neural network: Application to simulation of nanoscale circuits

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ABSTRACT

In this paper, we have applied artificial neural network (ANN) for modeling and simulation of carbon nanotube metal–oxide–semiconductor field-effect transistors (CNT-MOSFETs). The simulation is based on ANN model which reduces the computational time while keeping the accuracy of physics-based model like non-equilibrium Green's function (NEGF) formalism. Finally, the proposed ANN model is imported into HSPICE software as a subcircuit. Results show that the ANN model is suitable to be incorporated into Spice-like tools for nanoscale circuits simulation.

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1. Introduction

Over the last 40 years, semiconductor device technology has been developing at an amazing speed. The industry manages to squeeze more and more transistors by scaling down the size of a single transistor since reducing the physical dimensions of transistor increases the clock frequency of a circuit without increasing its power dissipation.

As the MOSFET gate length enters nanometer scale, short channel effect such as threshold voltage roll-off and drain-induced-barrier-lowering become increasingly significant, which limit the scaling capability of MOSFET [1,2].

Scaling MOSFETs to their limits is a key challenge faced by the semiconductor industry. Physically detailed simulations which capture the off-equilibrium transport (e.g. velocity overshoot) and the quantum mechanical effects that occur in these devices can complement experimental work in addressing these challenges [3,4].

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Carbon nanotubes (CNTs) [5,6] due to their excellent electrical properties are considered as promising building blocks for nano-electronic devices. The high current-carrying capacity and reduced charge carrier scattering, combined with the huge resilience of CNTs promise to solve challenges in the interconnect area. But the low effective electron–hole mass and the absence of dangling bonds addresses the need for a fast energy – efficient and high k dielectric compatible device for the future [7–9].

Transistor devices made of semiconducting single wall carbon nanotubes (SWCNTs) [6] can be considered as simple silicon MOS field – effect transistors with the silicon material replaced by the carbon nanotube structure. This new class of transistors which are known as carbon nanotube field-effect transistors (CNTFETs) are one of the current leading technologies to replace MOSFETs [10–12].

The physical structure of CNTFET is similar to the conventional MOSFET and its I – V and transfer characteristics are also very promising and is being suggested that CNTFET has the potential for successful replacement of MOSFET in nanoscale electronics.

Recently, CNTFETs have been fabricated successfully [13–15]. It has been reported that they have shown better performance than present silicon transistors with the equivalent sizes.

The device structure used in this study is shown in Fig. 1, where L_C is the intrinsic channel length and t_{ins} is the oxide thickness with

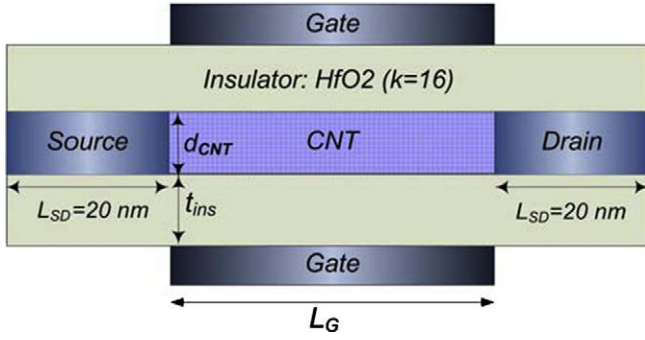


Fig. 1. Sketch of the device structure for the CNT-MOSFET using a cylindrical gate to ensure full gate control.

the relative dielectric constant k . A zigzag $(n, 0)$ carbon nanotube with diameter d_{CNT} is assumed. The nanotube diameter d_{CNT} is related to the chirality n in the following equation [16]:

$$d_{CNT} = \sqrt{3} \frac{a_{c-c} n}{\pi} \quad (1)$$

where a_{c-c} is the carbon–carbon bond length (1.42 Å). In order to simulate this device, self consistent solution of the Poisson and Schrödinger equations is used by means of NEGF formalism.

The NEGF method [17–19] provides a sound approach for simulating the non-equilibrium nanoscale systems. Using NEGF method for solving the Schrödinger equation, the density of states and the charge on the surface of the CNT are calculated. Subsequently, utilizing the calculated charge and solving the Poisson equation, the new electrostatic potential are obtained [20]. However, due to the complexity and time-consuming behavior of these analyses, it is being necessary to apply a fast method that can be used in SPICE-type circuit simulators. In this regard, therefore, a high computational speed is necessary if the model is to be implemented in a SPICE simulator.

Following the recent advances made in the understanding of carbon nanotube transistor operation, several models have been developed for implementation in SPICE-like simulators for designing and simulating the future analog and digital systems built with CNT devices. Kazmierski et al. [21] presented a carbon nanotube transistor modeling technique which is based on a numerical piece-wise non-linear approximation of the non-equilibrium mobile charge density. Dwyer et al. [22] developed a SPICE model of CNTFET nanoelectronics which is parameterizable. Paul et al. [23] proposed a quasi-analytical device model for intrinsic ballistic CNTFET which can be used in conventional circuit simulator like SPICE.

This paper presents the application of artificial neural network for the modeling and simulation of CNT-MOSFETs where, the proposed ANN model is being optimized based on data obtained by using the MATLAB script named moscnt.1.0 [24–26]. In this program, ballistic transport in CNT-MOSFETs is simulated using the NEGF formalism. A cylindrical transistor geometry with wrapped-around gate and doped source/drain regions is assumed as shown in Fig. 1.

Finally, we have shown that the proposed ANN model can be used as a block in circuit simulators like HSPICE, ADS and etc. for simulation of nanoscale circuits.

2. Neural network computations

The artificial neural networks are strong tools for prediction and simulation in engineering applications, which are composed of simple elements operating in parallel [27]. Neural network ap-

proach is a way of modeling data based on computer learning which are basically trained to perform complex functions in various fields of applications including pattern recognition, identification, classification, speech, vision and control systems [28].

The multi-layer perceptron (MLP) networks are the most widely used neural networks that consist of a great number of processing elements called neurons. Neurons, which are processing elements in a MLP, are connected to each other through a set of weights. These weights are adjusted based on an error-minimization technique called back-propagation rule. A diagram of a typical MLP neural network with one hidden layer is shown in Fig. 2.

The network consists of three layers named as input layer, hidden layer and output layer. Each layer has its own number of neurons. The input to the node l in the hidden layer is given by

$$\eta_l = \sum_{u=1}^q (x_u w_{ul}) + \theta_l \quad l = 1, 2, \dots, s \quad (2)$$

where s is the number of neurons in the hidden layer, q is the number of neurons in the input layer, θ is the bias term and w is the weighting factor [27]. The output from l th neuron of the hidden layer is given by

$$o_l = f(\eta_l) \quad (3)$$

where f is the activation function of the hidden layer. Some of the commonly used activation functions are threshold, Gaussian and tan-sigmoid functions. MLP neural networks often make use of the tan-sigmoid transfer function in the hidden layer, therefore, the output from l th neuron of the hidden layer is given by

$$o_l = \text{Tansig}(\eta_l) = \frac{2}{1 + \exp(-2\eta_l)} - 1 \quad (4)$$

The output of the j th neuron in the output layer is given by

$$y_j = \sum_{u=1}^s (o_u w_{uj}) + b_j \quad j = 1, 2, \dots, m \quad (5)$$

where b is the bias term, w is the weighting factor and m is the number of neurons in the output layer [27].

This network can be used as a general function approximator that can approximate any function with a finite number of neurons in the hidden layer.

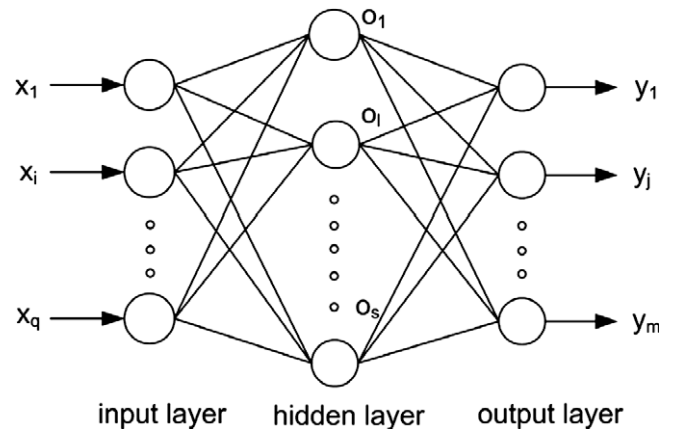


Fig. 2. Schematic diagram of MLP neural network.

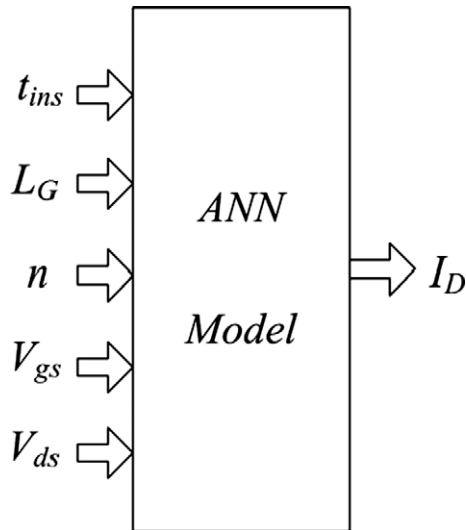


Fig. 3. A simplified overview of the proposed ANN model for CNT-MOSFET modeling.

The training of a network is a process where the set of adjusted parameters (weights and biases) is optimized in order to make the best prediction of the target variable on the basis of background variables. MLP networks are trained with the standard back-propagation algorithm [28]. Back-propagation algorithm basically consists of two steps: a forward step where the signal propagates through the computational units until it gets to the output layer and a backward step where all the synaptic weights are adjusted accordingly to an error correction rule. In this method, the adjusted parameters are determined iteratively to achieve a minimum mean square error between the network output and the target values.

In this paper, we have presented an ANN model to relate the input parameters i.e., L_G , V_{ds} , V_{gs} , t_{ins} and n to the output parameter I_D , where L_G is the channel length, V_{ds} is the drain-source voltage, V_{gs} is the gate-source voltage, t_{ins} is the oxide thickness, n is the chirality of the carbon nanotube and I_D is the drain current in CNT-MOSFET. A simplified overview of the proposed ANN model is shown in Fig. 3.

It is important to be noted that the number of input parameters of proposed ANN model can be extended to other parameters such as, temperature, oxide dielectric, . . . , etc.

3. Results and discussion

To build the ANN model, about 3000 data were obtained by simulation of CNT-MOSFET using moscnt.1.0. The minimum and maximum data ranges used for developing the ANN model are shown in Table 1.

About 2000 data were selected for training the ANN model and the remaining were used for testing. Training and testing data were

Table 1
Data ranges used for developing the ANN model.

Range	Input					Output
	t_{ins} (nm)	L_G (nm)	n	V_{gs} (V)	V_{ds} (V)	I_D (μA)
Min	1	5	10	0	0	0
Max	3	20	25	0.5	0.5	40

Table 2

Percentage mean relative error (MRE%) comparison for different ANN structures.

ANN structure	MRE%	
	Train	Test
5-9-8-1	0.96	1.09
5-11-6-1	1.07	1.22
5-7-4-7-1	1.37	1.5
5-5-5-5-1	2.09	2.26
5-7-9-1	1.55	1.64

selected randomly from the original data set. We used MATLAB 7.0.4 software for training the ANN models.

In this study, different neural network structures were tested and optimized to obtain the best ANN configuration for modeling of CNT-MOSFETs. We tested many different structures with two and three hidden layers with different number of neurons in each layer. Training was confined to 1000 epochs. The number of neurons for each hidden layer were in the range of 4–12.

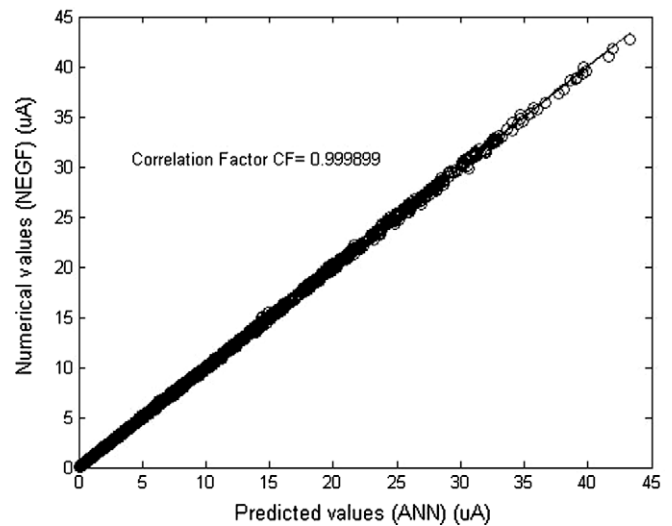


Fig. 4. Comparison of numerical (NEGF) and predicted (ANN) results for training data.

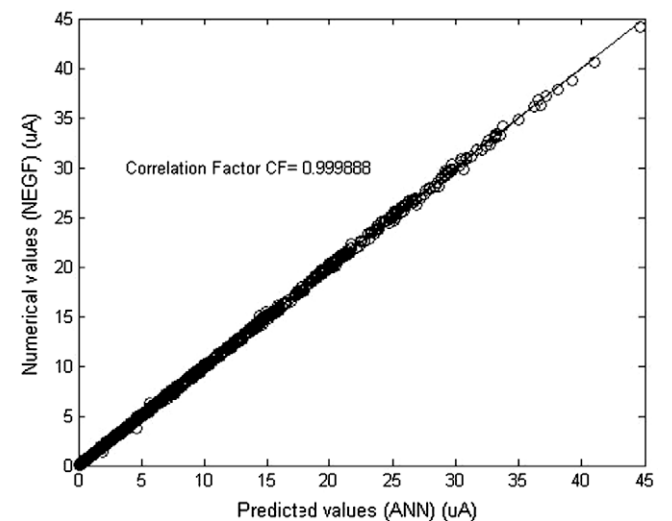


Fig. 5. Comparison of numerical (NEGF) and predicted (ANN) results for testing data.

Table 2 shows the comparison between different ANN model topologies, where percentage mean relative error (MRE%) is given by:

$$MRE\% = 100 \times \frac{1}{N} \times \sum_{i=1}^N \left| \frac{X_i(Num) - X_i(pred)}{X_i(Num)} \right| \quad (6)$$

where 'X(Num)' and 'X(Pred)' stand for numerical (NEGF) and predicted (ANN) values, respectively, and N is the number of data.

As it is shown in Table 2, the MLP model with 5-9-8-1 structure (i.e., five neurons in the input layer, nine neurons in the first hidden layer, eight neurons in the second hidden layer and one neuron in the output layer) has the least MRE%. Therefore, we selected this structure for modeling of CNT-MOSFETs.

The training and testing results of the proposed ANN model are shown in Figs. 4 and 5, respectively.

The comparison of current–voltage characteristics (I_D – V_{ds} and I_D – V_{gs}) between moscnt.1.0 simulation (NEGF) and the proposed ANN model for a CNT-MOSFET with $L_G = 20$ nm, $n = 17$ and $t_{ins} = 3$ nm is shown in Figs. 6 and 7. From these figures, it is observed that the proposed ANN model matches closely with the NEGF model (moscnt.1.0 simulation) for all ranges of biases.

Besides high accuracy, the speed of calculations of the ANN model to obtain the results are extremely fast. We measured the CPU times for ANN model against the numerical model implemented in moscnt.1.0. Table 3 compares the average CPU times for ANN and moscnt.1.0 simulations. It is clear that the ANN model is much faster than moscnt.1.0.

The obtained results show that the ANN approach can be used as an efficient tool for simulation of CNT-MOSFETs with high speed and good accuracy. So, the proposed ANN model can be used for simulation of nanoscale circuits.

3.1. Implementation into HSPICE

We can use the proposed ANN model as a subcircuit in HSPICE software. A CNT-MOSFET can be modeled as a voltage-controlled current source between drain and source where the current value can be calculated with the neural network equations and a null current source between gate and source (because the gate current

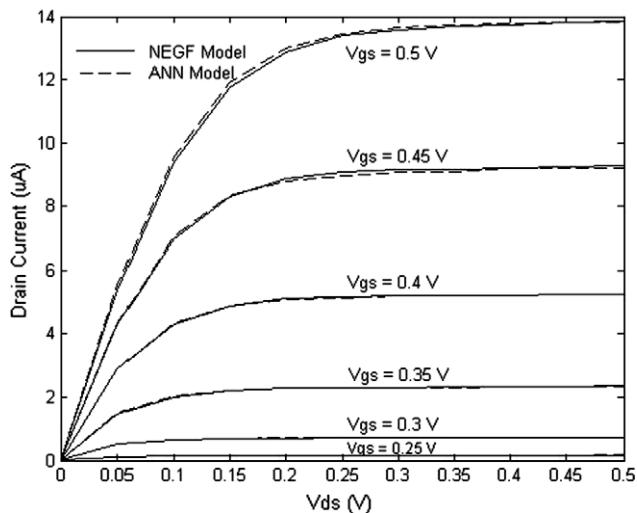


Fig. 6. Current–voltage characteristics curve (I_D – V_{ds}) for CNT-MOSFET ($L_G = 20$ nm, $n = 17$ and $t_{ins} = 3$ nm) using NEGF (solid line) and ANN (dashed line).

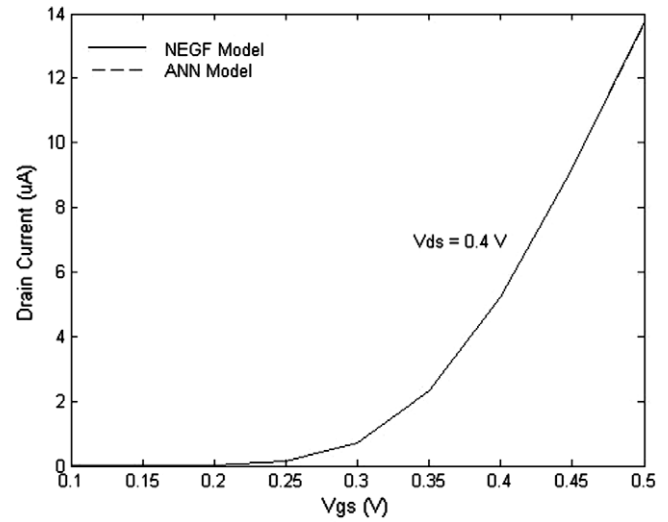


Fig. 7. Current–voltage characteristics curve (I_D – V_{gs}) for CNT-MOSFET ($L_G = 20$ nm, $n = 17$ and $t_{ins} = 3$ nm) using NEGF (solid line) and ANN (dashed line).

Table 3

Average CPU time (s) comparison between the proposed ANN model and moscnt.1.0.

No. of simulation data	moscnt.1.0	ANN
5	1890	Less than 0.05
10	3900	0.33
50	21750	0.78
100	43650	1.2

of the MOS transistor is always neglected [29]). The general syntax form in HSPICE software is:

```
.SUBCKT SubName D G S
ig G S 0
gdrain D S cur = 'neural network equations to obtain the drain current'
.ENDS
```

where 'SubName' is the reference name for the subcircuit model call, 'D', 'G' and 'S' stand for drain, gate and source nodes, respectively, 'ig' is a null current source between gate and source, 'gdrain' is the voltage-controlled current source and its current (I_D) is obtained by using the input parameters set $\{L_G, V_{ds}, V_{gs}, t_{ins}, n\}$ as shown in Fig. 3.

Table 4 shows the HSPICE input listing used to simulate the proposed ANN CNT-MOSFET model. In this HSPICE input listing, we have used the weights and biases of the neural network model in HSPICE environment to simulate the CNT-MOSFET neural based model. The advantage of this method is that we have simulated the complex and time consuming quantum mechanical calculations by using the simple mathematical Eqs. (2)–(5).

In order to validate our ANN model, the simulation of the CNT-MOSFET inverter that is constituted of a CNT-MOSFET in series with a resistor placed on its drain is proposed. Fig. 8 shows the transfer curve of CNT-MOSFET inverter gate composed of a CNT-MOSFET with $L_G = 20$ nm, $n = 17$ and $t_{ins} = 3$ nm. Fig. 9 shows the input and output signals of this inverter gate.

It is important to note that our CNT-MOSFET model can be realistically extended to other practical circuits with many devices like nano-current source.

Table 4

The HSPICE input listing used to simulate the proposed ANN CNT-MOSFET model.

```

*Wljk is the connecting weight between neuron j and neuron k in layer l
*xi (i = 1, ..., 9) is the output from i th neuron of the first hidden layer
*yj (j = 1, ..., 8) is the output from j th neuron of the second hidden layer
*f is the output of the only neuron in the output layer
*n1, n2 and n3 stand for drain, gate and source nodes, respectively
*the gate current (igate) is assumed to be zero
*Define the input parameters (channel length, oxide thickness and chirality)
.param LG = 5 tins = 1 n = 10

*Hidden layer 1
.param k1 = 'W111*par(tins) - W121*par(LG) - W131*par(n) - W141*V(GS) + W151*V(DS) + b11'
.param k2 = 'W112*par(tins) - W122*par(LG) - W132*par(n) - W142*V(GS) + W152*V(DS) + b12'
.param k3 = 'W113*par(tins) - W123*par(LG) - W133*par(n) - W143*V(GS) + W153*V(DS) + b13'
.param k4 = 'W114*par(tins) - W124*par(LG) - W134*par(n) - W144*V(GS) + W154*V(DS) + b14'
.param k5 = 'W115*par(tins) - W125*par(LG) - W135*par(n) - W145*V(GS) + W155*V(DS) + b15'
.param k6 = 'W116*par(tins) - W126*par(LG) - W136*par(n) - W146*V(GS) + W156*V(DS) + b16'
.param k7 = 'W117*par(tins) - W127*par(LG) - W137*par(n) - W147*V(GS) + W157*V(DS) + b17'
.param k8 = 'W118*par(tins) - W128*par(LG) - W138*par(n) - W148*V(GS) + W158*V(DS) + b18'
.param k9 = 'W119*par(tins) - W129*par(LG) - W139*par(n) - W149*V(GS) + W159*V(DS) + b19'

.param x1 = '(2/(1 + exp(-2*par(k1)))) - 1'
.param x2 = '(2/(1 + exp(-2*par(k2)))) - 1'
.param x3 = '(2/(1 + exp(-2*par(k3)))) - 1'
.param x4 = '(2/(1 + exp(-2*par(k4)))) - 1'
.param x5 = '(2/(1 + exp(-2*par(k5)))) - 1'
.param x6 = '(2/(1 + exp(-2*par(k6)))) - 1'
.param x7 = '(2/(1 + exp(-2*par(k7)))) - 1'
.param x8 = '(2/(1 + exp(-2*par(k8)))) - 1'
.param x9 = '(2/(1 + exp(-2*par(k9)))) - 1'

*Hidden layer 2
.param z1 = 'W211*par(x1) + W221*par(x2) - W231*par(x3) + W241*par(x4) + W251*par(x5) + W261*par(x6) +
W271*par(x7) - W281*par(x8) + W291*par(x9) + b21'
.param z2 = 'W212*par(x1) + W222*par(x2) - W232*par(x3) + W242*par(x4) + W252*par(x5) + W262*par(x6) +
W272*par(x7) - W282*par(x8) + W292*par(x9) + b22'
.param z3 = 'W213*par(x1) + W223*par(x2) - W233*par(x3) + W243*par(x4) + W253*par(x5) + W263*par(x6) +
W273*par(x7) - W283*par(x8) + W293*par(x9) + b23'
.param z4 = 'W214*par(x1) + W224*par(x2) - W234*par(x3) + W244*par(x4) + W254*par(x5) + W264*par(x6) +
W274*par(x7) - W284*par(x8) + W294*par(x9) + b24'
.param z5 = 'W215*par(x1) + W225*par(x2) - W235*par(x3) + W245*par(x4) + W255*par(x5) + W265*par(x6) +
W275*par(x7) - W285*par(x8) + W295*par(x9) + b25'
.param z6 = 'W216*par(x1) + W226*par(x2) - W236*par(x3) + W246*par(x4) + W256*par(x5) + W266*par(x6) +
W276*par(x7) - W286*par(x8) + W296*par(x9) + b26'
.param z7 = 'W217*par(x1) + W227*par(x2) - W237*par(x3) + W247*par(x4) + W257*par(x5) + W267*par(x6) +
W277*par(x7) - W287*par(x8) + W297*par(x9) + b27'
.param z8 = 'W218*par(x1) + W228*par(x2) - W238*par(x3) + W248*par(x4) + W258*par(x5) + W268*par(x6) +
W278*par(x7) - W288*par(x8) + W298*par(x9) + b28'

.param y1 = '2/(1 + exp(-2*par(z1))) - 1'
.param y2 = '2/(1 + exp(-2*par(z2))) - 1'
.param y3 = '2/(1 + exp(-2*par(z3))) - 1'
.param y4 = '2/(1 + exp(-2*par(z4))) - 1'
.param y5 = '2/(1 + exp(-2*par(z5))) - 1'
.param y6 = '2/(1 + exp(-2*par(z6))) - 1'
.param y7 = '2/(1 + exp(-2*par(z7))) - 1'
.param y8 = '2/(1 + exp(-2*par(z8))) - 1'

*Output layer
.param f = 'W311*par(z1) + W321*par(z2) + W331*par(z3) - W341*par(z4) + W351*par(z5) + W361*par(z6) +
W371*par(z7) + W381*par(z8) - b31'

*Define the subcircuit
.subckt CNT-MOSFET n1 n2 n3
igate n2 n3 0
gdrain n1 n3 cur = 'par(f)'
.ends

```

4. Conclusions

In this paper, the capability of artificial neural network approach for the modeling and simulation of carbon nanotube metal-oxide-semiconductor field-effect transistors is investigated. A numerical model of the current-voltage characteristics is used based on the 2-D numerical NEGF simulation by means of moscnt.1.0. With this numerical model, we obtained the required database in order to optimize the proposed ANN model. The com-

parison made between NEGF simulation and the proposed ANN model shows that there is an excellent agreement between the numerical and predicted values with least error. Also, it is shown that the ANN model is much faster than NEGF simulation. This means that the proposed model is an accurate and fast approximation of NEGF model. With these abilities, we, therefore, imported the neural based model CNT-MOSFET in HSPICE software. The results show that our model is an efficient tool for simulation of nanoscale circuits.

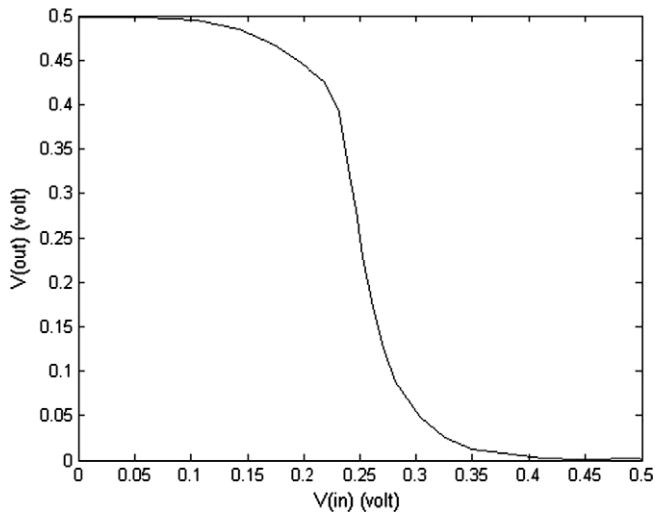


Fig. 8. The predicted transfer curve using the ANN model for the CNT-MOSFET inverter.

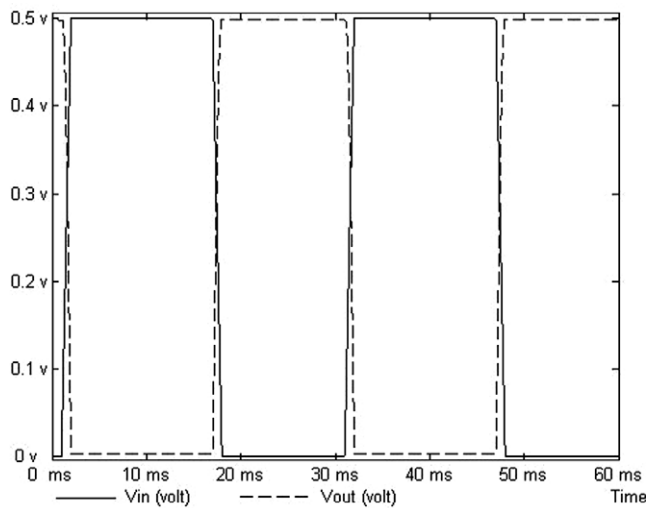


Fig. 9. The HSPICE input and output signals of our ANN inverter gate.

References

- [1] Numata T. Control of threshold-voltage and short-channel effects in ultrathin strained-SOI CMOS devices. *IEEE Trans Electron Dev* 2005;52(8):1780–6.
- [2] Lütze J, Venkatesan S. Techniques for reducing the reverse short channel effect in sub-0.5 μm CMOS. *IEEE Trans Electron Dev* 1995;16(9):373–5.
- [3] Jungemann C, Keith S, Bartels M, Meinerzhagen B. Efficient full-band monte carlo simulation of silicon devices. *IEICE Trans Electron* 1999;82(6):870–9.
- [4] Javanovic D, Venugopal R. Computational techniques for the nonequilibrium quantum field theory simulation of MOSFETs. In: IWCE 7th international workshop on computational electronics; 2000. p. 30–31.
- [5] Kreupl F. Carbon nanotubes in microelectronic applications. *Advanced micro & nanosystems* 2008;8:2–10.
- [6] Mceuen PL, Fuhrer MS, Park H. Single-walled carbon nanotube electronics. *IEEE Trans Nanotechnol* 2002;1(1):78–85.
- [7] Avouris P, Appenzeller J, Martel R, Wind SJ. Carbon nanotube electronics. *Proc IEEE* 2003;91(11):1772–84.
- [8] John DL. Simulation studies of carbon nanotube field-effect transistors. Ph.D. Thesis, University of british columbia; 2006.
- [9] Dresselhaus MS, Dresselhaus G, Avouris P. Carbon nanotubes: synthesis, structure properties and applications. Berlin: Ph. Avouris, Springer-Verlag; 2001.
- [10] Fiori G, Iannaccone G, Klimeck G. Performance of carbon nanotube field effect transistors with doped source and drain extensions and arbitrary geometry. *IEEE Trans Electron Dev*, Washington 2005:522–5.
- [11] Guo J, Koswatta S, Neophytou N, Lundstrom M. Carbon nanotube field-effect transistors. *Int J High Speed Electron Syst* 2006;16(4):897–912.
- [12] Javey A, Tu R, Farmer DB, Guo J, Gordon RG, Dai H. High performance n -type carbon nanotube field-effect transistors with chemically doped contacts. *Nano Lett* 2005;5(2):345–8.
- [13] Guo J, Javey A, Dai H, Lundstrom M. Performance analysis and design optimization of near ballistic carbon nanotube field-effect transistors. *IEEE Trans Electron Dev* 2004:703–6.
- [14] Ohnaka H, Kojima Y, Kishimoto S, Ohno Y, Mizutani T. Fabrication of carbon nanotube field effect transistors using plasma-enhanced chemical vapor deposition grown nanotubes. *Jpn J Appl Phys* 2006;45(6):5485–9.
- [15] Li J, Zhang Q, Yan Y, Li S, Chen L. Fabrication of carbon nanotube field-effect transistors by fluidic alignment technique. *IEEE Trans Nanotechnol* 2007;6(4):481–4.
- [16] Koswatta SO, Lundstrom MS, Anantram MP, Nikonov DE. Simulation of phonon-assisted band-to-band tunneling in carbon nanotube field-effect transistors. *Appl Phys Lett* 2005;87(25):253107–10.
- [17] Datta S. Nanoscale device modeling: the green's function method. *Superlattices Microstruct* 2000;28(4):253–77.
- [18] Datta S. Quantum transport from atom to transistor. 1st ed. Cambridge: Cambridge University Press; 2005.
- [19] Guo J, Lundstrom MS. Device simulation of SWNT-FETs. In: Javey A, Kong J, editors. Carbon nanotube electronics. Springer; 2007.
- [20] Hassaninia I, Sheikhi MH, Kordrostami Z. Simulation of carbon nanotube FETs with linear doping profile near the source and drain contacts. *Solid-state electron* 2008;52(6):980–5.
- [21] Kazmierski TJ, Zhou D, Al-Hashimi BM. Efficient circuit-level modelling of ballistic CNT using piecewise non-linear approximation of mobile charge density. In: IEEE conference on design, automation and test in Europe; 2008. p. 146–51.
- [22] Dwyer C, Cheung M, Sorin D. Semi-empirical SPICE models for carbon nanotube FET logic. In: 4th IEEE conference on nanotechnology, Germany, vol. 3. No. 3; 2004. p. 386–8.
- [23] Paul BC, Fujita S, Okajima M, Lee T. Modeling and analysis of circuit performance of ballistic CNFET. In: 43rd ACM/IEEE conference on design automation, vol. 3. No. 3; 2006. p. 717–22.
- [24] The nanoHUB. <<http://www.nanohub.org/resources/1818/>>.
- [25] Guo J, Datta S, Lundstrom MS, Anantram MP. Towards multiscale modeling of carbon nanotube transistors. *Int J Multiscale Comput Eng* 2004:257–76.
- [26] Koswatta SO, Nikonov DE, Lundstrom MS. Computational study of carbon nanotube p–i–n tunnel FETs. In: IEEE IEDM Technical Digest; 2005. p. 518–21.
- [27] Taylor JG. Neural networks and their applications. West sussex (UK): John Wiley & Sons Ltd.; 1996.
- [28] Gallant AR, White H. On learning the derivatives of an unknown mapping with multilayer feed forward networks, vol. 5. No. 1. Elsevier Science; 1992. p. 129–38.
- [29] Hammouda HB, Mhiri M, Gafsi Z, Besbes K. Neural-based models of semiconductor devices for HSPICE Simulation. *Am J Appl Sci* 2008;5(4):385–91.