A Compact Model for Nanowire Tunneling-FETs

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***Abstract*— The nanowire gate-all-around structure with the ultimate channel electrostatic integrity exhibits the best immunity to short channel effects and improved scaling capability compared with other multigate structures. In this article, both the tunneling current and capacitance models are developed simultaneously for nanowire tunneling field-effect transistors (FETs). Based on the same surface potential model, the developed current model and capacitance model share the common parameters and therefore can be easily integrated as a complete model for circuit-level simulations. Moreover, there is no iterative process involved during the model derivation indicating the models would be efficient for circuit simulations. The proposed models are also implemented into a circuit simulator with SPICE net-list to simulate the inverter, NAND, and NOR gates. Correct circuit behaviors obtained validate the model compatibility with the SPICE platform and usefulness for the further investigation of nanowire-based tunnel FET (TFET) circuits.**

***Index Terms*— BTBT, gate-all-around (GAA), model, nanowire, SPICE, tunnel field-effect transistor (TFET).**

I. Introduction

BASED on the quantum tunneling mechanism, tunnel field-effect transistors (TFETs) exhibit the potential to break the limitation of subthreshold swing (SS) of 60 mV/dec at room temperature and therefore offer much more steep switching characteristics and allow further reduced supply voltage [1]–[3]. This makes TFETs suitable for ultralow-power applications and widely considered as a promising alternative to MOSFETs [4].

Despite better SS characteristics, TFETs cannot avoid the nonideal effects, such as the drain-induced barrier lowering (DIBL) and short channel effects (SCEs), which are detrimental to the device performance [5]–[6]. To address these issues, innovation in the device structure is widely pursued. The nanowire gate-all-around (GAA) structures owning the nearly perfect channel electrostatic integrity of the gate field can exhibit the best immunity to SCEs and DIBL, and show better scaling capability [7]. Moreover, owing to the strong control efficiency of the gate over the channel potential, the nanowire TFET also gives improved SS and ON-state current compared with the planar devices [6].

Although a lot of simulation studies have been done for different aspects of nanowire TFETs, a SPICE-friendly predictive model including the drain current and terminal capacitance models is still in the preliminary stages of development. The models are extremely important for the practical applications of the nanowire TFETs. Some tunneling current models have already been published so far for nanowire TFETs [8]–[21]. However, [8]–[11] neglect the source depletion region resulting in inaccurate evaluation of the surface potential, tunneling distance, and tunneling current. Kumar *et al.* [12]–[14] ignore the channel mobile charges and can be only used for depletion region under small gate voltage. Both the source depletion region and channel mobile charges are considered in [15]–[19], but the adopted numerical techniques make the models relatively computational cumbersome. A predictive model is developed based on Wentzel–Kramer–Brillouin (WKB) approximation and validated with atomistic simulation, but the final formula for the tunneling current is not analytical [20]. In [21], a current model taking both the source depletion and mobile charges into account is proposed by assuming two different regimes: accumulation regime at large gate voltage and depletion regime at low gate voltage, which is relatively complex.

Moreover, besides the drain tunneling current, the model of the terminal capacitance used for transient simulation is also critical for the practical applications of nanowire TFETs. But it is still an issue. From the point of practical applications, the desirable capacitance model and current model should be compatible with each other. In this way, the models can be easily integrated as a complete model and incorporated into

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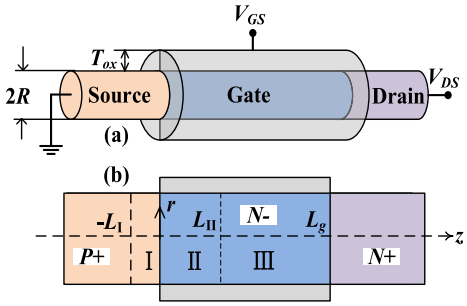

Fig. 1. (a) Structure of the nanowire TFETs and (b) corresponding schematic cross-section view.

the SPICE platform. Since there was not a model applicable for nanowire TFETs, the study on nanowire TFETs was mainly using relatively complex numerical methods. However, since circuit investigation usually includes many devices, it is time consuming and computationally inefficient. This may be one of the reasons that the study on the nanowire TFET circuits is seldom reported. Compared with the numerical methods, an analytical model could accelerate the circuit design process and facilitate the practical applications of nanowire TFETs [22].

In our work, we proposed a physics-based analytical model for the nanowire TFETs and both the source depletion and mobile charges are considered. In the model, the drain current and terminal capacitance models are based on the same surface potential derivation. Therefore, most parameters are common for the current and capacitance models, which makes them easily integrable as a complete model. Moreover, there is no iterative process and different regimes assumption adopted during the model derivation indicating the models are simple and efficient. The models can be also implemented into a circuit simulator with SPICE net-list and show better compatibility with the SPICE platform, thus the models are useful to the further investigation of nanowire-based TFET circuits.

II. Model Derivation

Fig. 1(a) gives an n-type GAA-TFET device and the schematic cross-section is also given in Fig. 1(b). The device parameters and symbols used in the model derivation are summarized in Table I. Numerical simulations in this article are carried out by using the commercial 2-D Synopsys Sentaurus TCAD tools. To consider the arbitrary tunneling barrier with a nonuniform electrical field, the dynamic nonlocal BTBT model is adopted. It should be noted that the quantum confinement effect is ignored considering the relatively large diameter of nanowire of 15 nm in our work and therefore Kane's model for bulk is adopted to obtain the BTBT probability. The parameters $A = 4 \times 10^{14}$ cm$^{-3}\cdot$s^{-1} and $B = 1.9 \times 10^{7}$ V$\cdot$cm^{-1} for Kane's model are used [23]–[25]. However, with the scaling of the nanowire diameter, the device would transit from a 3-D electron system to a 1-D electron system resulting in different C–V and I–V characteristics due to the increased bandgap and effective mass of silicon [26]. In this case, the quantum confinement must be considered [6], [14] and the modified Kane's model for lower-dimensional systems should be used Ma and Jena [27] and Pan and Chui [28]. Other models like the Shockley–Read–Hall (SRH) recombination, doping-dependent mobility, and the high-field saturation effects are also considered. To clearly present the overall train of thought of the model derivation and for the article readability, some tedious derivations are moved to the Appendix.

TABLE I
Parameters in the Numerical Simulations and Model Development

Symbol	Quantity	Values	Unit
L_g	Channel length	50	nm
R	Nanowire radius	7.5	nm
W_G	Gate metal work-function	4.2	eV
T_{ox}	Gate oxide thickness	2	nm
ε_{ox}	Gate oxide dielectric constant	22	
ε_{Si}	Channel dielectric constant	11.7	
N_S	Source doping density	1×10^{20}	cm^{-3}
N_C	Channel doping density	1×10^{15}	cm^{-3}
N_D	Drain doping density	5×10^{19}	cm^{-3}
E_g	Energy band-gap of channel material	1.12	eV
χ	Electronic affinity of channel material	4.09	eV
N_C	Density of state of the conduction band	3.2×10^{19}	cm^{-3}
N_V	Density of state of the valance band	1.8×10^{19}	cm^{-3}

This article focuses on a clear presentation of model development for GAA-TFETs. Even though some second-order effects, such as gate leakage current, ambipolar conduction, are critical for the device analysis, they are neglected for simplicity. Besides, from the practical point of view, the exclusion is reasonable in the preliminary stage of the core model development causing these effects not significantly affecting our discussion.

A. Model Derivation for the Surface Potential

The device given in Fig. 1 can be considered as three parts. The left part is source depletion region I, the middle part is channel depletion region II, and the right part is the drift-diffusion region III. The region I can be equivalent to a field-effect transistor (FET) with gate oxide thickness of $\pi T_{\rm ox}/2$ [29]. Considering that the ambipolar conduction near the channel/drain junction is detrimental to the digital applications and can be greatly suppressed, the drain depletion region is ignored [30], [31].

The 2-D Poisson equations are adopted to determine the potential distributions of the regions I and II

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial \psi_j(r,z)}{\partial r}\right)+\frac{\partial^2\psi_j(r,z)}{\partial z^2}=-\frac{qN_j}{\varepsilon_{\rm Si}} \tag{1}$$

in which the j can be I and II for different regions. $\psi_j(r,z)$ and $\varepsilon_{\rm Si}$ are the potential distribution in the channel body and the silicon dielectric constant, respectively. N_j is the doping concentration for each region. q is the electron charge. The potential in each region perpendicular to the channel surface can be written as (2) by using the parabolic approximation [32]

$$\psi_j(r,z)=\varphi_{m,j}(z)+p_{1,j}(z)r+p_{2,j}(z)r^2 \tag{2}$$

in which $\varphi_{m,j}(z)$ is the potential along the channel center at $r = 0$. The $\varphi_{m,j}(z)$, $p_{1,j}(z)$, and $p_{2,j}(z)$ are unknown parameters, which can be obtained by the boundary conditions.

The derivation is given by (A1) and (A2) in the Appendix. Then, substituting (2) into (1), (1) is reduced as follows:

$$\frac{d^2\varphi_{\mathrm{S},j}(z)}{dz^2} - \frac{\varphi_{\mathrm{S},j}(z) - \left(V_{\mathrm{GS}} - V_{\mathrm{FB},j}\right)}{\lambda_j^2} = -\frac{qN_j}{\varepsilon_{\mathrm{Si}}} \tag{3}$$

where $\varphi_{\mathrm{S},j}(z)$ is the surface potential at $r = R$. $\lambda_{\mathrm{I}} = (R\varepsilon_{\mathrm{Si}}\pi t_{\mathrm{ox}}/4\varepsilon_{\mathrm{ox}})^{1/2}$ and $\lambda_{\mathrm{II}} = (R\varepsilon_{\mathrm{Si}}t_{\mathrm{ox}}/2\varepsilon_{\mathrm{ox}})^{1/2}$, in which $t_{\mathrm{ox}} = R\ln(1 + T_{\mathrm{ox}}/R)$, are the scaling lengths for each region. $V_{\mathrm{FB},j}$ is the flat band voltage and V_{GS} is the gate–source voltage.

The following gives the general solution of (3):

$$\varphi_{\mathrm{S},j}(z) = A_j \exp\left(-\frac{z}{\lambda_j}\right) + B_j \exp\left(+\frac{z}{\lambda_j}\right) + \left(V_{\mathrm{GS}} - V_{\mathrm{FB},j} - \frac{qN_j}{\varepsilon_{\mathrm{Si}}}\lambda_j^2\right). \tag{4}$$

For region I, assuming its width is L_{I}, the potential $\varphi_{\mathrm{S,I}}(z)$ can be expressed as (5) and the derivation is given by (A3) and (A4) in the Appendix

$$\begin{cases} \varphi_{\mathrm{S,I}}(z) = \dfrac{qN_{\mathrm{eff}}}{2\varepsilon_{\mathrm{Si}}}(z + L_{\mathrm{I}})^2 + V_{\mathrm{BS}} \\ N_{\mathrm{eff}} = N_{\mathrm{I}} - \dfrac{\varepsilon_{\mathrm{Si}}}{q\lambda_{\mathrm{I}}^2}\left(V_{\mathrm{GS}} - V_{\mathrm{FB,I}} - V_{\mathrm{BS}}\right) \end{cases} \tag{5}$$

in which $V_{\mathrm{BS}} = V_{\mathrm{S}} - V_{\mathrm{t}} \times \log(N_{\mathrm{I}}/n_{i,\mathrm{I}})$ is potential in the neutral source region. The V_{S} and V_{t} are the source and thermal voltage, respectively. $n_{i,\mathrm{I}}$ is the intrinsic carrier density of the source.

In region II, the $\varphi_{\mathrm{S,II}}(z)$ is solved as (6) by solving A_{II} and B_{II} which are expressed by (A5) in the Appendix

$$\varphi_{\mathrm{S,II}}(z) = \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{\mathrm{q}N_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right) + \left(\varphi_{\mathrm{ch},} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{\mathrm{q}N_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)\right)\cosh\left(\frac{z - L_{\mathrm{II}}}{\lambda_{\mathrm{II}}}\right) \tag{6}$$

in which the φ_{ch} is the surface potential in region III. L_{II} is the width of region II.

For depletion region III, the φ_{ch} cannot be obtained analytically owing to the lots of mobile carriers. In our work, the method in [33] is adopted to determine an analytical expression for φ_{ch} and the following gives the result:

$$\varphi_{\mathrm{ch}} = F + V_{\mathrm{t}}\ln\left\{\frac{1}{V_{\mathrm{t}}}\left[\begin{array}{l} V_{\mathrm{t}} + \frac{\sqrt{F}}{\sqrt{F}+\gamma}\left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - F\right) \\ +\frac{1}{2}\left[\frac{\sqrt{F}}{\left(\sqrt{F}+\gamma\right)^2} - \frac{\gamma(F-2)}{2\left(\sqrt{F}+\gamma\right)^3}\right] \\ \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - F\right)^2 \end{array}\right]\right\} \tag{7}$$

$$F = \frac{1}{2}\left[V_{\mathrm{DS}} + \phi + \varphi_{\mathrm{ch,dep}} - \sqrt{\left(\varphi_{\mathrm{ch,dep}} - V_{\mathrm{DS}} - \phi\right)^2 + \delta^2}\right] \tag{8}$$

$$\varphi_{\mathrm{ch,dep}} = \left[\sqrt{V_{\mathrm{GS}} - V_{\mathrm{FB,II}} + \frac{\gamma^2}{4}} - \frac{\gamma}{2}\right]^2 \tag{9}$$

where $\gamma = (2\varepsilon_{\mathrm{Si}}qN_{\mathrm{II}})^{1/2}/(\varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}})$ and $\delta = 0.04$ is a small smoothing factor. $\phi = V_{\mathrm{t}}\ln(N_{\mathrm{inv}}/n_{i,\mathrm{II}})$ is the potential required to induce enough inversion charges to screen the modulation of gate bias and an empirical value of $N_{\mathrm{inv}} = 2.5 \times 10^{19}$ cm^{-3}

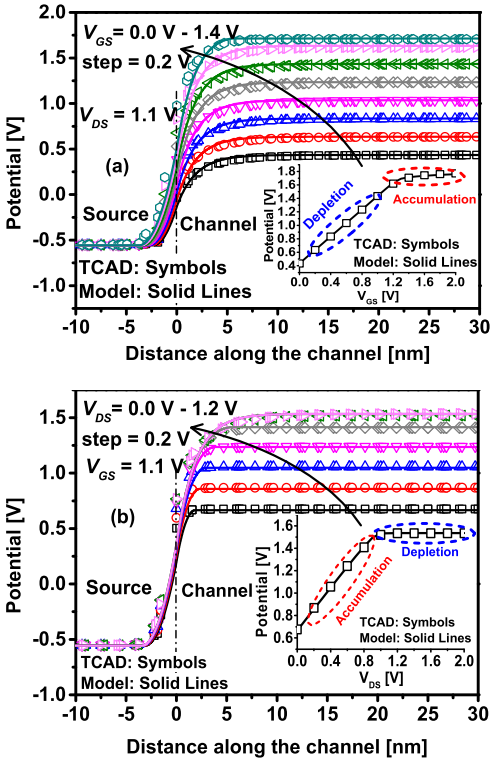

Fig. 2. Variation of surface potential along the channel with (a) V_{GS} and (b) V_{DS}. The inserts give the potential at the channel midpoint ($z = 25$ nm).

extracted from TCAD simulations is adopted. $n_{i,\mathrm{II}}$ is the intrinsic carrier density of the channel body.

Until now, the last unknown parameters are L_{I} and L_{II}, which would be determined by the aid of the continuity conditions at the source/channel interface. The derivation is listed by (A6)–(A8) in the Appendix. The model calculated surface potential along the channel with the TCAD results at $V_{\mathrm{DS}} = 1.1$ V is given in Fig. 2(a) and excellent agreements are obtained. Owing to the nonuniform modulation of V_{GS} on the potential, increased V_{GS} leads to a steeper potential profile near the source/channel interface resulting in a larger electric field, higher tunneling probability, and drain current. The insert presents the variation of the surface potential at the channel midpoint $z = 25$ nm with V_{GS}. The potential increases linearly with V_{GS} in the depletion region and then tends to slow down in the accumulation region after about $V_{\mathrm{GS}} = 1.2$ V. This is because a large amount of induced channel electrons in the accumulation region shield the gate electric field.

However, the large amount of induced electrons in the channel can also reduce the channel resistance and connect the source tunneling junction with the drain. In this case, the channel potential is mainly under the control of V_{DS}, as can be seen in Fig. 2(b) which gives the surface potential for different V_{DS} at $V_{\mathrm{GS}} = 1.1$ V. The insert also presents the variation of the potential at the channel midpoint $z = 25$ nm with V_{DS}. We can see that the potential linearly increases with V_{DS} in the accumulation region. However, with increased V_{DS}, the channel region starts to become depleted again owing to that the channel electrons are gradually drawn back to the drain. This results in gradually increased channel resistance blocking

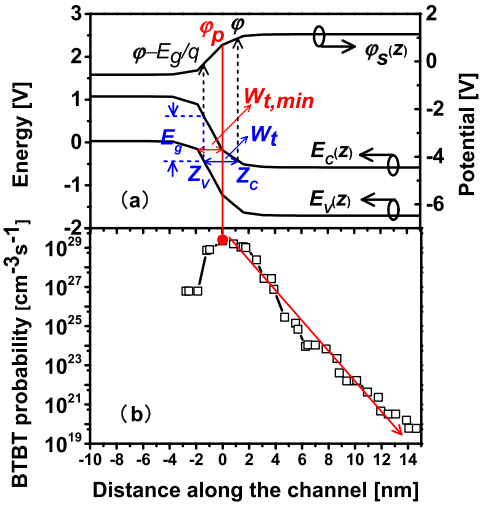

Fig. 3. Schematic of (a) energy band and surface potential distribution and (b) electron tunneling rate along the channel direction near the source junction at $V_{GS} = 1.1$ V and $V_{DS} = 0.5$ V.

the drain field far away from the tunneling junction. In this case, V_{DS} modulation on the channel potential is gradually reduced and the channel potential is almost unchanged with V_{DS}. Thus V_{GS} controls the potential once again. That is why the potential distribution for $V_{DS} = 1.0$ V and $V_{DS} = 1.2$ V in Fig. 2(b) are almost the same and this would lead to an unchanged drain current in the output characteristics.

B. Model for Drain Current

With the proposed potential model, the tunneling current can be obtained. Fig. 3(a) gives the schematic of the energy band and potential distribution near the tunneling junction. For a certain tunneling path from z_v to z_c in Fig. 3(a), the tunneling distance W_t equals the length of tunneling path z_c–z_v and the difference of the conduction energy band between the two points is right at the energy bandgap E_g indicating that the corresponding potential difference is E_g/q. Therefore, assuming the potential at z_c is φ, the potential at z_v is φ–E_g/q. This can be used to get values of z_c and z_v based on the already developed potential model and thus the W_t can be also obtained. Obviously, the W_t varies with the potential φ in the whole range of the interband tunneling window. Assuming that the shortest tunneling distance $W_{t,min}$ is obtained at the potential φ_p, then φ_p should satisfy the difference equation $dW_t/d\varphi = 0$. Thus $W_{t,min}$ can be determined by the following equation:

$$\begin{cases} \varphi_{s,\mathrm{II}}(z_c) = \varphi \\ \varphi_{s,\mathrm{II}}(z_v) = \varphi - \dfrac{E_g}{q} \\ W_t = z_c - z_v, \quad \dfrac{dW_t}{d\varphi}\Big|_{\varphi=\varphi_p} = 0. \end{cases} \tag{10}$$

By solving (10), $W_{t,min}$ can be figured out as following:

$$W_{t,min} = L_I + L_{II} + \lambda_{II} \cosh^{-1} H - \sqrt{\frac{2\varepsilon_{Si}}{qN_{eff}}\left(\varphi_p - \frac{E_g}{q} - V_{BS}\right)} \tag{11}$$

where H and φ_p are given in (A7) and (A9) in the Appendix, respectively.

Fig. 3(b) presents the electron BTBT probability aligned to the band diagram and surface potential. It can be seen that the largest tunneling probability G_{max} happens at the shortest tunneling distance $W_{t,min}$ and then exponentially decreases as W_t increases. According to Kane's model, the maximum electric field is approximately equal to $|E| = E_g/(qW_{t,min})$ and corresponds to the largest tunneling probability G_{max}. Therefore the G_{max} can be calculated directly by the following equation [16]:

$$G_{max} = A\frac{E_g^{p-\frac{1}{2}}}{(qW_{t,min})^p}\exp\left(-\frac{W_{t,min}}{\lambda_t}\right) \tag{12}$$

where $p = 2.5$ for the indirect tunneling process. $\lambda_t = (qBE_g^{1/2})^{-1}$ is the tunneling length decay. The $G(z)$ along the channel can be written as (13) considering the linearly increased tunneling distance with z

$$G(z) \approx G_{max}\exp\left(-\frac{|z - z_c|}{\lambda_t}\right). \tag{13}$$

Assuming that the tunneling current is uniform along the direction normal to the channel and integrating the tunneling probability over the whole tunnel volume, the tunneling current can be approximately determined

$$I_{DS} = q \cdot \iint G(z)d\Omega = q \cdot \pi \cdot R^2 \cdot \lambda_t \cdot G_{max}. \tag{14}$$

It should be pointed out that for the case $V_{DS} = 0$ V, the electric field and the largest BTBT probability given in (12) do not equal zero. Thus the tunneling current predicted by (14) also is nonzero at $V_{DS} = 0$ V, which is obviously not correct. This problem can be solved by multiplying a correction factor $f_{cor} = 1 - 2/(1 + \exp(qV_{DS}/fn \times V_t))$ to (14) [15]. The factor f_{cor} equals zero for $V_{DS} = 0$ V guaranteeing a zero current for zero V_{DS}. fn is an empirical parameter and set as $fn = 4.45V_{GS} + 2.3$ to make sure the model data math well with the numerical simulations for different V_{GS}. Finally, a closed-form analytical current is expressed as follows:

$$I_{DS} = q \cdot \pi \cdot R^2 \cdot \lambda_t \cdot G_{max} \cdot f_{cor}. \tag{15}$$

Fig. 4(a) gives the model calculated data and numerical simulations of the transfer curves. We should point out that the model behavior starts from about $V_{GS} = 0.15$ V at which the tunneling current starts to be higher than the reverse leakage current. The leakage current is mainly dominated by the carrier generation which can be described well by the mature SRH model and is not taken into account in our model. After $V_{GS} = 0.15$ V, the tunneling current increases with V_{GS}, but the increasing trend is gradually slowing down at large V_{GS}, which is highly consistent with the trend of the increased potential with V_{GS} as discussed in Fig. 2(a). It seems that the model results and the numerical simulations agree well with logarithmic coordinates. Relatively large deviation is presented for large $V_{GS} > 0.9$ V in linear coordinates. This deviation is due to the assumption in (14) that the $G(z)$ is uniformly distributed normally to the channel direction. Fig. 5 presents the 2-D cross-section distribution of the electron

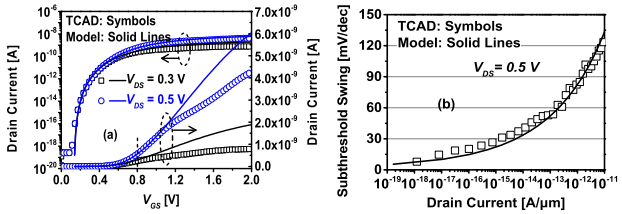

Fig. 4. (a) Transfer characteristics of the nanowire TFETs and (b) variation of SS with the drain current at $V_{DS} = 0.5$ V.

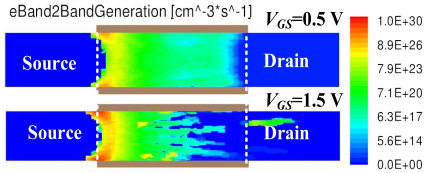

Fig. 5. 2-D cross-section distribution of the electron tunneling probability for different V_{GS} at $V_{DS} = 0.5$ V.

BTBT probability for $V_{GS} = 0.5$ and 1.5 V. It can be seen that even the electron BTBT probability tends to concentrate near the channel/oxide interface, the $G(z)$ can be still approximately treated as uniform normal to the channel direction for small V_{GS}. But for large V_{GS}, the BTBT probability is mainly distributed near the channel/oxide interface and the uniform assumption normal to the channel direction becomes unsuitable, which leads to overestimated tunneling current compared with the numerical data.

Despite the obvious deviation for larger V_{GS} than about 0.9 V in linear coordinates, the proposed current model captures the main outline of transfer characteristics and can predict results in excellent agreement with the TCAD simulations for V_{GS} smaller than 0.8 V. Considering that the TFETs are originally designed for applications with supply voltage smaller than 0.5 V, the developed model is still useful for the design of nanowire-based TFET circuits working on the low supply voltage. The SS versus I_{DS} characteristics at $V_{DS} = 0.5$ V are also given in Fig. 4(b). Good agreements between the model results and the TCAD simulations are achieved.

The output characteristics are given in Fig. 6 and good agreements are also obtained for lower V_{GS} than 0.8 V. Although the drain current gradually increases with V_{DS}, the increased V_{DS} also leads to reduced channel carrier density and once the channel becomes depleted, the V_{DS} cannot control the channel potential, thus the drain current becomes unchanged. This is also consistent with the potential variations as discussed in Fig. 2(b).

C. Model for Terminal Capacitance

Before the derivation of terminal capacitance, the terminal gate charge Q_G, source charge Q_S, and drain charge Q_D should be first obtained. The Q_S is mainly composed of the depletion charges in region I and therefore can be expressed by the following equation:

$$Q_S = -qN_{\text{eff}}\pi R_g^2 L_I. \tag{16}$$

The Q_D can be divided into two parts, namely the mobile inversion charges in the channel and the inner fringing charge

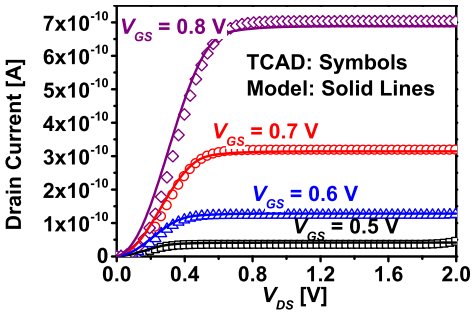

Fig. 6. Output characteristics of the nanowire TFETs.

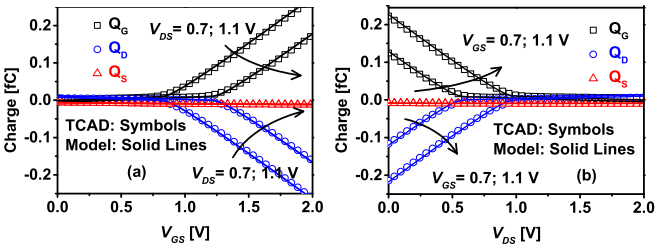

Fig. 7. Variation of the terminal charges versus (a) V_{GS} and (b) V_{DS}.

near the drain side

$$Q_D = -2\pi R(L_g - L_{II})\left(\frac{\varepsilon_{ox}}{t_{ox}}\right)(V_{GS} - V_{FB,III} - \varphi_{ch,III}) + \pi R^2 \varepsilon_{Si} E_{max} \tag{17}$$

$$E_{max} = \frac{V_{BD} - \varphi_{ch}}{\lambda_{II}} \tag{18}$$

where $V_{BD} = V_{DS} + V_t \times \log(N_D/n_i)$ is the neutral drain potential. With the aid of the charge conservation, the Q_G is determined by the following equation:

$$Q_G + Q_S + Q_D = 0. \tag{19}$$

Fig. 7 presents good agreements obtained between the model and numerical results. The Q_G increases with V_{GS} while decreases with V_{DS}. The different trends are due to the fact that the effect of the gate electric field tends to induce the electrons in the channel body from the drain while the drain electric field tends to draw the electrons back into the drain. Fig. 8(a) also gives that the Q_S increases with V_{GS} owing to that the L_I increases with V_{GS}. But the trend is different with V_{DS} shown in Fig. 8(b). The Q_S first increases with V_{DS} and then keeps unchanged, which is like the variation of drain current with V_{DS}. Actually, the mechanism is the same. For smaller V_{DS}, lots of electrons are induced in the channel and the channel resistance is small, thus the drain bias controls the channel potential and the source depletion width L_I and Q_S increase with V_{DS}. However, with increased V_{DS}, the channel becomes depleted and the large resistance blocks the drain field far away from the source/channel interface. Therefore the L_I and Q_S become unchanged with V_{DS}.

It should be noted that although the main outline of the curves of the Q_S can be calculated by the model as shown in the inserts, a relatively large deviation is also clearly observed. This is mainly owing to the assumption that the source depletion region I is taken as a regular cylinder. In fact, the potential along the source/channel interface is not constant

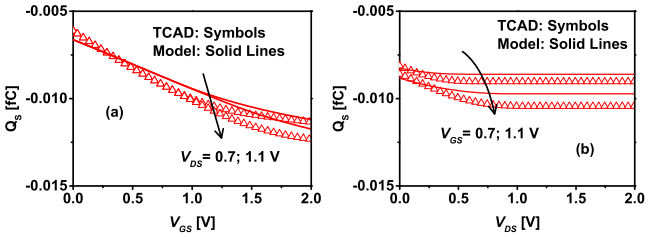

Fig. 8. Variation of the source charges versus (a) V_{GS} and (b) V_{DS}.

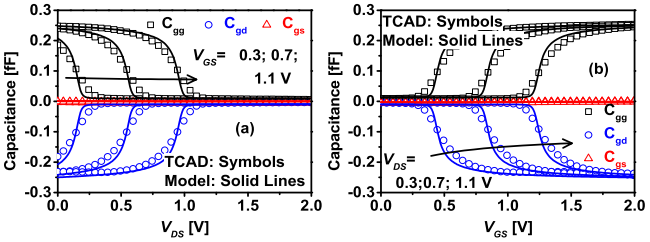

Fig. 9. Variation of the terminal capacitances with (a) V_{GS} and (b) V_{DS}.

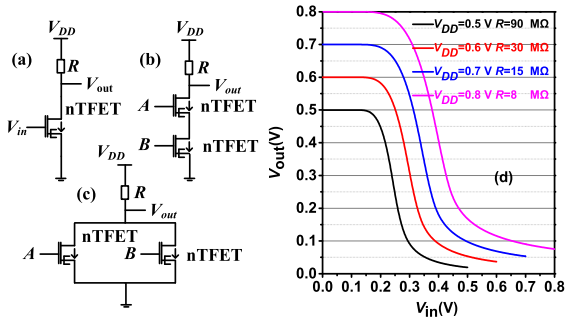

Fig. 10. Schematic of (a) inverter, (b) NAND gate, (c) NOR gate based on the GAA-TFETs, and (d) VTCs of the inverter based on Si GAA-TFET.

and thus the source depletion width L_I is actually varied with r, which is ignored for simplicity in the model derivation. Other reasons leading to the deviation include the error of the Taylor expansion adopted to derivate the surface potential in the region I.

The terminal capacitances can be determined by the difference method. Fig. 9 gives the model results compared with the numerical simulations. It can be seen obviously the main inflection and variation of the capacitance with the biases can be predicted by the models and good agreements are achieved.

III. Circuit Simulation

The TFET model is implemented into a circuit simulator with SPICE net-list and several GAA-TFET based circuits are simulated to verify the model compatibility with the SPICE platform. The TFET sample in [34] is used and Fig. 10 depicts the schematics of an inerter, NAND, and NOR gate consisting of a resistor and one or two n-type GAA-TFETs. The n-type GAA-TFETs are assumed to be 500 devices in parallel [35].

The voltage transfer characteristics (VTCs) of the inverter are given in Fig. 10(d) with different supply voltages (V_{DD}). Owing to the small ON-state current I_{ON} (large ON-state resistance R_{ON}) of the Si TFET, a relatively large pull-up resistance R is required to achieve switching voltages close to $V_{DD}/2$, corresponding to the maximum noise margins. With larger V_{DD}, the R_{ON} of the TFET is reduced resulting in smaller required R. The transient responses of the TFET inverters

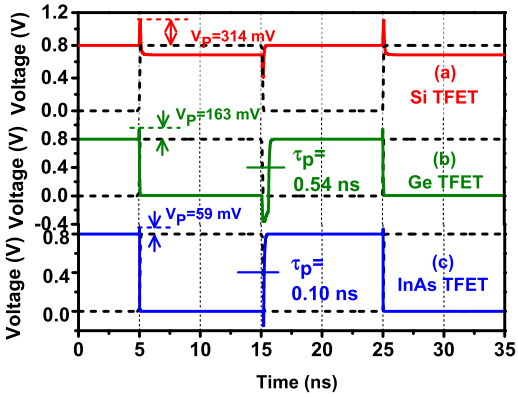

Fig. 11. Transient response of inverters based on (a) Si GAA-TFET, (b) Ge GAA-TFET, and (c) InAs GAA-TFET, respectively. R is fixed as 10 kΩ.

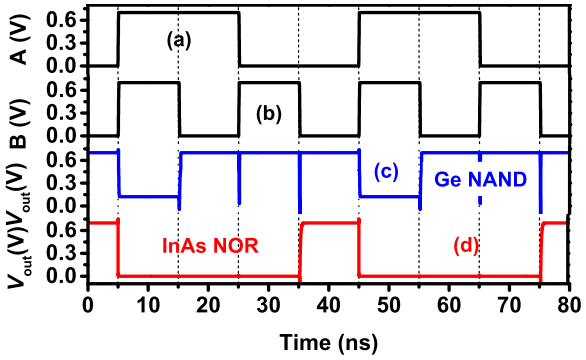

Fig. 12. Input voltages (a) A and (b) B are shown at $V_{DD} = 0.7$ V and the corresponding transient responses are also present for (c) NAND based on Ge GAA-TFET and (d) NOR based on InAs GAA-TFET.

based on different materials and fixed $R = 10$ kΩ are given in Fig. 11. The parameters A and B are 9.1×10^{16} cm^{-3}·s^{-1} and 4.9×10^{6} V·cm^{-1} for Ge and 3×10^{19} cm^{-3}·s^{-1} and 2.6×106 V·cm^{-1} for InAs [36]. Both the rise and fall times of the input voltage are set as 0.1 ns. It can be seen that the I_{ON} of the Si TFETs is too small to pull down the output, as reported in [37]. This can be solved with Ge and InAs TFET with larger I_{ON} and smaller R_{ON}. Owing to the largest I_{ON} and smallest Miller capacitance of InAs TFET [38], the InAs inverter also shows the smallest overshoot of 59 mV and rise delay of 0.1 ns (low-to-high transition of the output voltage).

The transient responses of the Ge TFET NAND and InAs TFET NOR with the input signals A/B at $V_{DD} = 0.7$ V are shown in Fig. 12. Correct circuit behaviors can be also obviously modeled. The instant burrs occur for the NAND when both the two n-type TFETs are turned on.

IV. Conclusion

In this article, both the drain current model and terminal capacitance model for a GAA TFET are developed. The TCAD simulation is used to verify the proposed models and good agreements are achieved in all operations between the model and numerical results. Based on the same analytical surface potential model, the proposed current and capacitance models can be easily integrated as a complete model owing to that most parameters and formulas are common. Moreover, there is no iterative process involved during the

model derivation indicating the models would be efficient for circuit simulations. Moreover, the proposed models can be implemented into the SPICE platform, thus the developed models can be useful for the design and investigation of nanowire-based TFET circuits.

Appendix Equation Section (Next)

Owing to the symmetrical device structure, the electric field along the direction normal to the channel interface at the intrinsic channel center equals zero. With the aid of the electric displacement vector continuity at the interface of oxide/silicon, the following equation can be achieved:

$$\begin{cases} \left.\dfrac{\partial \psi_j(r,z)}{\partial r}\right|_{r=0} = 0 \\ \psi_j(r,z)\big|_{r=R} = \varphi_{\mathrm{S},j}(z) \\ \left.\dfrac{\partial \psi_j(r,z)}{\partial r}\right|_{r=R} = \dfrac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{Si}}}\left(\dfrac{V_{\mathrm{GS}} - V_{\mathrm{FB},j} - \varphi_{\mathrm{S},j}(z)}{t_{\mathrm{ox}}}\right). \end{cases} \tag{A1}$$

Therefore, the unknown $\varphi_{m,j}(z)$, $p_{1,j}(z)$, and $p_{2,j}(z)$ can be solved as follows:

$$\begin{cases} p_{1,j}(z) = 0 \\ p_{2,j}(z) = \dfrac{\varepsilon_{\mathrm{ox}}}{2R\varepsilon_{\mathrm{Si}}}\left(\dfrac{V_{\mathrm{GS}} - V_{\mathrm{FB},j} - \varphi_{\mathrm{S},j}(z)}{t_{\mathrm{ox}}}\right) \\ \varphi_{m,j}(z) = \varphi_{\mathrm{S},j}(z) - p_{2,j}(z)R^2. \end{cases} \tag{A2}$$

By the Taylor expansion of (4) at $z = -L_{\mathrm{I}}$, the potential distribution of region I is determined as follows:

$$\varphi_{\mathrm{S,I}}(z) = C\left(1 + \frac{1}{2\lambda_{\mathrm{I}}^2}(z + L_{\mathrm{I}})^2\right) + \left(V_{\mathrm{GS}} - V_{\mathrm{FB,I}} - \frac{qN_{\mathrm{I}}}{\varepsilon_{\mathrm{Si}}}\lambda_{\mathrm{I}}^2\right). \tag{A3}$$

The parameter C can be determined with $\varphi_{\mathrm{S,I}}(-L_{\mathrm{I}}) = V_{\mathrm{BS}}$

$$C = V_{\mathrm{BS}} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,I}} - \frac{qN_{\mathrm{I}}}{\varepsilon_{\mathrm{Si}}}\lambda_{\mathrm{I}}^2\right). \tag{A4}$$

Substituting C into (A3), the potential $\varphi_{\mathrm{S,I}}(z)$ is obtained.

The unknown parameters A_{II} and B_{II} in (4) can be determined by the aid of the electric displacement vector continuity and potential continuity at the interface of regions II and III

$$\begin{cases} A_{\mathrm{II}} = \dfrac{1}{2}\left(\varphi_{\mathrm{ch,III}} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \dfrac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)\right)\exp\left(+\dfrac{L_{\mathrm{II}}}{\lambda_{\mathrm{II}}}\right) \\ B_{\mathrm{II}} = \dfrac{1}{2}\left(\varphi_{\mathrm{ch,III}} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \dfrac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)\right)\exp\left(-\dfrac{L_{\mathrm{II}}}{\lambda_{\mathrm{II}}}\right). \end{cases} \tag{A5}$$

Considering the potential continuity at the source/channel interface and assuming $\varphi_{\mathrm{S}}(0)$ is the potential at $z = 0$, then L_{I} and L_{II} can be written as follows from (5) and (6)

$$\begin{cases} L_{\mathrm{I}} = \sqrt{\dfrac{2\varepsilon_{\mathrm{Si}}}{qN_{\mathrm{eff}}}}\sqrt{\varphi_{\mathrm{S}}(0) - V_{\mathrm{BS}}} \\ L_{\mathrm{II}} = \lambda_{\mathrm{II}}\cosh^{-1}\left(\dfrac{\varphi_{\mathrm{S}}(0) - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)}{\varphi_{\mathrm{ch}} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)}\right). \end{cases} \tag{A6}$$

Substituting L_{I} into (5) and L_{II} into (6), the following equation is obtained considering the electric displacement vector continuity at the source/channel interface:

$$\begin{cases} 0 = \dfrac{2qN_{\mathrm{eff}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}[\varphi_s(0) - V_{\mathrm{BS}}] \\ \quad -\dfrac{\varepsilon_{\mathrm{Si}}^2}{\lambda_{\mathrm{II}}^2}\left[\varphi_{\mathrm{ch}} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \dfrac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)\right]^2 \times R^2 \\ H = \dfrac{\varphi_s(0) - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)}{\varphi_{\mathrm{ch}} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)} \\ R = \sinh\left(\cosh^{-1} H\right). \end{cases} \tag{A7}$$

By the equation $\sinh(\cosh^{-1}(H)) = (H^2 - 1)^{1/2}$, $\varphi_S(0)$ is determined in the following equation:

$$\begin{cases} \varphi_s(0) = \dfrac{-b - \sqrt{b^2 - 4c}}{2} \\ b = 2\left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \dfrac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}} + \dfrac{qN_{\mathrm{eff}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right) \\ c = 2\varphi_{\mathrm{ch}}\left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \dfrac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right) - \varphi_{\mathrm{ch}}^2 \\ \quad + \dfrac{2qN_{\mathrm{eff}}\lambda_{\mathrm{II}}^2 V_{\mathrm{BS}}}{\varepsilon_{\mathrm{Si}}}. \end{cases} \tag{A8}$$

By solving (10), the potential φ_p corresponding to the shortest tunneling path can be obtained

$$\begin{aligned} \varphi_p &= \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right) + \frac{qN_{\mathrm{eff}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}} \\ &\quad - \left\{\left(\frac{qN_{\mathrm{eff}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)^2 + \left[\varphi_{\mathrm{ch}} - \left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right)\right]^2 \right. \\ &\quad \left. + \frac{2qN_{\mathrm{eff}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}} \right. \\ &\quad \left. \times \left[\left(V_{\mathrm{GS}} - V_{\mathrm{FB,II}} - \frac{qN_{\mathrm{II}}\lambda_{\mathrm{II}}^2}{\varepsilon_{\mathrm{Si}}}\right) - \frac{E_g}{q} - V_{\mathrm{BS}}\right]\right\}^{\frac{1}{2}}. \end{aligned} \tag{A9}$$

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