Implementing High-Speed Memory Interfaces in Intel® Agilex™ M-Series FPGAs

Intel® Agilex™ FPGA Design Seminars

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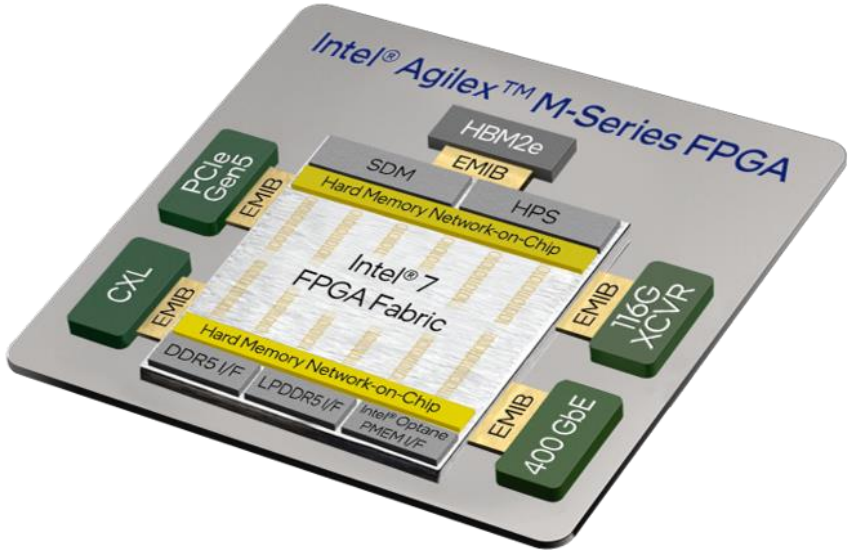
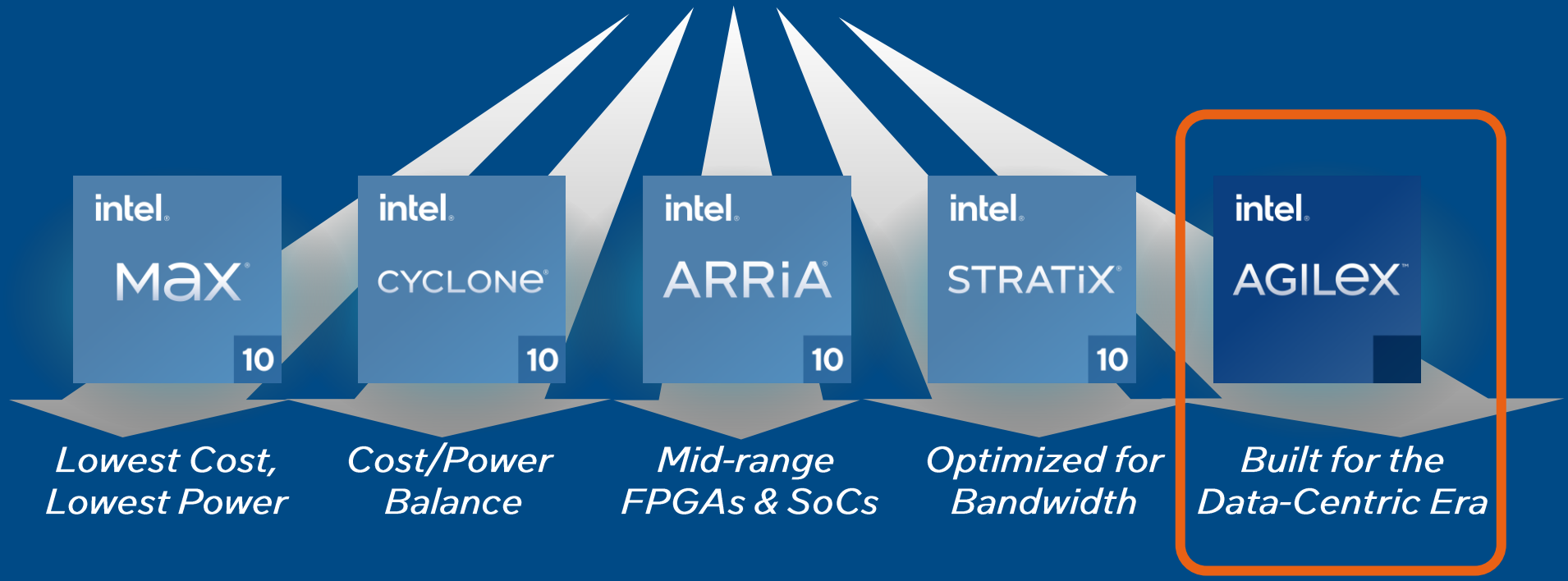
2022/09/06

Agenda

- Intel® Agilex™ FPGA Family Overview and performance advantages
- Intel® Agilex™ M-Series FPGA Memory Interface Solutions
- DDR5/LPDDR5 DRAM Memory Architecture
- System in Package HBM2e
- Intel® Agilex™ M-Series FPGA Memory Hardware Architecture
- Hard Memory Network-on-Chip (NoC)
- HBM2e+NoC use case
- Summary



Intel® FPGA Portfolio



Intel® FPGAs and SoC FPGAs for Every Application

Intel® Agilex™ FPGAs – for The Data-Centric World

PROCESS DATA

- 2nd Generation Intel® Hyperflex™ Architecture
- Average 50% Higher Performance*
- Up to 40% Lower Power*
- Up to 40 TFLOPS DSP Performance*

STORE DATA

- DDR4/5 and HBM2e
  High Bandwidth Memory
- Intel® OPTANE™
  Persistent Memory Support

MOVE DATA

- Hard Protocol IP
  100G/200G/400G Ethernet
  Compute Express Link[1]
  PCIe 4/5 x16
- 32/58/116G
  Transceiver Data Rates

[1] Consult rollout schedule

*See Intel.com/performanceindex for configuration details

Performance and Power Advantages

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Intel® Agilex™ FPGAs Performance Overview

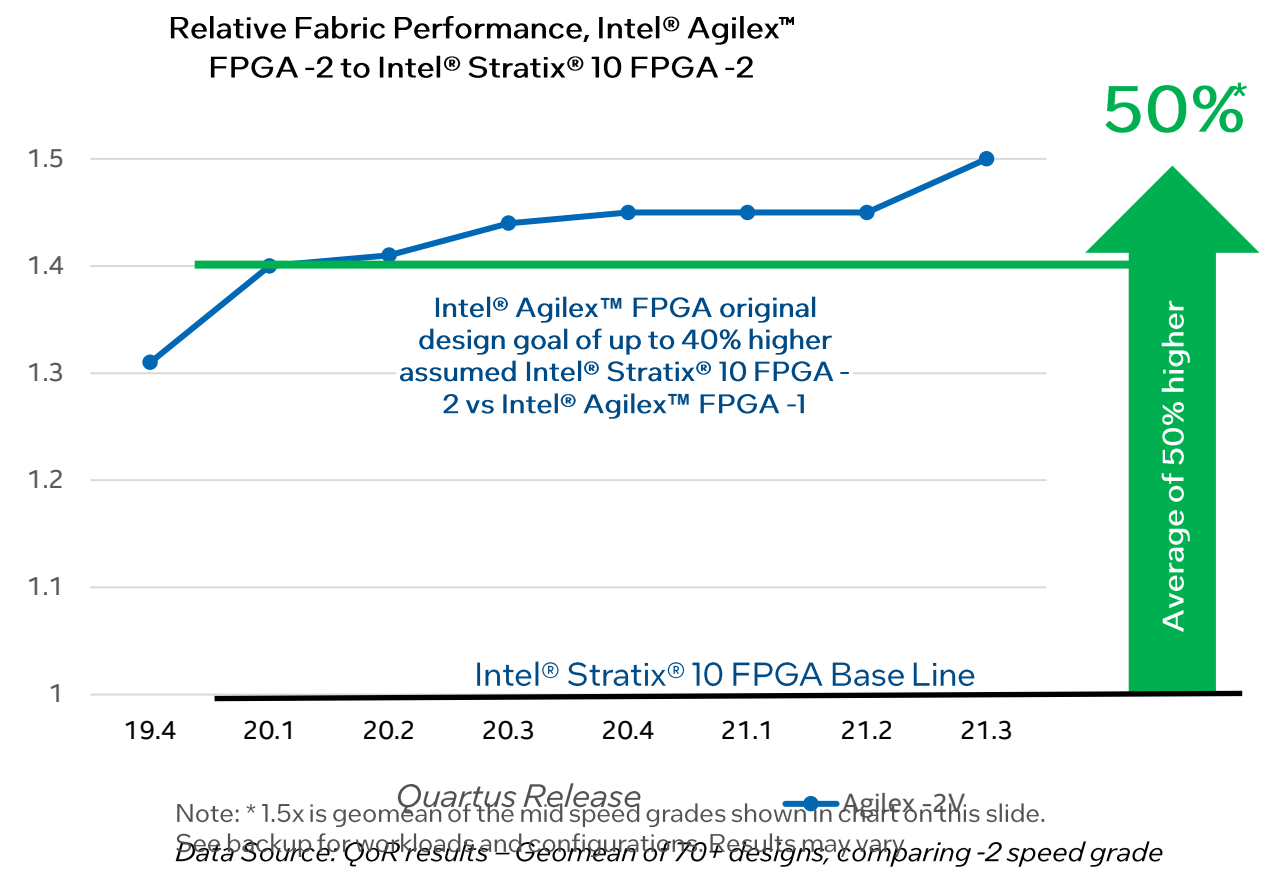
- **Process**
  - Intel® 10nm SuperFin Technology (F and I-Series)
  - Intel 7 Process (M-Series)
  - Close collaboration with foundry to optimize process
  - Transistor tuning and metal stack optimizations for Agilex™
- **Architecture**
  - 2nd generation Intel® Hyperflex™ architecture
  - ALM, routing & floorplan improvements for performance
- **Tools**
  - Innovation in Intel® Quartus® Prime Software to improve performance

Up to 50% Higher Performance Compared to Intel® Stratix® 10 Devices

*See Configuration Details for performance info

Intel® Agilex™ FPGA Power/Performance Improvements over Intel® Stratix® 10 FPGA

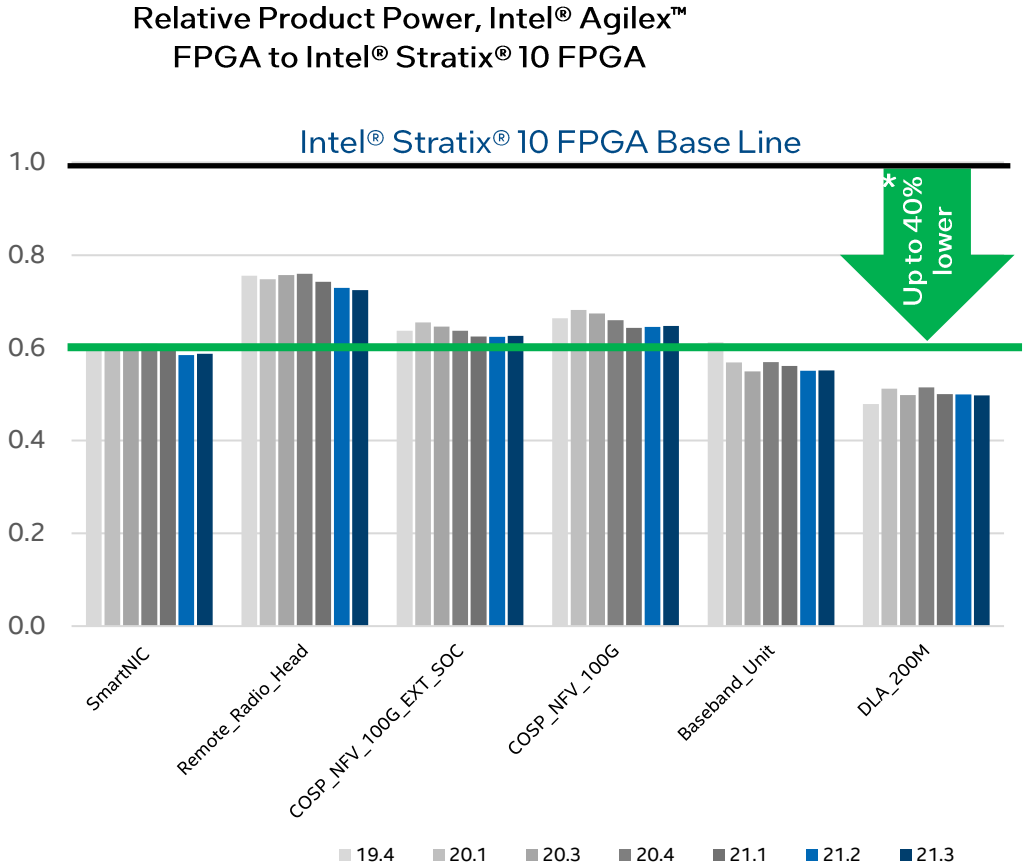
Fabric Performance - Higher is Better



Note: * 1.5x is geomean of the mid speed grades shown in chart on this slide.
See backup for workloads and configurations. Results may vary.

Data Source: QoR results – Geomean of 70+ designs, comparing -2 speed grade

Total Power - Lower is Better



Data Source:
Intel® Agilex™ FPGA -3E AGF014 PTC
Intel® Stratix® 10 FPGA different device dependent on design 110/210/250-2 (PTC)

Steady Execution to Exceed Power and Performance Goals

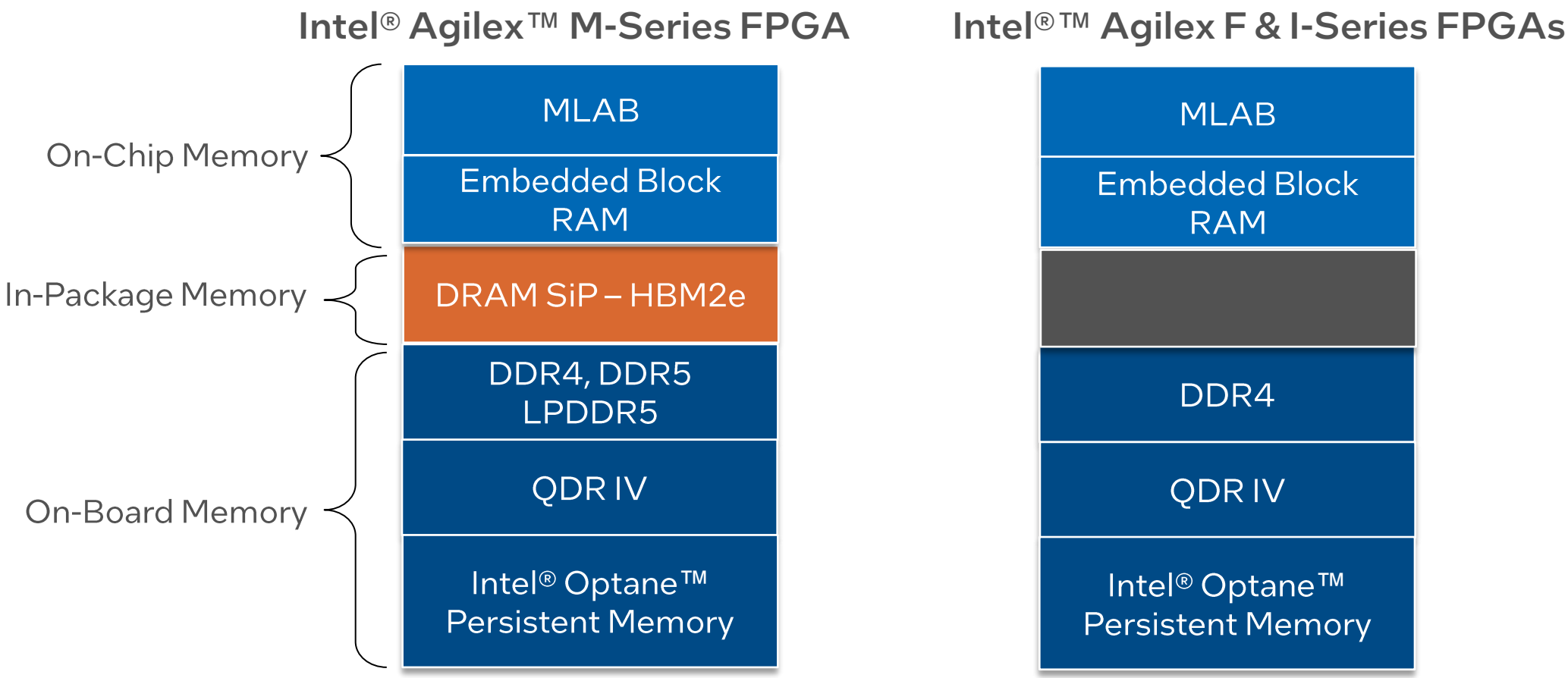
*See Configuration Details for performance info

Intel® Agilex™ FPGA Variants

	F-Series Wide range of applications	I-Series High-performance Xeon attach and BW-intensive apps	M-Series Compute-intensive applications with highest memory BW req's
Logic Capacity	573K-2.7M LE	up to 4.0M LE	up to 4.0M LE
On-chip Memory	5-35 MB	up to 48 MB	up to 46 MB
DSP blocks	up to 8k	up to 12.5k	up to 12.5k
XCVR speeds	32/58G	32/58/116G	up to 116G
Hard PCIe	PCIe Gen4	PCIe Gen5	PCIe Gen5
Off-chip Memory*	DDR4 + Optane™ 200	DDR4 + Optane 200	LPDDR5/DDR5
Hard Crypto / Ethernet	200G / 400GbE	200G / 400GbE	400GbE
Security	Triple-modular redundant hard processor, encryption, boot order, tamper detection		
ARM SoC	Quad-core Arm Cortex-A53 up to 1.41 GHz, NEON co-processor, DMA, cache, etc		
Coherency Option		Compute Express Link (CXL)	
High-Bandwidth Memory Option			16GB/32GB HBM2e

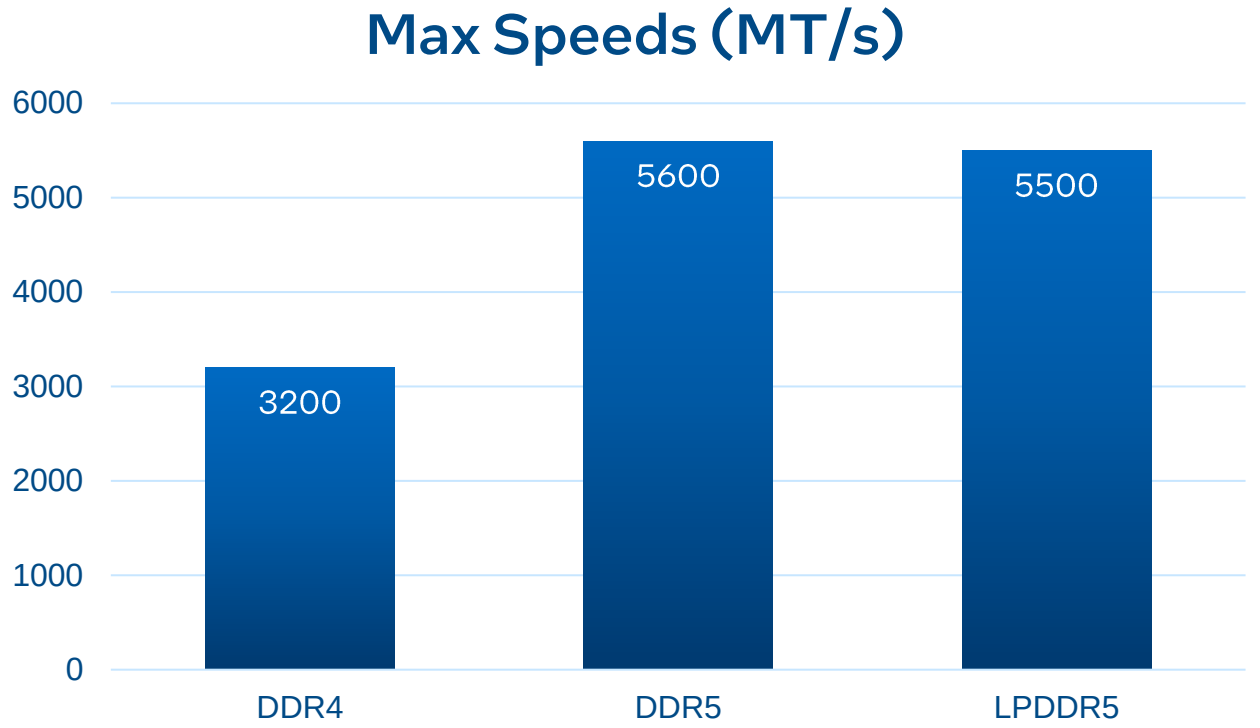
Intel® Agilex™ M-Series Memory Interface Solutions

Intel® Agilex™ FPGA Series Memory Hierarchy



Wide Range of Memory Options to Address Your Design's Low-latency, High-throughput, and Low-power Needs

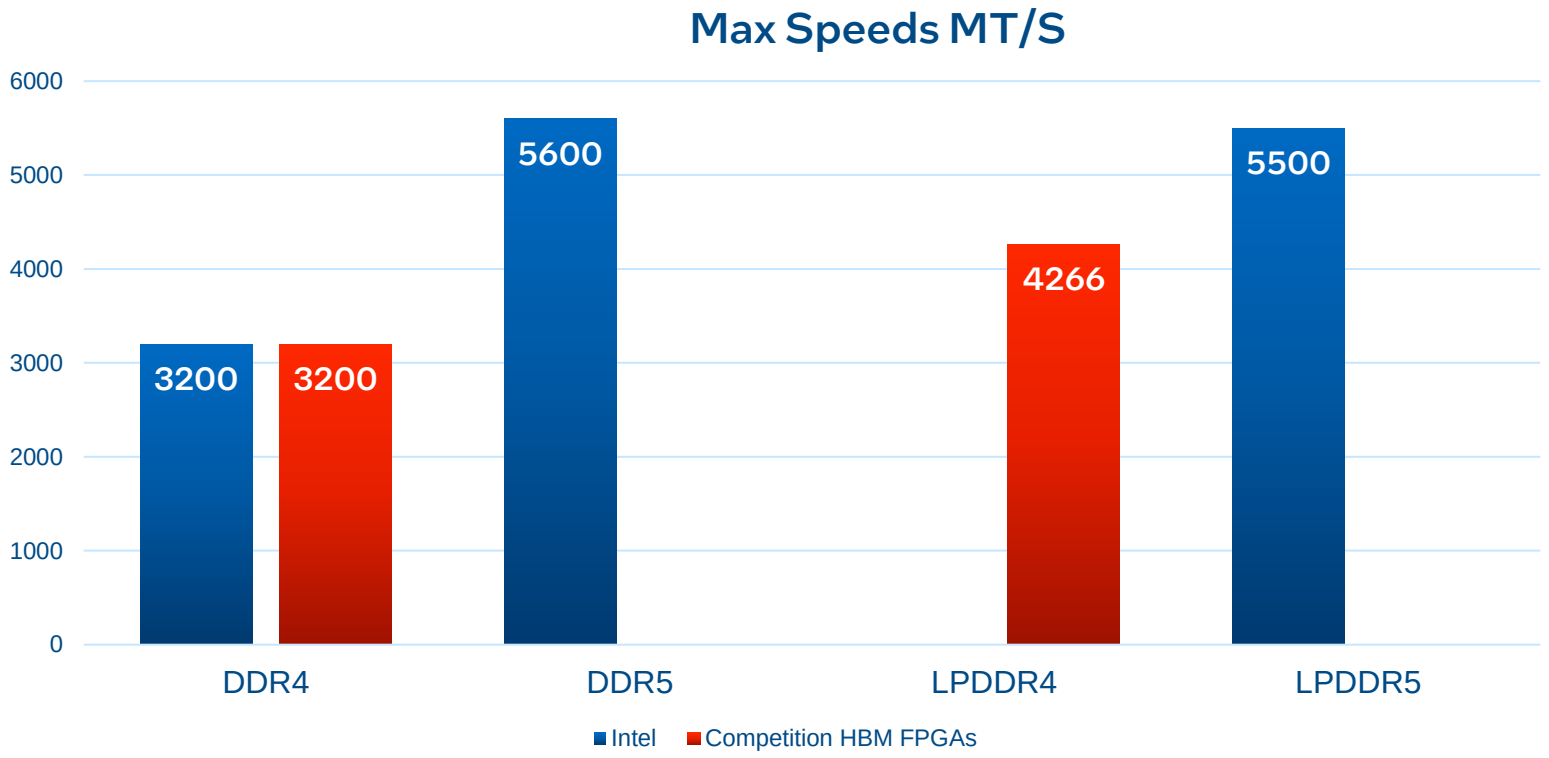
Intel® Agilex™ M-Series FPGA DRAM EMIF Performance



Up to 179.2 GBps Memory Bandwidth

*1.75X speed improvement based on comparison between competition DDR4 & Intel Agilex-M series FPGA DDR5, see Performance/Power Configuration slide for details

Intel® Agilex™ M-Series FPGA DRAM Support Vs Competition



Intel® Agilex™ M-Series FPGA Supports High-performance, High-density DDR5, and LPDDR5 vs Competition

DDR5 LPDDR5 DRAM Memory Architecture

DDR4 VS DDR5 DRAM

DDR5 memory is JEDEC (JESD79-5) standard compliant

Feature	Intel® Stratix® 10 FPGA DDR4	Intel® Agilex™ M-Series FPGA DDR5	DDR5 Benefits
Maximum data rate	2667 MT/s	5600 MT/s	2X better performance
I/O voltage	1.2V	1.1V	Lower power
DRAM device density	2 Gb-16 Gb	16 Gb-64 Gb	Larger density DIMMs
Power management	Motherboard	PMIC on the DIMM	Reduces board PDN design complexity when using DIMM
Prefetch	8n	16n	Enables higher data rates for the same internal clock rate as DDR4
DIMM topology	1 Channel/DIMM with 64 data bits 72 bits/channel with error correction code (ECC)	2 independent channels/DIMM with 80-bits total or 40 bits per channel with ECC	Higher memory efficiency and lower latency
On-Die termination (ODT)	DQ, DQS, DM/DBI	DQ, DQS, DM, CA bus	CA ODT improves SI and saves BOM costs by eliminating the external termination

LPDDR5

- LPDDR5 is a component not DIMM
- Intel FPGAs supports a data width of x16 and x32
- Vendors usually put 2, 4, or 8 of these chips onto a single “package”
- Each “package” can have 2 or 4 channels, with each channel containing 1 or 2 ranks. Each rank is built from one LPDDR5 component

Mem I/F	Memory Types	DRAM width	No. of Channels & Channel Width*	IO96 Resources Utilized	
				No. of IO96 Blocks	Memory controllers per IO96
LPDDR5	Component	x32	1Ch - x32	1	1
		x32	2Ch - x64	2	2
		x16	2Ch - x32	1	2
		x16	4Ch - x64	2	4

* Preliminary and subject to change

System in Package HBM2e

HBM2e In-Package Memory Device

	FPGA Core Speed		
	-1	-2	-3
Spec Supported	JESD235C		
No. of Channels	8		
No. of Pseudo Channels (PC)	16		
Effective Bus width/Stack	1026-bit		
Height supported/Stack	4H/8H		
Max Density/Stack (4H/8H)	8 GB/16 GB		
Speed (MHz)	1600 MHz	1400 MHz	1000 MHz
Max Parallel Bandwidth(GB/s)	409.6	358.4	256
Max Bandwidth/Pin(Gb/s)	3.2	2.8	2

HBM2e VS HBM2

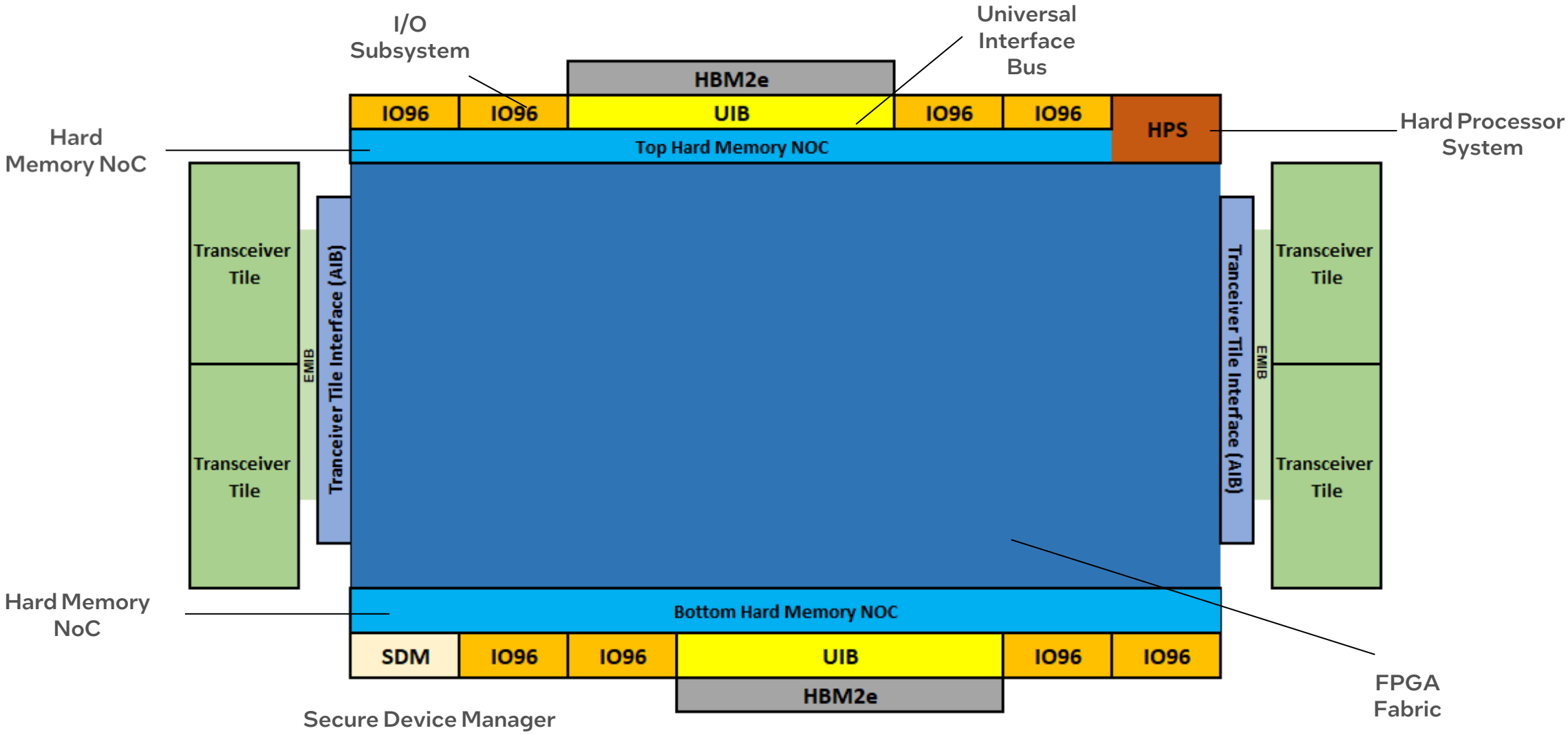
	Intel® Agilex™ M-Series FPGA HBM2e	Intel® Stratix® 10 MX FPGA HBM2
JEDEC Standard	JESD235C	JESD235A
Max Bandwidth/Stack	410 GB/s	256 GB/s
Max Die Capacity	2GB	1GB
Available Stack Heights	4H/8H	4H/8H
Available Densities (4H/8H)	8 GB/16 GB	4 GB/8 GB
Max Channels Per Stack	8 channels/16 Pseudo Channels	
Bus width/Stack	1024-bits	
Voltage	1.2V	

Up to 820 GBps Memory Bandwidth*; 7X Higher Bandwidth than GDDR6

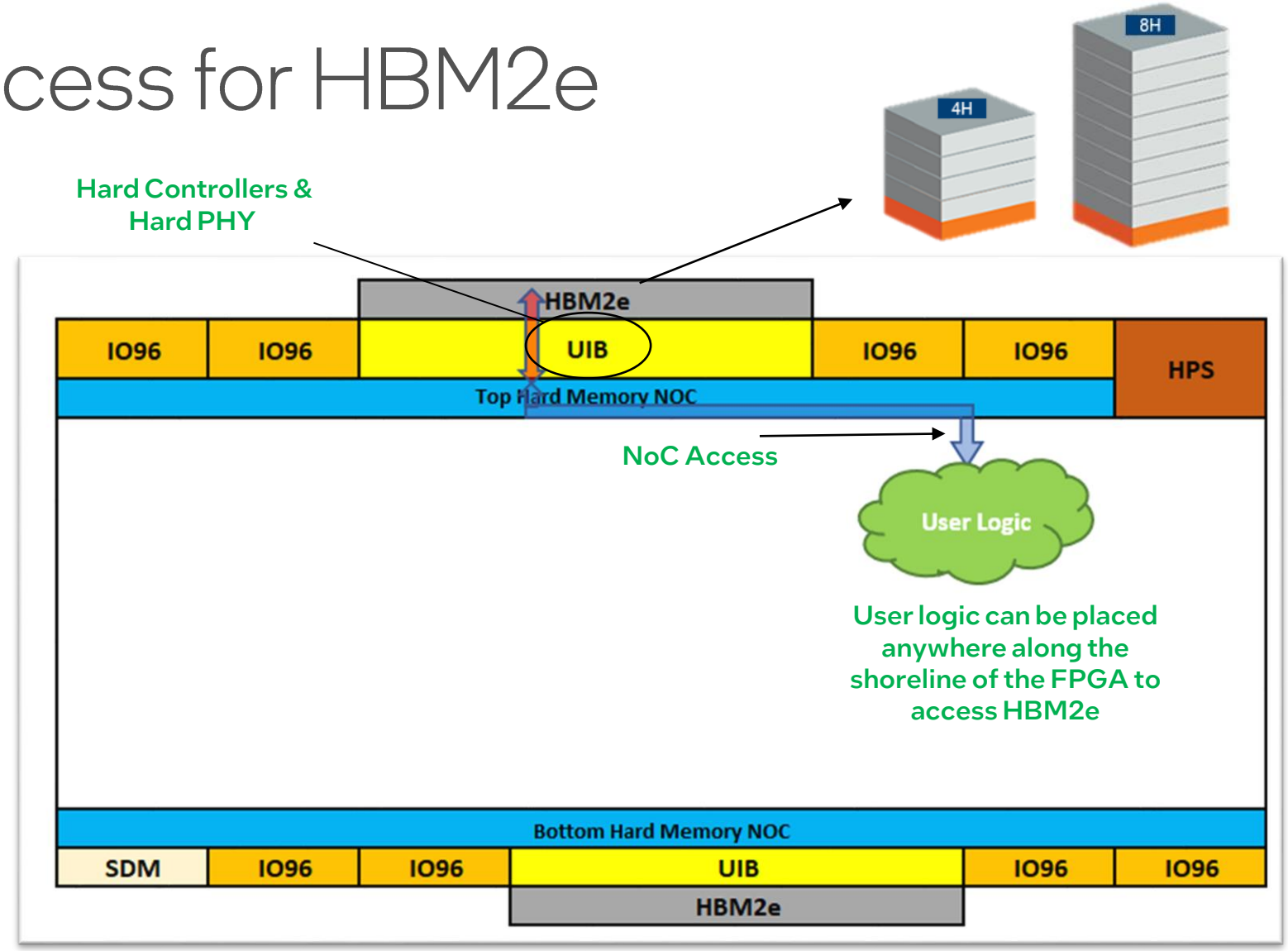
* Actual throughput may vary based on controller's efficiency & traffic access patterns.

Intel® Agilex™ M-Series Memory Hardware Architecture

Intel® Agilex™ M-Series Device Floorplan



NoC Access for HBM2e

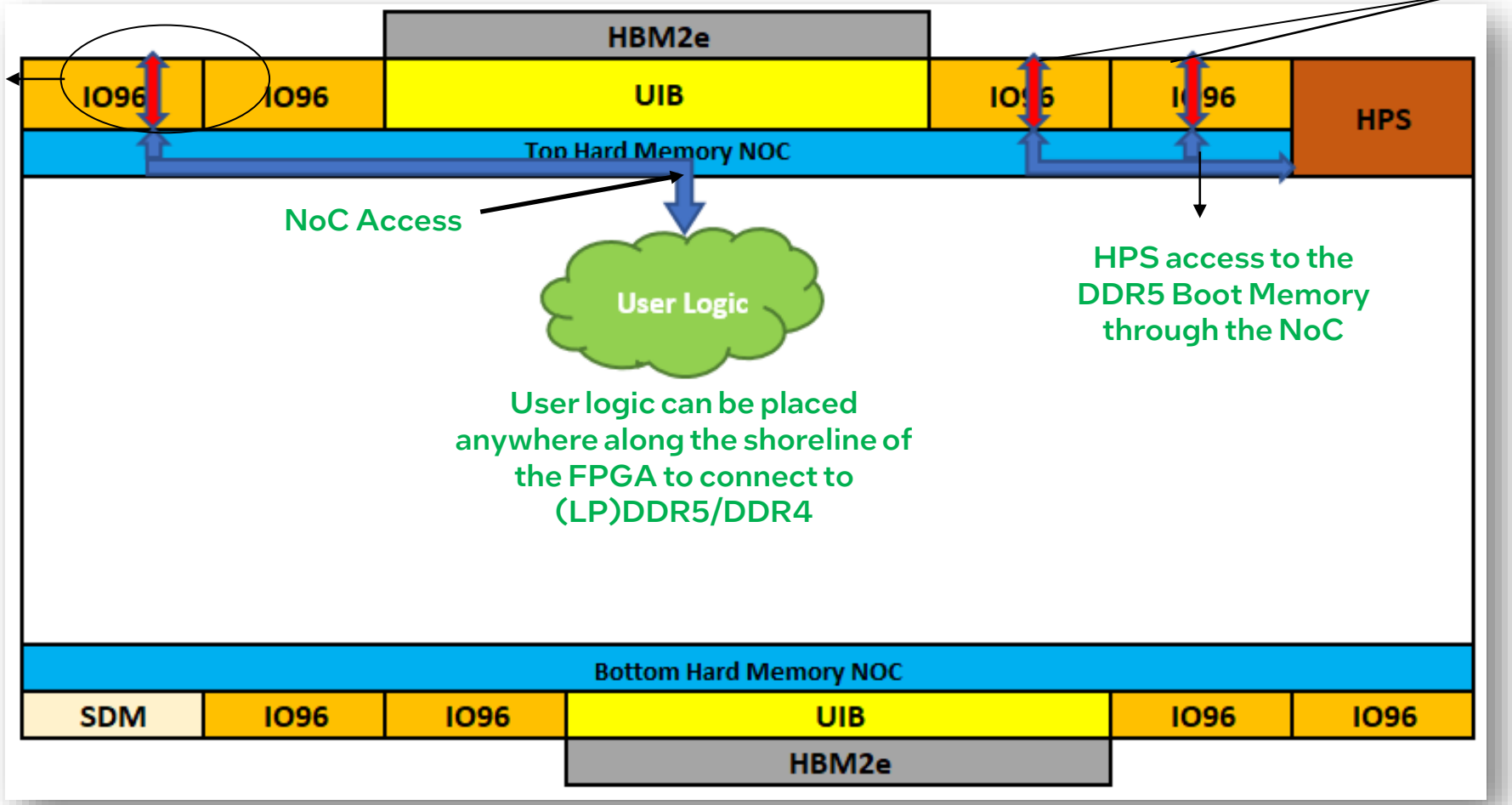


[1] Timing & electrically compatible with DDR5 DIMM

[2] Timing & electrically compatible with DDR4 DIMM

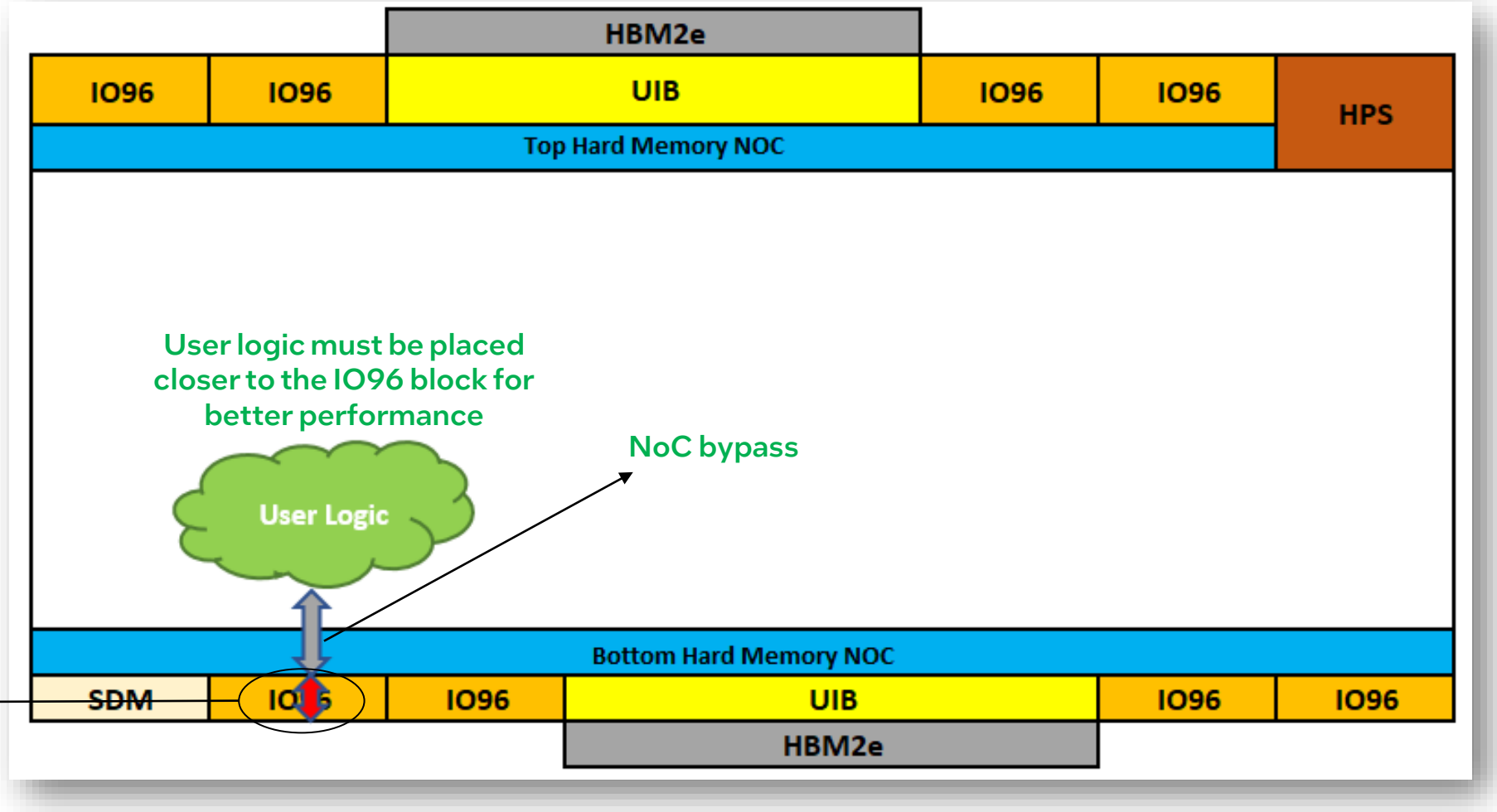
NoC Access for (LP)DDR5/DDR4

Hard Controller & Hard PHY

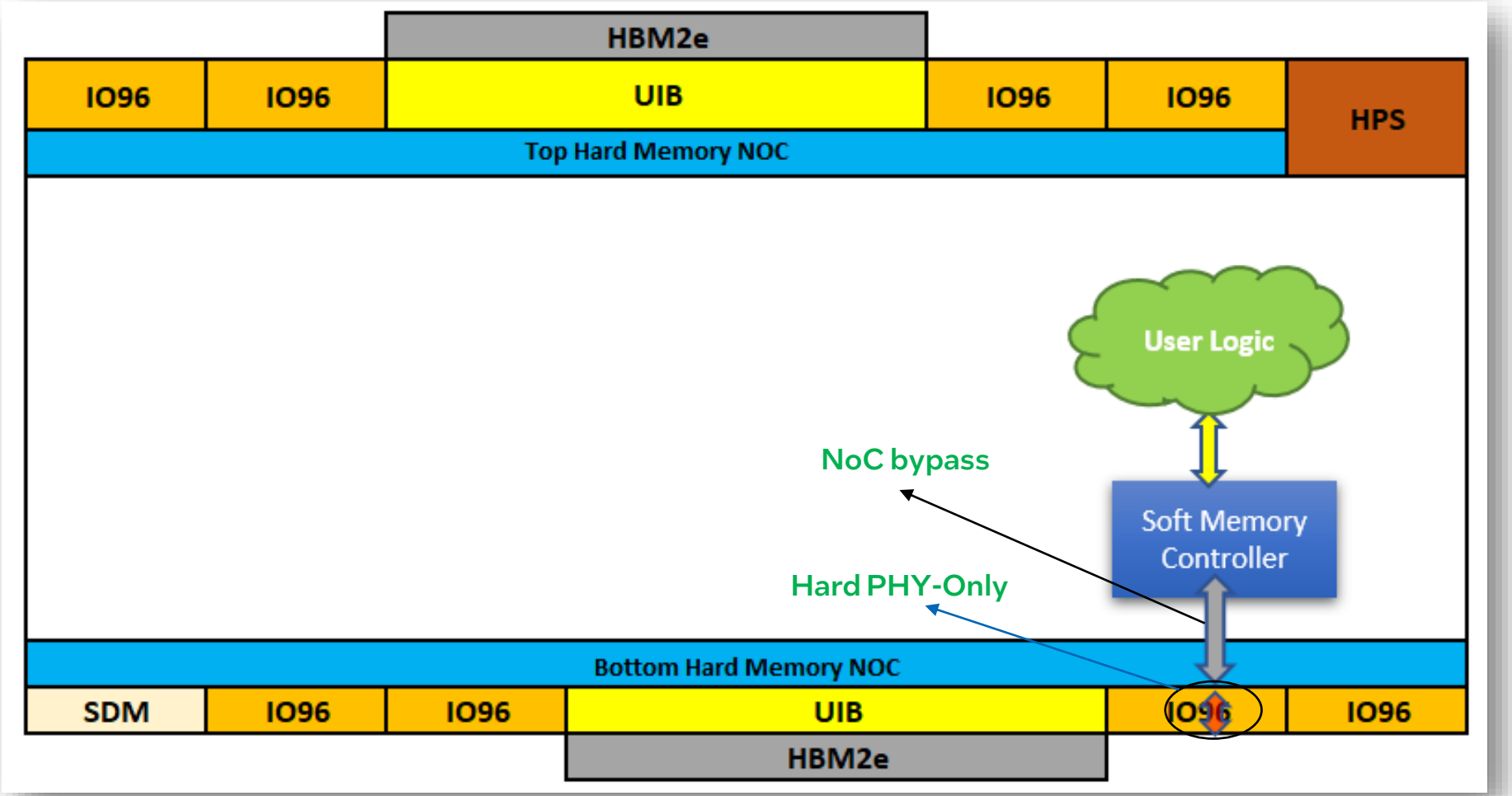


Two possible IO96 connection from HPS to Boot Memory

NoC Bypass for (LP)DDR5/DDR4

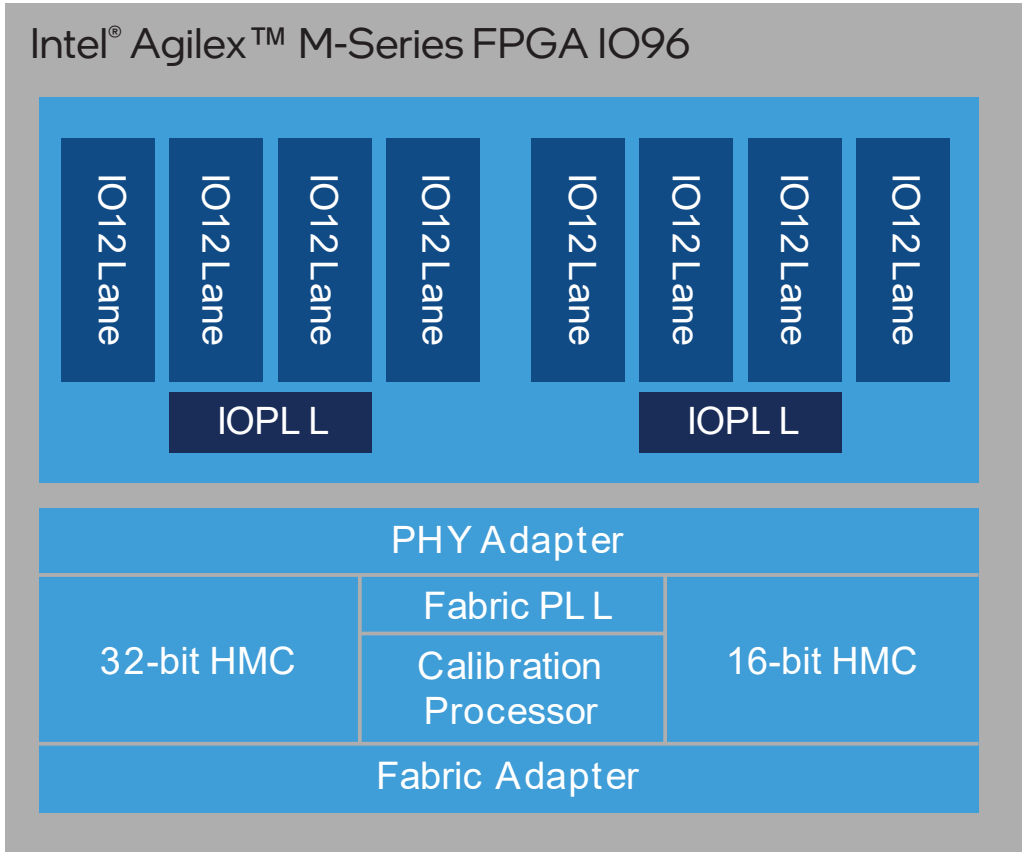


NOC Bypass for QDR IV and Intel® Optane™ Persistent Memory



I/O Subsystem (IO96)

- Enhanced I/O Subsystem to support channels that can fit within a single IO96 (96 pins/bank)
- Supports Hard Memory NoC
- Supports asynchronous and synchronous clocking
- One HMCs for a single x32 channel or two HMCs for two x16 channels



- HMC – Hard Memory Controller
- 32-bit HMC handles 32-bit data + 8-bit ECC
- 16-bit HMC handles 16-bit data + 8-bit ECC

I/O Subsystem Differences Between Intel® Agilex™ FPGA Families

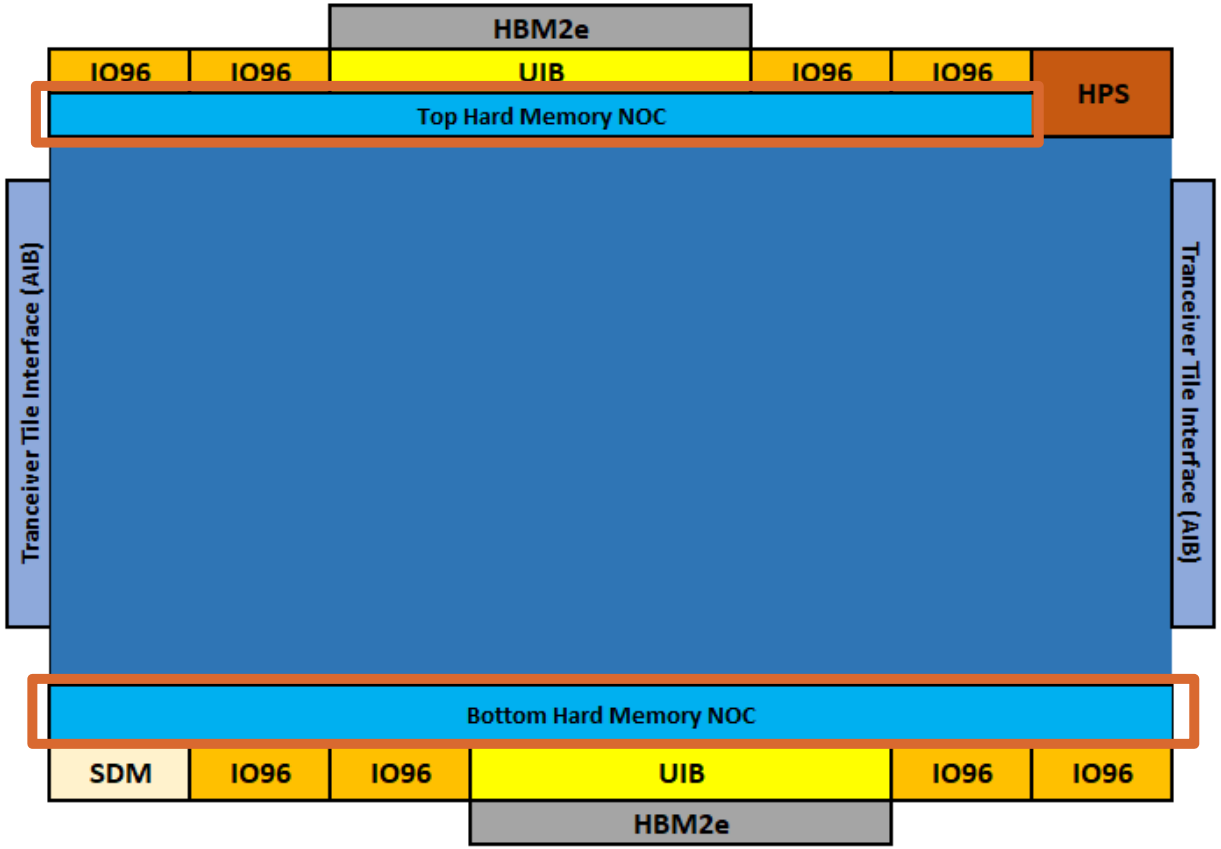
Feature	Intel® Agilex™ F & I Series FPGA	Intel® Agilex™ M-Series FPGA
Protocol Support	DDR4, QDR IV	DDR4, DDR5, LPDDR5, QDR IV
User interface (data)	Avalon® memory-mapped or Avalon® streaming interface	AXI4
User-interface (calibration/debug)	Avalon memory-mapped interface	AXI4-Lite
Memory NoC	No memory NoC. (Direct access to controller from fabric)	Supported for HMC-based protocols. Two access modes are enabled - Direct access to controller from fabric[1] - NoC access to controller
ECC-support	Supported through soft-logic (except HPS-EMIF)	Hardened support for syndrome calculation and update
Calibration	Interface along an I/O-EDGE calibrated by a single processor	Interfaces in different I/O-banks calibrated by different processors

Hard Memory Network-on-Chip (NoC)

Hard Memory NoC

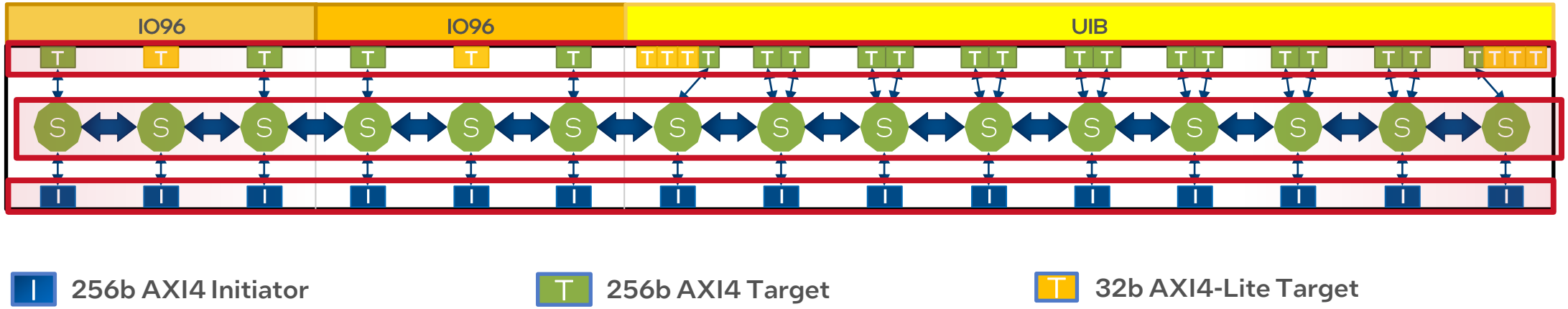
- Facilitates high bandwidth data movement between FPGA fabric and NoC-attached memories without using FPGA routing resources

- Memory NoC bypass mode for fabric/peripheral interfaces available for SDM, EMIF, LVDS, PHYLITE, and GPIO



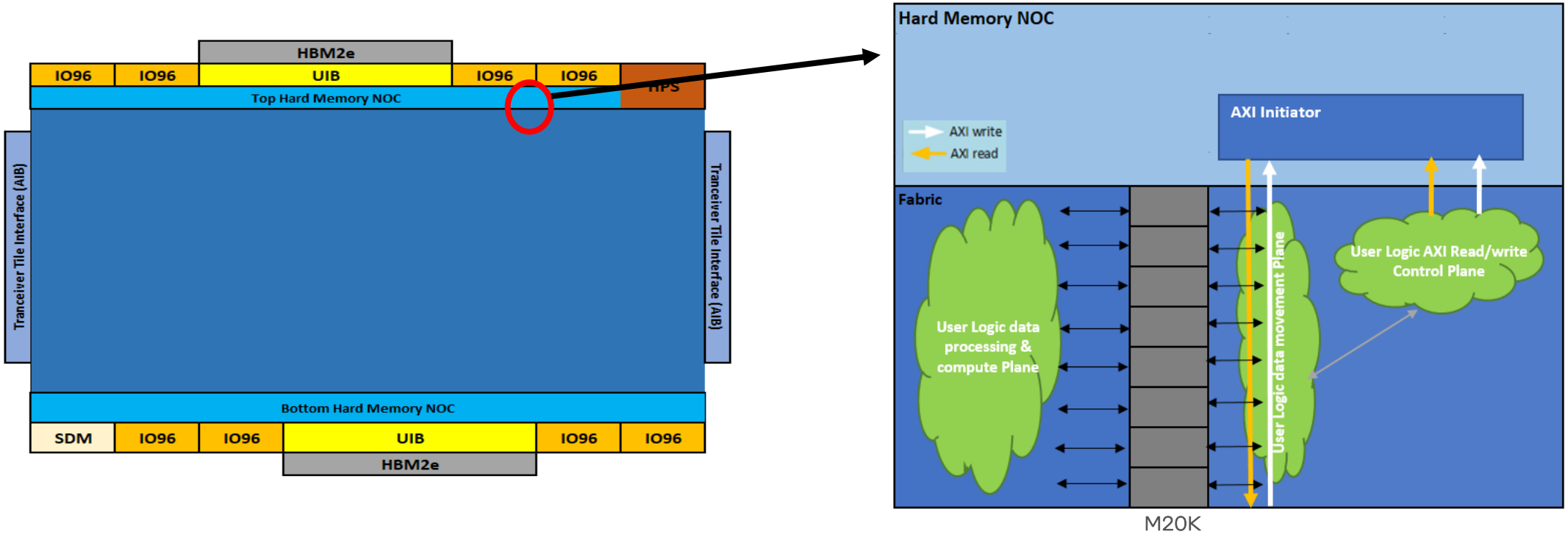
Hard Memory NoC Terminology

- Access points to the NoC
  - Initiators – Connect to user logic AXI4 ports that initiate requests
  - Targets – Connect to NOC attached memories and provide responses
- Full hardened crossbar configuration support
- Switches in the NoC route requests and responses between initiators and targets using proprietary protocol
- Initiator-bridges index target-bridges through Virtual Addressing



Hard Memory NoC – Horizontal Network

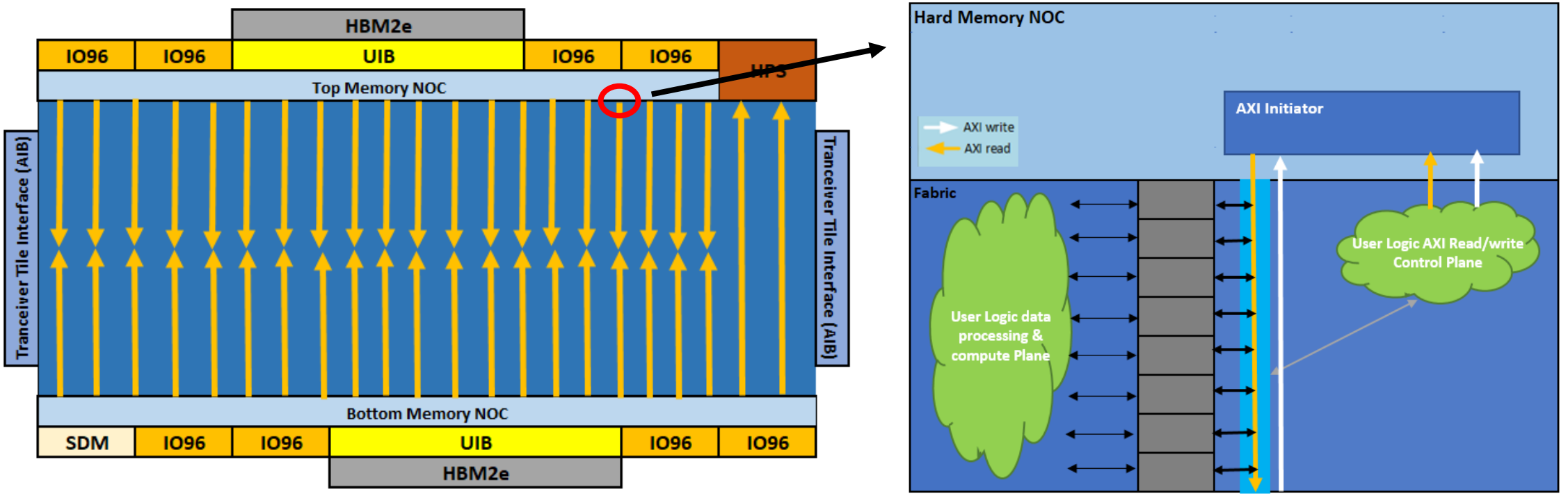
- Horizontal network enables high-bandwidth data movement from user logic to NoC-attached memories
- User logic AXI4 Ports connect to initiator AXI4 ports



Allows High-bandwidth Data Movement from FPGA Fabric to Memories

Hard Memory NoC – Vertical Network

- Optionally enables dedicated high-bandwidth read data path from AXI4 Initiators to on-chip M20Ks



Eliminates Routing Hotspots and Spreads Read Data Vertically into the FPGA

HBM2e + NOC Use Case Application

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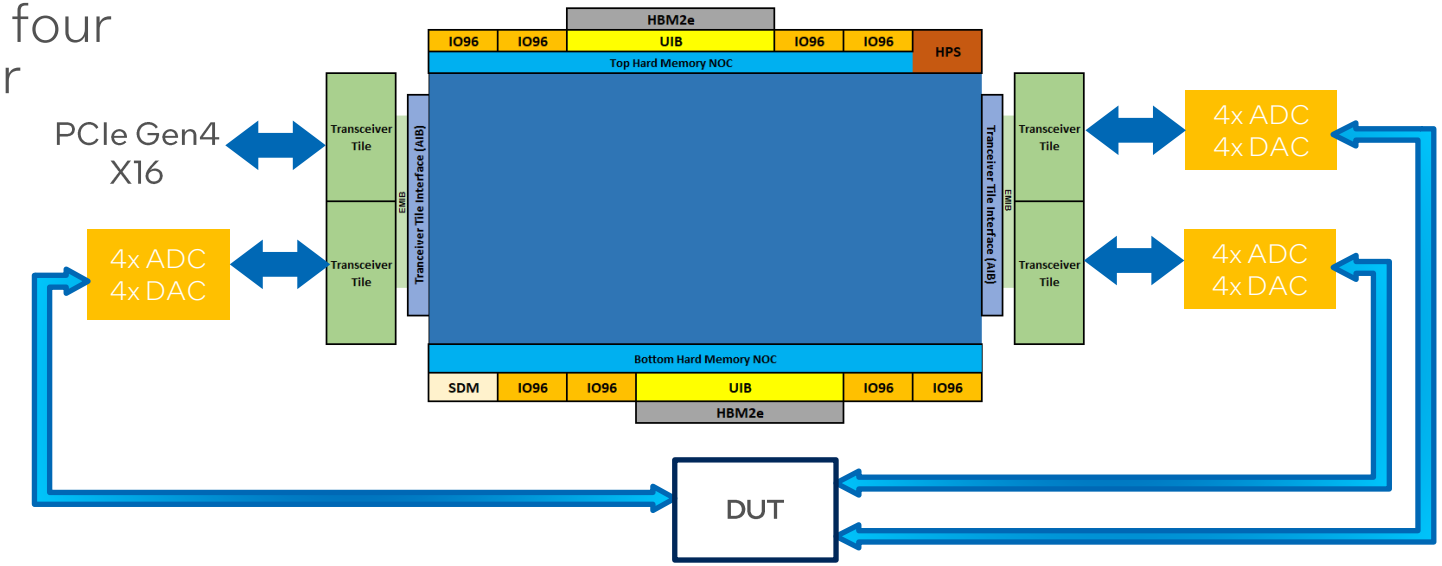
RF Analog Hardware in-the-Loop Testing

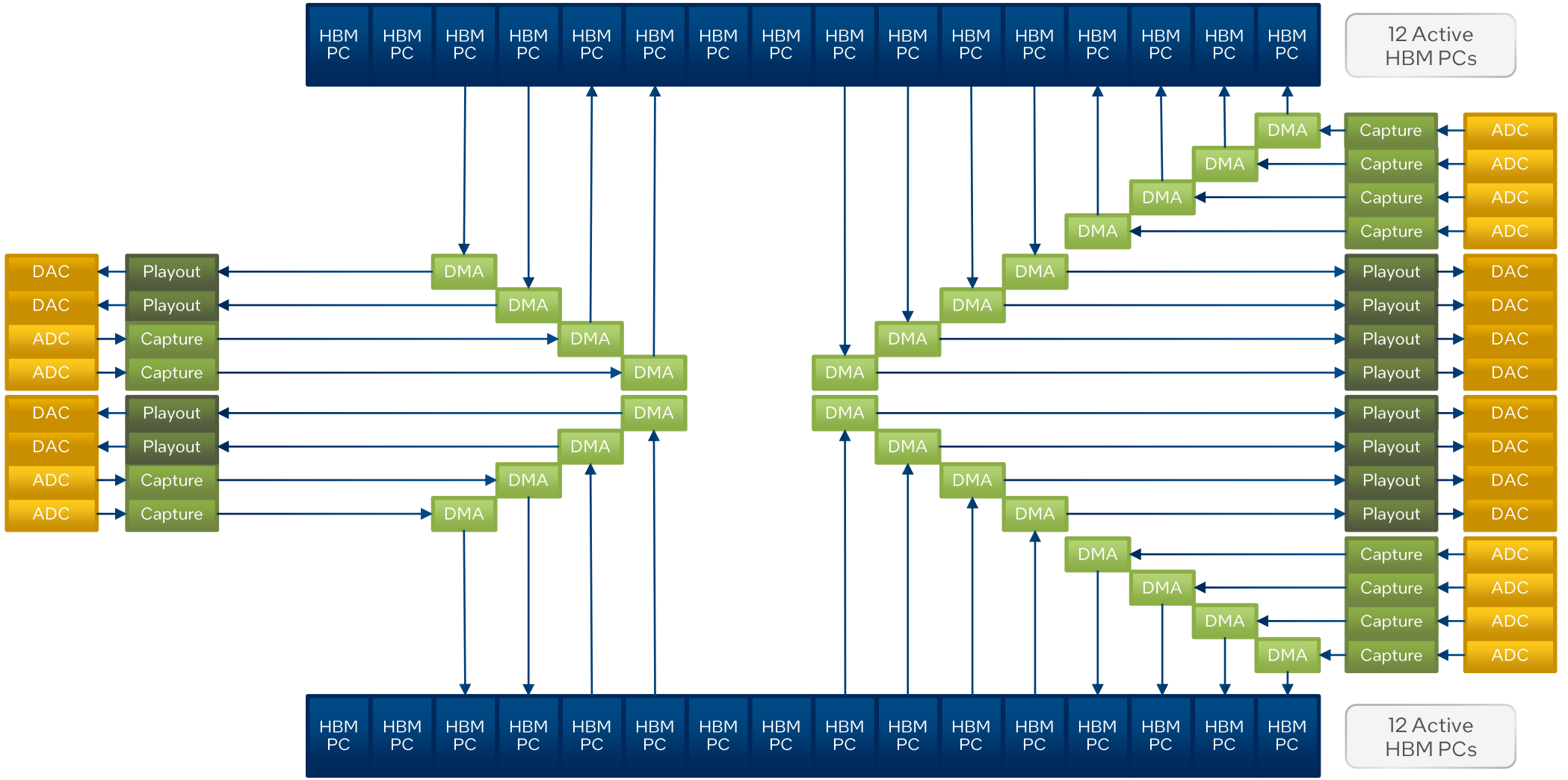
- Microwave RF systems – 5G, radar – need high-power high-frequency amplifiers
- Test approach
  - Construct a set of waveforms to exercise device under test (DUT)
  - Continuously play waveforms into the DUT
  - Capture output waveforms for analysis
  - Analyze waveforms
    - Data reduction via FFT after capture
  - Based on analysis, choose new set of waveforms to play
    - Loading of new waveforms overlapped with capture (PCIe 4.0x16: 32 GB/s)

Potential Hardware Solution

- FPGA interfaces
  - Three sets of four digital-to-analog converter (DAC) + four analog-to-digital converter (ADC) on the board
  - PCIe tile
  - 2 x HBM2e stack
- Waveform data
  - 12 channels DAC, 12 channels ADC
  - up to 4Gsps / channel
  - Word length 16I + 16Q
  - 15.625 GB/s per channel (total 375 GB/s)



Dataflow – Data Playout and Capture



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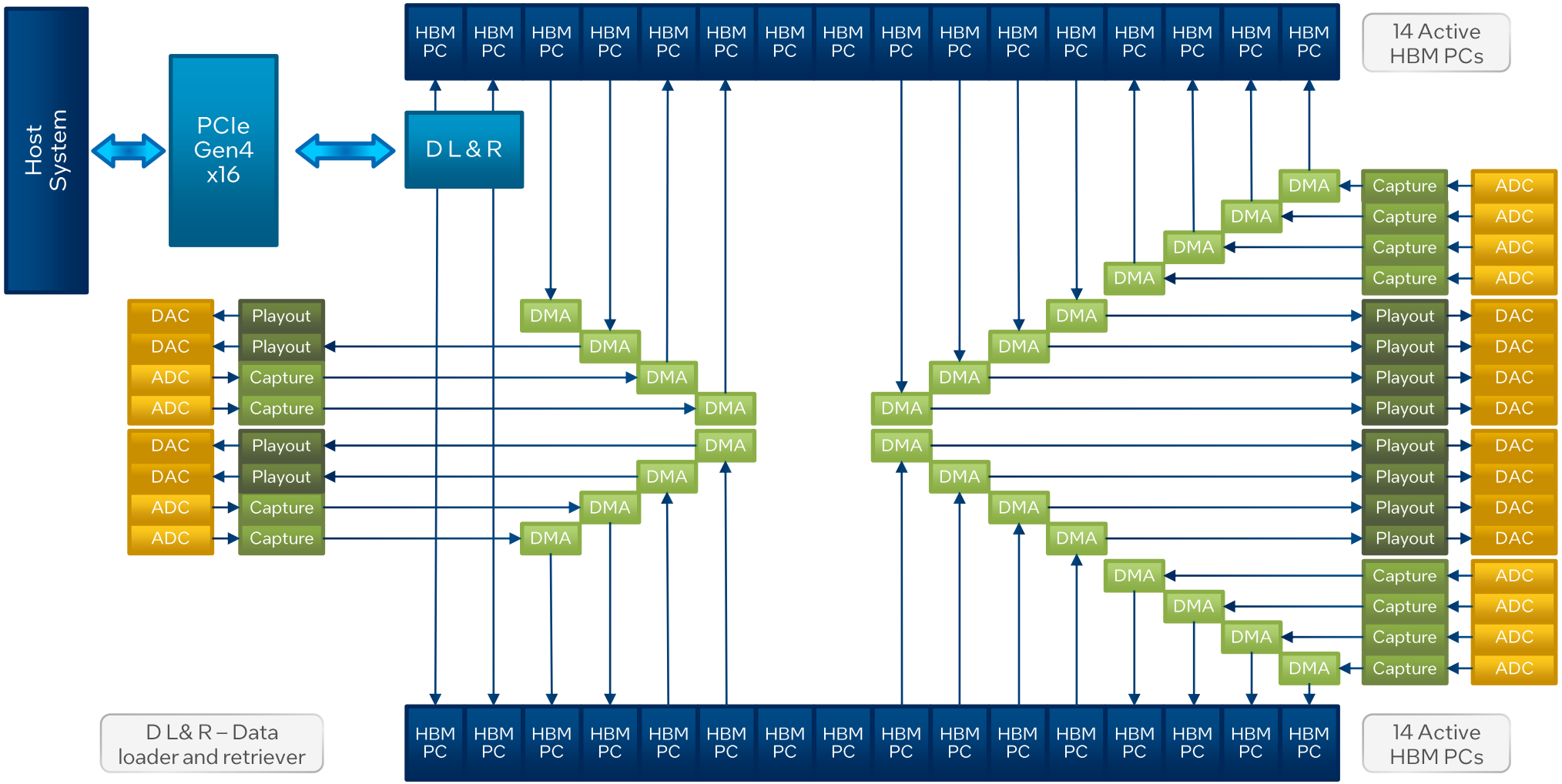

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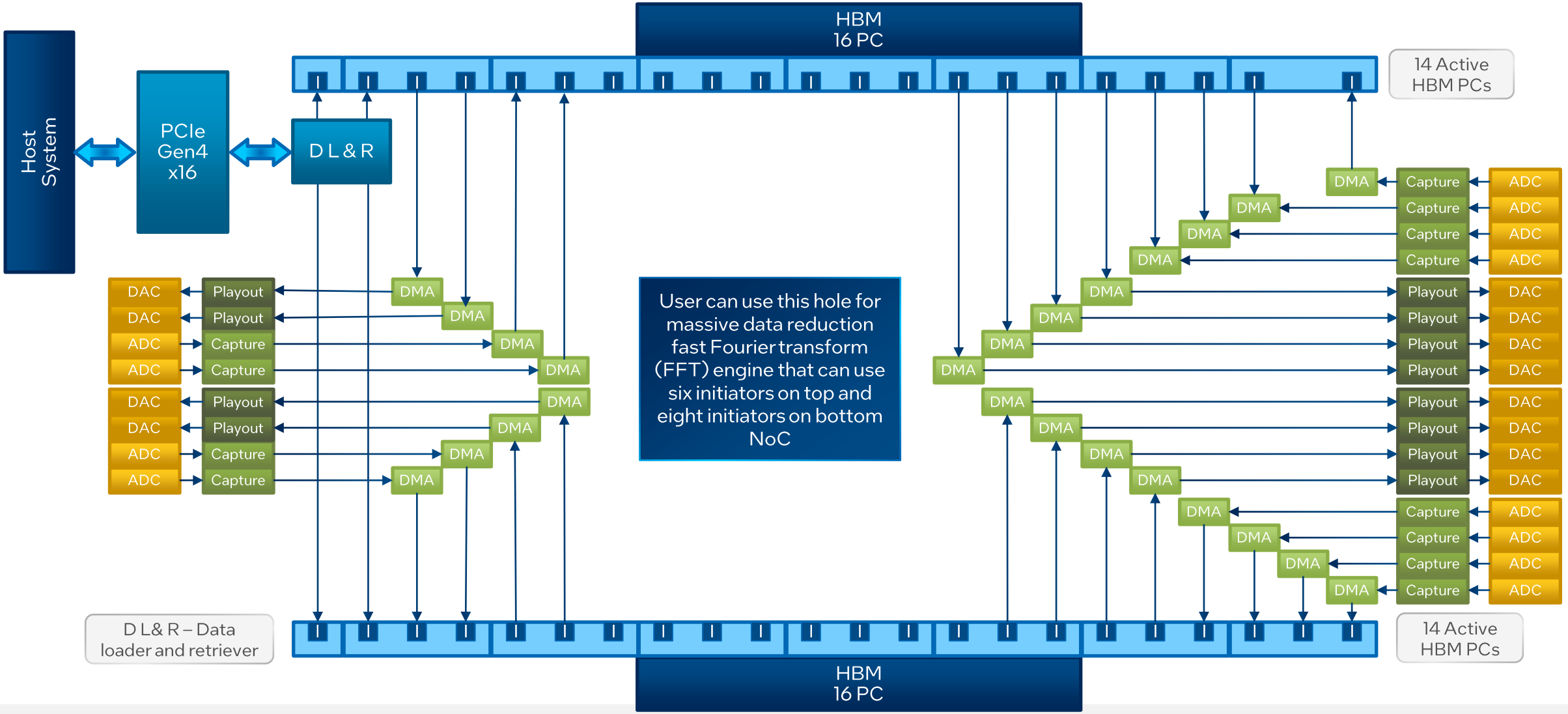

Summary

- Intel® Agilex™ M-Series FPGA offers wide range of memory solutions for high throughput, low power, low latency needs
- Intel Agilex M-Series FPGA supports high-performance and low-power DDR5 and LPDDR5 compared to competition and in-package HBM2e
- Hard memory NoC provides a high speed and efficient way of transferring data between the NoC attached memories and fabric
- Additional resources
  - Refer to the Intel Agilex M-Series FPGA Memory white paper for product details, benefits, and use cases
  - Check out the Intel Agilex M-Series FPGA product page
  - Contact your Intel sales representative for further information

Intel® Agilex™ FPGA Performance/Power Configuration Details

1. Average of 50% Higher Performance Compared to Intel® Stratix® 10 FPGAs)

- Derived from testing an example design suite comparing maximum clock speed (Fmax) achieved in Intel® Stratix® 10 devices with the Fmax achieved in Intel® Agilex™ devices, using Intel® Quartus® Prime Software 21.3. On average, designs running in the comparable mid-speed grade of Intel® Agilex™ FPGAs achieve a geomean of 50% improvement in Fmax compared to the same designs running in the most popular speed grade of Intel® Stratix® 10 devices, tested August 2021.

2. Up to 40% Lower Total Power Compared to Intel® Stratix® 10 FPGAs)

- Derived from testing an example design suite comparing total power estimates of each design running in Intel® Stratix® 10 FPGAs compared to the total power consumed by the same design running in Intel® Agilex™ FPGAs. Power estimates of Intel® Stratix® 10 FPGA designs are obtained from Intel® Stratix® 10 Early Power Estimator; power estimates for Intel® Agilex™ FPGA designs are obtained using Intel® FPGA Power and Thermal Calculator (PTC), and internal Intel® analysis and architecture simulation and modeling, tested April 2021 (PTC 21.1).

3. Up to 40 TFLOPs of DSP Performance (FP16 Configuration)

- Each Intel® Agilex™ DSP block can perform two FP16 floating-point operations (FLOPs) per clock cycle. Total FLOPs for FP16 configuration is derived by multiplying 2x the maximum number of DSP blocks to be offered in a single Intel® Agilex™ FPGA by the maximum clock frequency that will be specified for that block.

4. Over 2x Better Fabric Performance per Watt vs. Competing 7nm FPGAs

- Agilex M-Series >2x fabric performance/W results are based on projections of Agilex AGM039-R31B compared to measurements on Agilex AGI027-R31B, and power comparison of AGF014-2 to a Xilinx Versal FPGA fabric of equivalent density, where Agilex AGI027-R31B is projected to have the same core fabric performance/watt as measured on AGF014-2. Comparison assumes Xilinx Versal HBM has the same core fabric as similar Versal devices without HBM as of October 2021.

5. Memory Bandwidth; 1.75x Performance vs Competition

- Intel Agilex M-Series theoretical maximum bandwidth of 1.099 TBps with 2 banks of HBM2e using ECC as data and 8 DDR5 DIMMs as compared to Xilinx Versal HBM memory bandwidth of 1.056 TBps from https://www.xilinx.com/products/silicon-devices/acap/versal-hbm.html#productAdvantages and from https://www.xilinx.com/content/dam/xilinx/support/documentation/selection-guides/versal-hbm-product-selection-guide.pdf as of October 14, 2021 and to Achronix Speedster 7t memory bandwidth of 0.5 TBps from https://www.achronix.com/sites/default/files/docs/Speedster7t_Product_Brief_PB033.pdf as of October 14th 2021

Results have been estimated or simulated using internal Intel® analysis, architecture simulation, and modeling, and provided to you for informational purposes. Any differences in your system hardware, software or configuration may affect your actual performance.

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