SONIX TECHNOLOGY CO ., LTD

SNC7312 Series Datasheet

SNC73121

SNC73122

SNC73123

SNC73124

SNC73125

SNC73126

Content

AMENDMENT HISTORY

Version	Date	Description
Version 1.0	2016/04/15	First release
Version 1.1	2016/05/4	Update SNC73125 Pin Assignment
Version 1.2	2016/06/1	Update SNC73126 Pin Assignment
Version 1.3	2017/01/5	Modify multi-function pin about SNC73125 Remove P1.1/P4.5/P4.4
Version 1.4	2017/03/30	Add Version B information Chapter 2.1/2.2/2.3

1 Introduction

1.1 General Description

The SNC7312 chip is the 32-bit Cortex™ M0 processor for multi-media application. It runs up to 96MHz and optimizes ARM CMSIS Standard DSP Library. SNC7312, compare to other M0 processor, it has better audio process ability and is comparable with CMSIS DSP Library provided by ARM.

SNC7312 not only support stereo MP3/WMA/AAC playback, but also provides some advance audio algorithm: voice charger, beat detection…and so on. With ARM integrate development environment, such as Keil, user can easily start up their system.

In image process filed, cmos sensor interface and PPU are equipped with SNC7312. PPU helps to 2D picture moving and game design. SNC7312 also support SDRAM interface for motion JPEG recording.

In SNC7312, other peripherals are embedded; including TFT LCD Interface, SPI master/slave interface, SD/MMC controller, SDIO Host, USB2.0 high speed device/Host, audio ADC, Stereo DAC, builded-in amplifier and 6-ch SAR ADC.

1.2 Features

Cortex M0

- **Working voltage: 2.7V ~ 3.6V**
- **Core**
  - ARM@Cortex-M0 core runs up to 96MHz
  - Support low power sleep mode
  - Single-cycle 32-bit hardware multiplier
  - Serial Wire Debug supports
- **Interrupt sources**
  - ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC)
  - 1 for DSP signal
- **System clocks**
  - High clock:
    - 12MHz XTAL
    - 12MHz IHRC
  - Low clock:
    - 32768Hz XTAL
    - 32768Hz ILRC (1V)
  - PLL pumps form XTAL or IHRC and divider to 24MHz~96MHz for system clock
- **Memory**
  - M0 System
    - ROM size: 64KB
    - M0 PRAM size: 64KB
  - M0/DSP share RAM: 456KB
- **Operating modes**
  - Normal mode
  - Deep-sleep mode
  - Deep power-down mode
- **LVD/LVR**
  - LVR: 0.9V for Core, 2.1V for IO
  - LVD: 1.0V for Core, 2.5V for IO
  - Auto shutdown LVD: 1.8V for IO
- **LDO output 1.2V**
- **ROM Remap**
- **ISO Block mode**
  - Deep power down function
  - Deep power down with RTC wakeup function
  - RTC Clock: 32KXTAL, ILRC (3V)

DSP

- **Built-in a 16-bit S9KE2 DSP**
- **System Clock**
  - 96MHz by setting divider
- **96MIPS CPU performance at CPU 96MHz**
- **Memory**
  - ROM size: 64K*16 bits
  - PRAM / WRAM size: share with M0
- **1 Interrupt Sources**
  - 1 for M0 signal
- **Share IO**

OID Decoder

- **Support dot pattern format : OID_Code_v3**
- **The OID3 provides up to 268M indexes for general code used**
- **OID sensor interface**
- **Light source timing control**

PPU

- **Sprite RAM: 1K * 16**
- **Palette RAM: 256 for Text1, 256 for Text2 and 256 for sprite**
- **Address capability: up to 96K*16**
- **Picture resolution: 640 x 480 pixels (VGA)**
- **2 layers of text screen (background) and 256 sprites available**
- **Support maximum 65536 colors**
- **Programmable 4,16, 64, 256 and 65536 color modes**
- **Text**
  - 4 / 16 / 256 / 65536 colors
  - Horizontal/Vertical scrolling function
  - Vertical compression/extension function
  - 512(H)x256(V) and 1024(H)x512(V) pixels for normal display
  - Character Size (H): 8 / 16 / 32 / 64 pixels
  - Character Size (V): 8 / 16 / 32 / 64 pixels
  - Character mapped or Pixel bitmap
- **Sprite**
  - 4 / 16 / 256 colors

- Each Sprite is consisted of 1 character
- Locatable anywhere on the screen
- Max. 40 sprites (8 x 8 pixels) per line
- Scaling and Rotation
- Size (H): 8 / 16 / 32 / 64 / 128 / 256 pixels
- Size (V): 8 / 16 / 32 / 64 / 128 / 256 pixels
- Horizontal / Vertical Flip function for normal display and scaling display

◆ **Color special effect**
- Brightness Adjustment (16-level)

Peripherals and on-chip resources

◆ **Working voltage 2.7V ~ 3.6V**

◆ **I/O Pins:**
- 72 I/O pins (P0.0~P0.15, P1.0~P1.15, P2.0~P2.15, P3.0~P3.15, P4.0~P4.7)

◆ **16-Bits Sigma Delta ADC**
- With AGC + HPF + LPF function
- SNR 96dB
- MIC interface, max gain 67dB

◆ **24-bit Sigma Delta Stereo DAC**
- Can drive the L/R Channel Earphone.
- SNR 90dB
- Build-in audio amplifier

◆ **UART*2 interface provided**

◆ **Timer**
- Two 16-bit and two 32-bit general purpose timers/counters with a total of four capture inputs and 8 PWMs.

◆ **Programmable Watch Dog Timer (WDT)**
- Programmable watchdog frequency with watchdog clock source select and divider.

◆ **SPI (Serial Peripheral Interface)**
- Support 1/2/4 bit mode
- Maximum 48MHz Clock frequency
- Support run program on SPI Flash

◆ **SSP*2**
- Compatible with Motorola SPI, and 4-wire TI SSI bus.
- Synchronous Serial Communication. Salve mode work at 12MHz; Master mode work at 24MHz

◆ **MSP**
- Master/Slave mode
- Support general call address

◆ **I2S Interface**
- Master/Slave mode
- Supports Left/Right justified format

◆ **10-bit SAR ADC**
- 6 input channel (AIN0 ~ AIN5)
- Input Range 0V~3.3V(VDDA)
- No missing code : 8 bit

◆ **SLC NAND/XtraROM controller**
- 8 bit ECC provided

◆ **SD/MMC controller*2**
- Support SD Card1.0/2.0 commands
- Support 1-bit / 4-bit / SPI mode
- Support SDIO mode

◆ **USB 2.0 High Speed device**
- Supports Storage and HID Class
- Supports Control/Bulk/Interrupt interface

◆ **USB 2.0 High Speed EHCI host**
- Supports USB WiFi dongle
- Supports Control/Bulk interface

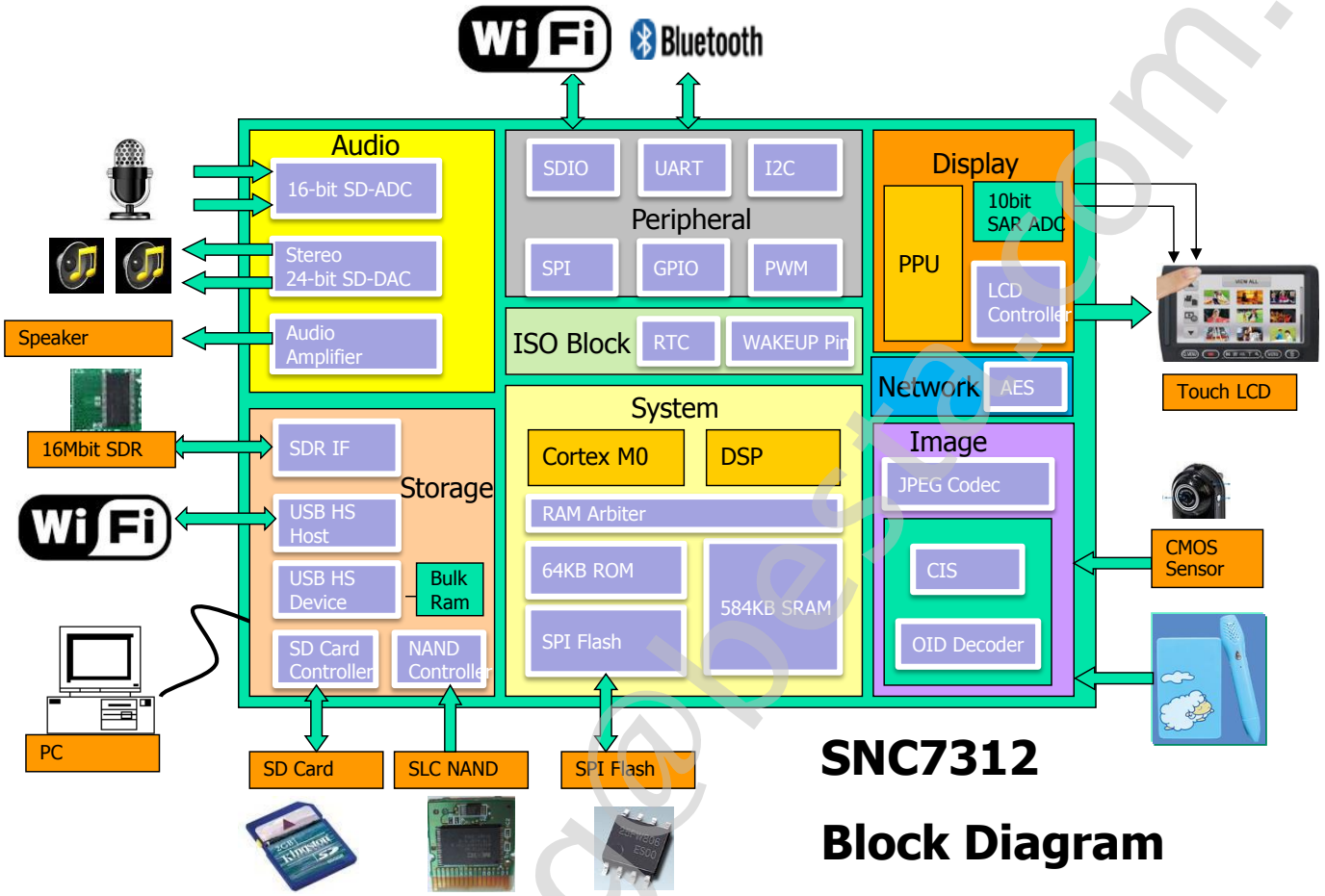
◆ **CMOS Image Sensor (CIS) Hardware**
- Supports 2M/VGA/CIF/QVGA/QCIF/QQVGA resolution (up to 30 frame/s at VGA resolution)
- Supports Scaling and Windowing

◆ **Hardware JPEG 422/420 codec (up to 30 frame/s at VGA resolution)**

◆ **CSTN/TFT LCD Interface**
- 8080 8/16Bit MCU-IF
- UPS051(8-bit serial RGB)
- UPS052(8-bit serial dummy RGB)
- 16/18-bit parallel mode

◆ **SDRAM Interface**
- Support 16Mb SDRAM

1.3 Block Diagram



2 Parts Information List and Pin Configuration

2.1 Part Number Description

SNC7312 Series Part Number description:

Body	Version	Code	Package Type	Description
SNC73121	B	1	FG	All Pin Only support version B
SNC73122	B	1	FG	All Pin and SiP 16MbSDR Pin assignment is the same with SNC73121 Only support version B
SNC73123	B	1	JG	WiFi CAM Only
SNC73124	B	1	JG	SiP 16Mb SDR WiFi CAM with SDCard Recording Pin assignment is the same with SNC73123
SNC73125	B	1	JG	SiP 4Mb SPI Flash WiFi CAM with smaller PCB
SNC73126	B	1	JG	SiP 4Mb SPI Flash All-in-one quad-copter

2.2 Part Number & Feature Selection Table

SNC7312 Series Peripherals:

Part Number	Pkt Type	IO	USB	TFT	CIS	SD Card	24-bit DAC	16-bit ADC	SAR-ADC	Audio AMP
SNC73121 B1FG	LQFP-128	72	Host/ Device	8/16-bit Mode	O	X2	O	O	6-CH	O
SNC73122 B1FG	LQFP-128	72	Host/ Device	8/16-bit Mode	O	X2	O	O	6-CH	O
SNC73123 B1FG	QFN68	40	Host	(*1)8-bit mode	O	X1	-	-	6-CH	-
SNC73124 B1JG	QFN68	40	Host	(*1)8-bit mode	O	X1	-	-	6-CH	-
SNC73125 B1JG	QFN48	31	Host	(*1)8-bit mode	O	X1	-	-	1-CH	-
SNC73126 B1JG	QFN68	41	Host	(*1)8-bit mode	O	X1	-	-	6-CH	-

Part Number	NAND	PWM IO	UART	SPI	I2C	I2S	OID	SIP 16Mb SDRAM	SIP 4Mb SPIFlash
SNC73121 B1FG	X1	X8	X2	X2	X1	(*2)X3	(*1)X1	-	-
SNC73122 B1FG	X1	X8	X2	X2	X1	(*2)X3	(*1)X1	O	-
SNC73123 B1JG	-	X4	X2	-	X1	(*2)X1	-	-	-
SNC73124 B1JG	-	X4	X2	-	X1	(*2)X1	-	O	-
SNC73125 B1JG	-	X2	X1	-	X1	(*2)X1	-	-	O
SNC73126 B1JG	-	X8	X2	X2	X1	(*2)X1	-		O

(*1) Share with CIS

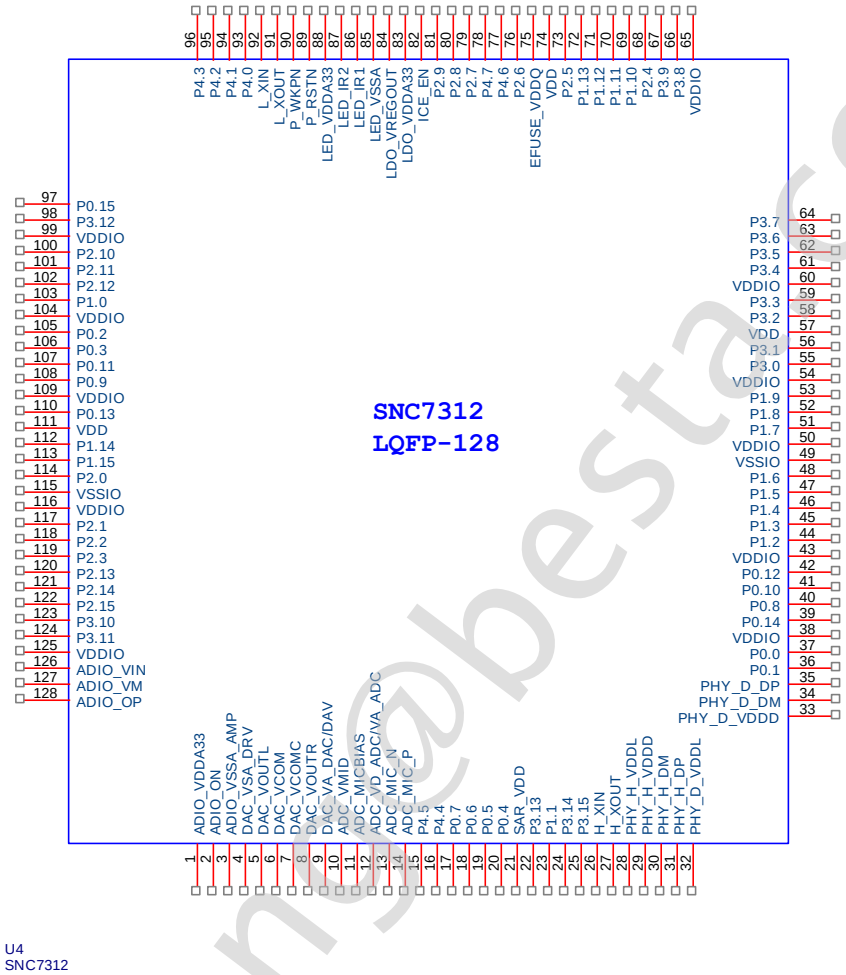
(*2) Share with SDCard1 and TFT

2.3 IC Version History

Function	A version	B version
P4.0/P4.1	Not support PWM	Support PWM CT16B0_PWMIO1/ CT16B1_PWMIO1
SAR-ADC	8-bit resolution	10-bit resolution
SDIO Byte mode/ Interrupt mode	Not support	Support
DSP access ram range	0x2000_0000~0x2003_0000	0x2000_0000~0x2007_2000
DSP timer interrupt	Not support	Support timer CT320

2.4 Pin Information

2.4.1 SNC73121/SNC73122 LQFP-128 Diagram



2.4.2 SNC73121/ SNC73122 Pin Assignment

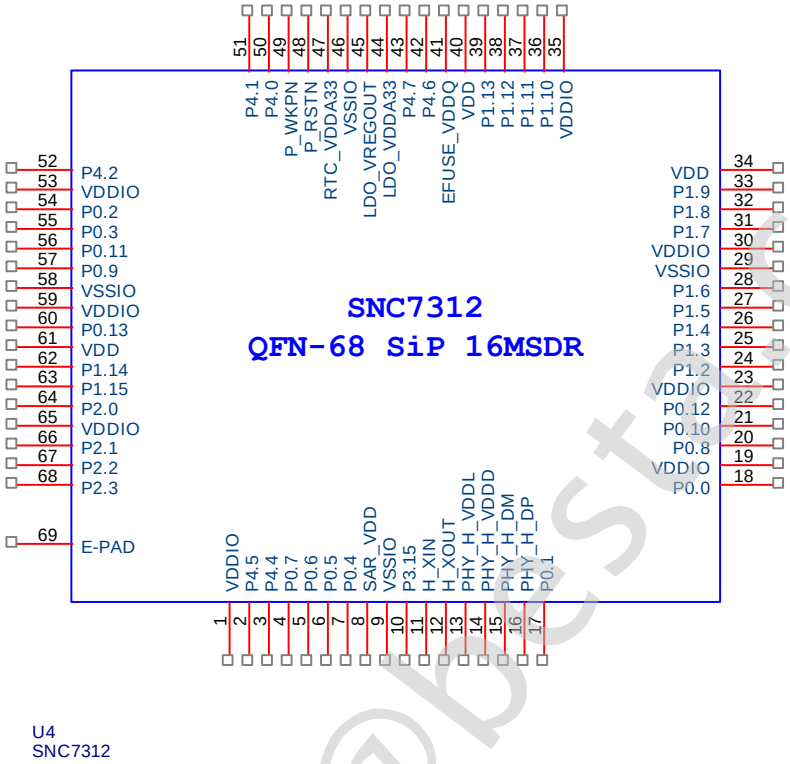
Pin No.	Symbol	I/O	Descriptions
1	ADIO_VDDA33	P	Audio amplifier positive power supply
2	ADIO_ON	O	Audio amplifier audio output
3	ADIO_VSSA_AMP	P	Audio amplifier negative power supply
4	DAC_VSA_DRV	P	DAC Drv negative power supply
5	DAC_VOUTL	O	DAC L-channel output
6	DAC_VCOM	I	DAC VCOM reference power
7	DAC_VCOMC	I	DAC VCOMC reference power
8	DAC_VOUTR	O	DAC R-channel output
9	DAC_VDDA33	P	DAC power supply
10	ADC_VMID	I	ADC VMID reference power
11	ADC_MICBIAS	O	ADC MIC reference power
12	ADC_VDDA33	P	ADC power supply
13	ADC_MIC_N	I	ADC MIC differential input
14	ADC_MIC_P	I	ADC MIC differential input
15	P4.5	IO	SAR ADC Channel 5 & GPIO4 Pin5
16	P4.4	IO	SAR ADC Channel 4 GPIO4 Pin4
17	P0.7	IO	SAR ADC Channel 3 GPIO0 Pin7
18	P0.6	IO	SAR ADC Channel 2 GPIO0 Pin6
19	P0.5	IO	SAR ADC Channel 1 GPIO0 Pin5
20	P0.4	IO	SAR ADC Channel 0 GPIO0 Pin4
21	SAR_VDDA33	P	SAR ADC power supply
22	P3.13	IO	GPIO3 Pin13
23	P1.1	IO	GPIO1 Pin1
24	P3.14	IO	GPIO3 Pin14
25	P3.15	IO	GPIO3 Pin15
26	H_XIN	I	12MHz Xtal in
27	H_OUT	O	12MHz Xtal out
28	PHY_H_VDDL	P	USB Host core power supply
29	PHY_H_VDDA33	P	USB Host 3.3V power supply
30	PHY_H_DM	IO	USB Host D-
31	PHY_H_DP	IO	USB Host D+
32	PHY_D_VDDL	P	USB Device core power supply
33	PHY_D_VDDD	P	USB Device 3.3V power supply
34	PHY_D_DM	IO	USB Device D-

35	PHY_D_DP	IO	USB Device D+
36	P0.1	IO	GPIO0 Pin1
37	P0.0	IO	GPIO0 Pin0
38	VDDIO	P	IO Positive power supply
39	P0.14	IO	GPIO0 Pin14
40	P0.8	IO	GPIO0 Pin8
41	P0.10	IO	GPIO0 Pin10
42	P0.12	IO	GPIO0 Pin12
43	VDDIO	P	IO Positive power supply
44	P1.2	IO	GPIO1 Pin2
45	P1.3	IO	GPIO1 Pin3
46	P1.4	IO	GPIO1 Pin4
47	P1.5	IO	GPIO1 Pin5
48	P1.6	IO	GPIO1 Pin6
49	VSSIO	P	IO Negative power supply
50	VDDIO	P	IO Positive power supply
51	P1.7	IO	GPIO1 Pin7
52	P1.8	IO	GPIO1 Pin8
53	P1.9	IO	GPIO1 Pin9
54	VDDIO	P	IO Positive power supply
55	P3.0	IO	GPIO3 Pin0
56	P3.1	IO	GPIO3 Pin1
57	VDD	P	Core Positive power supply
58	P3.2	IO	GPIO3 Pin2
59	P3.3	IO	GPIO3 Pin3
60	VDDIO	P	IO Positive power supply
61	P3.4	IO	GPIO3 Pin4
62	P3.5	IO	GPIO3 Pin5
63	P3.6	IO	GPIO3 Pin6
64	P3.7	IO	GPIO3 Pin7
65	VDDIO	P	IO Positive power supply
66	P3.8	IO	GPIO3 Pin8
67	P3.9	IO	GPIO3 Pin9
68	P2.4	IO	GPIO2 Pin4
69	P1.10	IO	GPIO1 Pin10
70	P1.11	IO	GPIO1 Pin11

71	P1.12	IO	GPIO1 Pin12
72	P1.13	IO	GPIO1 Pin13
73	P2.5	IO	GPIO2 Pin5
74	VDD	P	Core Positive power supply
75	EFUSE_VDDQ	I	Efuse input, should connect to ground
76	P2.6	IO	GPIO2 Pin6
77	P4.6	IO	GPIO4 Pin6
78	P4.7	IO	GPIO4 Pin7
79	P2.7	IO	GPIO2 Pin7
80	P2.8	IO	GPIO2 Pin8
81	P2.9	IO	GPIO2 Pin9
82	ICE_EN	I	DSP ICE enable pin
83	LDO_VDDA33	I	LDO 3.3V intput
84	LDO_VREGOUT	O	LDO core power output
85	LED_VSSA	P	OID LED ground
86	LED_IR1	O	OID LED driver1
87	LED_IR2	O	OID LED driver2
88	LED_VDDA33	P	OID LED power
89	P_RSTN	I	RESET pin
90	P_WKPN	I	Deep power down Wakeup pin
91	L_OUT	P	32768 xtal output
92	L_XIN	IO	32768 xtal input
93	P4.0	IO	GPIO4 Pin0
94	P4.1	IO	GPIO4 Pin1
95	P4.2	IO	GPIO4 Pin2
96	P4.3	IO	GPIO4 Pin3
97	P0.15	IO	GPIO0 Pin15
98	P3.12	IO	GPIO3 Pin12
99	VDDIO	P	IO Positive power supply
100	P2.10	IO	GPIO2 Pin10
101	P2.11	IO	GPIO2 Pin11
102	P2.12	IO	GPIO2 Pin12
103	P1.0	IO	GPIO1 Pin0
104	VDDIO	P	IO Positive power supply
105	P0.2	IO	GPIO0 Pin2
106	P0.3	IO	GPIO0 Pin3

107	P0.11	IO	GPIO0 Pin11
108	P0.9	IO	GPIO0 Pin9
109	VDDIO	P	IO Positive power supply
110	P0.13	IO	GPIO0 Pin13
111	VDD	P	IO Core power supply
112	P1.14	IO	GPIO1 Pin14
113	P1.15	IO	GPIO1 Pin15
114	P2.0	IO	GPIO2 Pin0
115	VSSIO	P	IO Negative power supply
116	VDDIO	P	IO Positive power supply
117	P2.1	IO	GPIO2 Pin1
118	P2.2	IO	GPIO2 Pin2
119	P2.3	IO	GPIO2 Pin3
120	P2.13	IO	GPIO2 Pin13
121	P2.14	IO	GPIO2 Pin14
122	P2.15	IO	GPIO2 Pin15
123	P3.10	IO	GPIO3 Pin10
124	P3.11	IO	GPIO3 Pin11
125	VDDIO	P	IO Positive power supply
126	ADIO_VIN	I	Audio amplifier audio input
127	ADIO_VM	I	Audio amplifier voltage reference
128	ADIO_OP	O	Audio amplifier audio output

2.4.3 SNC73123/SNC73124 QFN68 Diagram



*There is E-Pad in QFN68 package, please check chpater7-Package outline information

*Notice that the E-PAD needs to connect to PCB Ground Layer.

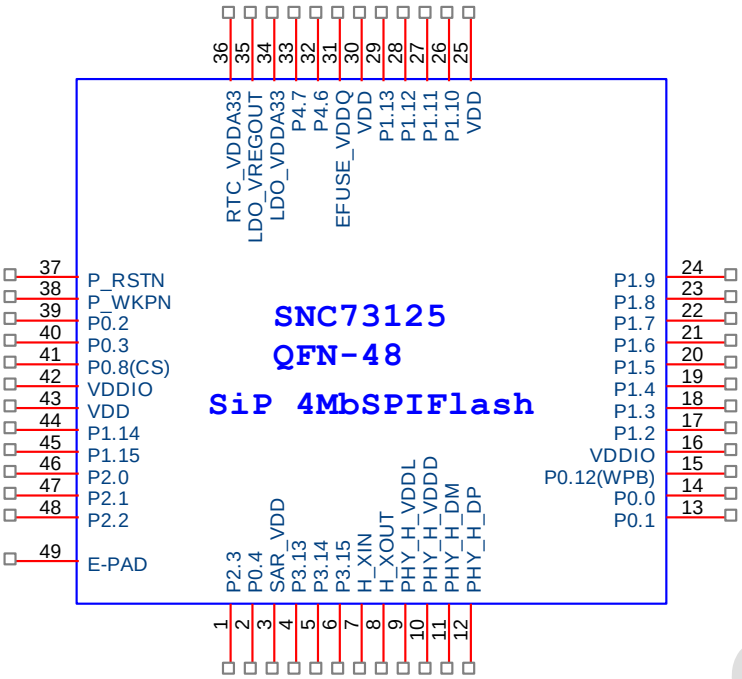
2.4.4 SNC73123/SNC73124 Pin Assignment

Pin No.	Symbol	I/O	Descriptions
1	VDDIO	P	IO Positive power supply
2	P4.5	IO	SAR ADC Channel 5 & GPIO4 Pin5
3	P4.4	IO	SAR ADC Channel 4 GPIO4 Pin4
4	P0.7	IO	SAR ADC Channel 3 GPIO0 Pin7
5	P0.6	IO	SAR ADC Channel 2 GPIO0 Pin6
6	P0.5	IO	SAR ADC Channel 1 GPIO0 Pin5
7	P0.4	IO	SAR ADC Channel 0 GPIO0 Pin4
8	SAR_VDDA33	P	SAR ADC power supply
9	VSSIO	P	IO Negative power supply
10	P3.15	IO	GPIO3 Pin15
11	H_XIN	I	12MHz Xtal in
12	H_OUT	O	12MHz Xtal out
13	PHY_H_VDDL	P	USB Host core power supply
14	PHY_H_VDDA33	P	USB Host 3.3V power supply
15	PHY_H_DM	IO	USB Host D-
16	PHY_H_DP	IO	USB Host D+
17	P0.1	IO	GPIO0 Pin1
18	P0.0	IO	GPIO0 Pin0
19	VDDIO	P	IO Positive power supply
20	P0.8	IO	GPIO0 Pin8
21	P0.10	IO	GPIO0 Pin10
22	P0.12	IO	GPIO0 Pin12
23	VDDIO	P	IO Positive power supply
24	P1.2	IO	GPIO1 Pin2
25	P1.3	IO	GPIO1 Pin3
26	P1.4	IO	GPIO1 Pin4
27	P1.5	IO	GPIO1 Pin5
28	P1.6	IO	GPIO1 Pin6
29	VSSIO	P	IO Negative power supply
30	VDDIO	P	IO Positive power supply
31	P1.7	IO	GPIO1 Pin7
32	P1.8	IO	GPIO1 Pin8
33	P1.9	IO	GPIO1 Pin9
34	VDD	P	Core Positive power supply

35	VDDIO	P	IO Positive power supply
36	P1.10	IO	GPIO1 Pin10
37	P1.11	IO	GPIO1 Pin11
38	P1.12	IO	GPIO1 Pin12
39	P1.13	IO	GPIO1 Pin13
40	VDD	P	Core Positive power supply
41	EFUSE_VDDQ	I	Efuse input, should connect to ground
42	P4.6	IO	GPIO4 Pin6
43	P4.7	IO	GPIO4 Pin7
44	LDO_VDDA33	I	LDO 3.3V intput
45	LDO_VREGOUT	O	LDO core power output
46	VSSIO	P	IO Negative power supply
47	RTC_VDDA33	P	IO & RTC Positive power supply
48	P_RSTN	I	RESET pin
49	P_WKPN	I	Deep power down Wakeup pin
50	P4.0	IO	GPIO4 Pin0
51	P4.1	IO	GPIO4 Pin1
52	P4.2	IO	GPIO4 Pin2
53	VDDIO	P	IO Positive power supply
54	P0.2	IO	GPIO0 Pin2
55	P0.3	IO	GPIO0 Pin3
56	P0.11	IO	GPIO0 Pin11
57	P0.9	IO	GPIO0 Pin9
58	VSSIO	P	IO Negative power supply
59	VDDIO	P	IO Positive power supply
60	P0.13	IO	GPIO0 Pin13
61	VDD	P	IO Core power supply
62	P1.14	IO	GPIO1 Pin14
63	P1.15	IO	GPIO1 Pin15
64	P2.0	IO	GPIO2 Pin0
65	VDDIO	P	IO Positive power supply
66	P2.1	IO	GPIO2 Pin1
67	P2.2	IO	GPIO2 Pin2
68	P2.3	IO	GPIO2 Pin3

69	E-PAD	P	Package E-Pad, should connect to Ground in PCB.

2.4.5 SNC73125 QFN48 Diagram



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SNC7312

*There is E-Pad in QFN68 package, please check chpater7-Package outline information

*Notice that the E-PAD needs to connect to PCB Ground Layer.

2.4.6 SNC73125 Pin Assignment

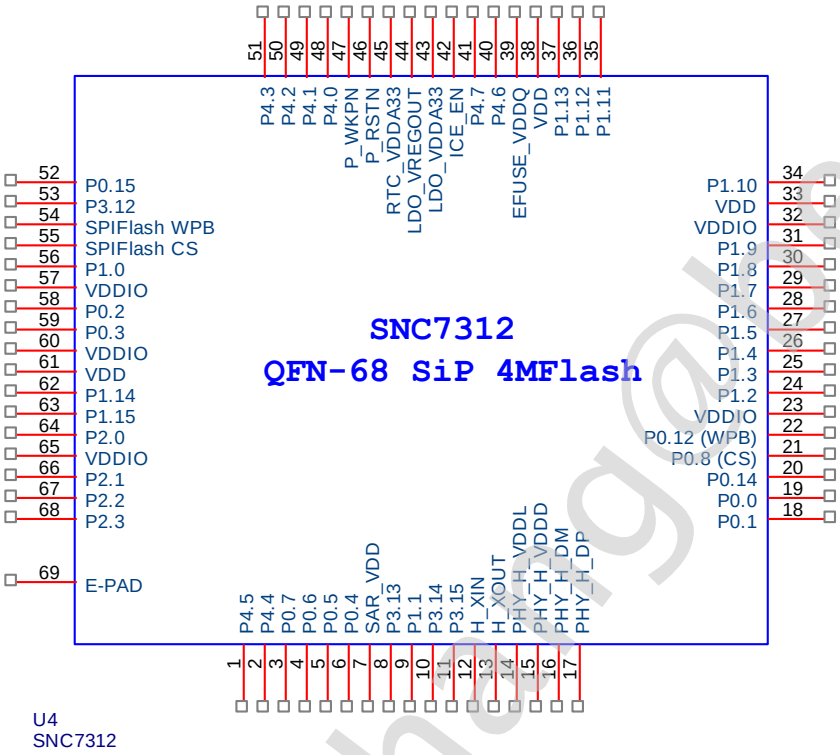
Pin No.	Symbol	I/O	Descriptions
1	P2.3	IO	GPIO2 Pin3
2	P0.4	IO	SAR ADC Channel 0 GPIO0 Pin4
3	SAR_VDDA33	P	SAR ADC power supply
4	P3.13	IO	GPIO3 Pin13
5	P3.14	IO	GPIO3 Pin14
6	P3.15	IO	GPIO3 Pin15
7	H_XIN	I	12MHz Xtal in
8	H_OUT	O	12MHz Xtal out
9	PHY_H_VDDL	P	USB Host core power supply

10	PHY_H_VDDA33	P	USB Host 3.3V power supply
11	PHY_H_DM	IO	USB Host D-
12	PHY_H_DP	IO	USB Host D+
13	P0.1	IO	GPIO0 Pin1
14	P0.0	IO	GPIO0 Pin0
15	P0.12	IO	GPIO0 Pin12 & Flash WPB Pin
16	VDDIO	P	IO Positive power supply
17	P1.2	IO	GPIO1 Pin2
18	P1.3	IO	GPIO1 Pin3
19	P1.4	IO	GPIO1 Pin4
20	P1.5	IO	GPIO1 Pin5
21	P1.6	IO	GPIO1 Pin6
22	P1.7	IO	GPIO1 Pin7
23	P1.8	IO	GPIO1 Pin8
24	P1.9	IO	GPIO1 Pin9
25	VDD	P	Core Positive power supply
26	P1.10	IO	GPIO1 Pin10
27	P1.11	IO	GPIO1 Pin11
28	P1.12	IO	GPIO1 Pin12
29	P1.13	IO	GPIO1 Pin13
30	VDD	P	Core Positive power supply
31	EFUSE_VDDQ	I	Efuse input, should connect to ground
32	P4.6	IO	GPIO4 Pin6
33	P4.7	IO	GPIO4 Pin7
34	LDO_VDDA33	I	LDO 3.3V input
35	LDO_VREGOUT	O	LDO core power output
36	RTC_VDDA33	P	IO & RTC Positive power supply
37	P_RSTN	I	RESET pin
38	P_WKPN	I	Deep power down Wakeup pin
39	P0.2	IO	GPIO0 Pin2
40	P0.3	IO	GPIO0 Pin3
41	P0.8	IO	GPIO0 Pin8 & Flash CS Pin
42	VDDIO	P	IO Positive power supply
43	VDD	P	IO Core power supply
44	P1.14	IO	GPIO1 Pin14
45	P1.15	IO	GPIO1 Pin15

46	P2.0	IO	GPIO2 Pin0
47	P2.1	IO	GPIO2 Pin1
48	P2.2	IO	GPIO2 Pin2

49	E-PAD	P	Package E-Pad, should connect to Ground in PCB.

2.4.7 SNC73126 QFN68 Diagram



*Pin21 should connect to Pin55

*Pin22 should connect to Pin54

*There is E-Pad in QFN68 package, please check chpater7-Package outline information

*Notice that the E-PAD needs to connect to PCB Ground Layer.

2.4.8 SNC73126 Pin Assignment

Pin No.	Symbol	I/O	Descriptions
1	P4.5	IO	SAR ADC Channel 5 GPIO4 Pin5
2	P4.4	IO	SAR ADC Channel 4 GPIO4 Pin4
3	P0.7	IO	SAR ADC Channel 3 GPIO0 Pin7
4	P0.6	IO	SAR ADC Channel 2 GPIO0 Pin6
5	P0.5	IO	SAR ADC Channel 1 GPIO0 Pin5
6	P0.4	IO	SAR ADC Channel 0 GPIO0 Pin4
7	SAR_VDDA33	P	SAR ADC power supply
8	P3.13	IO	GPIO3 Pin13
9	P1.1		GPIO1 Pin11
10	P3.14	IO	GPIO3 Pin14
11	P3.15	IO	GPIO3 Pin15
12	H_XIN	I	12MHz Xtal in
13	H_OUT	O	12MHz Xtal out
14	PHY_H_VDDL	P	USB Host core power supply
15	PHY_H_VDDA33	P	USB Host 3.3V power supply
16	PHY_H_DM	IO	USB Host D-
17	PHY_H_DP	IO	USB Host D+
18	P0.1	IO	GPIO0 Pin1
19	P0.0	IO	GPIO0 Pin0
20	P0.14	IO	GPIO0 Pin14
21	P0.8	IO	GPIO0 Pin8 & Flash CS Pin, should connect to Pin55
22	P0.12	IO	GPIO0 Pin12 & Flash WPB Pin, should connect to Pin54
23	VDDIO	P	IO Positive power supply
24	P1.2	IO	GPIO1 Pin2
25	P1.3	IO	GPIO1 Pin3
26	P1.4	IO	GPIO1 Pin4
27	P1.5	IO	GPIO1 Pin5
28	P1.6	IO	GPIO1 Pin6
29	P1.7	IO	GPIO1 Pin7
30	P1.8	IO	GPIO1 Pin8
31	P1.9	IO	GPIO1 Pin9
32	VDDIO	P	IO Positive power supply
33	VDD	P	Core Positive power supply
34	P1.10	IO	GPIO1 Pin10

35	P1.11	IO	GPIO1 Pin11
36	P1.12	IO	GPIO1 Pin12
37	P1.13	IO	GPIO1 Pin13
38	VDD	P	Core Positive power supply
39	EFUSE_VDDQ	I	Efuse input, should connect to ground
40	P4.6	IO	GPIO4 Pin6
41	P4.7	IO	GPIO4 Pin7
42	ICE_EN	I	DSP ICE debug enable pin
43	LDO_VDDA33	I	LDO 3.3V input
44	LDO_VREGOUT	O	LDO core power output
45	RTC_VDDA33	P	IO & RTC Positive power supply
46	P_RSTN	I	RESET pin
47	P_WKPN	I	Deep power down Wakeup pin
48	P4.0	IO	GPIO4 Pin0
49	P4.1	IO	GPIO4 Pin1
50	P4.2	IO	GPIO4 Pin2
51	P4.3	IO	GPIO4 Pin3
52	P0.15	IO	GPIO0 Pin15
53	P3.12	IO	GPIO3 Pin12
54	SPIFlash WPB	IO	SiP SPIFlash Pin, should connect to P0.12
55	SPIFlash CS	IO	SiP SPIFlash Pin, should connect to P0.8
56	P1.0	IO	GPIO1 Pin0
57	VDDIO	P	IO Positive power supply
58	P0.2	IO	GPIO0 Pin2
59	P0.3	IO	GPIO0 Pin3
60	VDDIO	P	IO Positive power supply
61	VDD	P	IO Core power supply
62	P1.14	IO	GPIO1 Pin14
63	P1.15	IO	GPIO1 Pin15
64	P2.0	IO	GPIO2 Pin0
65	VDDIO	P	IO Positive power supply
66	P2.1	IO	GPIO2 Pin1
67	P2.2	IO	GPIO2 Pin2
68	P2.3	IO	GPIO2 Pin3

69	E-PAD	P	Package E-Pad, should connect to Ground in PCB.

2.5 Multi-function IO

GPIO	Multi-function IO1	Multi-function IO2	Multi-function IO3	Multi-function IO4	Multi-function IO5	SNC 73121/ 73122	SNC 73123	SNC 73124	SNC 73125	SNC 73126
P0.0	I2C_CLK					●	●	●	●	●
P0.1	I2C_DAT					●	●	●	●	●
P0.2	UART0_Tx					●	●	●	●	●
P0.3	UART0_Rx					●	●	●	●	●
P0.4	SAR-AIN00					●	●	●	●	●
P0.5	SAR-AIN01					●	●	●		●
P0.6	SAR-AIN02					●	●	●		●
P0.7	SAR-AIN03					●	●	●		●
P0.8	SPICS1			*SPI0_CS		●	●	●	●	●
P0.9	SPISCK		*SD1_CMD	*SPI0_SCK		●	●	●		
P0.10	SPIMISO		*SD1_D0	*SPI0_MISO		●	●	●		
P0.11	SPIMOSI		*SD1_D1	*SPI0_MOSI		●	●	●		
P0.12	SPIED2	*UART0_Tx	*SD1_D2			●	●	●	●	●
P0.13	SPIED3	*UART0_Rx	*SD1_D3			●	●	●		
P0.14	HOST_PPC	CLKOUT		SPI0_CS		●				●
P0.15			NF_CS	SPI0_SCK		●				●
P1.0		CT16B0_ CAP0	NF_RB	SPI0 _MISO		●				●
P1.1		CT32B0_ CAP0	NF_ALE	SPI0 _MOSI		●				●
P1.2		CIS_VSYNC	NF_WE	OID_ SEN_D[0]	*HSYNC/ LCM_RE	●	●	●	●	●
P1.3		CIS_HSYNC	NF_RE	OID_ SEN_D[1]	*VSYNC/ LCM_WE	●	●	●	●	●
P1.4	SD0_CLK	CIS_MLCK	NF_WP	OID_ SEN_CLK	*DE/ LCM_CS	●	●	●	●	●
P1.5	SD0_CMD	CIS_PCLK	NF_CLE	OID_ SEN_CMD	*DCLK/ EA0	●	●	●	●	●
P1.6	SD0_D0	CIS_D0	NF_D0	OID_	*ED0	●	●	●	●	●

				GPIO[0]						
P1.7	SD0_D1	CIS_D1	NF_D1	OID_ GPIO[1]	*ED1	●	●	●	●	●
P1.8	SD0_D2	CIS_D2	NF_D2	OID_ GPIO[2]	*ED2	●	●	●	●	●
P1.9	SD0_D3	CIS_D3	NF_D3	OID_CLK	*ED3	●	●	●	●	●
P1.10		CIS_D4	NF_D4	OID_DAT	*ED4	●	●	●	●	●
P1.11		CIS_D5	NF_D5		*ED5	●	●	●	●	●
P1.12		CIS_D6	NF_D6		*ED6	●	●	●	●	●
P1.13		CIS_D7	NF_D7		*ED7	●	●	●	●	●
P1.14	SD1_CLK		I2S2-MCLK			●	●	●	●	●
P1.15	SD1_CMD		I2S2-SDIN			●	●	●	●	●
P2.0	SD1_D0		I2S2-SDOUT			●	●	●	●	●
P2.1	SD1_D1		I2S2-BCLK			●	●	●	●	●
P2.2	SD1_D2		I2S2-WS			●	●	●	●	●
P2.3	SD1_D3					●	●	●	●	●
P2.4	HSYNC	LCM_RE	I2S0-MCLK			●				
P2.5	VSYNC	LCM_WE	I2S0-SDIN			●				
P2.6	DE	LCM_CS	I2S0-SDOUT			●				
P2.7	DCLK	EA0	I2S0-BCLK			●				
P2.8	ED0	ED0	I2S0-WS			●				
P2.9	ED1	ED1	I2S1-MCLK			●				
P2.10	ED2	ED2	I2S1-SDIN			●				
P2.11	ED3	ED3	I2S1-SDOUT			●				
P2.12	ED4	ED4	I2S1-BCLK			●				
P2.13	ED5	ED5	I2S1-WS			●				
P2.14	ED6	ED6				●				
P2.15	ED7	ED7				●				
P3.0	ED8	ED8	*NF_CS			●				
P3.1	ED9	ED9	*NF_RB			●				
P3.2	ED10	ED10	*NF_ALE			●				
P3.3	ED11	ED11	*NF_WE			●				
P3.4	ED12	ED12	*NF_RE			●				
P3.5	ED13	ED13	*NF_WP	*SD0_CLK		●				
P3.6	ED14	ED14	*NF_CLE	*SD0_CMD		●				
P3.7	ED15	ED15	*NF_D0	*SD0_D0		●				

P3.8	ED16		*NF_D1	*SD0_D1		●				
P3.9	ED17		*NF_D2	*SD0_D2		●				
P3.10			*NF_D3	*SD_D3		●				
P3.11			*NF_D4			●				
P3.12	DSP_ ICE_SCK	CT16B0_ PWMIO0	*NF_D5	*OID_ SEN_D[0]		●				●
P3.13	DSP_ ICE_CSB	CT16B1_ PWMIO0	*NF_D6	*OID_ SEN_D[1]		●			●	●
P3.14	DSP_ ICE_MOSI	CT32B0_ PWMIO0	*NF_D7	*OID_ SEN_CLK		●			●	●
P3.15	DSP_ ICE_MISO	CT32B1_ PWMIO0		*OID_ SEN_CMD		●	●	●	●	●
P4.0	UART1_TxD	CT16B0_ PWMIO1	SPI1_CS	*OID_ GPIO[0]		●	●	●		●
P4.1	UART1_RxD	CT16B1_ PWMIO1	SPI1 _SCK	*OID_ GPIO[1]		●	●	●		●
P4.2		CT32B0_ PWMIO1	SPI1 _MISO	*OID_ GPIO[2]		●	●	●		●
P4.3		CT32B1_ PWMIO1	SPI1 _MOSI	*OID_CLK		●				●
P4.4	SAR-AIN4			*OID_DAT		●	●	●		●
P4.5	SAR-AIN5					●	●	●		●
P4.6	SWD_CLK	*CT16B0_ PWMIO0				●	●	●	●	●
P4.7	SWD_DAT	*CT16B1_ PWMIO0				●	●	●	●	●

Note: (*) means IO switch, there are some DIP function with IO switch function

1. *UART0*
2. *SDCard0 IF*
3. *SDCard1 IF*
4. *OID IF*
5. *NAND Flash IF*
6. *8-bit TFT/8080 IF*
7. *PWM16B0_PWMIO0 & PWM16B1_PWMIO0*
8. *SPI0*

The register can be referred to chapter 4.3: Pin Control Register in SNC7312 Register Table.pdf

3 Functional Description

3.1 Memory

SNC7312 provides some private libraries for user to save more memory size, such as USB library, FAT system…and so on. There are total 64KB in internal ROM. For Cortex M0, there is one PRAM, 64KB sizes, dedicatedly for CPU program. Besides, SNC7312 owns a large internal memory, totally 456KB sizes, shares with all peripheral and CPU. For some part number, such as SNC73122 and SNC73124, there is internal 2MB SDR inside the chip.

Another CPU, 16-bit DSP, there is one dedicated ROM for DSP program. DSP ROM provides hi-compression algorithm, such as MP3, for audio application in SNC7312.

More detail memory map is as below table:

Internal RAM Address Range	Size	Usage	M0	DSP	PPU	GDMA	Peripheral DMA
0x00000000 ~ 0x0000FFFF	64KB	ROM	***R***	**--**	**--**	--	--
0x10000000 ~ 0x1000FFFF	64KB	Program RAM	***R***				
0x20000000 ~ 0x20000FFF	4KB	Global RAM	***R/W***	***R/W***	***R***	R/W	R/W
0x20001000 ~ 0x20001FFF	4KB	Global RAM	***R/W***	***R/W***	***R***	R/W	R/W
0x20002000 ~ 0x20011FFF	64KB	Global RAM	***R/W***	***R/W***	***R***	R/W	R/W
0x20012000 ~ 0x20021FFF	64KB	Global RAM	***R/W***	***R/W***	***R***	R/W	R/W
0x20022000 ~ 0x20029FFF	32KB	Global RAM	***R/W***	***R/W***	***R***	R/W	R/W
0x2002A000 ~ 0x20031FFF	32KB	Global RAM	***R/W***	***R/W***	***R***	R/W	R/W
0x20032000 ~ 0x20071FFF	256KB	Global RAM	***R/W***	***R/W***	***R***	R/W	R/W
0x20080000 ~ 0x2027FFFF (Only exist in SNC73122 & SNC73124)	2MB	SDRAM	***R/W***		***R***		
0x00000~ 0x10000	64KW	ROM		R			
External SPIFlash Address Range	**Size**	**Usage**	**M0**	**DSP**	**PPU**	**GDMA**	**Peripheral DMA**
0x60000000~ 0x61000000	16MB	SPIFlash	R	--	--	R	R

3.2 System Manager

3.2.1 System Reset

A system reset is generated when one of the following events occurs:

- Power-on reset
  - 0.7V core power LVR trigger
  - Reset Pin trigger
  - When reset releases,re-start from ROM
- LVR reset
  - 0.7V core power LVR trigger
  - 2.1V IO power LVR trigger
  - When reset releases,re-start from ROM
- RST pin (external reset)
  - 1/2 * IO power trigger
  - When reset releases,re-start from ROM
- DPDWAKEUP reset
  - When wakeup from DPD mode, system will reset and re-start from ROM
- Watchdog Timer reset (WDT reset)
  - Reset and re-start from ROM
- Software reset (SW reset)
  - Reset and re-start from PRAM

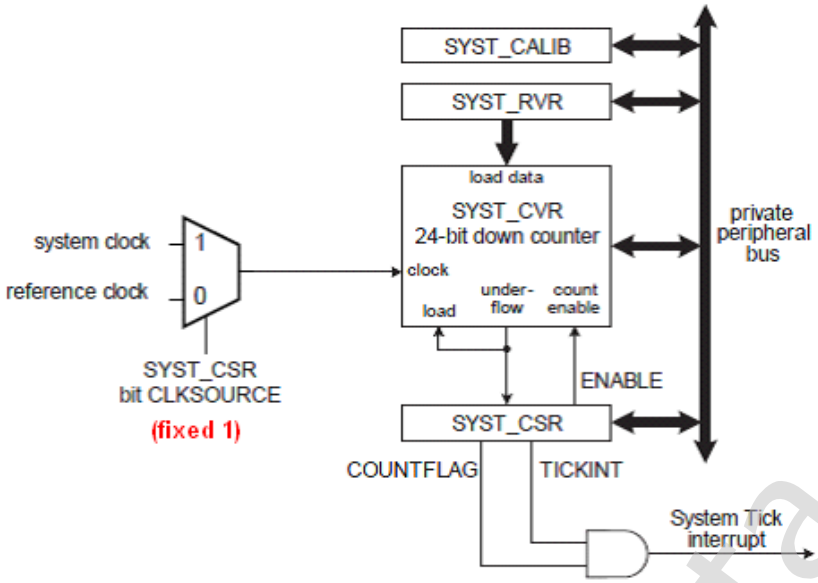
Note: The register can be referred to chapter 4.6: System Reset Status Register in SNC7312 Register Table.pdf

3.2.2 System Tick Timer (SysTick)

The SysTick timer is an integral part of the Cortex-M0, and it is a 24-bit timer that counts down to zero and generates an interrupt. The SysTick timer is intended to generate a fixed 10-ms interrupt for use by an operating system or other system management software. Since the SysTick timer is a part of the Cortex-M0, it facilitates porting of software by providing a standard timer that is available on Cortex-M0 based devices.

The system tick timer is enabled through the SysTick control register. The system tick timer clock is fixed to half the frequency of the system clock.

Here is the block diagram of the SysTick timer:



Note: The register can be referred to chapter 6: Stick Registers in SNC7312 Register Table.pdf

3.2.3 Nested vectored interrupt controller (NVIC)

All interrupts including the core exceptions are managed by the NVIC. NVIC has the following Features:

- The NVIC supports 32 vectored interrupts.
- 4 programmable interrupt priority levels with hardware priority level masking.
- Low-latency exception and interrupt handling.
- Efficient processing of late arriving interrupts.
- Implementation of System Control Registers
- Software interrupts generation.

Interrupt and Exception Vectors:

Execution No.	Priority	Function	Description	Address Offset
0	-	-	Reserved	0x0000 0000
1	-3	Reset	Reset	0x0000 0004
2	-2	NMI_Handler	Non maskable interrupt.	0x0000 0008
3	-1	HardFault_Handler	All class of fault	0x0000 000C
4~10	Reserved	Reserved	Reserved	-
11	Settable	SVCCalll		0x0000 002C
12~13	Reserved	Reserved	Reserved	-
14	Settable	PendSV		0x0000 0038
15	Settable	SysTick		0x0000 003C
16	Settable	IRQ0	Ram crash	0x0000 0040
17	Settable	IRQ1/	DSP Issue Interrupt	0x0000 0044
18	Settable	IRQ2/	USBDev	0x0000 0048
19	Settable	IRQ3/	CIS	0x0000 004C
20	Settable	IRQ4/	PPU HBLK	0x0000 0050
21	Settable	IRQ5/	SD-DAC I2S0	0x0000 0054
22	Settable	IRQ6/	SD-ADC I2S1	0x0000 0058
23	Settable	IRQ7/	DMA SD/NF_0	0x0000 005C
24	Settable	IRQ8/	SPI1	0x0000 0060
25	Settable	IRQ9/	I2S_2 (general)	0x0000 0064
26	Settable	IRQ10/	DMA CSC	0x0000 0068

27	Settable	IRQ11/	DMA JPEG	0x0000 006C
28	Settable	IRQ12/	CIS Vsync	0x0000 0070
29	Settable	IRQ13/	SPI0	0x0000 0074
30	Settable	IRQ14/	PPU VBLK	0x0000 0078
31	Settable	IRQ15/	I^2C	0x0000 007C
32	Settable	IRQ16/	CT16B0	0x0000 0080
33	Settable	IRQ17/	CT16B1	0x0000 0084
34	Settable	IRQ18/	CT32B0	0x0000 0088
35	Settable	IRQ19/	CT32B1	0x0000 008C
36	Settable	IRQ20/	GPIO interrupt status of port 4 / Key WKP	0x0000 0090
37	Settable	IRQ21/	UART0	0x0000 0094
38	Settable	IRQ22/	SD / NF_0_ECC / SDIO	0x0000 0098
39	Settable	IRQ23/	DMA SD/NF_0	0x0000 009C
40	Settable	IRQ24/	SAR ADC	0x0000 00A0
41	Settable	IRQ25/	WDT / UART1	0x0000 00A4
42	Settable	IRQ26/	USB EHCI Host	0x0000 00A8
43	Settable	IRQ27/	RTC	0x0000 00AC
44	Settable	IRQ28/	GPIO interrupt status of port 3	0x0000 00B0
45	Settable	IRQ29/	GPIO interrupt status of port 2	0x0000 00B4
46	Settable	IRQ30/	GPIO interrupt status of port 1	0x0000 00B8
47	Settable	IRQ31/	GPIO interrupt status of port 0	0x0000 00BC

Note: The register can be referred to chapter 3: NVIC Registers in SNC7312 Register Table.pdf

3.2.4 System Operation Mode

The chip builds in two operating mode for difference clock rate and power saving reason.

- Normal mode
- Deep Power-down mode
  - Wakeup from WAKEUP Pin
  - Wakeup from RTC

When system is entered Deep Power-down mode, all GPIO are return to default setting.(input floating mode)

Note1: When WAKEUP Pin is pressed, DPD mode cannot be entered. Program should detect WAKEUP release and return to high level and then enter DPD mode.

Note2: The register can be referred to chapter 2.3: Power Control Registers in SNC7312 Register Table.pdf

3.3 PPU Function

3.3.1 Overview

SNC7312 series support PPU function that will activate graphic processing and turn on TFT/8080 controller to display. PPU can support up to 2 layers of Text and 256 Sprites on one screen. However, the Text and Sprite can be controlled independently to display on screen.

3.3.2 Features

- Sprite RAM: 1K * 16
- Palette RAM: 256 for Text1, 256 for Text2 and 256 for sprite
- Address capability: up to 96K*16
- Picture resolution: 640 x 480 pixels (VGA)
- 2 layers of text screen (background) and 256 sprites available
- Support maximum 65536 colors
- Programmable 4,16, 64, 256 and 65536 color modes
- Text
    - 4 / 16 / 256 / 65536 colors
    - Horizontal/Vertical scrolling function
    - Vertical compression/extension function
    - 512(H)x256(V) and 1024(H)x512(V) pixels for normal display
    - Character Size (H): 8 / 16 / 32 / 64 pixels
    - Character Size (V): 8 / 16 / 32 / 64 pixels
    - Character mapped or Pixel bitmap
- Sprite
    - 4 / 16 / 256 colors
    - Each Sprite is consisted of 1 character
    - Locatable anywhere on the screen
    - Max. 40 sprites (8 x 8 pixels) per line
    - Scaling and Rotation
    - Size (H): 8 / 16 / 32 / 64 / 128 / 256 pixels
    - Size (V): 8 / 16 / 32 / 64 / 128 / 256 pixels
    - Horizontal / Vertical Flip function for normal display and scaling display
- Color special effect
    - Brightness Adjustment (16-level)

Note: The register can be referred to chapter 7: PPU Registers in SNC7312 Register Table.pdf

3.4 General Purpose I/O (GPIO)

3.4.1 Overview

Digital ports can be configured input/output by SW.

- Each individual port pin can serve as external interrupt input pin.
- Interrupts can be configured on single falling or rising edges and on both edges.
- Individual interrupt levels can be programmed.
- All GPIO pins are inputs and floating by default.
- All GPIO pins are different driving and sink current.
- Internal pull-up resistor or bus keeper function

3.4.2 GPIO Mode

The GPIO Mode bits in the GPIO_PnCFG (n=0,1,2,3,4) register allow the selection of on-chip pull-up resistors for each pin or select the repeater mode. The possible on-chip resistor configurations are pull-up enabled or no pull-up/pull-down (default).

The repeater mode enables the pull-up resistor if the pin is at logic HIGH and enables the pull-down resistor if the pin is at logic LOW. This causes the pin to retain its last known state if it is configured as an input and is not driven externally. The state retention is not applicable to the Deep power-down mode. Repeater mode may typically be used to prevent a pin from floating (and potentially using significant power if it floats to an indeterminate state) if it is temporarily not driven.

Note: The register can be referred to chapter 8: GPIO Registers in SNC7312 Register Table.pdf

3.5 16-Bit / 32-Bit Timer with Capture Function

3.5.1 Overview

Each Counter / timer is designed to count cycles of the peripheral clock (PCLK) or an externally supplied clock and can optionally generate interrupts or perform other actions at specified timer values based on four match registers. Each counter / timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, up to two match registers can be used to provide a single-edge controlled PWM output on the match output pins. It is recommended to use the match registers that are not pinned out to control the PWM cycle length.

3.5.2 Features

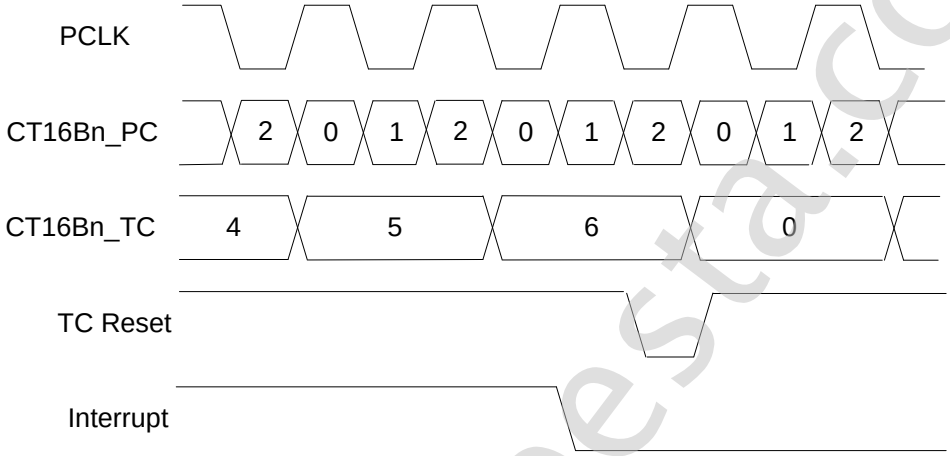
- Two 16-bit / 32-bit counter / timers with a programmable 16-bit / 32-bit pre-scalar.
- Counter or timer operation
- Two 16-bit / 32-bit capture channels that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- The timer and pre-scalar may be configured to be cleared on a designated capture event. This feature permits easy pulse-width measurement by clearing the timer on the leading edge of an input pulse and capturing the timer value on the trailing edge.
- Four 16-bit / 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Up to three (CT16B0) or two (CT16B1) PWM outputs corresponding to match registers with the following capabilities:
  - Set LOW on match.
  - Set HIGH on match.
  - Toggle on match.
  - Do nothing on match.
- For each timer, up to four match registers (MR0~MR3) can be configured as PWM allowing to use up to three match outputs as single edge controlled PWM outputs.

3.5.3 Pin Description

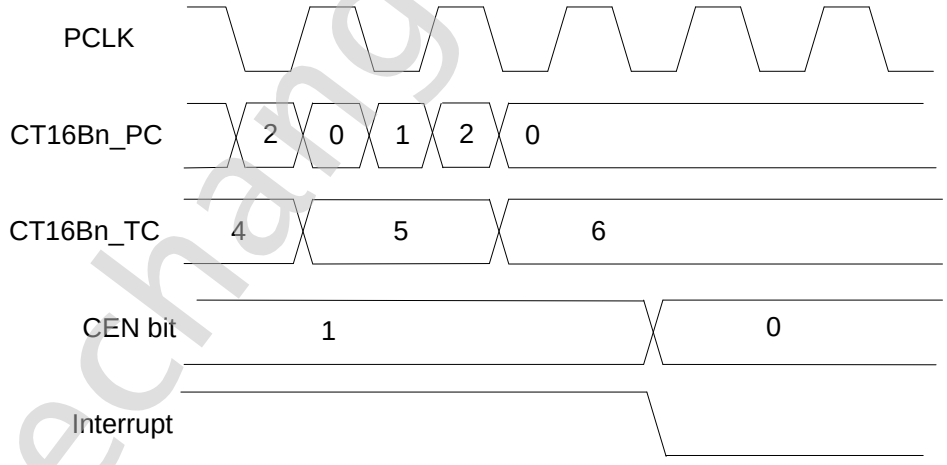
Pin Name	Type	Description	GPIO Configuration
CT16Bn_CAP0	I	Capture channel input 0	Depends on GPIOn_CFG
CT16Bn_PWM	O	Output channel of Match/PWM output.	
CT32Bn_CAP0	I	Capture channel input 0	Depends on GPIOn_CFG
CT32Bn_PWM	O	Output channel of Match/PWM output.	

3.5.4 Timer Operation

The following figure shows a timer configured to reset the count and generate an interrupt on match. The CT16Bn_PRE / CT32Bn_PRE register is set to 2, and the CT16Bn_MRx / CT32Bn_MRx register is set to 6. At the end of the timer cycle where the match occurs, the timer count is reset. This gives a full length cycle to the match value. The interrupt indicating that a match occurred is generated in the next clock after the timer reached the match value.



The following figure shows a timer configured to stop and generate an interrupt on match. The CT16Bn_PRE register is set to 2, and the CT16Bn_MRx register is set to 6. In the next clock after the timer reaches the match value, the CEN bit in CT16Bn_TMRCTRL register is cleared, and the interrupt indicating that a match occurred is generated.



Note: The register can be referred to chapter 9&10: CT16Bn&CT32Bn Registers in SNC7312 Register Table.pdf

3.5.5 PWM

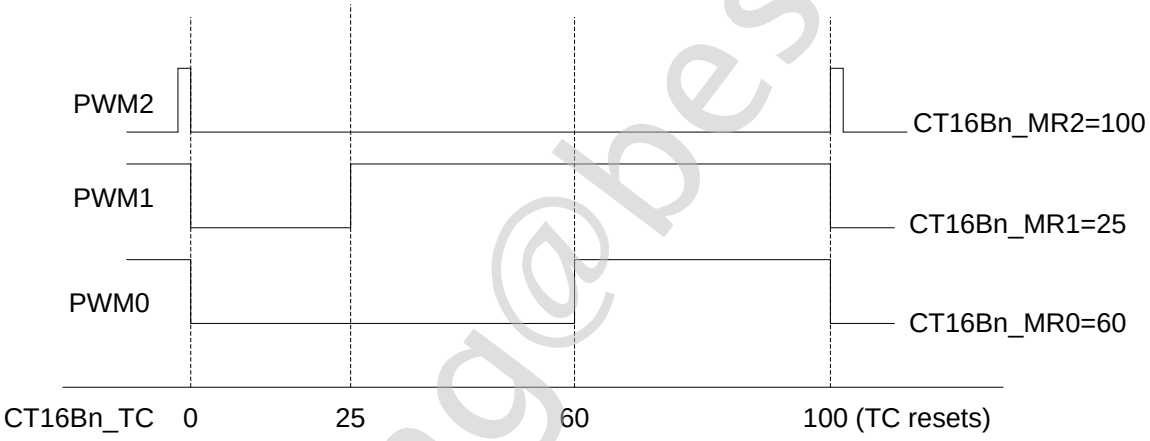
All single edge controlled PWM outputs go LOW at the beginning of each PWM cycle (timer is set to zero) unless their match value in CT16Bn_MR0~3 registers is equal to zero.

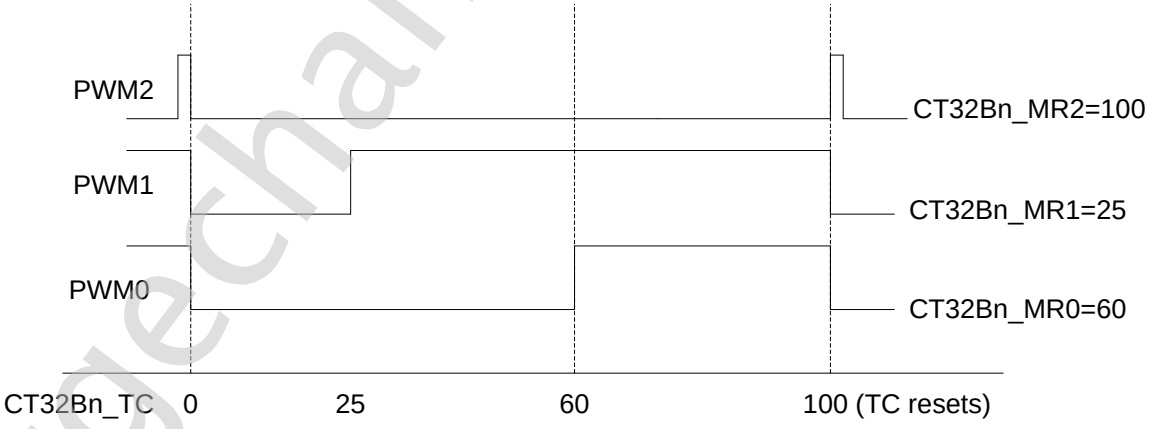
Each PWM output will go HIGH when its match value is reached. If no match occurs, the PWM output remains continuously LOW.

If a match value larger than the PWM cycle length is written to the CT16Bn_MR0~3 registers, and the PWM signal is HIGH already, then the PWM signal will be cleared on the next start of the next PWM cycle.

If a match register contains the same value as the timer reset value (the PWM cycle length), then the PWM output will be reset to LOW on the next clock tick. Therefore, the PWM output will always consist of a one clock tick wide positive pulse with a period determined by the PWM cycle length.

If a match register is set to zero, then the PWM output will go to HIGH the first time the timer goes back to zero and will stay HIGH continuously.





Note: When the match outputs are selected to perform as PWM outputs, the timer reset (MRnRST) and timer stop (MRnSTOP) bits in CT16Bn_MCTRL / CT32Bn_MCTRL register must be set to zero except for the match register setting the PWM cycle length. For this register, set the MRnR bit to one to enable the timer reset when the timer value matches the value of the corresponding match register.

3.6 Watch Dog Timer (WDT)

3.6.1 Overview

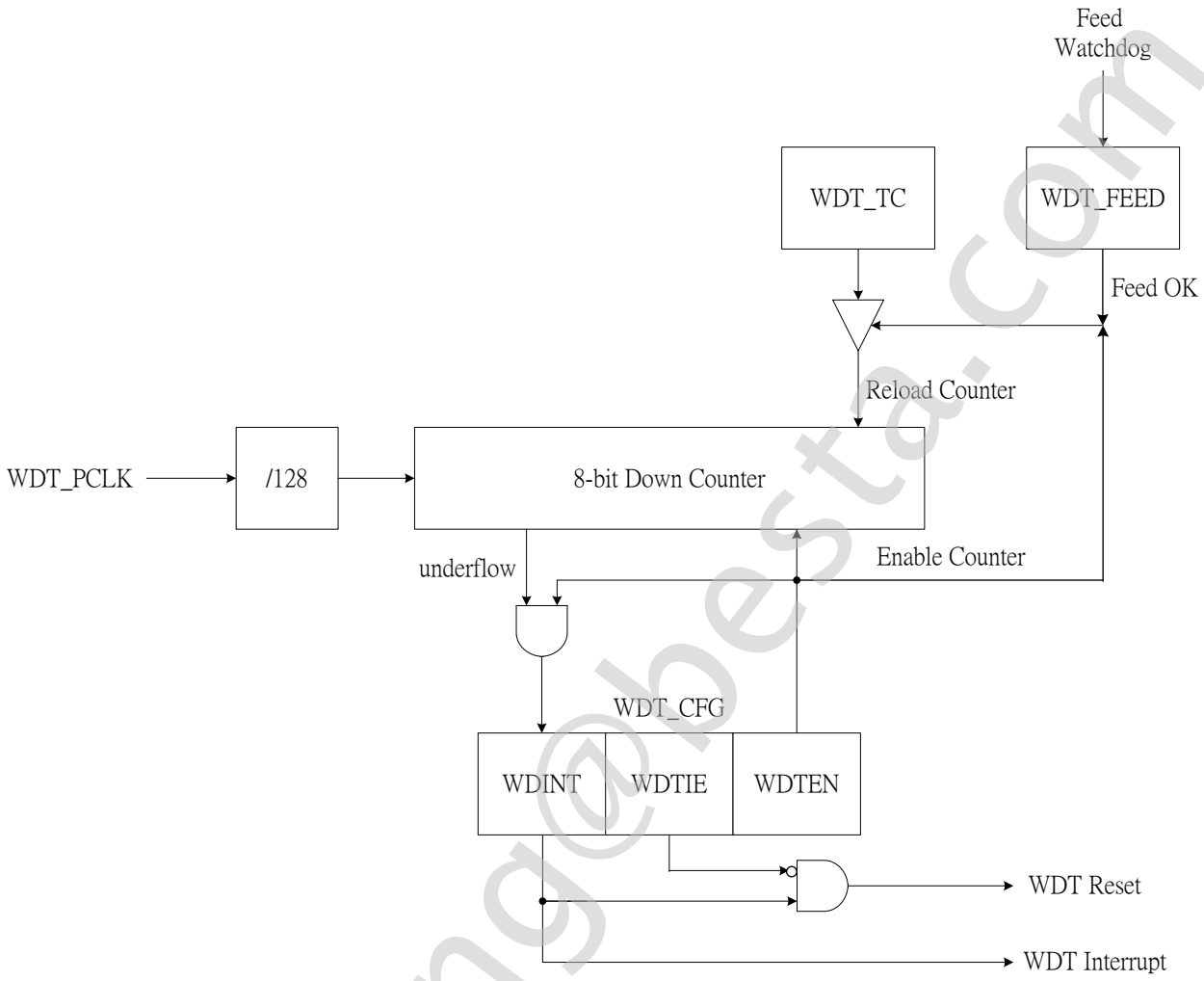
The purpose of the WDT is to reset the MCU within a reasonable amount of time if it enters an erroneous state. When enabled, the WDT will generate a system reset or interrupt if the user program fails to “feed” (or reload) the WDT within a predetermined amount of time.

The WDT consists of a divide by 128 fixed pre-scalar and a 8-bit counter. The clock is fed to the timer via a pre-scalar. The timer decrements when clocked. The minimum value from the counter decrements is 0x01. Hence the minimum WDT interval is (TWDT_PCLK × 128 × 1) and the maximum WDT interval is (TWDT_PCLK × 128 × 256).

When the WDT is started by setting the WDTEN in WDT_CFG register, the time constant value is loaded in the watchdog counter and the counter starts counting down. When the WDT is in the reset mode and the counter underflows, the CPU will be reset, loading the stack pointer and program counter from the vector table as in the case of external reset. Whenever the value 0x55AA is written in WDT_FEED register, the WDT_TC value is reloaded in the watchdog counter and the watchdog reset or interrupt is prevented.

WDT reset or interrupt will occur any time the watchdog is running and has an operating clock source.

3.6.2 Block Diagram



Note: The register can be referred to chapter 9&10: CT16Bn&CT32Bn Registers in SNC7312 Register Table.pdf

3.7 Real Time Clock (RTC)

3.7.1 Overview

SNC7312 RTC module is an independent timer and has independent 3.3V power. The RTC provides a set of continuously running counters which can be used to provide a clock-calendar function with suitable software.

3.7.2 Features

- The RTC clock source could be any of the following:
  - 32K ILRC
  - LX'TAL
- RTC period: 0.5s, 1s, 5s, 10s, 30s, 60s
- RTC interrupt support in Normal mode.
- Auto Wake-up from DPD mode periodly.
- Alarm function support in DPD mode
  - Alarm value can store in ISO BK Register, when RTC wakeup from DPD mode, ROM code will check if counting to alram value. If not reach to the alarm value, ROM code will enter DPD again.
  - For example, withthe condition ofwake-up period=0.5s,alarmscale=60, the system will wake up and boot code at 30s

Note: The register can be referred to chapter2.2: ISO RTC Register in SNC7312 Register Table.pdf

3.8 SPI / SSP

3.8.1 Overview

The SSP is a Synchronous Serial Port controller capable of operation on a SPI, and 4-wire SSI bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. Data transfers are in principle full duplex, with frames of 4 to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice it is often the case that only one of these data flows carries meaningful data.

3.8.2 Features

- Compatible with Motorola SPI, and 4-wire TI SSI bus.
- Synchronous Serial Communication.
- Supports master or slave operation.
- 8-frame FIFO for both transmitter and receiver.
- 4-bit to 16-bit frame.
- Maximum SPI speed of 24 MHz (master) or 12 MHz (slave).
- Data transfer format is from MSB or LSB controlled by register.
- The start phase of data sampling location selection is 1st-phase or 2nd-phase controlled register.

3.8.3 Pin Description

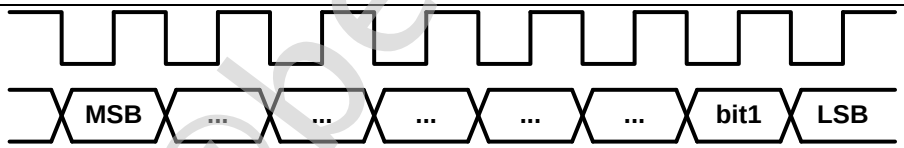
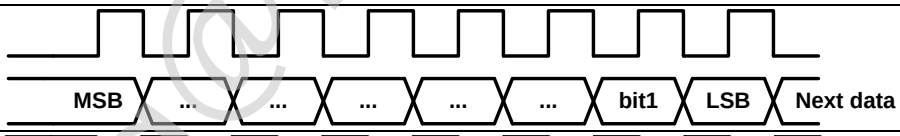
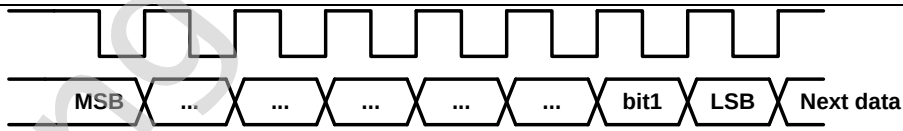
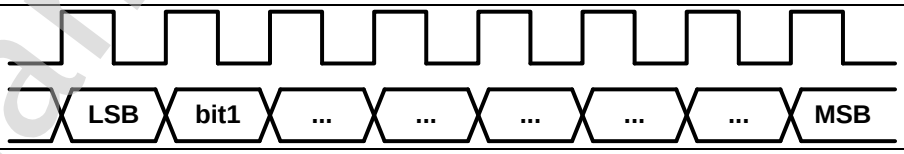
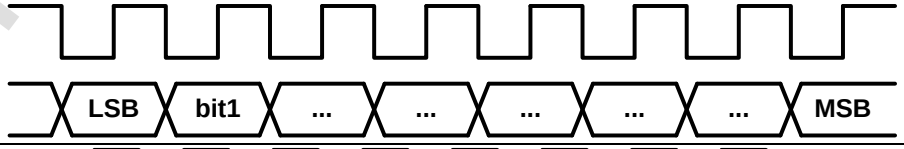
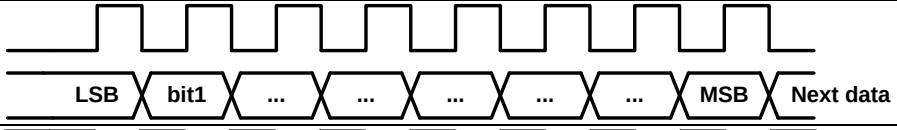
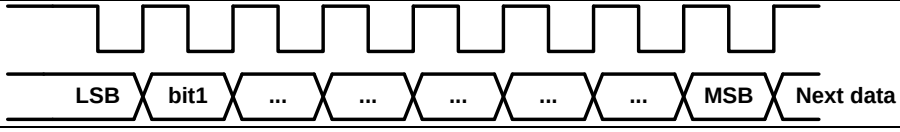
Pin Name	Type	Description	GPIO Configuration
SCKn	O	SSP Serial clock (Master)	
	I	SSP Serial clock (Slave)	Depends on GPIOn_CFG
SELn	O	SPI Slave Select/SSI Frame Sync (Master)	
	I	SSP Slave Select (Slave)	Depends on GPIOn_CFG
MISOn	I	Master In Slave Out (Master)	Depends on GPIOn_CFG
	O	Master In Slave Out (Slave)	
MOSIn	O	Master Out Slave In (Master)	
	I	Master Out Slave In (Slave)	Depends on GPIOn_CFG

3.8.4 Interface Description

The SPI interface is a 4-wire interface where the SSEL signal behaves as a slave select. The main feature of the SPI format is that the inactive state and phase of the SCK signal are programmable through the CPOL and CPHA bits in SSPn_CTRL1 register.

When the “CPOL” clock polarity control bit is LOW, it produces a steady state low value on the SCK pin. If the CPOL clock polarity control bit is HIGH, a steady state high value is placed on the CLK pin when data is not being transferred. The “CPHA” clock phase bit controls the phase of the clock on which data is sampled. When CPHA=1, the SCK first edge is for data transition, and receive and transmit data is at SCK 2nd edge. When CPHA=0, the 1st bit is fixed already, and the SCK first edge is to receive and transmit data.

The SPI data transfer timing as following figure:

MLSB	CPOL	CPHA	SCK Idle Status	Diagrams
0	0	1	Low	
0	1	1	High	
0	0	0	Low	
0	1	0	High	
1	0	1	Low	
1	1	1	High	
1	0	0	Low	
1	1	0	High	

Note: The register can be referred to chapter12: SSP Register in SNC7312 Register Table.pdf

3.9 Inter-Integrated Circuit (I2C)

3.9.1 Overview

The I^2C-bus is bidirectional for inter-IC control using only two wires: a Serial Clock Line (SCL) and a Serial Data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I^2C is a multi-master bus and can be controlled by more than one bus master connected to it. It is also SMBus 2.0 compatible.

Depending on the state of the direction bit (R/W), two types of data transfers are possible on the I^2C-bus:

- Data transfer from a master transmitter to a slave receiver.
  The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte.
- Data transfer from a slave transmitter to a master receiver.
  The first byte (the slave address) is transmitted by the master. The slave then returns an acknowledge bit. Next follows the data bytes transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since a Repeated START condition is also the beginning of the next serial transfer, the I^2C bus will not be released.

The I^2C interface is byte oriented and has four operating modes:

- Master transmitter mode
- Master receiver mode
- Slave transmitter mode
- Slave receiver mode

3.9.2 Features

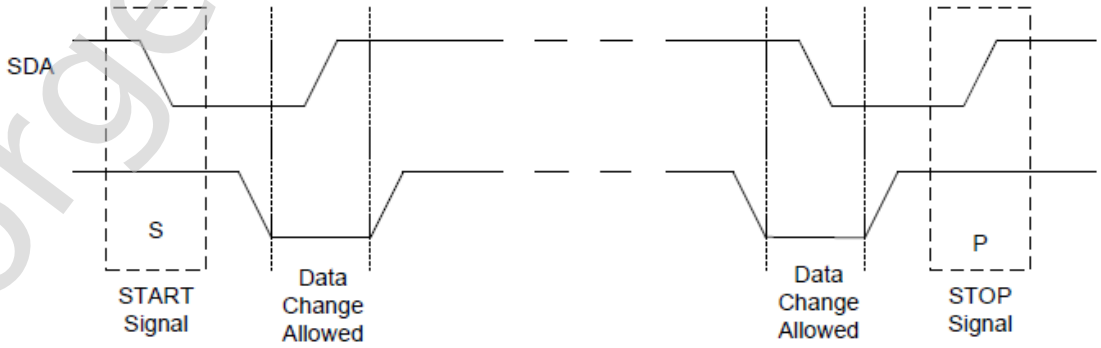
- Standard I²C-compliant bus interfaces may be configured as Master or Slave.
- I²C Master features:
  - Clock generation
  - Start and Stop generation
- I²C Slave features:
  - Programmable I²C Address detection
  - Optional recognition of up to four distinct slave addresses
  - Stop bit detection
- Supports different communication speeds:
  - Standard Speed (up to 200KHz)
  - Fast Speed (up to 400 KHz)
  - Fast-mode Plus (up to 1MHz)
- Arbitration is handled between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I²C transfer rates.
- Data transfer is bidirectional between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization is used as a handshake mechanism to suspend and resume serial transfer.
- Monitor mode allows observing all I²C -bus traffic, regardless of slave address.
- I²C -bus can be used for test and diagnostic purposes.
- Generation and detection of 7-bit/10-bit addressing and General Call.

Note: I2C mini speed is 200KHz

3.9.3 Pin Description

Pin Name	Type	Description	GPIO Configuration
SCLn	I/O	I2C Serial clock	Output with Open-drain Input depends on GPIOn_CFG
SDAn	I/O	I2C Serial data	Output with Open-drain Input depends on GPIOn_CFG

3.9.4 Wave Characteristics



3.9.5 Arbitration and Synchronization Logic

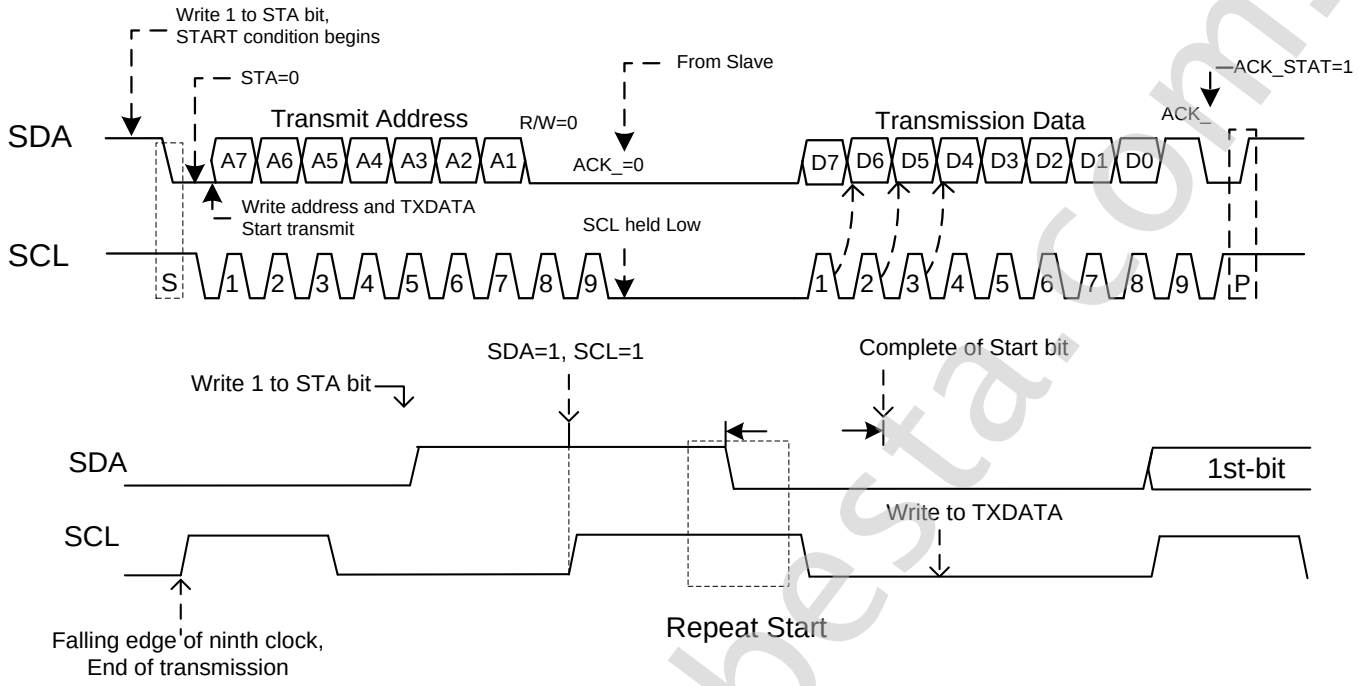
In the master transmitter mode, the arbitration logic checks that every transmitted logic 1 actually appears as a logic 1 on the I2C-bus. If another device on the bus overrules a logic 1 and pulls the SDA line low, arbitration is lost, and the I2C block immediately changes from master transmitter to slave receiver. The I2C block will continue to output clock pulses (on SCL) until transmission of the current serial byte is complete.

Arbitration may also be lost in the master receiver mode. Loss of arbitration in this mode can only occur while the I2C block is returning a “not acknowledge” to the bus. Arbitration is lost when another device on the bus pulls this signal low. Since this can occur only at the end of a serial byte, the I2C block generates no further clock pulses.

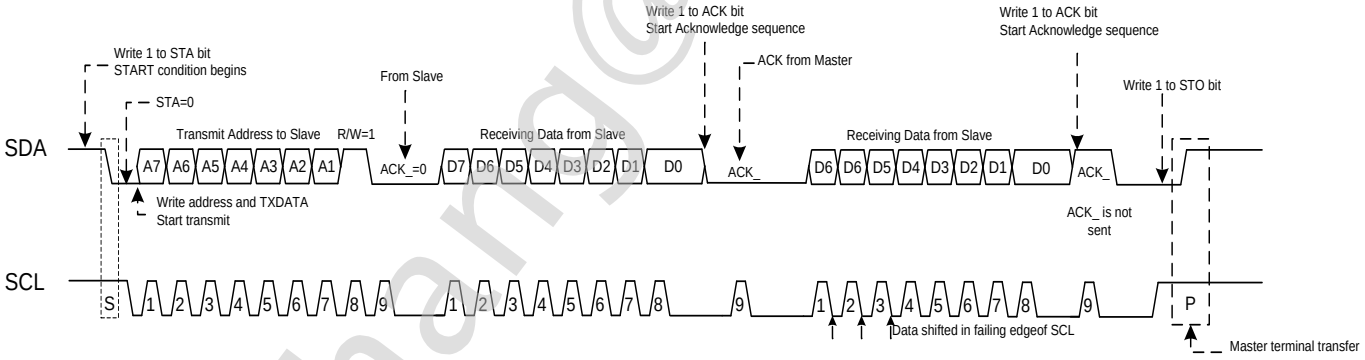
Note: The register can be referred to chapter13: I2C Register in SNC7312 Register Table.pdf

3.9.6 I2C Operating Modes

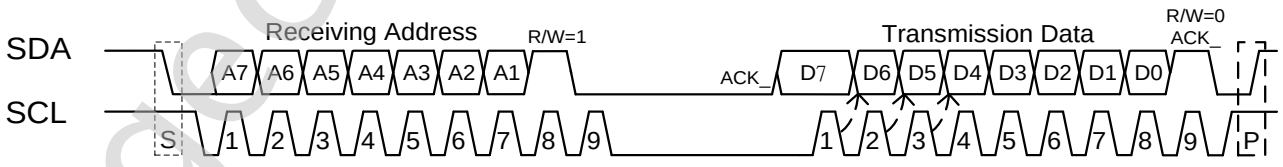
Master Transmitter Mode



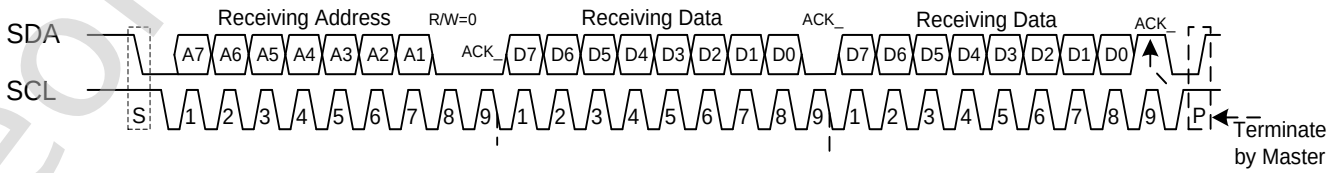
Master Receiver Mode



Slave Transmitter Mode



Slave Receiver Mode



3.10 Universal Asynchronous serial Receiver and Transmitter (UART)

3.10.1 Overview

The UART offers a flexible means of full-duplex data exchange with external equipment requiring an industry standard NRZ asynchronous serial data format. The serial interface is applied to low speed data transfer and communicate with low speed peripheral devices.

The UART offers a very wide range of baud rates using a fractional baud rate generator.

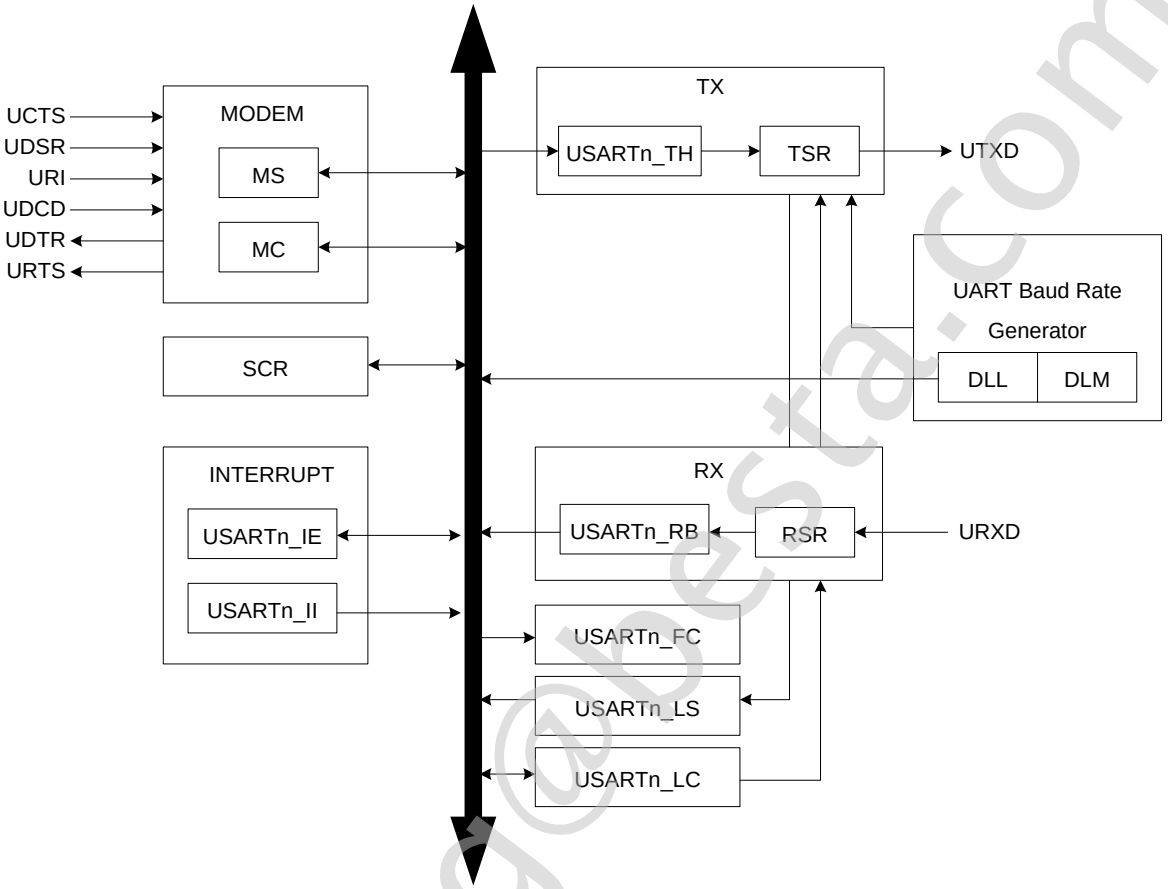
3.10.2 Features

- Full-duplex, 2-wire asynchronous data transfer.
- Single-wire half-duplex communication
- 16-byte receive and transmit FIFOs
- Register locations conform to 16550 industry standard.
- Receiver FIFO trigger points at 1, 4, 8, and 14 bytes.
- Built-in baud rate generator.
- Software or hardware flow control.

3.10.3 Pin Description

Pin Name	Type	Description	GPIO Configuration
UTXDn	O	Serial Transmit data.	
URXDn	I	Serial Receive data.	Depends on GPIOn_CFG

3.10.4 Block Diagram



3.10.5 Baud Rate Calculation

The UART baud rate is calculated as:

$$UART_{BAUDRATE} = \frac{UARTn\_PCLK}{Oversampling \times (256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL)}$$

Where UARTn_PCLK is the peripheral clock, UARTn_DLM and UARTn_DLL are the standard UART baud rate divider registers, and DIVADDVAL and MULVAL are UART fractional baud rate generator specific parameters in UARTn_FD register.

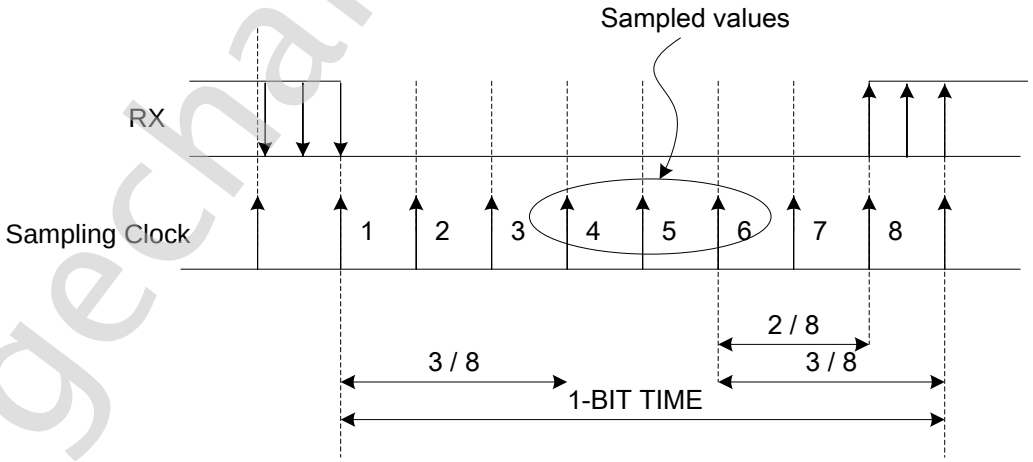
The value of MULVAL and DIVADDVAL should comply with the following conditions:

- 1 ≤ MULVAL ≤ 15
- 0 ≤ DIVADDVAL ≤ 14
- DIVADDVAL< MULVAL
- Oversampling is 8 or 16

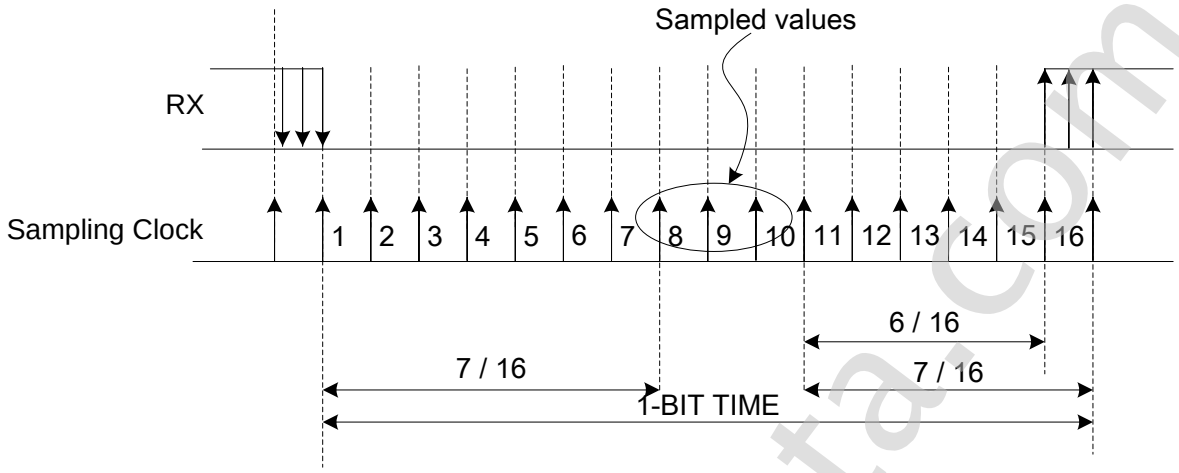
The value of the UARTn_FD register should not be modified while transmitting/receiving data or data may be lost or corrupted.

The oversampling method can be selected by programming the OVER8 bit in UARTn_FD register and can be either 16 or 8 times the baud rate clock.

- OVER8=1: Oversampling by 8 to achieve higher speed (up to UARTn_PCLK/8). In this case the maximum receiver tolerance to clock deviation is reduced.



- OVER8=0: Oversampling by 16 to increase the tolerance of the receiver to clock deviations. In this case, the maximum speed is limited to maximum UARTn_PCLK/16



If the UARTn_FD register value does not comply to these two requests, then the fractional divider output is undefined. If DIVADDVAL is zero then the fractional divider is disabled, and the clock will not be divided.

UART can operate with or without using the Fractional Divider. The desired baud rate can be achieved using several different Fractional Divider settings. The following algorithm illustrates one way of finding a set of DLM, DLL, MULVAL, and DIVADDVAL values. Such set of parameters yields a baud rate with a relative error of less than 1.1% from the desired one.

The following example illustrates selecting the DIVADDVAL, MULVAL, DLM, and DLL to generate BR = 115200 when UARTn_PCLK = 12 MHz, and Oversampling = 16.

$$UART_{BAUDRATE} = \frac{UARTn\_PCLK}{Oversampling \times (256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL)}$$

$$115200 = \frac{12000000}{16 \times (256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL)}$$

$$(256 \times DLM + DLL) \times (1 + DIVADDVAL / MULVAL) = 6.51$$

Since the value of MULVAL and DIVADDVAL should comply to the following conditions:

- 1 ≤ MULVAL ≤ 15
- 0 ≤ DIVADDVAL ≤ 14
- DIVADDVAL< MULVAL

Thus, the suggested UART settings would be: DLM = 0, DLL = 4, DIVADDVAL = 5, and MULVAL = 8. The baud rate generated is 115384, and has a relative error of 0.16% from the originally specified 115200.

Note: The register can be referred to chapter14: UART Register in SNC7312 Register Table.pdf

3.11 Audio (Inter-IC Sound (I2S) / Codec)

3.11.1 Overview

The I^2S bus specification defines a 4-wire serial bus, having one data in, one data out, one clock, and one word select signal. The basic I2S connection has one master, which is always the master, and one slave.

The Codec contains 16-Bit Sigma-delta ADC for Audio in and 24-Bit Sigma-delta DAC for Audio out. 16-Bit Sigma-delta ADC defines pins having one MIC difference input positive, one MIC difference input negative, one Microphone Bias Voltage output, two power supply input pins for Sigma-delta ADC, and one Sigma-delta ADC VMID output. 16-Bit Sigma-delta DAC defines pins having one Sigma-delta DAC output positive, Sigma-delta DAC output negative, two power supply input pins for Sigma-delta DAC Driver, two power supply input pins for Sigma-delta DAC, one Sigma-delta DAC VMID output, and one Sigma-delta DAC Common mode output. The codec circuit requires a 2.7~3.6 V operating voltage supply.

3.11.2 Features

- I^2S can operate as either master or slave.
- Capable of handling 8/16/24/32-bit data length.
- Mono and stereo audio data supported.
- I^2S and MSB justified data format supported.
- 8 word (32-bit) FIFO data buffers are provided.
- Generate interrupt requests when buffer levels cross a programmable boundary.
- Controls include reset, stop and mute options separately for I^2S input and I^2S output.
- There are 3 I^2S controller inside
  - I^2S _0 for DAC and general I2S with DMA
  - I^2S _1 for ADC only with DMA
  - I^2S _2 for general I2S

3.11.3 Pin Description

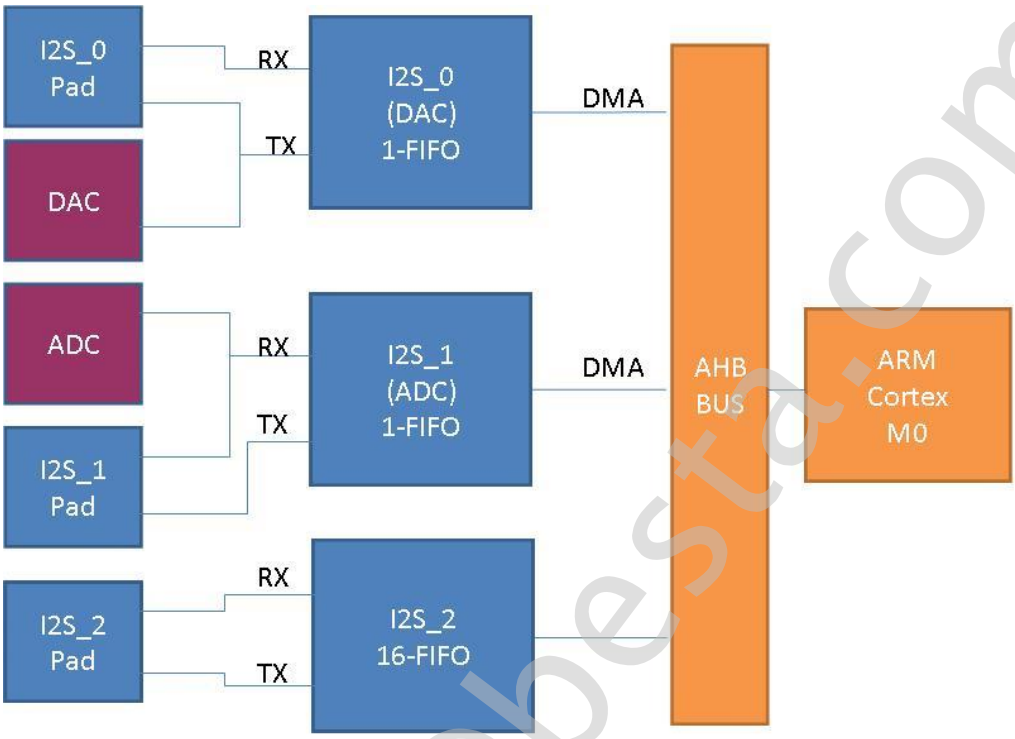
I²S pin description

Pin Name	Type	Description	GPIO Configuration
I2SBCLK	O	I2S Bit clock (Master)	
	I	I2S Bit clock (Slave)	Depends on GPIOn_CFG
I2SWS	O	I2S Word Select (Master)	
	I	I2S Word Select (Slave)	Depends on GPIOn_CFG
I2SDIN	I	I2S Received Serial data	Depends on GPIOn_CFG
I2SDOUT	O	I2S Transmitted Serial data	Depends on GPIOn_CFG
I2SMCLK	O	I2S Master clock output	
	I	I2S Master clock input from GPIO	Depends on GPIOn_CFG

Codec pin description

Pin Name	Type	Description	GPIO Configuration
AVDD_ADC, AVSS_ADC	P	Power supply input pins for Sigma-delta ADC.	-
VMID_ADC	P	Sigma-delta ADC VMID output.	-
MIC_BIAS	P	Sigma-delta ADC Microphone Bias Voltage output.	-
MIC_P	I/O	Sigma-delta ADC MIC difference input (+).	Depends on GPIOn_CFG
MIC_N	I/O	Sigma-delta ADC MIC difference input (-).	Depends on GPIOn_CFG
AVDD_DAC, AVSS_DAC	P	Power supply input pins for Sigma-delta DAC.	-
AVDD_DRV, AVSS_DRV	P	Power supply input pins for Sigma-delta DAC Driver.	-
VCOM_DAC	P	Sigma-delta DAC Common mode output.	-
VMID_DAC	P	Sigma-delta DAC VMID output.	-
VOUTP	I/O	Sigma-delta DAC output (+).	-
VOUTN	I/O	Sigma-delta DAC output (-).	-

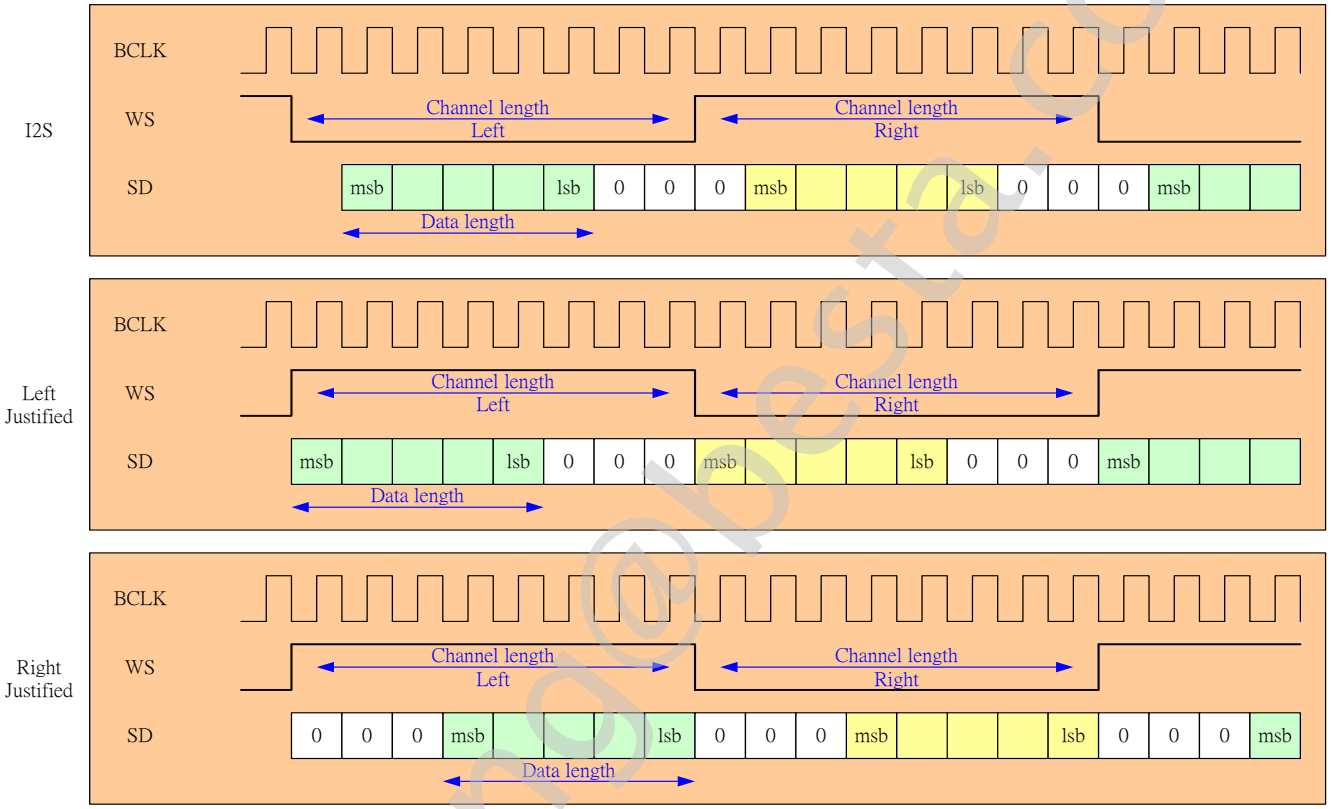
3.11.4 Block Diagram



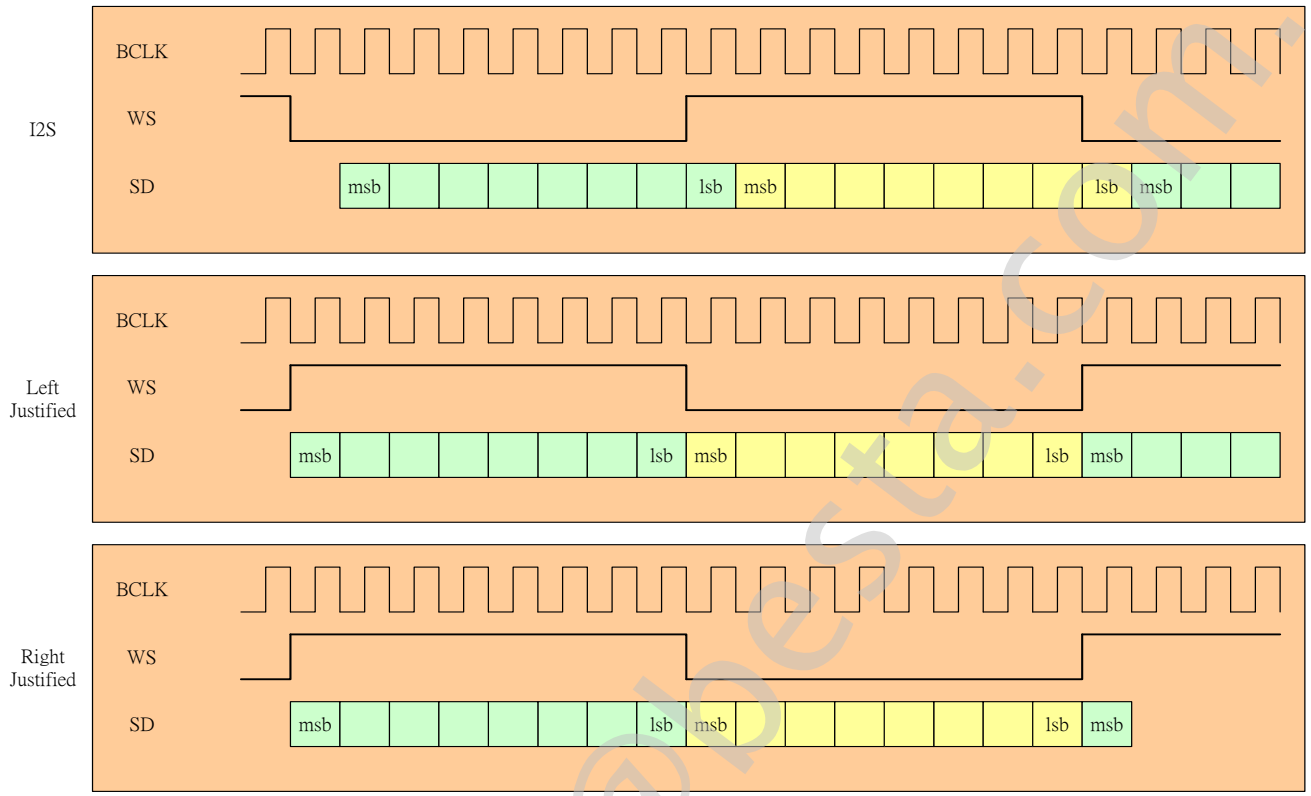
3.11.5 I2S Operation

- Standard I2S
- Right-justified Data Format
- MSB (Left)-justified Data Format

Channel Length > Data Length



Channel Length = Data Length



3.11.6 FIFO Operation

Mono

8bit

N+3	N+2	N+1	N
N+7	N+6	N+5	N+4

16bit

N+1	N
N+3	N+2

24 bit

	N
	N+1

32 bit

N
N+1

Stereo

8bit

RIGHT +1	LEFT +1	RIGHT	LEFT
RIGHT +3	LEFT +3	RIGHT +2	LEFT +2

16bit

RIGHT	LEFT
RIGHT +1	LEFT+1

24 bit

	LEFT
	RIGHT

32 bit

LEFT
RIGHT

Note: The register can be referred to chapter15&16: Audio-ADC & Audio-DAC (I2S) Register in SNC7312 Register Table.pdf

3.12 SAR ADC

3.12.1 Overview

There is 8-bit SAR ADC controllers inside SNC7312. This analog to digital converter has 4-input sources with up to 256-step resolution to transfer analog signal into 8-bits digital data. In SNC7312, we provide an interrupt to info user that ADC result is ready. However, the interrupt event is optional for user.

3.12.2 Features

- Provide 2 sets SAR ADC controller
- Support 4-input sources(AIN0 ~ AIN3)
- Support 8-bit resource
- Support conversion rate(system frequency = 96MHz)
  –128KHz/64KHz/32KHz/16KHz/8KHz/4KHz/2KHz/1KHz

Note: The register can be referred to chapter21: SAR-ADC Control Register in SNC7312 Register Table.pdf

3.13 Serial Flash Controller

3.13.1 Overview

There is serial flash controller inside SNC7312 for user control the SPI flash easily.

3.13.2 Features

- 1-bit/ 2-bit/ 4-bit operation
- 6MHz,12MHz , 24MHz , 48MHz four kinds of clock frequency
- Program on SPI Flash
- DMA access

Note: The register can be referred to chapter22: SPIFlash control Register in SNC7312 Register Table.pdf

3.14 SD Card Host

3.14.1 Overview

There are two sets of SDCard host controller. Support DMA read/write SDCard..

3.14.2 Features

- SD Card (1/4 bits SD mode, SPI mode).
- SDCard max. speed is 48MHz
- Supports SD Card1.0/2.0 commands

Note: The register can be referred to chapter23: SDCard Control Register in SNC7312 Register Table.pdf

3.15 CMOS Image Sensor (CIS)

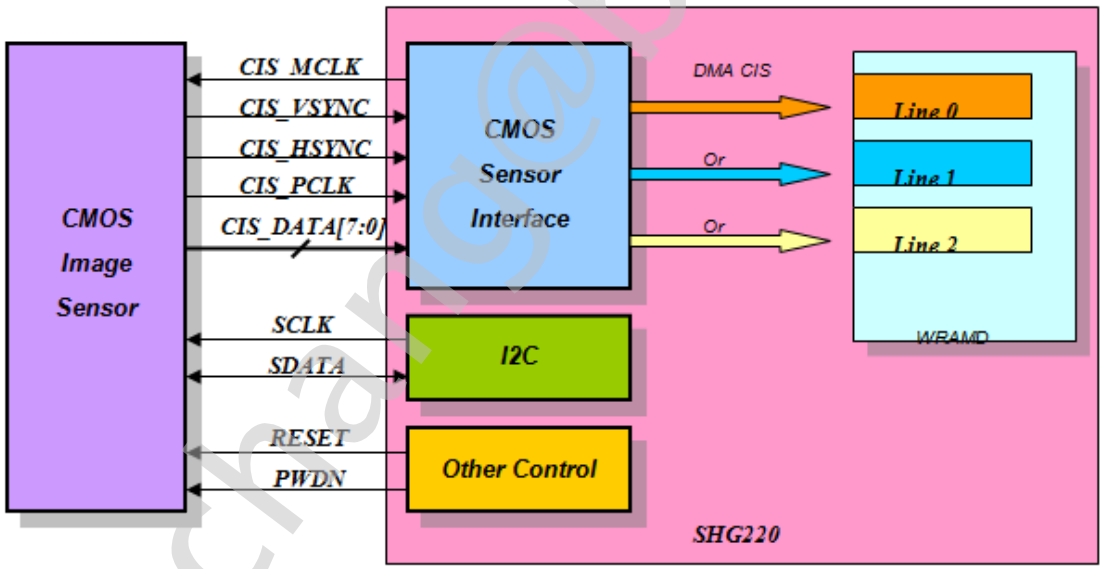
3.15.1 Overview

The CIS Interface communication is based on an advanced 12-pin interface - CIS Clock, VSYNC, HREF, Pixel Clock and eight data lines. Frequency of CIS Clock which output to CIS module can be chosen among 24MHz and 12MHz. Besides, VSYNC, HSYNC and Pixel Clock signal from CIS Module can be set up the active timing at rising or falling edge. An interrupt flag will be issued after a line data is transmitted to RAM, which informs system to access data that is stored at WRAM.

3.15.2 Features

- Support VGA/ CIF/ QVGA/ QCIF/ QQVGA resolution
- Support CMOS Image Sensor output 16bits RGB565/YUV and 8-bit RGB data format.
- Support adjustable V-SYNC, H-Ref and Pixel-Clock edge trigger selection
- Support adjustable MCLK clock output- 24MHz ,12MHz, 6MHz
- Support Window Setting and Scaling

3.15.3 Block Diagram



Note: The register can be referred to chapter24: CIS Control Register in SNC7312 Register Table.pdf

3.16 TFT LCD Interface

3.16.1 Overview

The built-in TFT LCD interface supports UPS051 / UPS052 / Parallel RGB mode with resolution of 320(H) x 240(V).

3.16.2 Features

- Support UPS051 mode
- Support UPS052 mode
- Support Parallel RGB mode

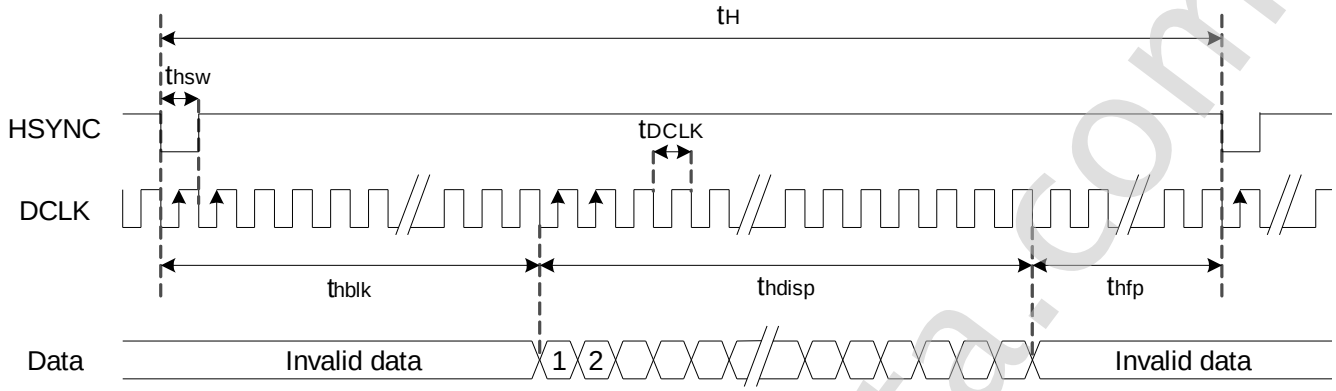
3.16.3 Pin Description

Symbol	I/O	Description
HSYNC	O	Horizontal sync output
VSYNC	O	Vertical sync output
DCLK	O	output data clock
D5	O	Data output; MSB
D4	O	Data output
D3	O	Data output
D2	O	Data output
D1	O	Data output
D0	O	Data output; LSB

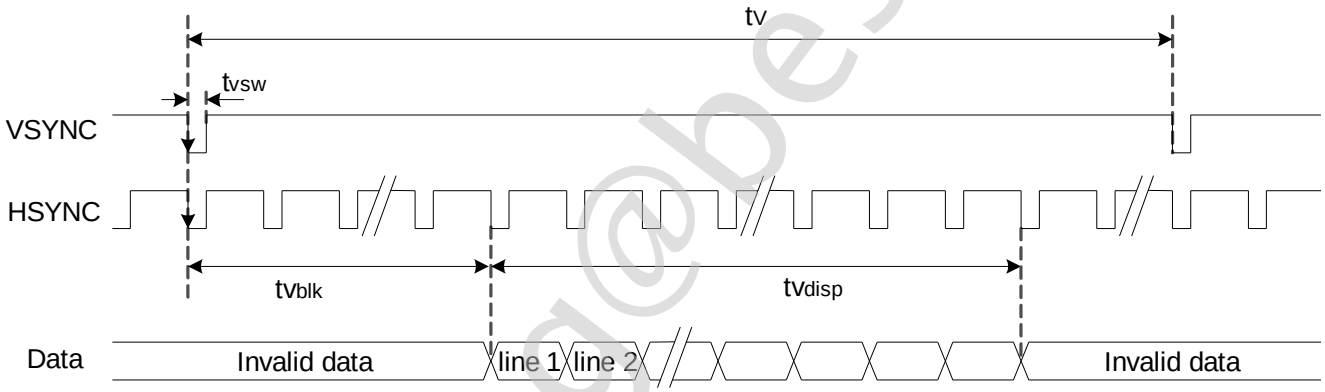
Note: The register can be referred to chapter24: TFT Control Register in SNC7312 Register Table.pdf

3.16.4 Wave Characteristics

Horizontal Timing



Vertical Timing



3.17 8080 MCU Interface

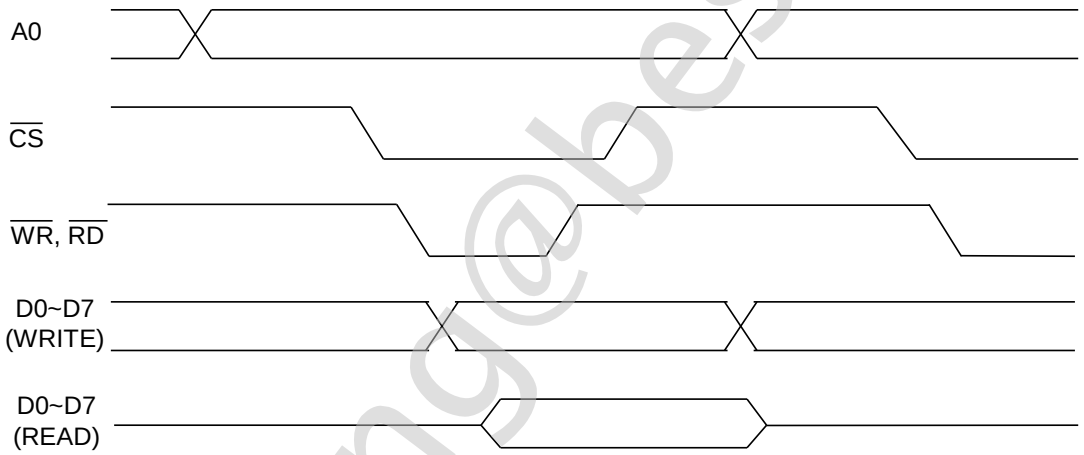
3.17.1 Overview

In 8-bit interface LCD controller, LCD display data is stored in LCD driver. Any change of LCD display was sends out to external LCD driver's RAM by addressing different SRAM space. The interface emulates the 8080/6800-series interface to speed up the interface data moving processing.

3.17.2 Features

- Support 8-bit/16-bit data bus
- Under 8-bit data bus, auto access word data (high byte first or low byte first)
- Adjustable access signal pulse

3.17.3 Wave Characteristics



Note: The register can be referred to chapter26: MCU8080 Control Register in SNC7312 Register Table.pdf

3.18 JPEG Codec

3.18.1 Overview

This JPEG codec is support video rate JPEG encoder or JPEG decoder. It is support JFIF format and it can work at the either encoder or decoder mode at the same time. It can support YCbCr 422 and 420 depend on the external block function.

3.18.2 Features

- Support video rate JPEG encoder/decoder
- Support base-line DCT, Fix Huffman table. (2 AC, 2 DC, typical Huffman table at ISO-IEC 10918-1)
- Support JFIF format
- Support format: YCbCr 422 and 420.
- Share DCT, Zigzag, Quantizer and FIFO for both encoder and decoder
- It can operate at either JPEG-encoder or JPEG-decoder mode
- Encoder data input format: YCbCr 8*8 block 8 bits data input
- Encoder data output format: JPEG bit-stream 8 bits data output
- Decoder data input format: JPEG bit-stream 8 bits data input
- Decoder data output format: YCbCr 8*8 block 8 bits data output

Note: The register can be referred to chapter27: JPEG Control Register in SNC7312 Register Table.pdf

3.19 Color Space Converter (CSC)

3.19.1 Overview

The CSC can convert pixel data from RGB (565) to YCbCr (422 or 420) format, or from YCbCr (422 or 420) to RGB (565) format.

3.19.2 Features

- RGB (565) to YCbCr (422 or 420) convert function.
- YCbCr (422 or 420) to RGB (565) convert function.
- Direct raw data to line buffer movement.
- RGB input/output sequence: (R0, G0, B0), (R1, G1, B1)…
- YCbCr 422 input/output sequence:
  (Y1, Y0), (Y3, Y2), (Cb23, Cb01), (Cr23, Cr01)
  (Y5, Y4), (Y7, Y6), (Cb67, Cb34), (Cr67, Cr34)
- YCbCr 420input/output sequence:
  (Y1, Y0), (Y3, Y2), (Cb4567, Cb0123), (Cb4567, Cr0123)
  (Y5, Y4), (Y7, Y6), (Cb4567, Cb0123), (Cr4567, Cb0123)

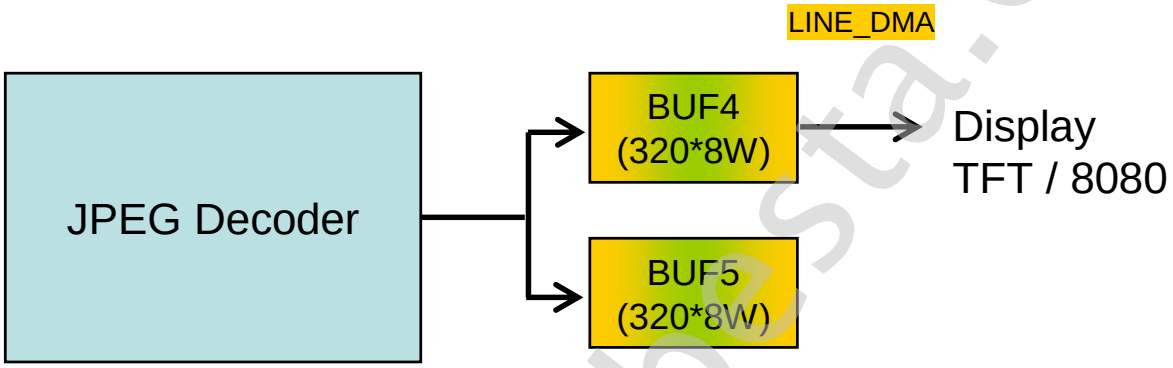
Note: The register can be referred to chapter28: CSC Control Register in SNC7312 Register Table.pdf

3.20 Line DMA

3.20.1 Overview

Users can move RGB565 data from AHB-RAM to TEXT3 line buffer to display via Line DMA. It provides two buffer addresses for setting, and it will be exchanged when it has been enabled. In order to avoid display error, users must fill up the content before switching the buffer address.

3.20.2 Block Diagram



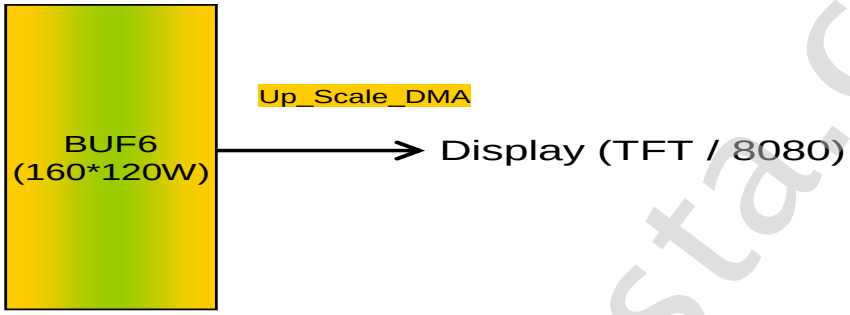
Note: The register can be referred to chapter29: Line DMA Register in SNC7312 Register Table.pdf

3.21 4.22 Up Sample Scaling DMA

3.21.1 Overview

SNC7312 provides an Up-scaling function, which can enlarge QQVGA size to QVGA or VGA size.

3.21.2 Block Diagram



Note: The register can be referred to chapter30: Up Sample DMA Register in SNC7312 Register Table.pdf

3.22 SDRAM

3.22.1 Overview

SNC7312 series provide SDRAM device. SDRAM is a high-speed CMOS synchronous DRAM containing 16 Mbits. It is internally configured as a dual 512K word x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16 bit banks is organized as 2048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of a Bank Activate command which is then followed by a Read or Write command.

3.22.2 Feature

- Provide SDRAM controller
- 512K word x 16-bit x 2-bank
- Self-refresh mode: standard
- Auto Refresh and Self Refresh
- 4096 refresh cycles/64ms or 2049 refresh cycles/8ms
- Programmable Mode registers:
  CAS Latency: 2, or 3
  Burst Length: 2
- Support SDRAM PLL rate 80Mhz (system frequency = 96MHz)

Note: The register can be referred to chapter31: SDRAM Controller Register in SNC7312 Register Table.pdf

4 Electrical Characteristic

4.1 Absolute Maximum Rating

Items	Symbol	Min	Max	Unit
Supply Voltage	VDD	2.7	3.6	V
Input Voltage	VIN	VSS-0.3	VDD-0.3	V
Operating Temperature	TOP	0	55.0	℃
Storage Temperature	TSTG	-55.0	125.0	℃

4.2 Electrical Characteristic

Item	Sym.	Min.	Typ.	Max.	Unit	Condition (TA=25 ℃)
Operating Voltage VDD	V_{DD}	2.7	3.3	3.6	V	
Operating Voltage CVDD	CV_{DD}	1.08	1.2	1.32	V	Internal regulator supply
Normal current 48MHz	I_{NOR48}		40		mA	Normal mode SPLL on
Normal current 96MHz	I_{NOR96}		60		mA	Normal mode SPLL on
RTC current	I_{RTC}		3		uA	V_{DD}=3.3V, 32768 X'tal, 60s wakeup
Standby current	I_{SBY}	-	800	-	nA	Deep power down V_{DD}=3.3V, No load
IHRC	IHRC		12		MHz	Error 1%
SAR ADC ENOB	ENOB		9		bit	
SAR ADC INL	INL		1		bit	
SAR ADC DNL	DNL		1		bit	
SD-ADC SNR	SNR		99		dB	
SD-DAC SNR	SNR		92		dB	

4.3 GPIO Sink / Driving Current

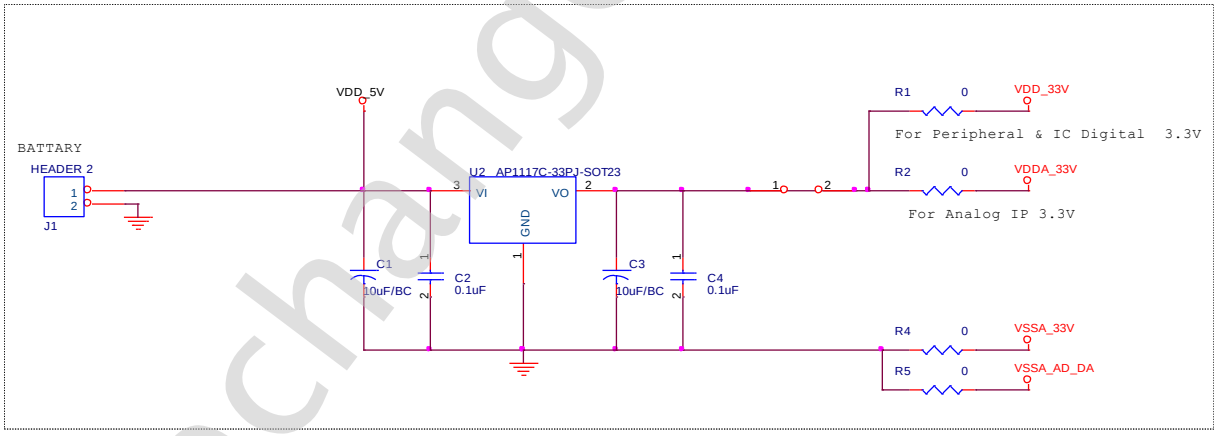
Pin Name	Sink (mA)	Driving (mA)
P0.0	13.2	25.4
P0.1	13.2	25.4
P0.2	13.6	25.7
P0.3	13.6	25.7
P0.4	13.4	25.0
P0.5	13.3	25.0
P0.6	13.5	25.0
P0.7	13.5	25.0
P0.8	18.3	37.6
P0.9	18.6	37.7
P0.10	18.8	37.5
P0.11	18.6	37.5
P0.12	18.2	37.4
P0.13	18.6	37.5
P0.14	13.3	25.6
P0.15	13.1	24.5
P1.0	13.7	25.8
P1.1	13.5	25.3
P1.2	13.8	25.8
P1.3	13.8	25.7
P1.4	19.0	37.8
P1.5	19.0	37.7
P1.6	19.0	37.7
P1.7	19.1	37.8
P1.8	19.1	37.8
P1.9	19.1	37.7
P1.10	13.8	25.3
P1.11	13.7	25.3
P1.12	13.8	25.3
P1.13	13.7	25.3
P1.14	18.7	37.6
P1.15	18.7	37.6
P2.0	18.8	37.6
P2.1	18.7	37.6
P2.2	18.7	37.6
P2.3	18.6	37.6
P2.4	13.7	25.4
P2.5	13.7	25.4
P2.6	13.7	25.4
P2.7	13.7	25.4
P2.8	13.8	25.4
P2.9	13.7	25.4
P2.10	13.7	25.6
P2.11	13.7	25.6
P2.12	13.7	25.6
P2.13	13.6	25.6
P2.14	13.6	25.6
P2.15	13.6	25.6
P3.0	13.8	25.6
P3.1	13.8	25.6
P3.2	13.8	25.6

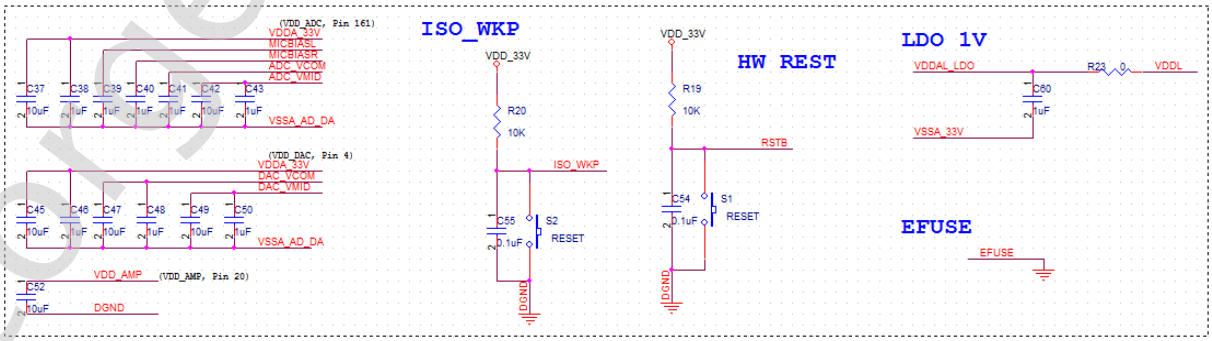
P3.3	13.8	25.5
P3.4	13.8	25.5
P3.5	19.0	37.4
P3.6	18.9	37.4
P3.7	18.8	37.1
P3.8	19.0	37.6
P3.9	19.0	37.6
P3.10	18.7	37.7
P3.11	13.5	25.3
P3.12	13.1	24.4
P3.13	13.5	25.2
P3.14	13.6	25.2
P3.15	13.5	25.1
P4.0	13.1	24.5
P4.1	13.1	24.5
P4.2	13.1	24.5
P4.3	13.1	24.5
P4.4	13.6	25.1
P4.5	13.6	25.1
P4.6	13.7	25.5
P4.7	13.7	25.3

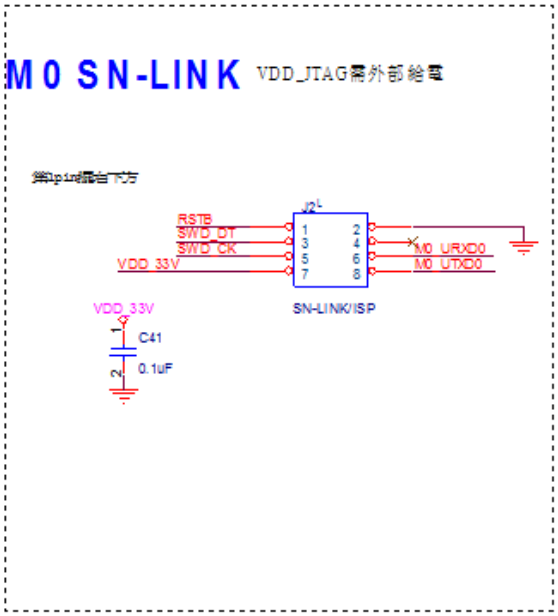
4 Application Circuit

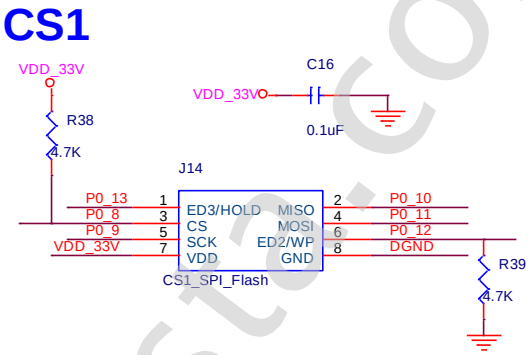
There are some notifications about circit design.

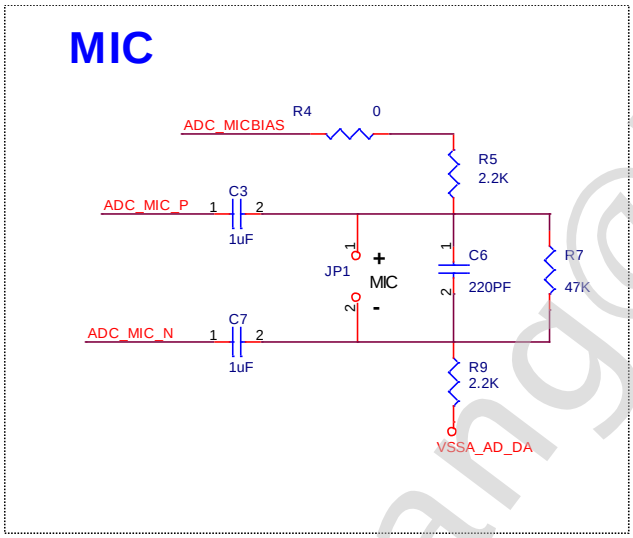
- LDO 1.2V output capacitance should be near to IC and the value is 1uF.
- IC EFUSE pin should be short to ground.
  - SNC73121/SNC73122: Pin-75 (EFUSE)
  - SNC73123/SNC73124: Pin-41 (EFUSE)
  - SNC73125: Pin-31 (EFUSE)
- SPIFlash add pull-high and pull-low resistances.
  - SNC7312 IOs in DPD mode are in input floating.
  - SPIFlash CS pin should be added pull-high resistance.
  - SPIFlash WP pin should be added pull-low resistance.(If use protect function)
- Package E-Pad
  - There is an E-Pad in QFN package.
  - SNC73123/SNC73124/SNC73125 use E-pad as ground pin. So E-pad should connect to bigger ground layer plan in PCB layout.
- External reset resistance and capacitance
  - External reset signal is low-active reset.
  - External reset signal < 1/2VDD is low and system reset. Otherwise, external reset signal > 1/2VDD is high.
  - If there is large capacitance in 3V power, reset resistance and capacitance should be re-arrangement.

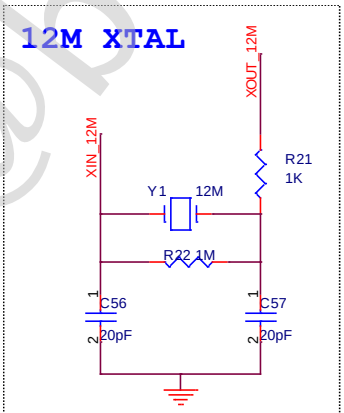


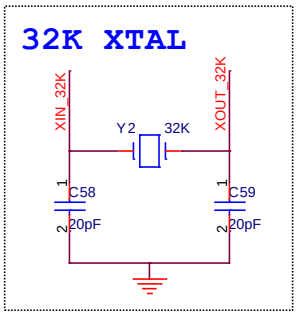


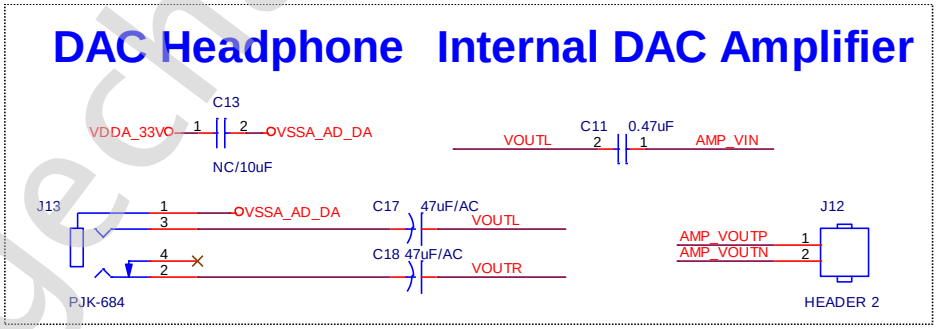


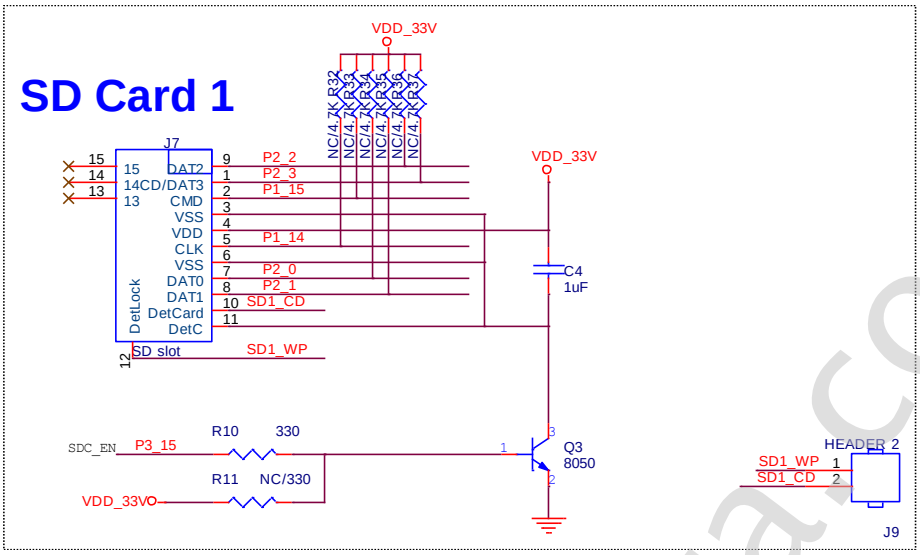


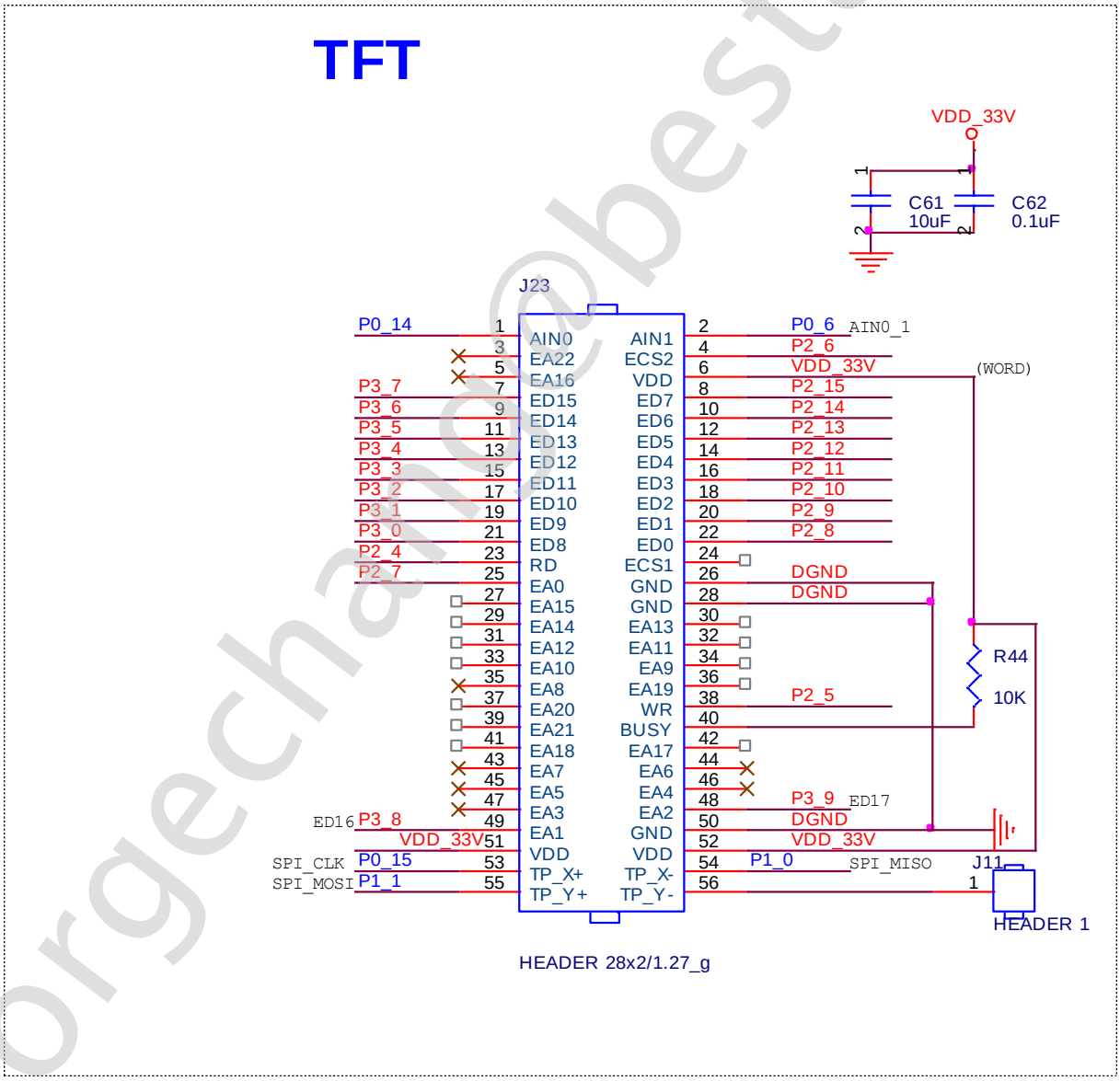


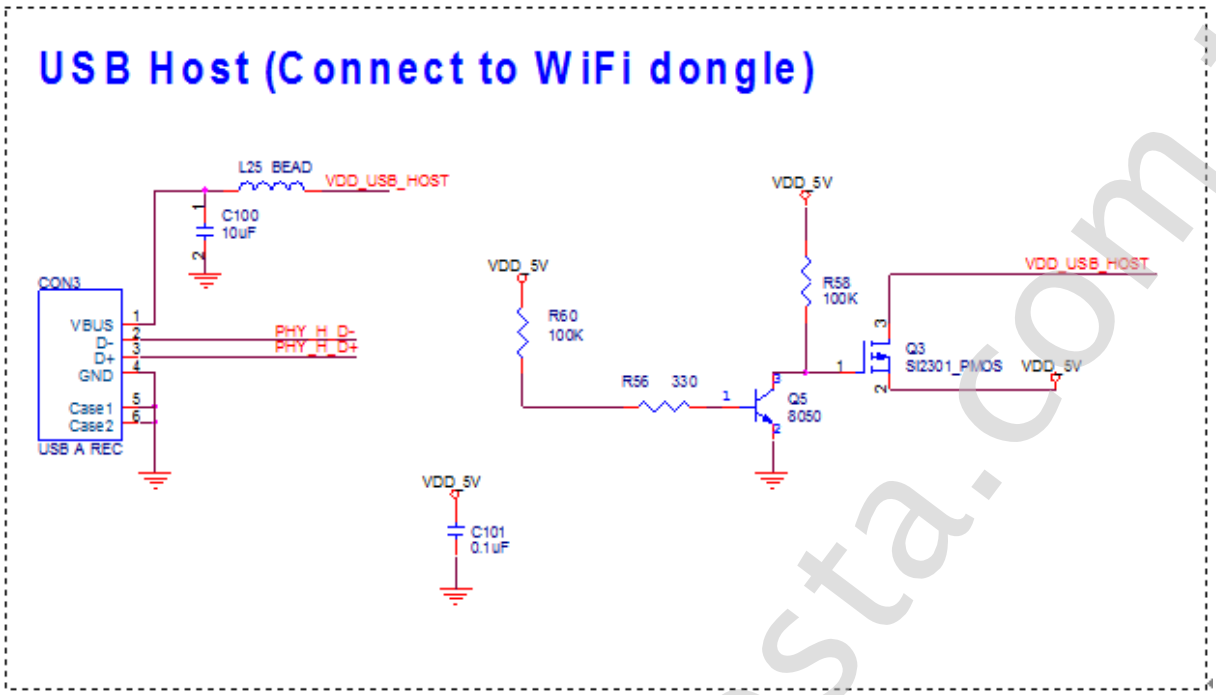


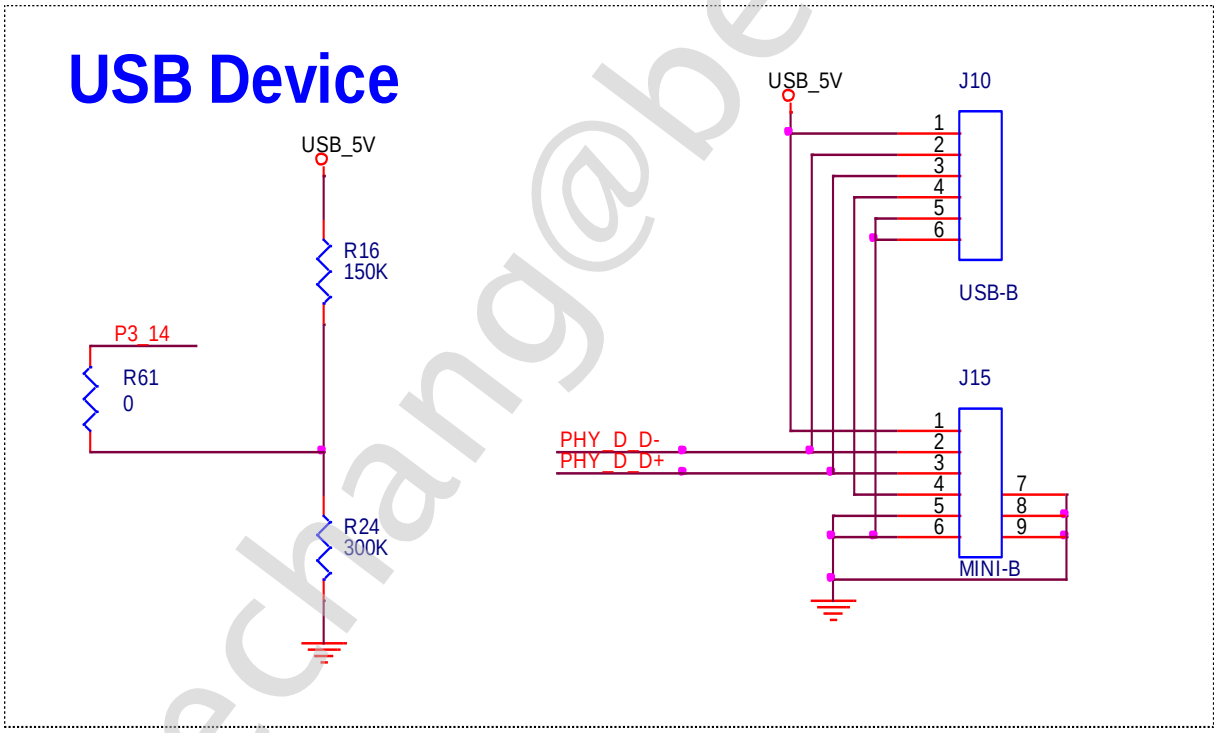








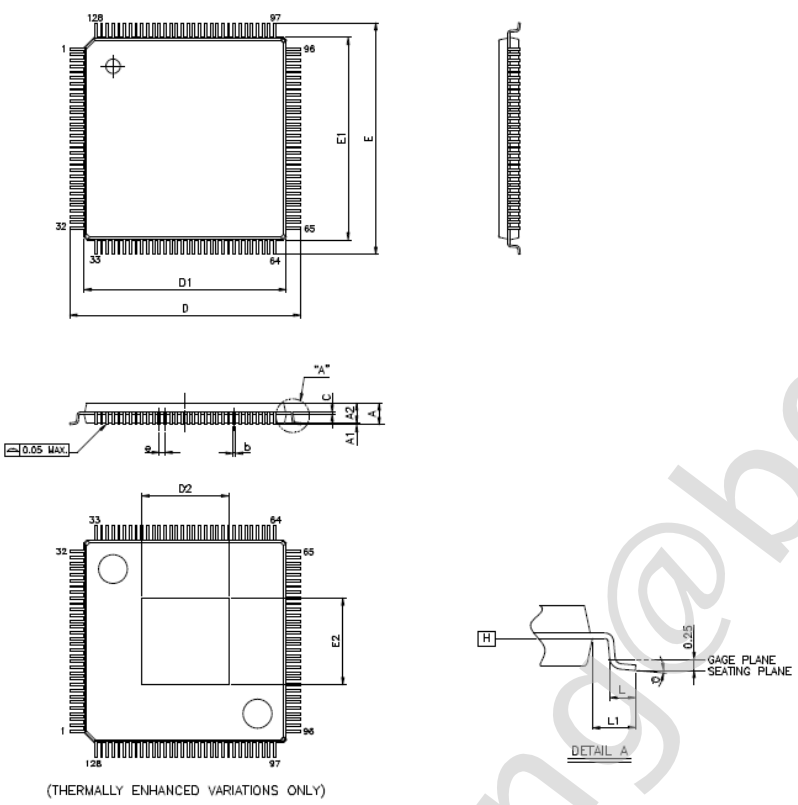




5 Package Information

4.4 LQFP128

LQFP-128 14x14x1 mm



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	0.16	0.23
c	0.09	--	0.20
D	16.00 BSC		
D1	14.00 BSC		
E	16.00 BSC		
E1	14.00 BSC		
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

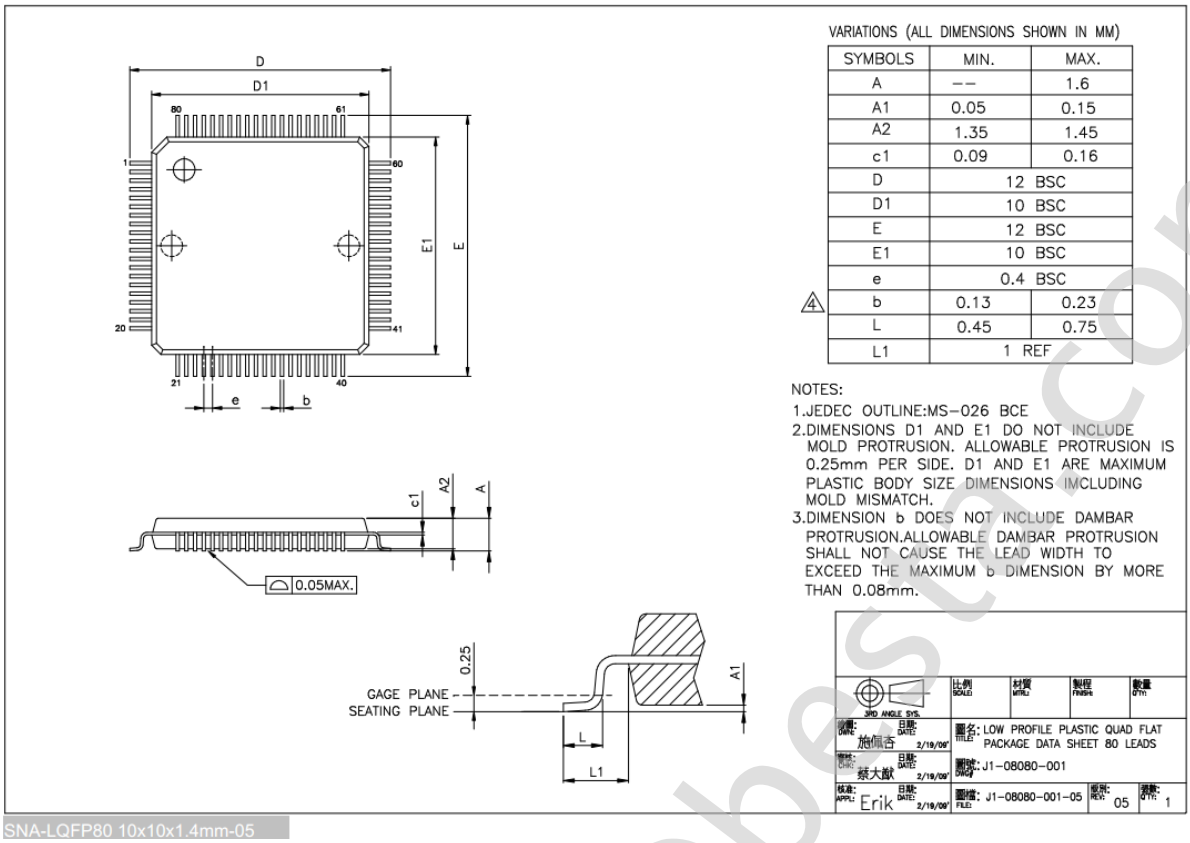
THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	E2		D2	
	MIN.	MAX.	MIN.	MAX.
23FX23E	5.10	5.99	5.10	5.99

NOTES:
1.JEDEC NO. : N/A.
2.DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

4.5 LQFP80

10x10mm



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	MAX.
A	--	1.6
A1	0.05	0.15
A2	1.35	1.45
c1	0.09	0.16
D	12 BSC	
D1	10 BSC	
E	12 BSC	
E1	10 BSC	
e	0.4 BSC	
4 b	0.13	0.23
L	0.45	0.75
L1	1 REF	

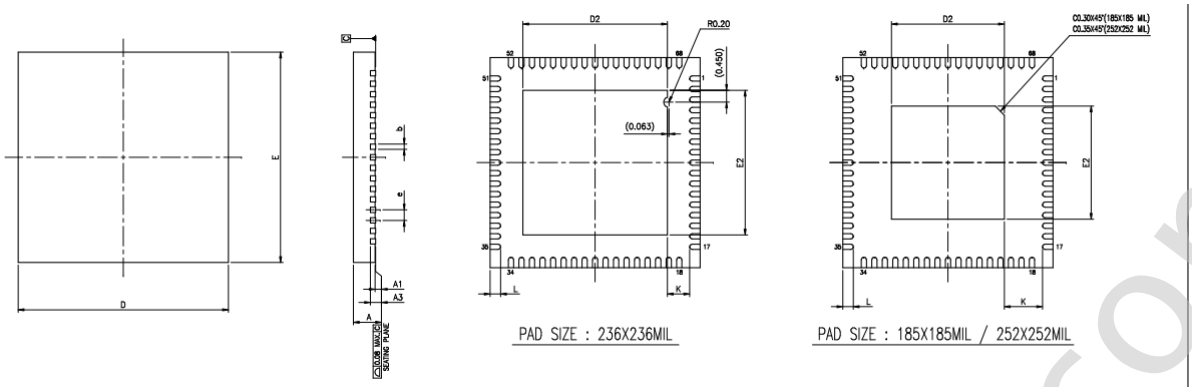
NOTES:
1.JEDEC OUTLINE:MS-026 BCE
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

3RD ANGLE SYS.	比例 SCALE:	材質 MTRL:	製程 Finish:	數量 QTY:
設計: 施佩杏 日期: 2/19/09	圖名: LOW PROFILE PLASTIC QUAD FLAT PACKAGE DATA SHEET 80 LEADS			
審核: 蔡大猷 日期: 2/19/09	圖號: J1-08080-001			
核准: Erik 日期: 2/19/09	圖檔: J1-08080-001-05	修改: REV: 05	張數: QTY: 1	

SNA-LQFP80 10x10x1.4mm-05

4.6 QFN68

8x8 mm



JEDEC OUTLINE	PACKAGE TYPE					
	MO-220			MO-220		
PKG CODE	WQFN(X868)			VQFN(Y868)		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.80	0.85	0.90
A1	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25
D	8.00 BSC			8.00 BSC		
E	8.00 BSC			8.00 BSC		
e	0.40 BSC			0.40 BSC		
L	0.35	0.40	0.45	0.35	0.40	0.45
K	0.20	–	–	0.20	–	–

	E2			D2			LEAD FINISH		JEDEC CODE
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
185X185 MIL	4.20	4.30	4.40	4.20	4.30	4.40	V	X	N/A
⚠5 236X236 MIL	5.40	5.50	5.60	5.40	5.50	5.60	V	X	N/A
⚠5 252X252 MIL	6.10	6.20	6.30	6.10	6.20	6.30	V	X	VLLE-1

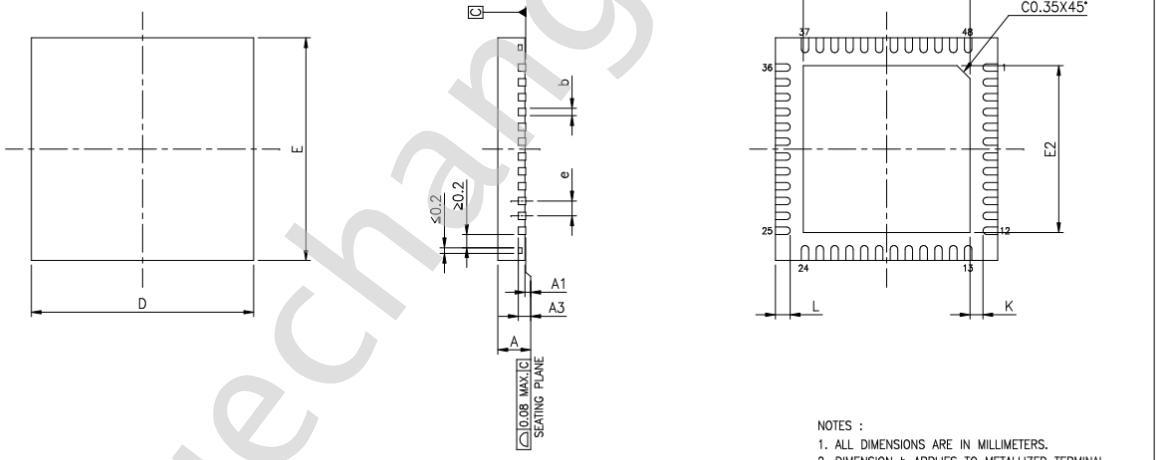
NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

超豐電子股份有限公司
GREATEK ELECTRONICS INC.

3RD ANGLE SYS.	比例 SCALE:	材質 MTRL:	製程 FINISH:	數量 QTY:
繪圖: 施佩杏 DWN:	日期: DATE: 3/8/13	圖名: THERMALLY ENHANCED PLASTIC VERY THIN AND VERY VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE QFN 68 TERMINALS (8.0X8.0mm)X868/Y868	
審核: 黃柏瑄 CHK:	日期: DATE: 3/11/13	圖號: J1-10068-001 DWG#	
核准:	日期:		

4.7 QFN48

6x6 mm



JEDEC OUTLINE	PACKAGE TYPE														
	MO-220			MO-220			MO-248			MO-248			MO-248		
PKG CODE	VQFN(Y648)			WQFN(X648)			UQFN(W648)			TQFN(Z648) OPTION 1			TQFN(N/A) OPTION 2		
SYMBOLS	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.70	0.75	0.80	0.50	0.55	0.60	0.40	0.45	0.50	0.40	0.45	0.50
A1	0.00	0.02	0.05	0.00	0.02	0.05	0.00	0.02	0.05	0.00	0.02	0.05	0.00	0.02	0.05
A3	0.203 REF.			0.203 REF.			0.150 REF.			0.127 REF.			0.203 REF.		
b	0.15	0.20	0.25	0.15	0.20	0.25	0.15	0.20	0.25	0.15	0.20	0.25	0.15	0.20	0.25
D	6.00 BSC			6.00 BSC			6.00 BSC			6.00 BSC			6.00 BSC		
E	6.00 BSC			6.00 BSC			6.00 BSC			6.00 BSC			6.00 BSC		
e	0.40 BSC			0.40 BSC			0.40 BSC			0.40 BSC			0.40 BSC		
K	0.20	–	–	0.20	–	–	0.20	–	–	0.20	–	–	0.20	–	–

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE	VQFN	WQFN	UQFN	TQFN OPTION 1	TQFN OPTION 2
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
157X157* MIL	4.57	4.62	4.67	4.57	4.62	4.67	0.35	0.40	0.45	V	X	XJJE-1				V	
185X185* MIL	4.45	4.50	4.55	4.45	4.50	4.55	0.35	0.40	0.45	V	X	(W)VJJE-1	V	V			
⚠5 181X181* MIL	4.35	4.40	4.45	4.35	4.40	4.45	0.40	0.45	0.50	V	X	N/A	V	V			
189X189* MIL	4.35	4.40	4.45	4.35	4.40	4.45	0.30	0.40	0.50	V	X	N/A				V	
187X187* MIL	4.57	4.62	4.67	4.57	4.62	4.67	0.35	0.40	0.45	V	X	UJJE-1				V	

"*"表示此用字元,此此用字元可能與其它不同字元所取代,實際的字元請參照bonding diagram所示.

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

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繪圖: 施佩杏 DWN:	日期: DATE: 11/26/13	圖名: THERMALLY ENHANCED PLASTIC VERY THIN AND VERY VERY THIN AND EXTRA THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE QFN 48 TERMINALS (5.0X5.0mm) Y648/U648/W648/Z648/12548	
審核: 黃柏瑄 CHK:	日期: DATE: 11/26/13	圖號: J1-10048-003 DWG#	
核准:	日期:		

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SONiX Technology Co., Ltd.(Headquarters)
Address: 10F-1, No.36, Taiyuan Street, Chupei City, Hsinchu, Taiwan
Tel: (886)3-5600-888
Fax: (886)3-5600-889
http://www.sonix.com.tw/masterpage-en

SONiX Technology Taipei Sales Office
Address: 15F-2, No.171 Song Ted Road, Taipei, Taiwan
Tel: (886)2-2759-1980
Fax: (886)2-2759-8180
mkt@sonix.com.tw | sales@sonix.com.tw

SONiX Technology Japan Office
Address: Kobayashi bldg. 2F, 4-8-27,Kudanminami, Chiyodaku,Tokyo, 102-0074, Japan
Tel: (81)3-6272-6070
Fax: (81)3-6272-6165
jpsales@sonix.com.tw

SONiX Technology Hong Kong Sales Office
Address: Unit 2603, 26/F CCT Telecom Building, No. 11 Wo Shing Street, Fo Tan, New Territories, Hong Kong
Tel: (852)2723-8086
Fax: (852)2723-9179
hk@sonix.com.tw

SONiX Technology Co., Ltd.(China)
Address: High Tech Industrial Park, Shenzhen, China
Tel: (86)755-2671-9666
Fax: (86)755-2671-9786
mkt@sonix.com.tw | sales@sonix.com.tw

SONiX Technology Cheng Du Office
Address: Tian Fu Software Park, Cheng Du City, China
Tel: (86)28-8533-1818
Fax: (86) 28-8533-1816
mkt@sonix.com.tw | sales@sonix.com.tw

United State Contact
Tim Lightbody
Tel: (1)-714-330-9877
tlightbody@earthlink.net

Canada Contact
Andrew Wright
Tel: (1)-905-246-0191
andreww@sonix.com.tw