Cao Gao

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Research Interests

I am interested in computer architecture, hardware/software interface, and operating system in general. Currently working on evaluating mobile applications and improving mobile hardware and systems.

Education

- **Ph.D. , *Computer Science and Engineering, University of Michigan, Ann Arbor, MI*** *2014.1 – 2017.5 (Expected)*
  Area of Specialization: Computer Engineering --- Hardware Advisor: Prof. Trevor Mudge
- **M.S., *Computer Science and Engineering, University of Michigan, Ann Arbor, MI*** *2012.9 – 2013.12*
  Overall GPA: 4.0/4.0
- **B.Eng. , *College of Electrical Engineering, Zhejiang University, Hangzhou, Zhejiang, China*** *2008.9 – 2012.6*
  Major: Electronic and Information Engineering Area of Emphasis: VLSI design
  Member of Chu Kochen Honors College Minor: English
  Overall GPA: 3.91/4.0 Rank: top 5%
- ***National Cheng Kung University, Tainan, Taiwan, R.O.C*** *2010.9 – 2011.1*
  Exchange student in College of Electrical Engineering and Computer Science Overall GPA: 93.7/100

Employment

- ***ARM Ltd., Austin, TX*** *2014.6 – 2014.8*
  R&D Intern at the Mobile System Group

Publications

- C. Gao, A. Gutierrez, M. Rajan, R.G. Dreslinski, T. Mudge, and C.J. Wu. *A Study of Mobile Device Utilization*. 2015 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2015.
- C. Gao, A. Gutierrez, R.G. Dreslinski, T. Mudge, K. Flautner, and G. Blake. *A Study of Thread Level Parallelism on Mobile Devices.* 2014 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), March 2014.

Major Projects and Courses

University of Michigan:

- *A Study of Mobile Device Utilization* *Summer 2013 - Present*
  Analyzed the CPU and GPU utilization of a wide range of commonly used mobile applications
- *EECS 583 – Advanced Compilers* Grade: A *Fall 2013*
  Design of a loop-distribution compiler optimization technique in LLVM
- *EECS 570 – Parallel Computer Architecture* Grade: A *Winter 2013*
  Fine-grained energy-efficient reconfigurable Networks-on-Chip router architecture
- *EECS 470 – Computer Architecture* Grade: A *Fall 2012*
  Design of a 2-way superscalar, out-of-order processor with early recovery and tag broadcast
  Ranked 2nd among all groups, 1st in clock frequency
- *EECS 578 – Computer-Aided Design Verification of Digital Systems* Grade: A+ *Fall 2012*
  Design of quantitative metrics for hardware design bugs

Zhejiang University:

- *Remapping Method for Fault-tolerance Networks-on-Chip* 2011.7-2012.3
  Proposed a mapping scheme for NoC, and a task remapping method for fault-tolerance
- *Intelligent Humidity Controller Based on High-Performance Embedded CPU* 2010.5-2011.7
  Implemented a humidity controller on FPGA

Skills

Programming: Verilog, VHDL, C, C++, Assembly Language (RISC)
Environments: Linux, Android, Windows and Mac development, scripting
Languages: Fluent in English, native Mandarin speaker