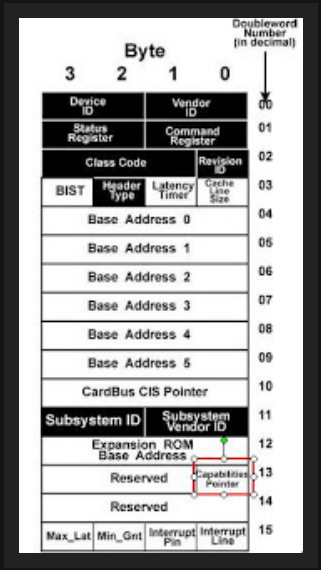
Dios 記事本

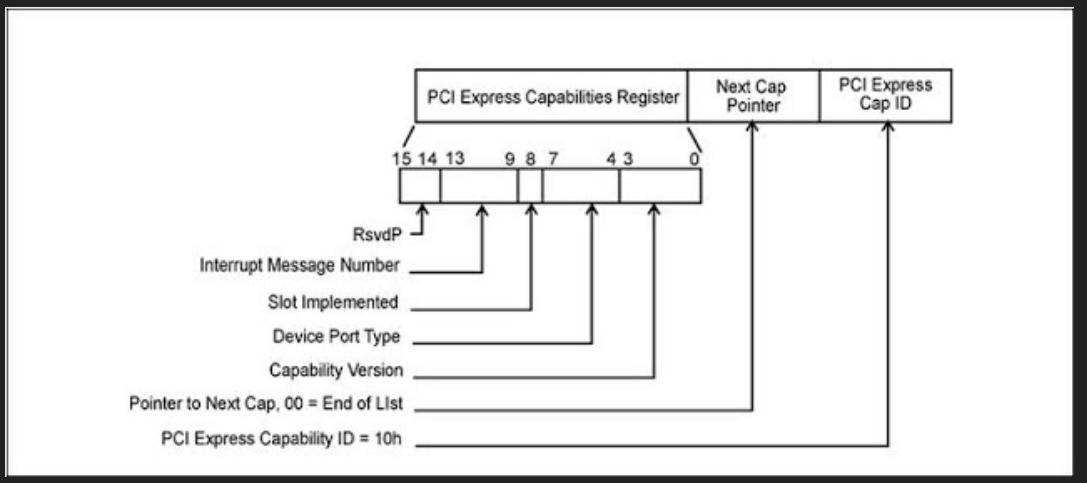
2011年5月25日 星期三

PCIE ASPM

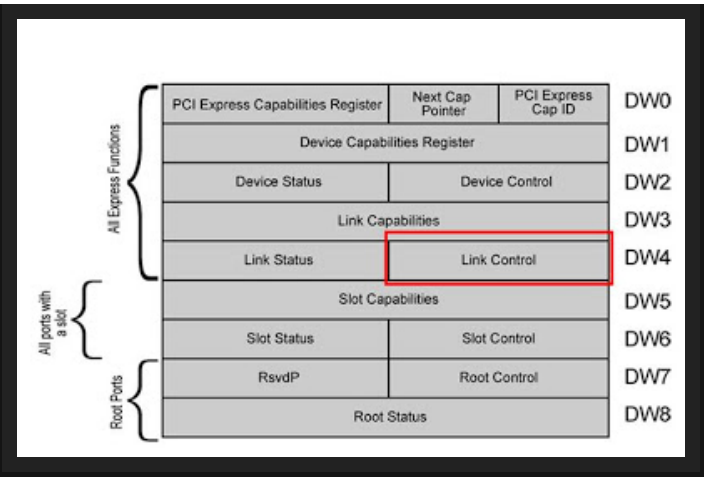
最近常在找PCIE ASPM register,所以寫下來避免自己忘記。
ASPM control register 是存在PCIE Link Control Register。至於如何找到Link Control Register。
1.先找到PCIE Capability List Pointer Register ，而此Register 存在PCI Congfiguration Registers Offset 0x34



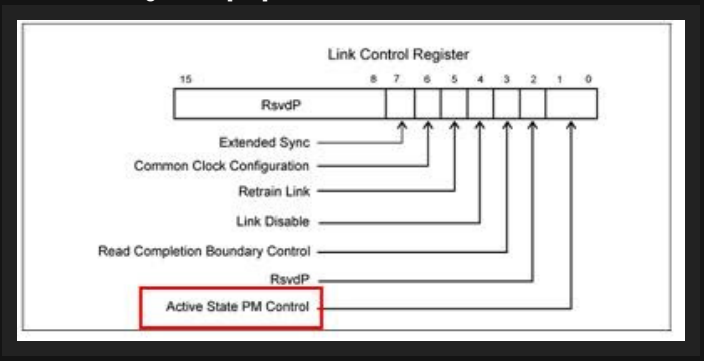
2.檢查Capability ID ((1^{st} byte))是否為0x10，如果不是，讀取Next Capability Pointer Register (2^{nd} byte),讀取下一個Capability.



3. 當Capability ID 為0x10時，Link Control Register就是在目前Capability的Offset+0x10為Link Control Register

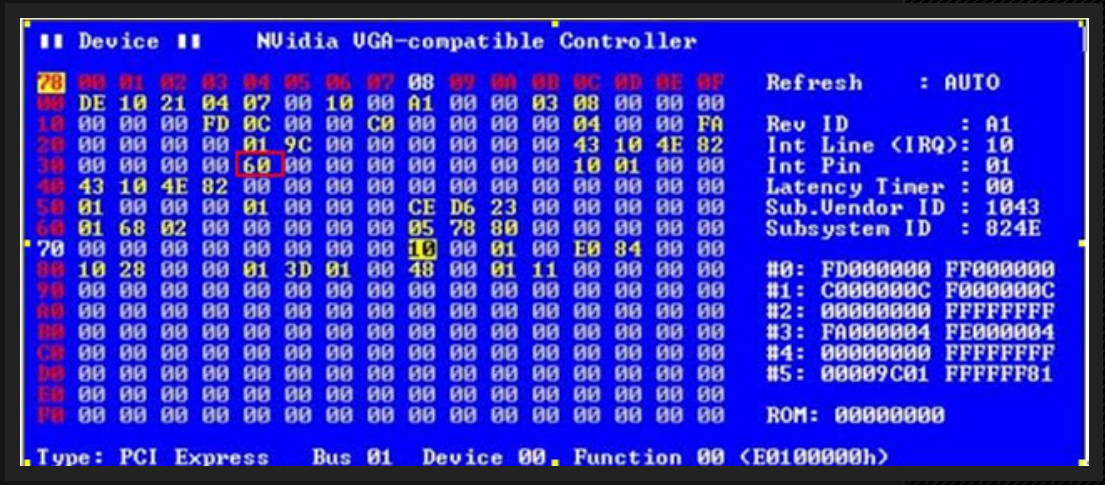


4. Check Link Control Register bit[0:1]

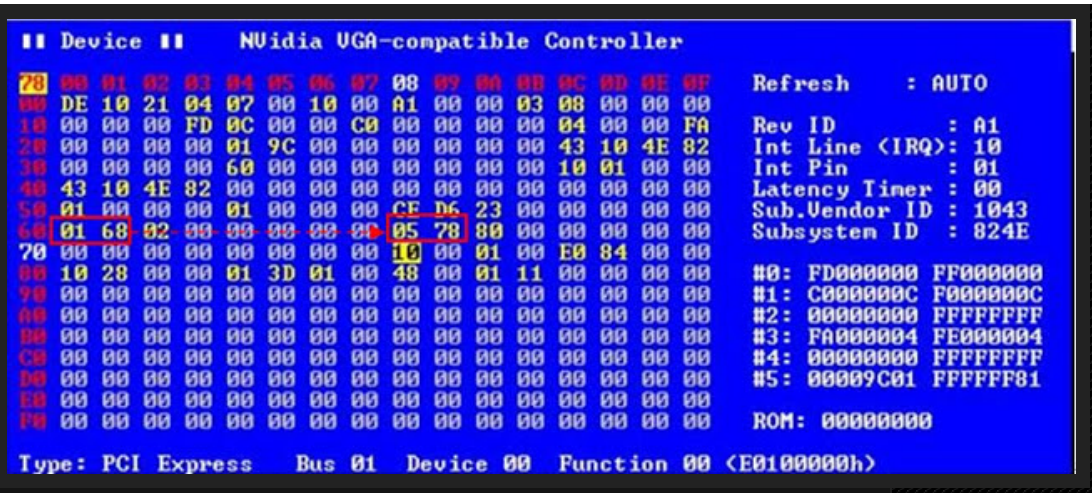


Bits	Definition
00	Disabled
01	L0s Entry Enabled
10	L1 Entry Enabled
11	L0s and L1 Entry Enabled

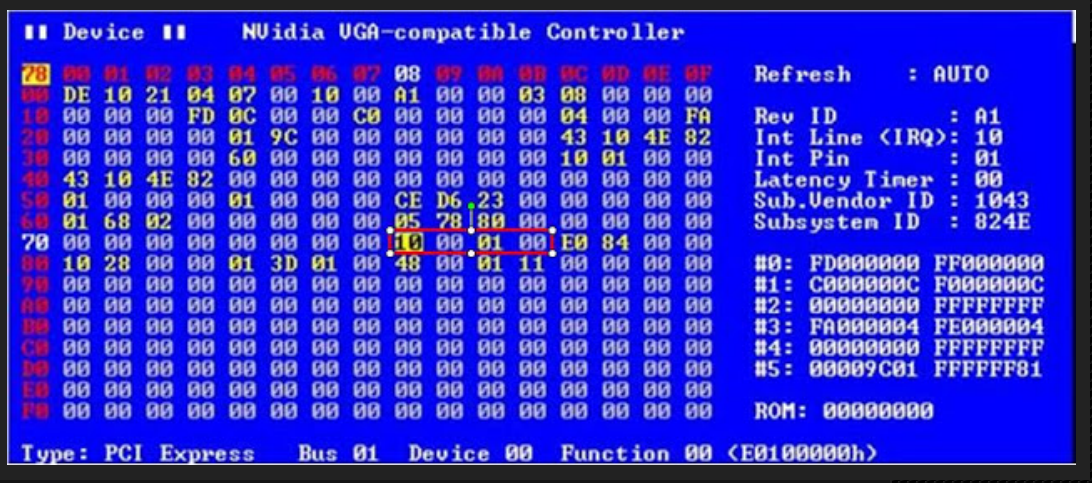
下面就舉個例子來看，比較容易清楚。
1.先找Capability List Pointer Register (offset 0x34), 此register 的值是0x60，表示Capability List 是從Offset 0x60開始。



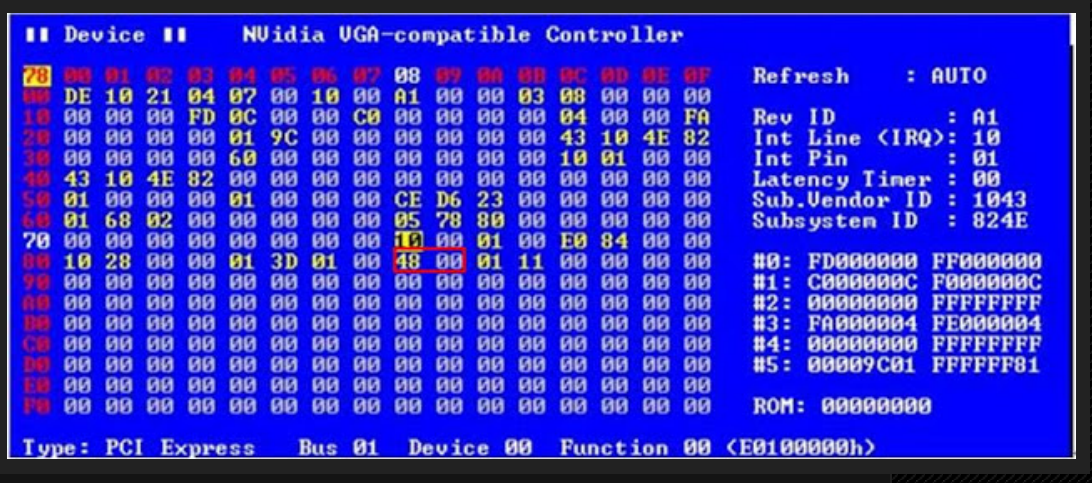
2. 我們要檢查Capability ID是否為0x10,可以看到0ffset 0x60的值是0x01，代表不是PCIE Capability，所以我們要找Next Capability,而Next Capability在Offset 0x61 是0x68，



同樣的Capaiblity ID 為0x05也不是PCIE Capability，所以要找下一個Capability為0x78.



在Offset 0x78的值為0x10，代表是PCIE Capability ID,所以我們可以找到Link Control Register在Offset 0x88~0x89



Check Link Control Register bit[0:1]為0，所以此PCIE Device ASPM 設定為 L0s and L1均為Disable

Table H-1: Capability IDs

ID	Capability
00h	Reserved
01h	PCI Power Management Interface – This capability structure provides a standard interface to control power management features in a PCI device. It is fully documented in the *PCI Power Management Interface Specification*. This document is available from the PCI SIG as described in Chapter 1 of this specification.
02h	AGP – This capability structure identifies a controller that is capable of using Accelerated Graphics Port features. Full documentation can be found in the *Accelerated Graphics Port Interface Specification*. This is available at http://www.agpforum.org.
03h	VPD – This capability structure identifies a device that supports Vital Product Data. Full documentation of this feature can be found in Section 6.4 and Appendix I of this specification.
04h	Slot Identification – This capability structure identifies a bridge that provides external expansion capabilities. Full documentation of this feature can be found in the *PCI to PCI Bridge Architecture Specification*. This document is available from the PCI SIG as described in Chapter 1 of this specification.
05h	Message Signaled Interrupts – This capability structure identifies a PCI function that can do message signaled interrupt delivery as defined in Section 6.8 of this specification.
06h	CompactPCI Hot Swap – This capability structure provides a standard interface to control and sense status within a device that supports Hot Swap insertion and extraction in a CompactPCI system. This capability is documented in the *CompactPCI Hot Swap Specification PICMG 2.1, R1.0* available at http://www.picmg.org.
07h	PCI-X – Refer to the *PCI-X Addendum to the PCI Local Bus Specification* for details.
08h	HyperTransport – This capability structure provides control and status for devices that implement HyperTransport Technology links. For details, refer to the HyperTransport I/O Link Specification available at http://www.hypertransport.org.

ID	Capability
09h	Vendor Specific – This ID allows device vendors to use the capability mechanism for vendor specific information. The layout of the information is vendor specific, except that the byte immediately following the "Next" pointer in the capability structure is defined to be a length field. This length field provides the number of bytes in the capability structure (including the ID and Next pointer bytes). An example vendor specific usage is a device that is configured in the final manufacturing steps as either a 32-bit or 64-bit PCI agent and the Vendor Specific capability structure tells the device driver which features the device supports.
0Ah	Debug port
0Bh	CompactPCI central resource control – Definition of this capability can be found in the *PICMG 2.13 Specification* (http://www.picmg.com).
0Ch	PCI Hot-Plug – This ID indicates that the associated device conforms to the Standard Hot-Plug Controller model.
0Dh	PCI Bridge Subsystem Vendor ID
0Eh	AGP 8x
0Fh	Secure Device
10h	PCI Express
11h	MSI-X – This ID identifies an optional extension to the basic MSI functionality.
12h-0FFh	Reserved

References:
PCI Express System Architecture
PCI Express 3.0 Spec

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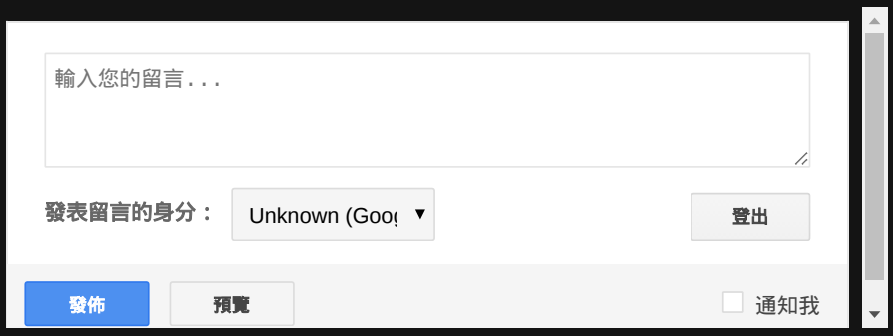
沒有留言:

張貼留言



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訂閱： 張貼留言 (Atom)