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KCU105 PCIe Design Creation

October 2017

Revision History

Date	Version	Description
10/09/17	12.0	Updated for 2017.3.
06/20/17	11.0	Updated for 2017.2.
04/19/17	10.0	Updated for 2017.1.
12/19/16	9.0	Updated for 2016.4.
10/13/16	8.0	Updated for 2016.3.
06/08/16	7.0	Updated for 2016.2.
04/13/16	6.0	Updated for 2016.1
11/24/15	5.0	Updated for 2015.4.
10/06/15	4.0	Updated for 2015.3
06/30/15	3.0	Updated for 2015.2.
04/30/15	2.0	Updated for 2015.1. Added AR64404.
03/06/15	1.0	Initial version.

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Overview

- Kintex UltraScale PCIe x8 Gen 3 Capability
- Xilinx KCU105 Board
- KCU105 Software Install and Board Setup
- KCU105 Setup
- Generate x8 Gen 3 PCIe Core
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 - Compile Example Design
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Kintex UltraScale PCIe x8 Gen 3 Capability

► KCU105 Supports PCIe Gen 1, Gen 2, and Gen 3 Capability

- x8, x4, x2, or x1 Gen 1, Gen 2, and Gen 3 lane width
- x8 Gen 3 supported in -2 and -3 speed grades
- See [DS892](#) for details

► LogiCORE PIO Example Design

- RDF0316 - KCU105 PCIe Design Files (2017.3 C) ZIP file

► UltraScale Integrated Block for PCI Express

- See [PG156](#) for details

Kintex UltraScale PCIe x8 Gen 3 Capability

➤ Integrated Block for PCI Express

- PCI Express 3.0 Specification

➤ Configurable for Endpoint or Root Port Applications

- KCU105 configured for Endpoint Applications

➤ GTH Transceivers implement a fully compliant PHY

➤ Large range of maximum payload size

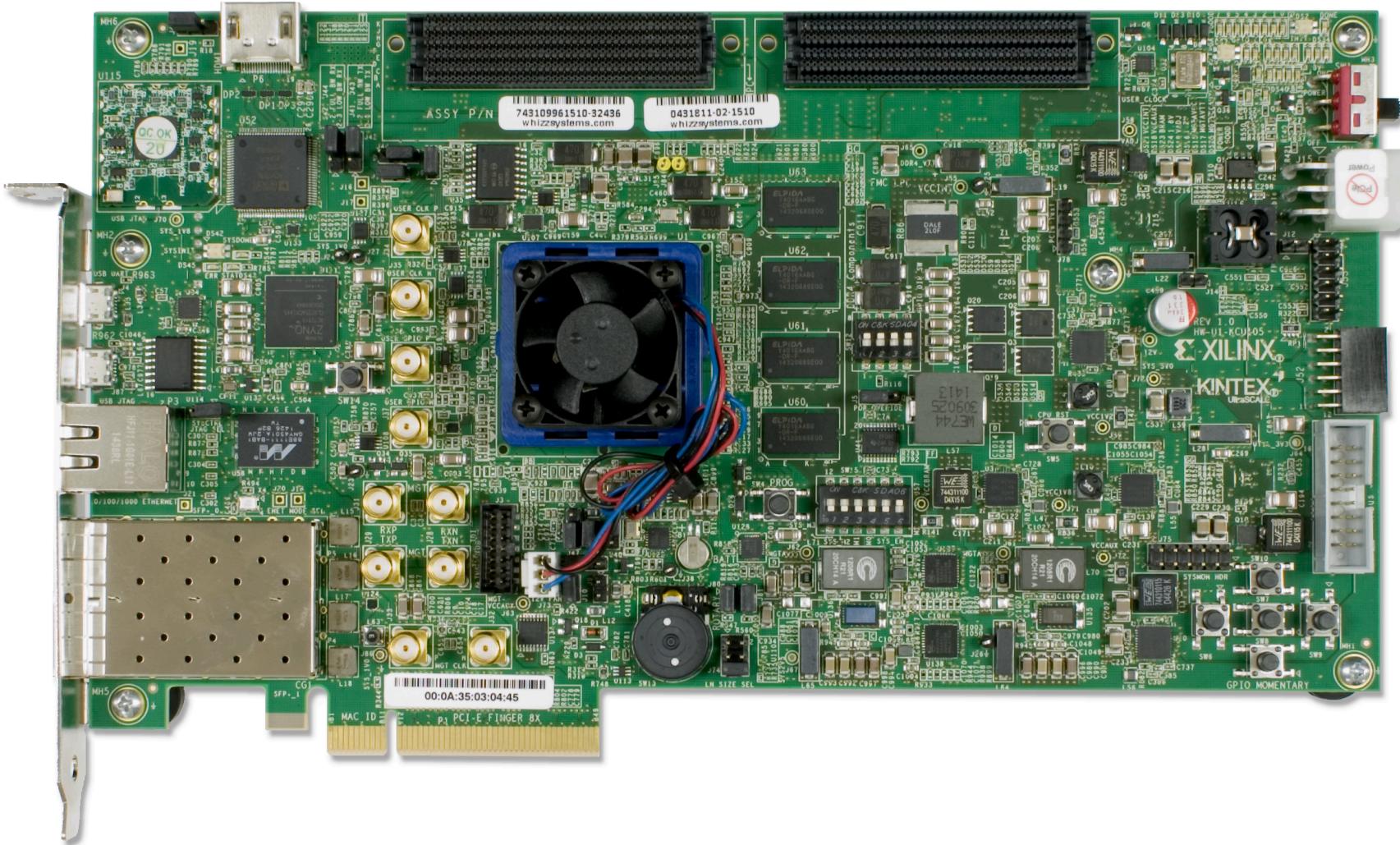
- 128 / 256 / 512 / 1024 bytes

➤ Configurable BAR spaces

- Up to 6 x 32 bit, 3 x 64 bit, or a combination
- Memory or IO
- BAR and ID filtering

➤ Management and Statistics Interface

Xilinx KCU105 Board



KCU105 Software Install and Board Setup

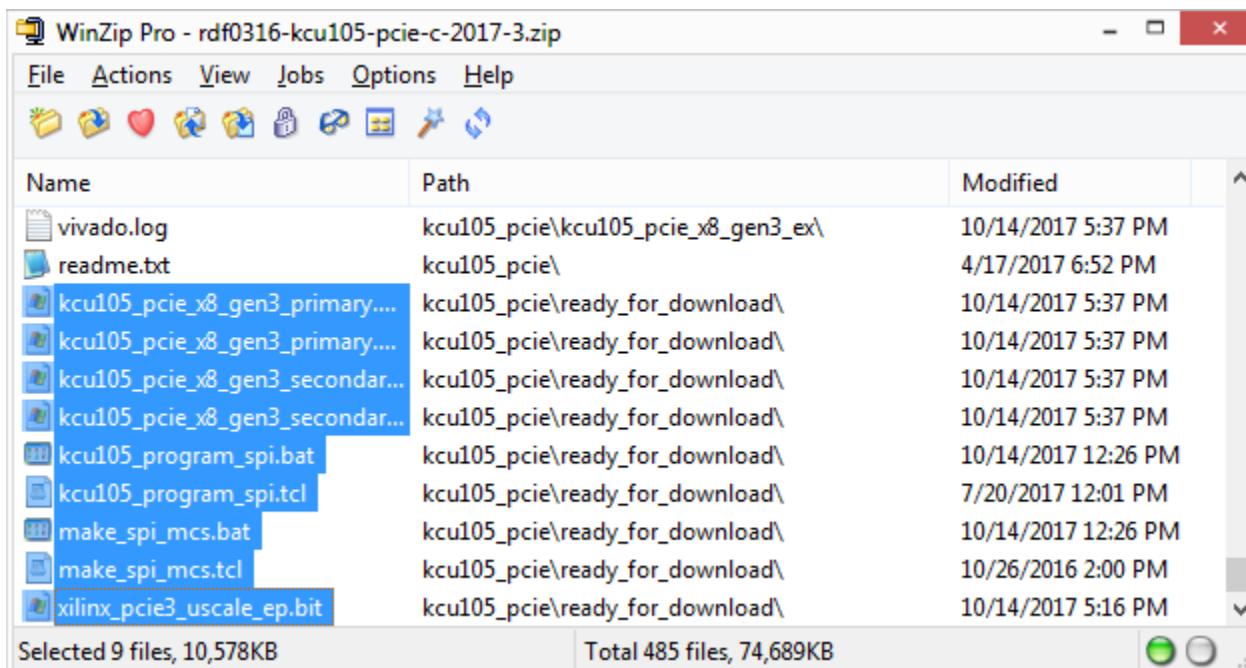
► Refer to XTP352 – KCU105 Software Install and Board Setup for details on:

- Software Requirements
- KCU105 Board Setup



Files needed for PCIe design

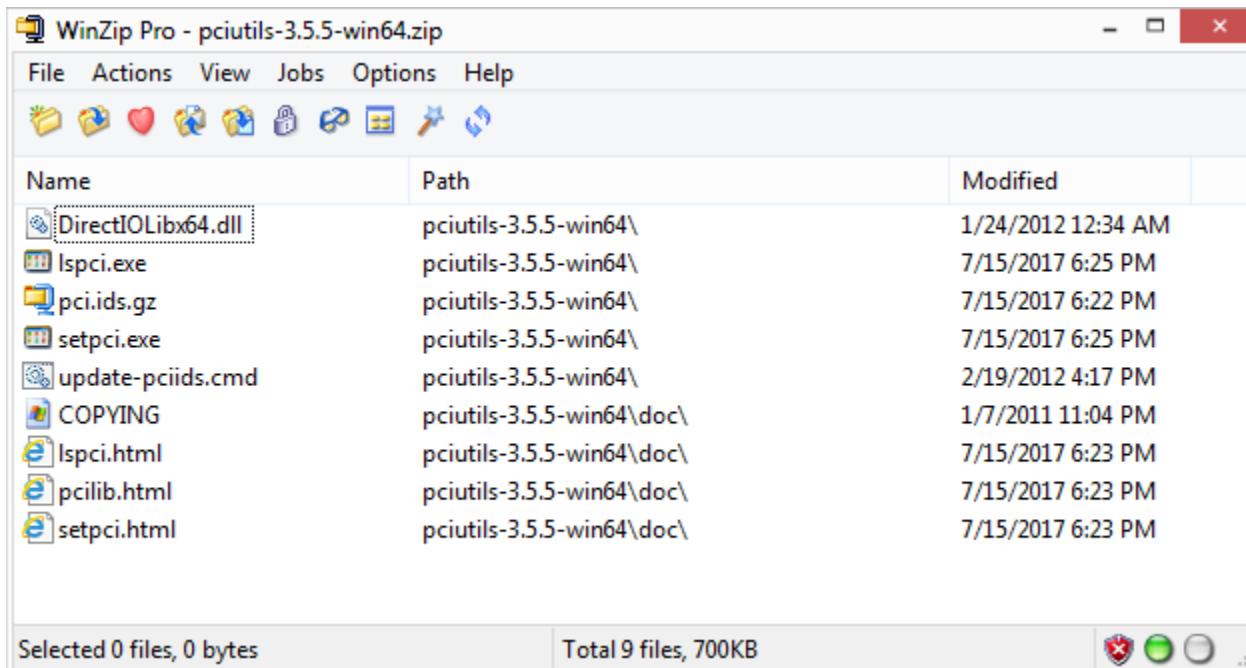
- Open the KCU105 PCIe Design Files (2017.3 C) ZIP file, and extract these files to your C:\ drive:
 - kcu105_PCIE\ready_for_download*



lspci Software Requirement

► lspci for Windows

- Free [download](#)
- Unzip to the C:\ drive of the test PC



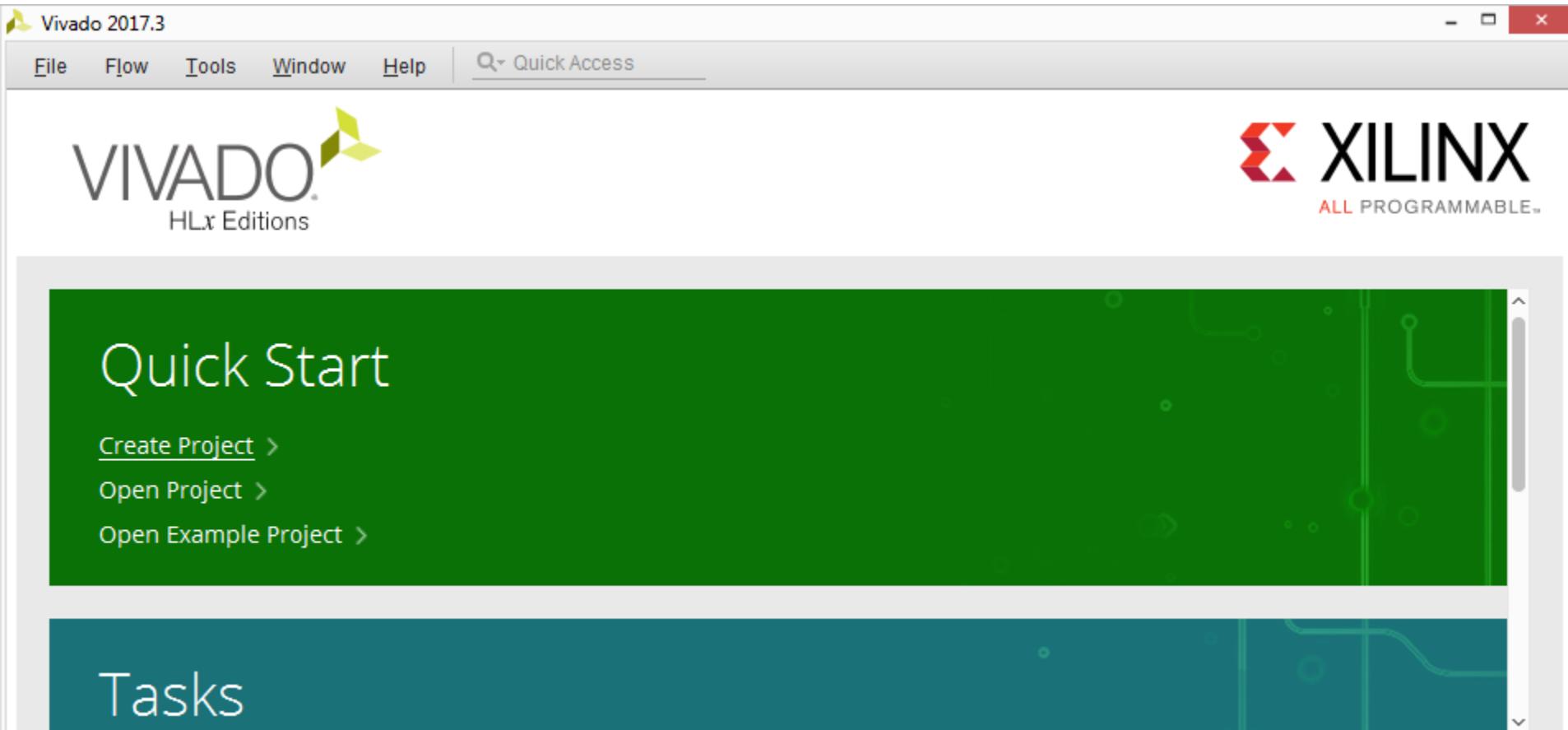
Generate x8 Gen 3 PCIe Core

Generate x8 Gen 3 PCIe Core

► Open Vivado

Start → All Programs → Xilinx Design Tools → Vivado 2017.3 → Vivado

► Select Create Project



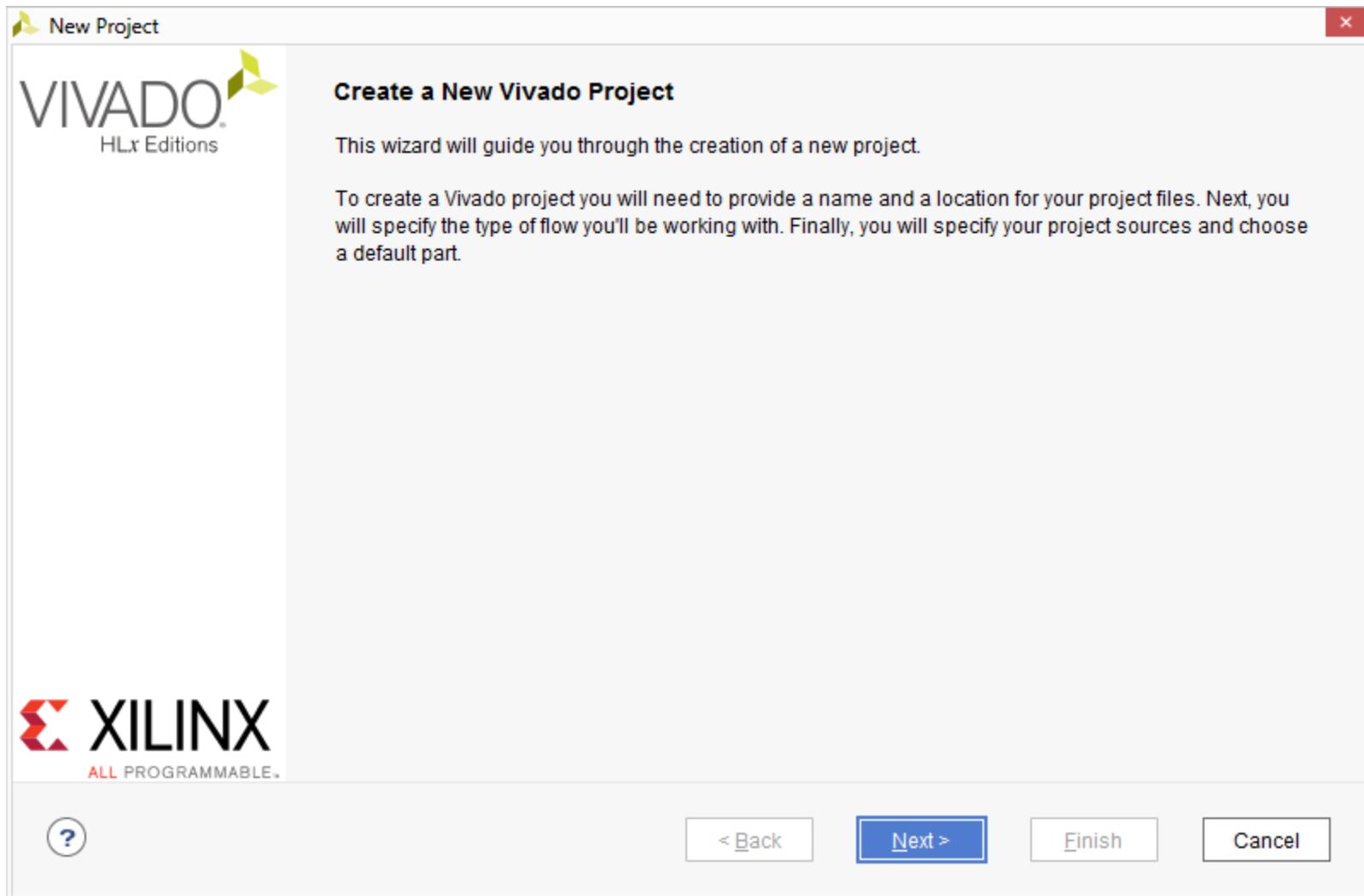
New Project Wizard will guide you through the process of selecting design sources and a target device for a new project.

Note: Presentation applies to the KCU105

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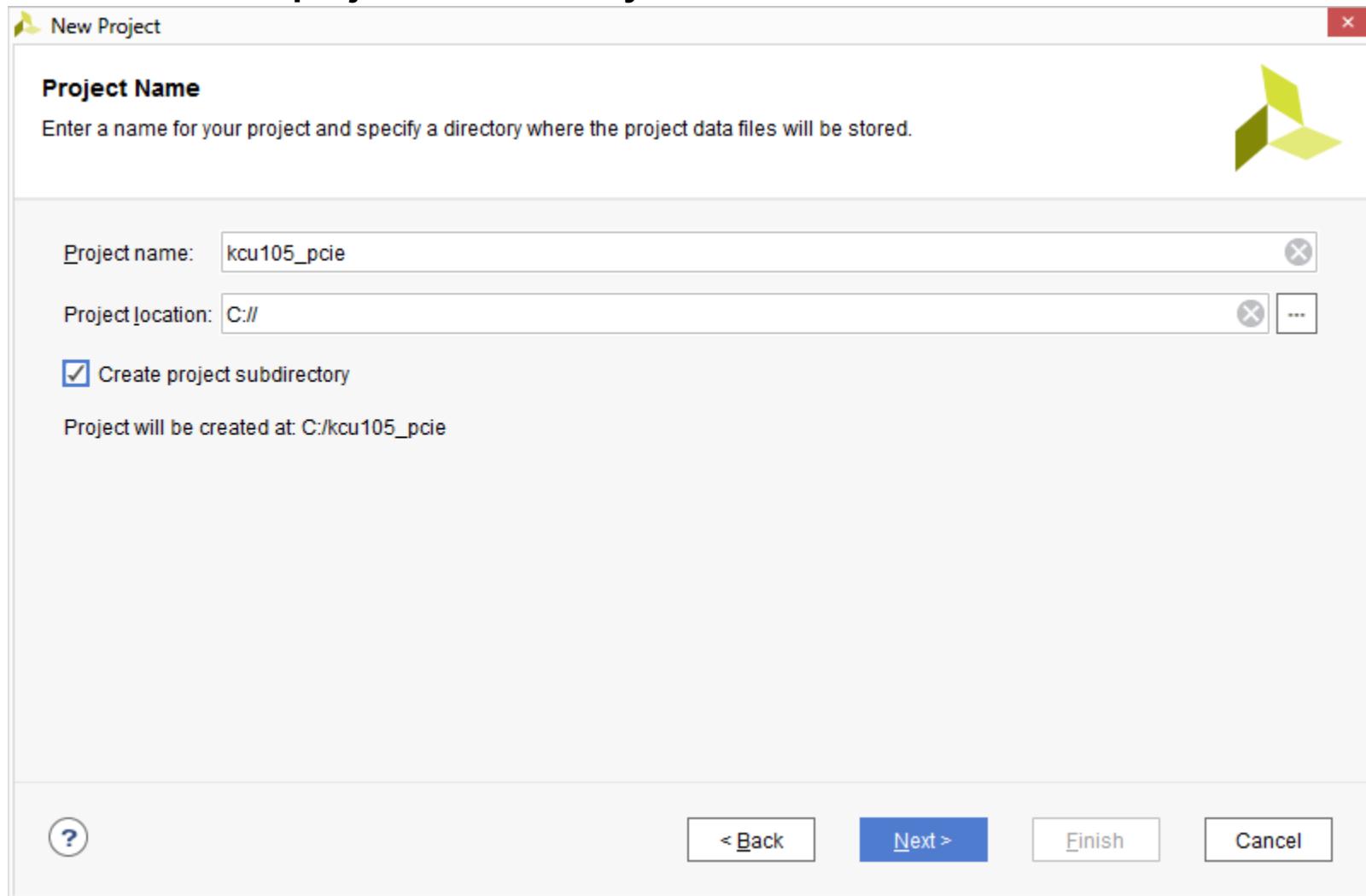
Generate x8 Gen 3 PCIe Core

► Click Next



Generate x8 Gen 3 PCIe Core

- Set the Project name and location to **kcu105_pcnie** and **C:/**
 - Check **Create project subdirectory**



Note: Vivado generally requires forward slashes in paths

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Generate x8 Gen 3 PCIe Core

► Select RTL Project

- Select **Do not specify sources at this time**

New Project

Project Type
Specify the type of project to create.



RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
 Do not specify sources at this time

Post-synthesis Project: You will be able to add sources, view device resources, run design analysis, planning and implementation.
 Do not specify sources at this time

I/O Planning Project
Do not specify design sources. You will be able to view part/package resources.

Imported Project
Create a Vivado project from a Synplify, XST or ISE Project File.

Example Project
Create a new Vivado project from a predefined template.

[?](#) [< Back](#) [Next >](#) [Finish](#) [Cancel](#)

Generate x8 Gen 3 PCIe Core

► Select the KCU105 Evaluation Platform

New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select: Parts Boards

Filter/ Preview

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

Search:

Display Name	Vendor	Board Rev	Part
Kintex-7 KC705 Evaluation Platform	xilinx.com	1.1	xc7k325tffg900-2
Kintex-UltraScale KCU105 Evaluation Platform	xilinx.com	1.0	xcu040-ffva1156-2-e
Kintex UltraScale+ KCU116 Evaluation Platform	xilinx.com	1.0	xcu5n-ffvh676-2-e

Board Connectors Target Connections

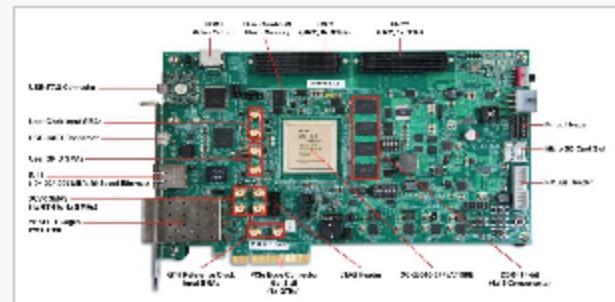
?

< Back

Next >

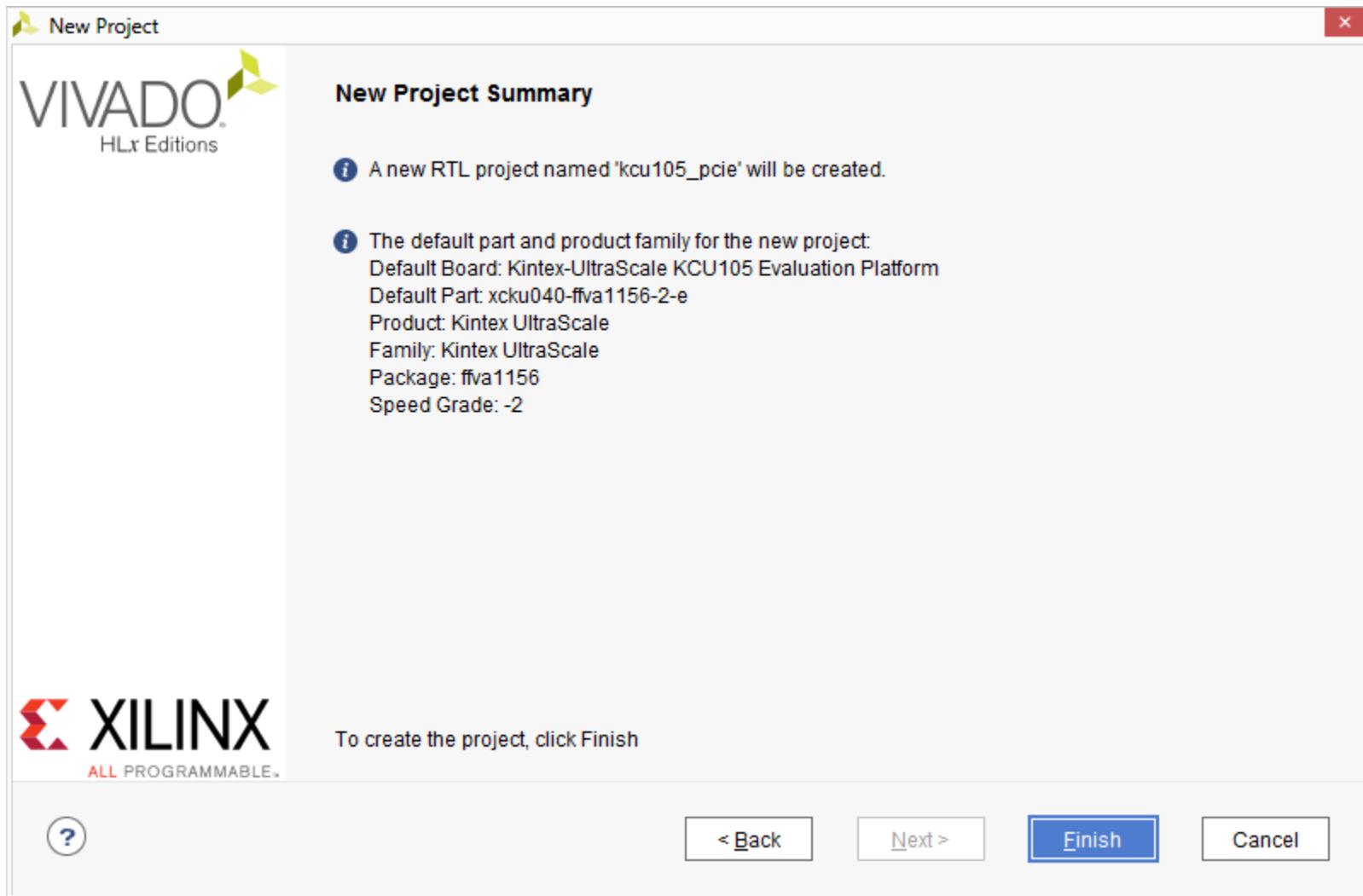
Finish

Cancel



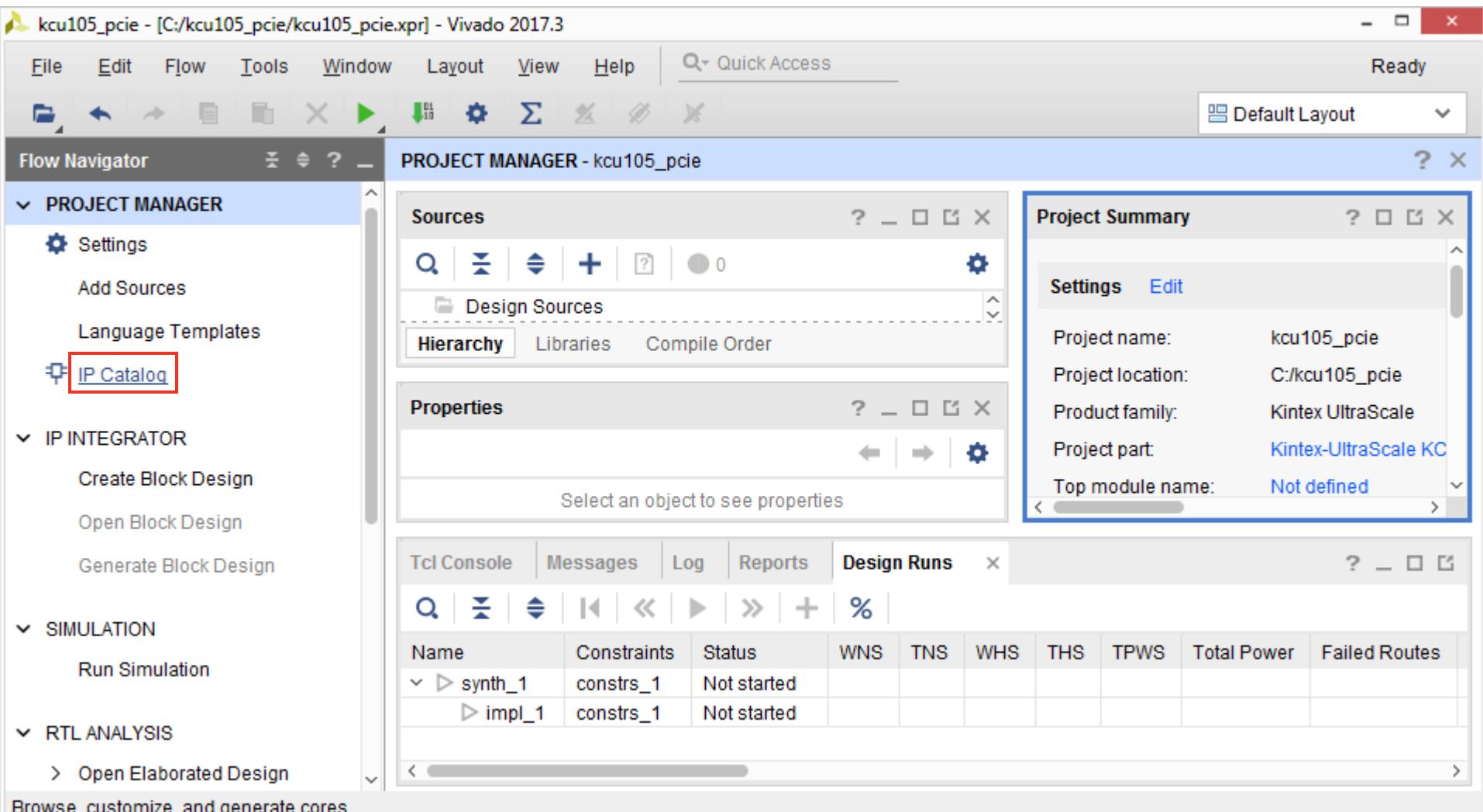
Generate x8 Gen 3 PCIe Core

► Click Finish



Generate x8 Gen 3 PCIe Core

► Click on IP Catalog



Generate x8 Gen 3 PCIe Core

► Select UltraScale FPGA Gen3 Integrated Block for PCI Express, v4.4 under Standard Bus Interfaces

The screenshot shows the Vivado 2017.3 interface with the project "kcu105_PCIE" open. The left sidebar contains sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, and RTL ANALYSIS. The IP INTEGRATOR section is expanded, showing options like Create Block Design, Open Block Design, and Generate Block Design. The central area is the PROJECT MANAGER, which has tabs for Project Summary and IP Catalog. The IP Catalog tab is selected, displaying the "Cores" section. Under "Standard Bus Interfaces" > "PCI Express", the "UltraScale FPGA Gen3 Integrated Block for PCI Express" is selected, highlighted with a blue border. Below the table, the "Details" section shows the selected IP's name and version: "Name: UltraScale FPGA Gen3 Integrated Block for PCI Express" and "Version: 4.4". The bottom navigation bar includes tabs for Tcl Console, Messages, Log, Reports, and Design Runs.

Name	Status	License	
AXI Bridge for PCI Express Gen3 Subsystem	AXI4, AXI4-Stream	Production	Included
DMA/Bridge Subsystem for PCI Express (PCIe)	AXI4, AXI4-Stream	Production	Included
PCIe PHY IP		Production	Included
UltraScale FPGA Gen3 Integrated Block for PCI E...	AXI4-Stream	Production	Included

IP: UltraScale FPGA Gen3 Integrated Block for PCI Express

Note: Presentation applies to the KCU105

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Generate x8 Gen 3 PCIe Core

► Right click on **UltraScale FPGA Gen3 Integrated Block for PCI Express** and select **Customize IP...**

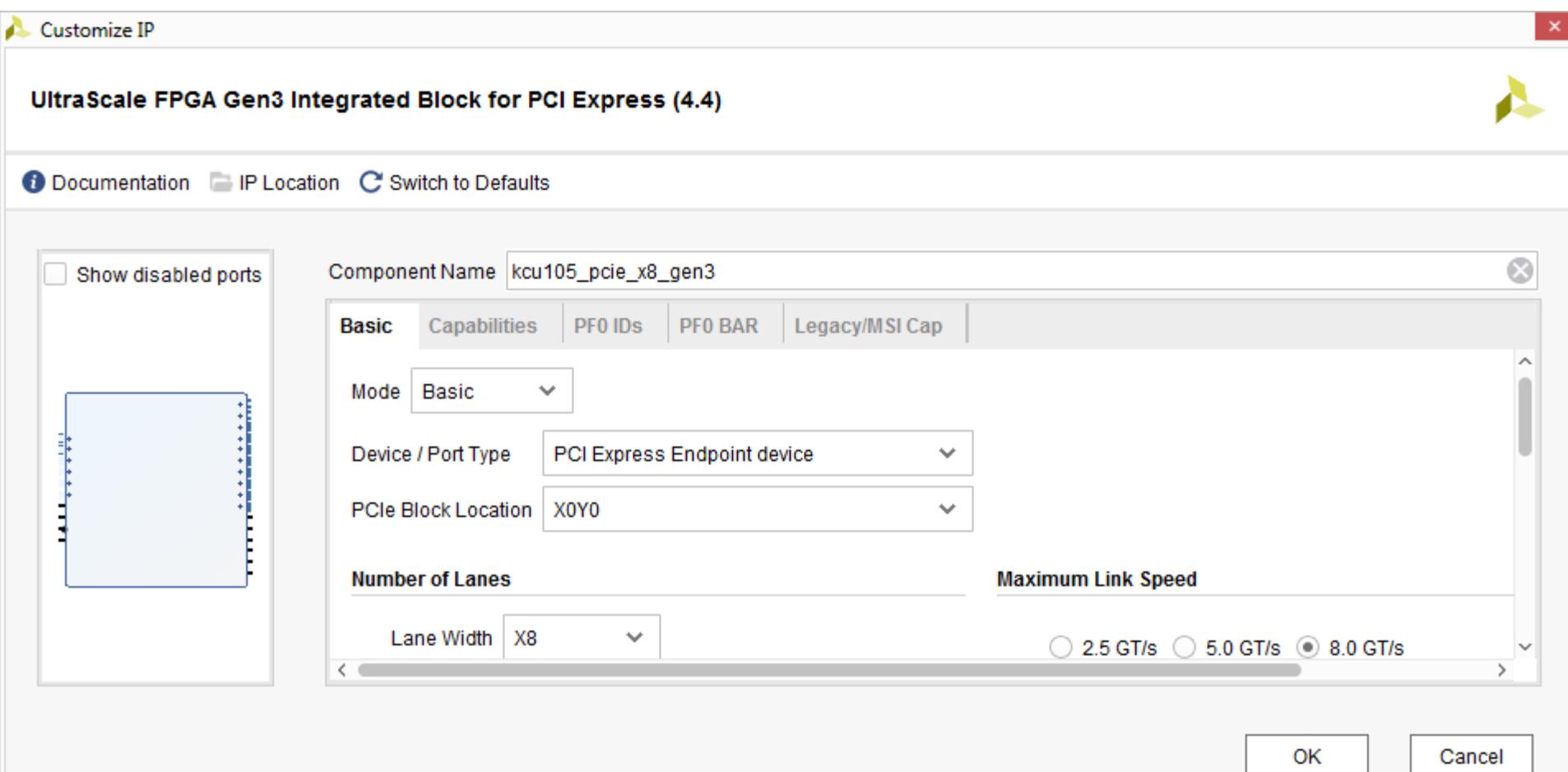
The screenshot shows the Vivado 2017.3 interface with the project "kcu105_PCIE" open. The left sidebar has sections for PROJECT MANAGER, IP INTEGRATOR, SIMULATION, and RTL ANALYSIS. The PROJECT MANAGER section is expanded, showing options like Settings, Add Sources, Language Templates, and IP Catalog. The IP Catalog option is selected. The main area is the PROJECT MANAGER - kcu105_PCIE window, which contains tabs for Project Summary and IP Catalog. The IP Catalog tab is active, showing a list of cores under Cores | Interfaces. The list includes AXI4, Standard Bus Interfaces, PCI Express, AXI Bridge for PCI Express Gen3 Subsystem, DMA/Bridge Subsystem for PCI Express (PCIe), PCIe PHY IP, and UltraScale FPGA Gen3 Integrated Block for PCI E... (which is highlighted). Below the list is a Details panel showing Name: UltraScale FPGA Gen3 Integrated Block for PCI E and Version: 4.4. A context menu is open over the highlighted core, with options Properties..., IP Settings..., Add Repository..., Refresh All Repositories, Customize IP... (which is highlighted in blue), License Status, and Compatible Families.

Name	Status	License
AXI4	Production	Included
Standard Bus Interfaces		
PCI Express		
AXI Bridge for PCI Express Gen3 Subsystem	AXI4, AXI4-Stream	Production
DMA/Bridge Subsystem for PCI Express (PCIe)	AXI4, AXI4-Stream	Production
PCIe PHY IP		Production
UltraScale FPGA Gen3 Integrated Block for PCI E...		Included

Generate x8 Gen 3 PCIe Core

► Under the **Basic** tab,

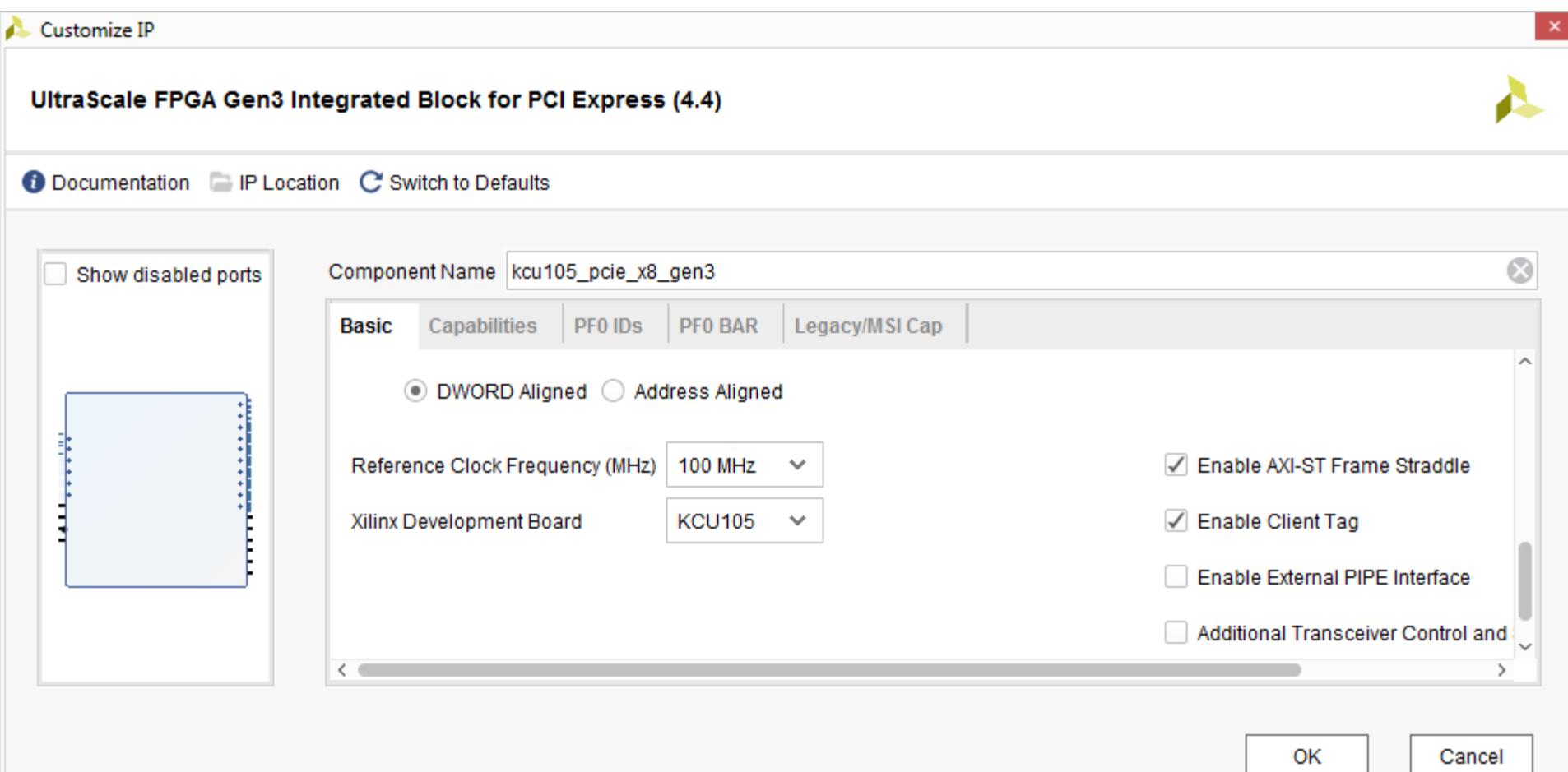
- Set Component name to **kcu105_pcie_x8_gen3**
- Set the Lane Width to **X8**
- Set the Max Link Speed to **8.0 GT/s**



Generate x8 Gen 3 PCIe Core

► Under the **Basic** tab,

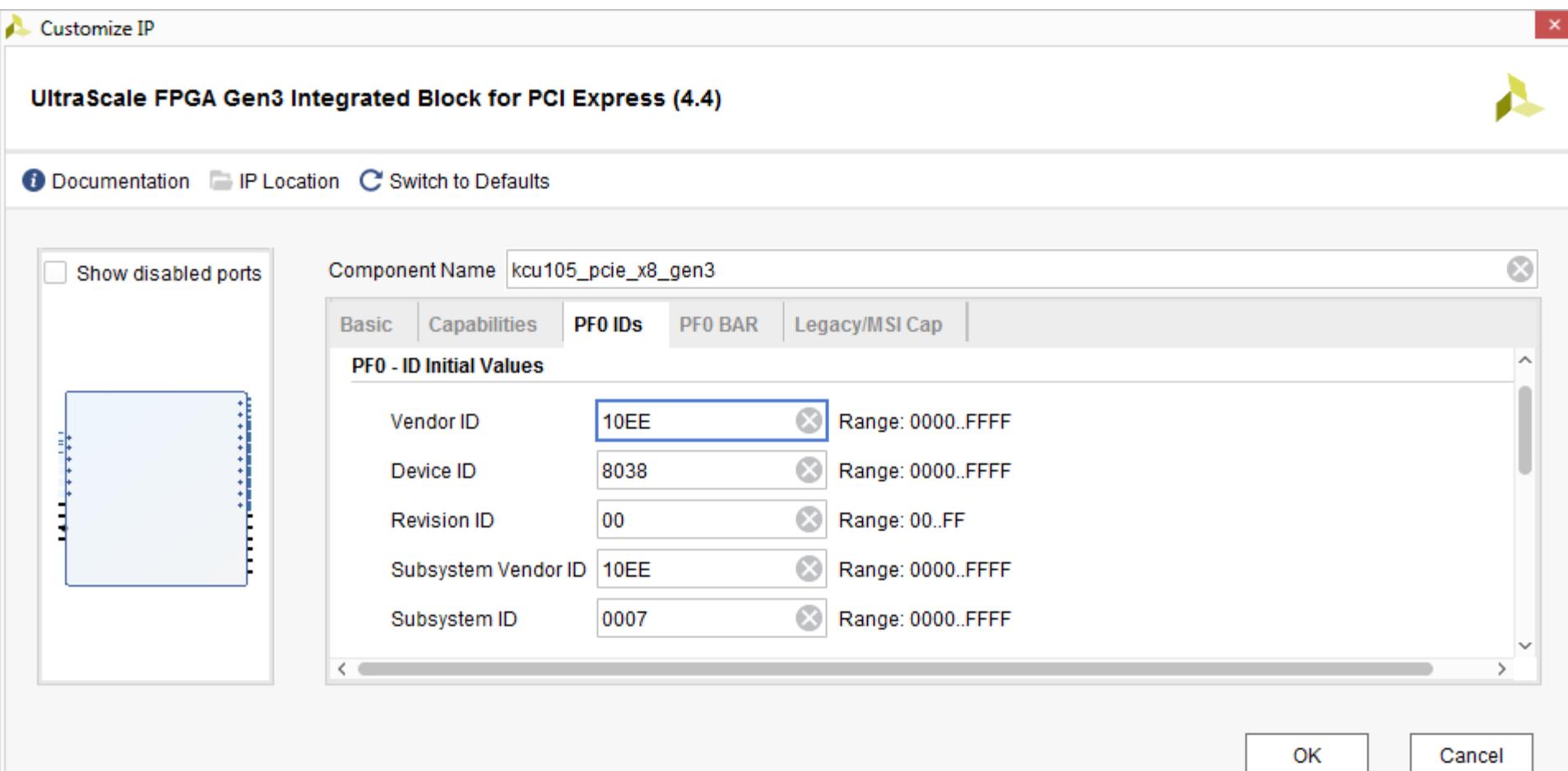
- Set the Ref Clock to **100 MHz**
- Set Development Board to **KCU105**



Generate x8 Gen 3 PCIe Core

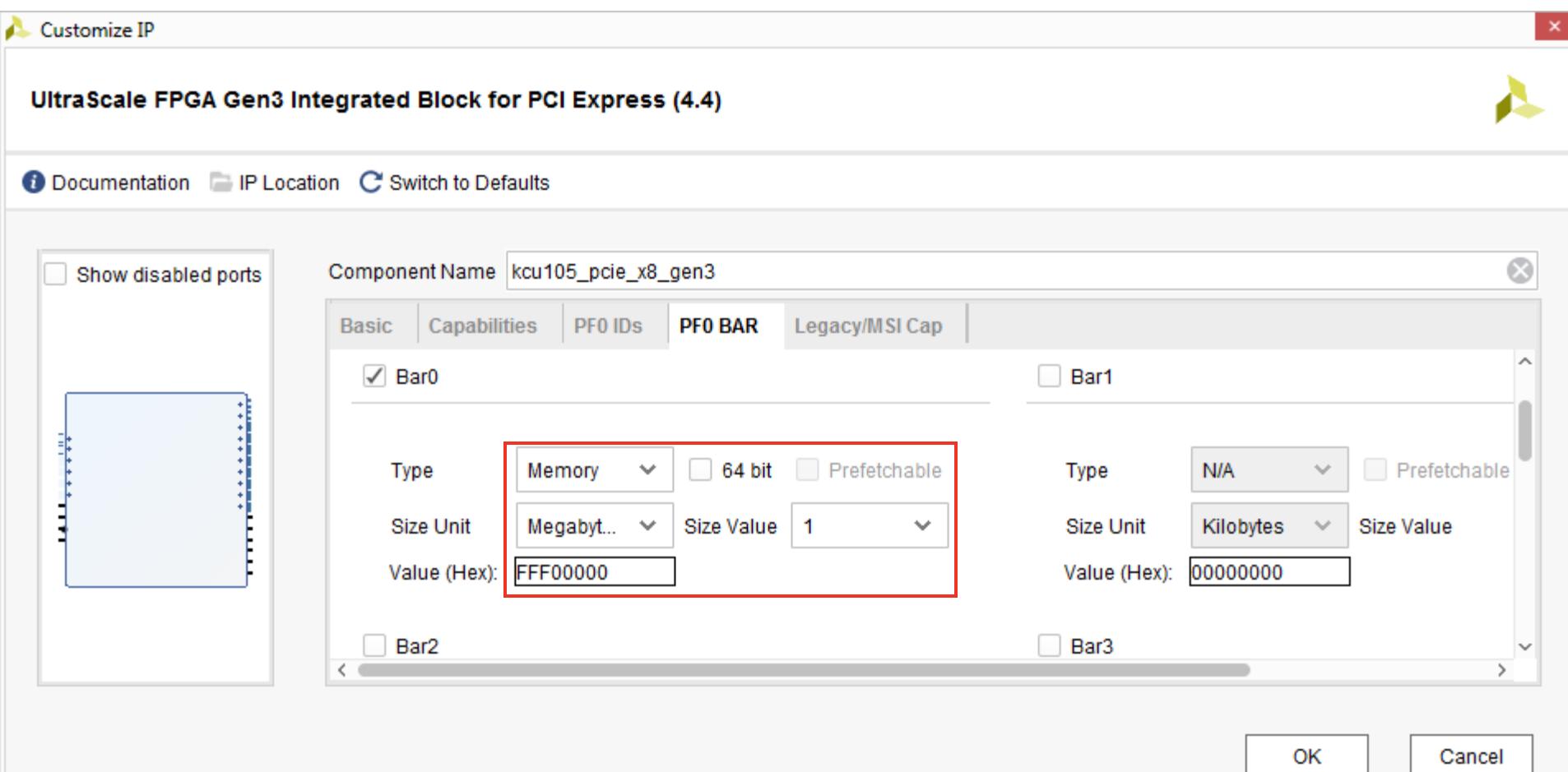
► Under the **PF0 IDs** tab, note the ID Initial Values

- Vendor ID = **10EE**; Device ID = **8038**; Revision ID = **00**
- Subsystem Vendor ID = **10EE**; Subsystem ID = **0007**



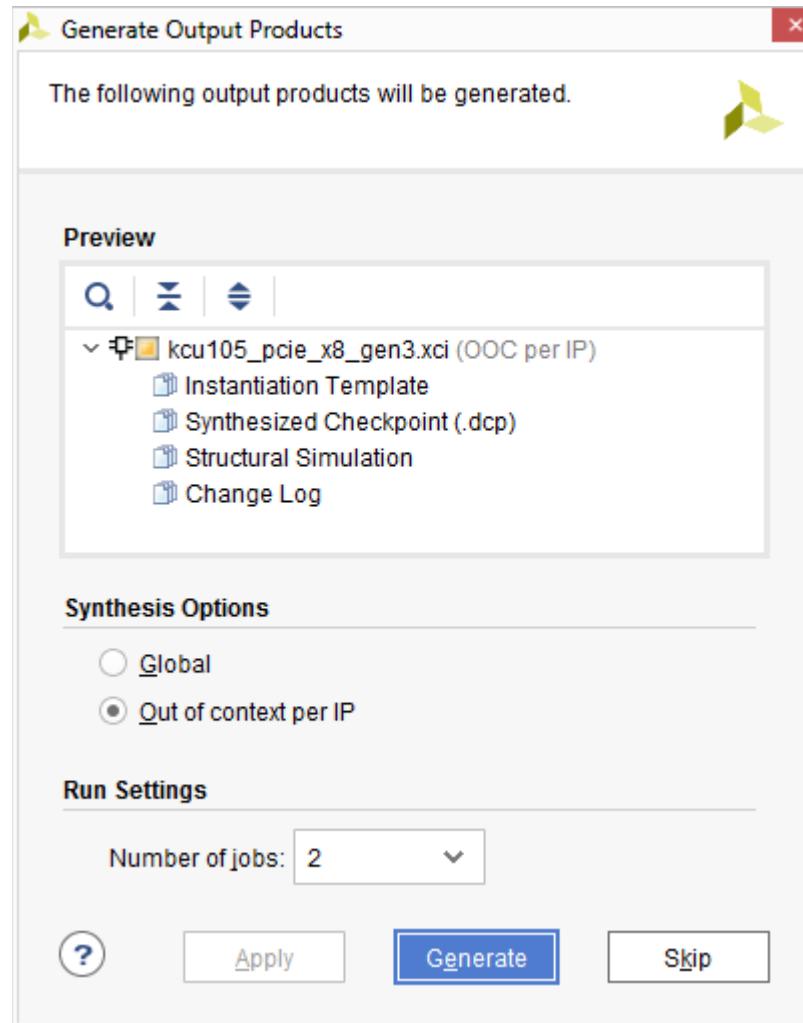
Generate x8 Gen 3 PCIe Core

- Under the PF0 BAR tab, set BAR 0
 - Set to 1 Megabytes
- Click OK



Generate x8 Gen 3 PCIe Core

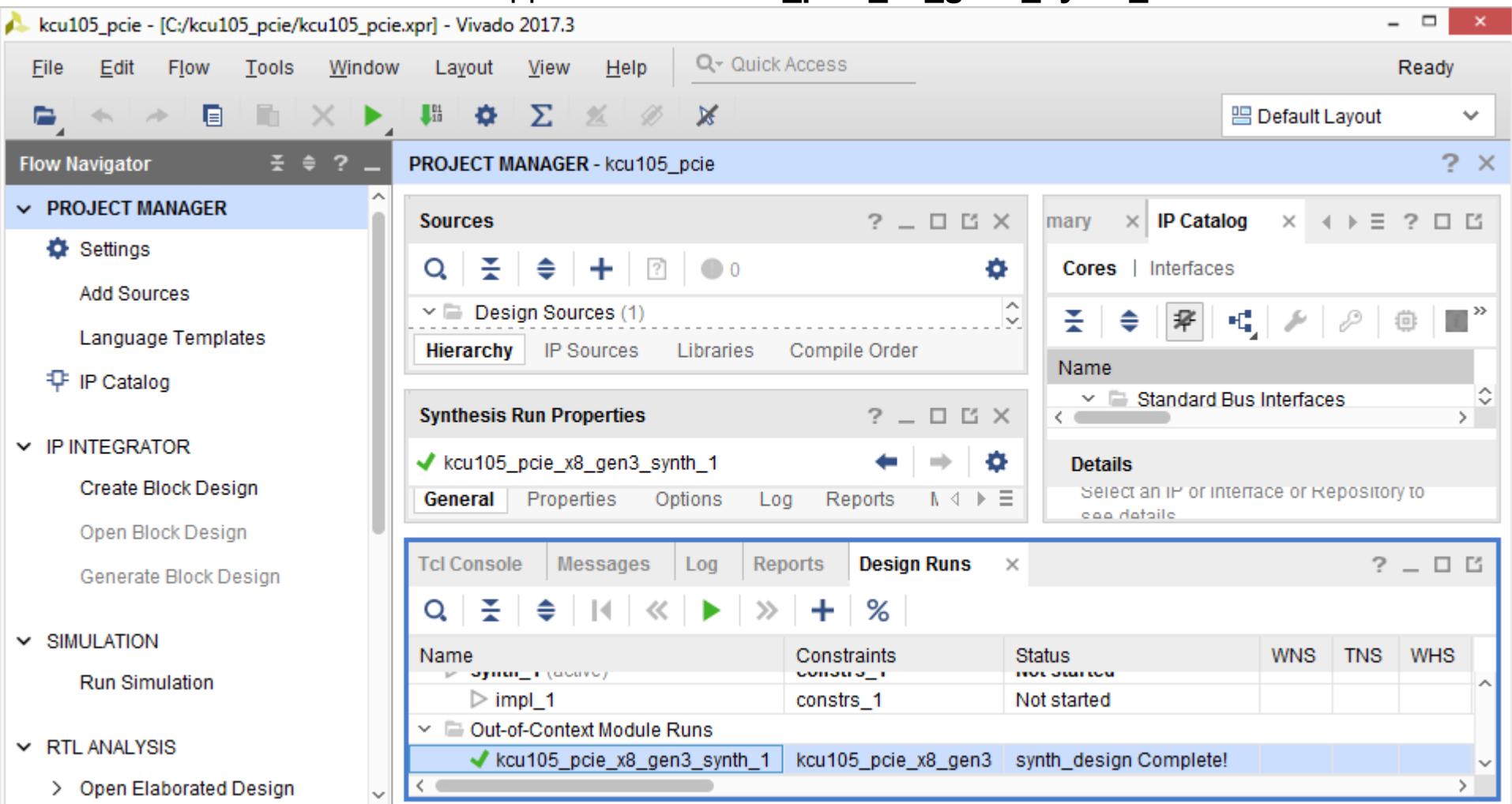
► Click Generate



Generate x8 Gen 3 PCIe Core

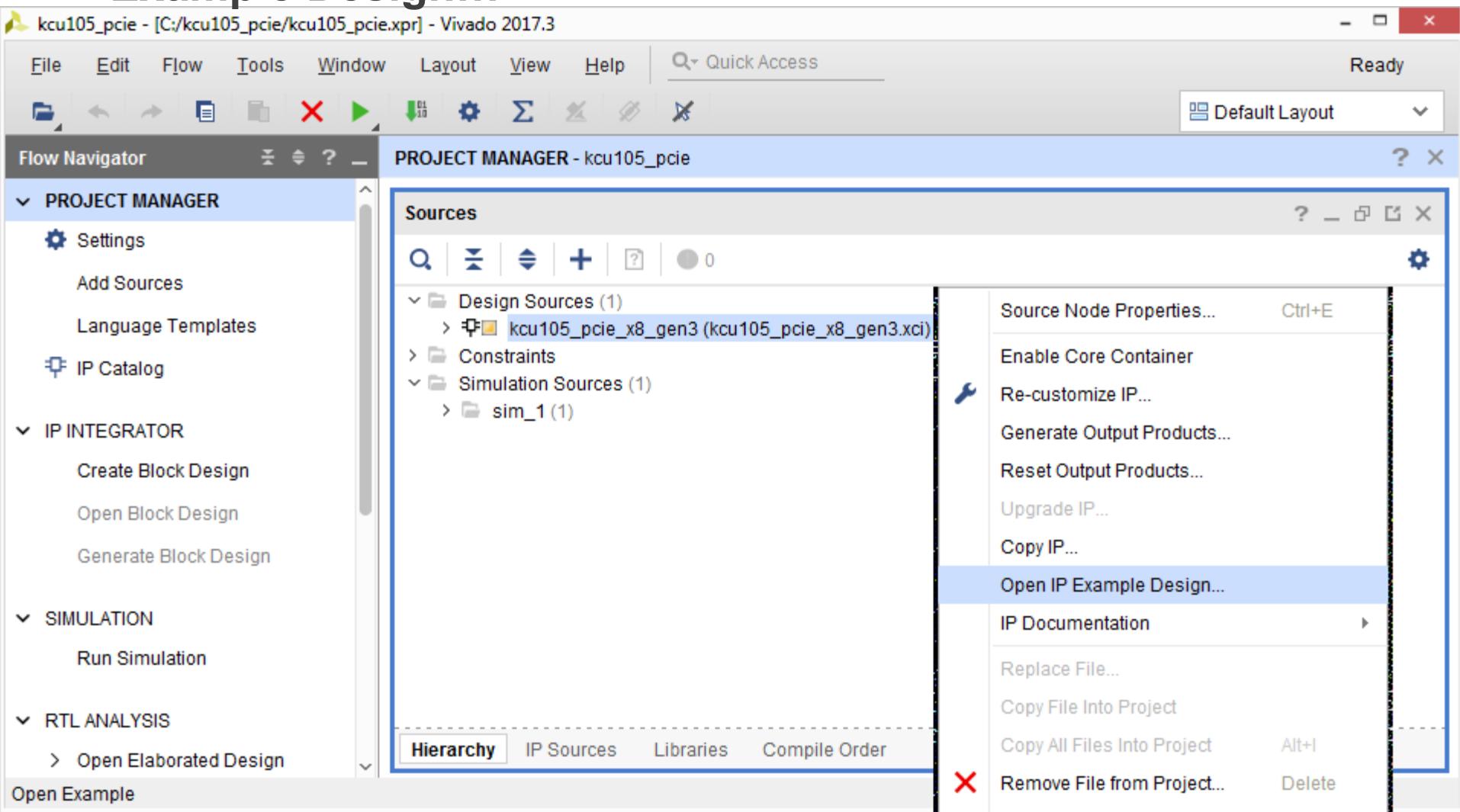
► PCIe design appears in Design Sources

- Wait until checkmark appears on **kcu105_pcie_x8_gen3_synth_1**



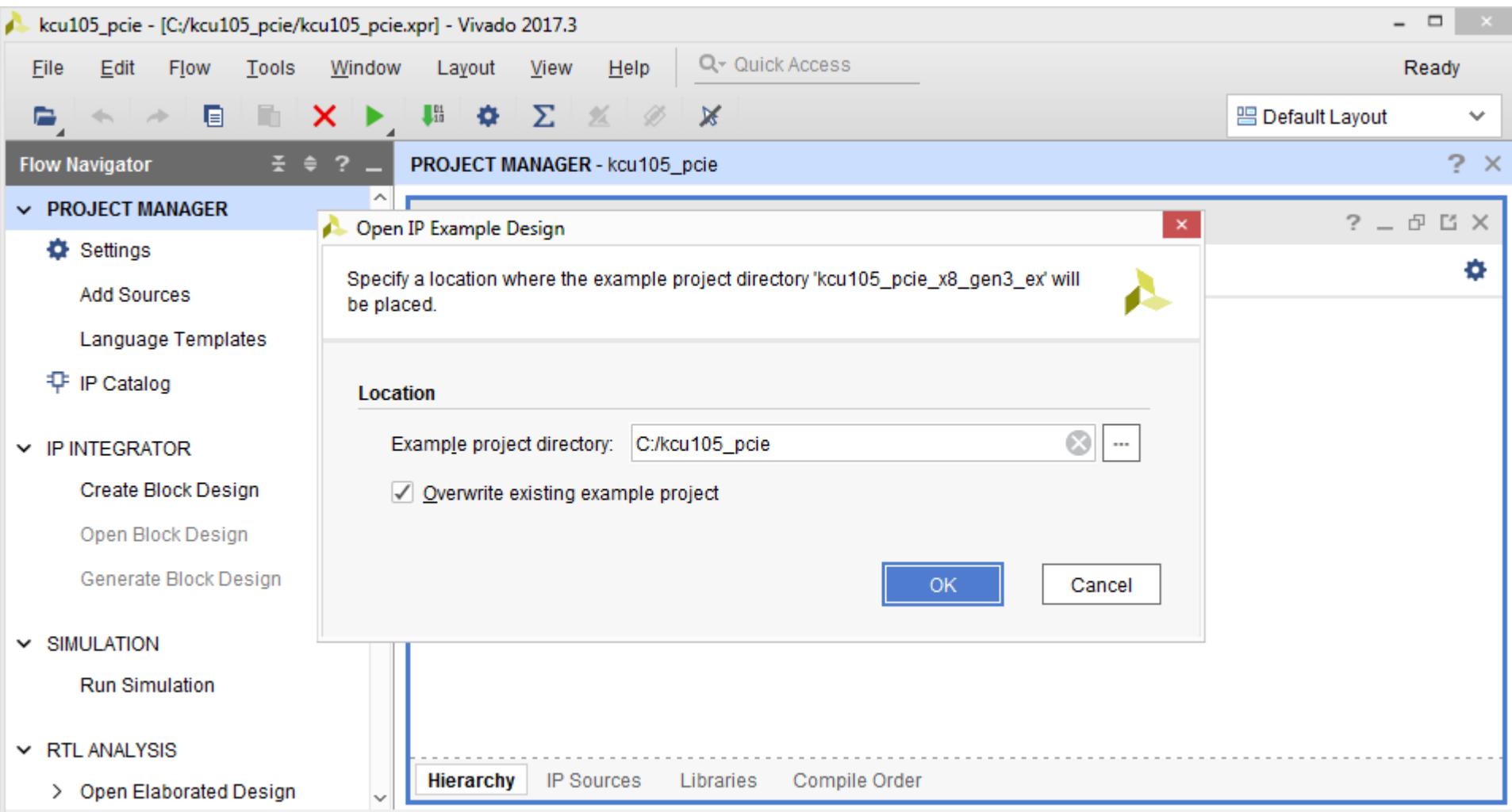
Generate x8 Gen 3 PCIe Core

► Right-click on **kcu105_pcie_x8_gen3** and select **Open IP Example Design...**



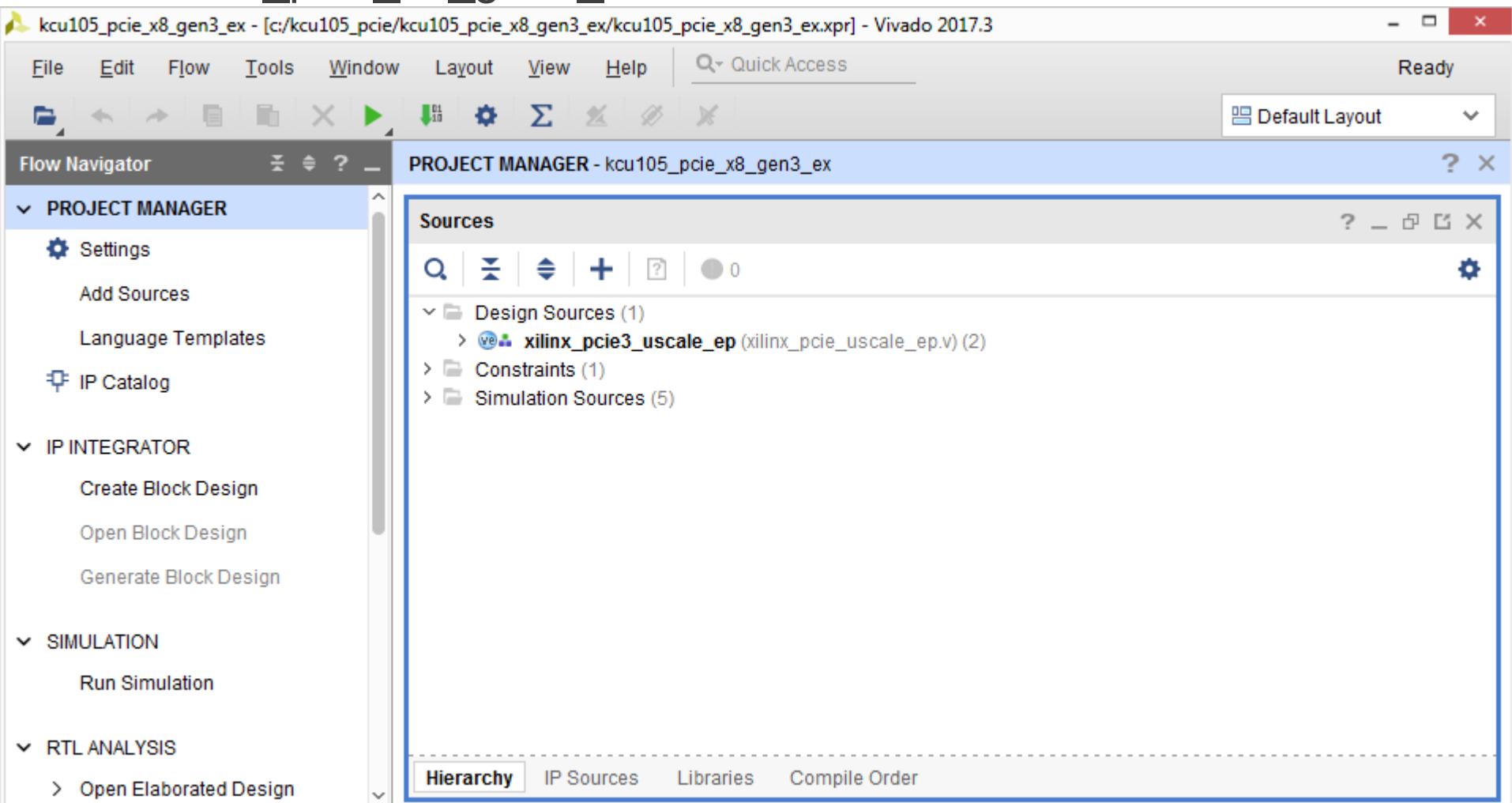
Generate x8 Gen 3 PCIe Core

► Set the location to **C:/kcu105_pcnie** and click **OK**



Generate x8 Gen 3 PCIe Core

- A new project is created under <design path>/
kcu105_pcie_x8_gen3_ex



Note: The original project window can be closed

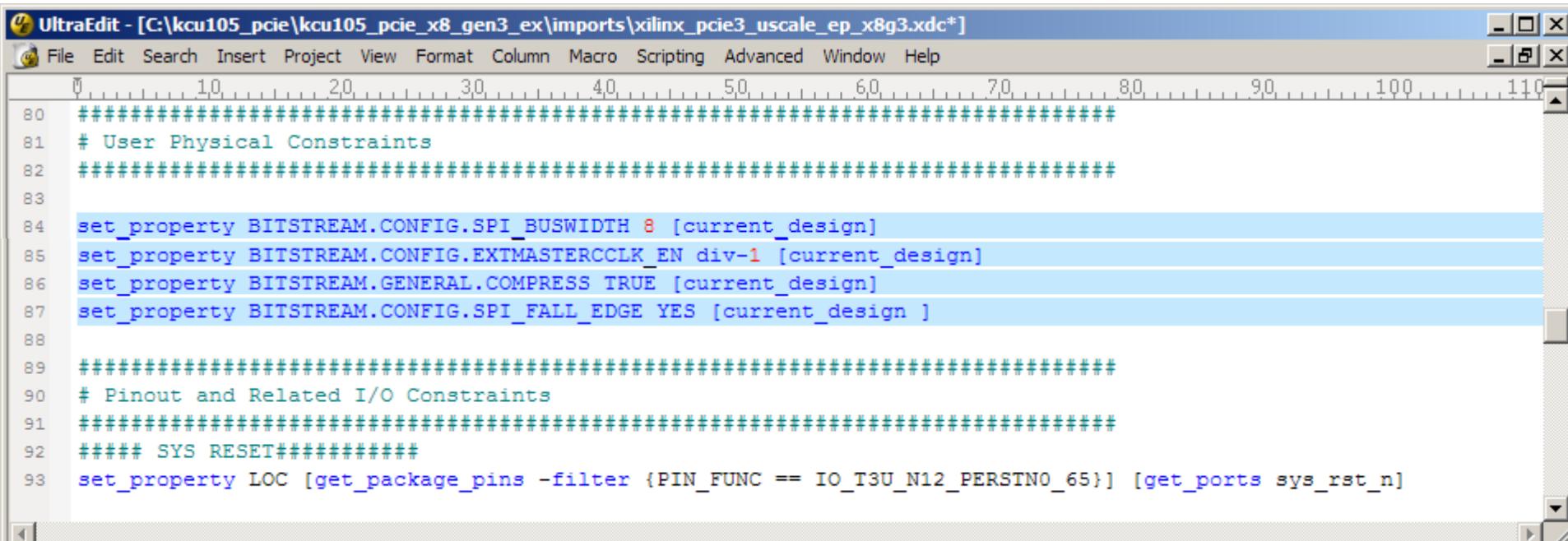
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Modify PCIe Core

► As per [UG570](#), [UG949](#), and [N25Q256 Flash](#) specifications

- In the XDC file, `xilinx_pcie3_uscale_ep_x8g3.xdc`, add these lines:

```
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]
```



The screenshot shows the UltraEdit text editor displaying the `xilinx_pcie3_uscale_ep_x8g3.xdc` file. The file contains XDC constraints for a PCIe core. The newly added configuration properties are highlighted in blue. The code is as follows:

```
#####
# User Physical Constraints
#####

set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design]

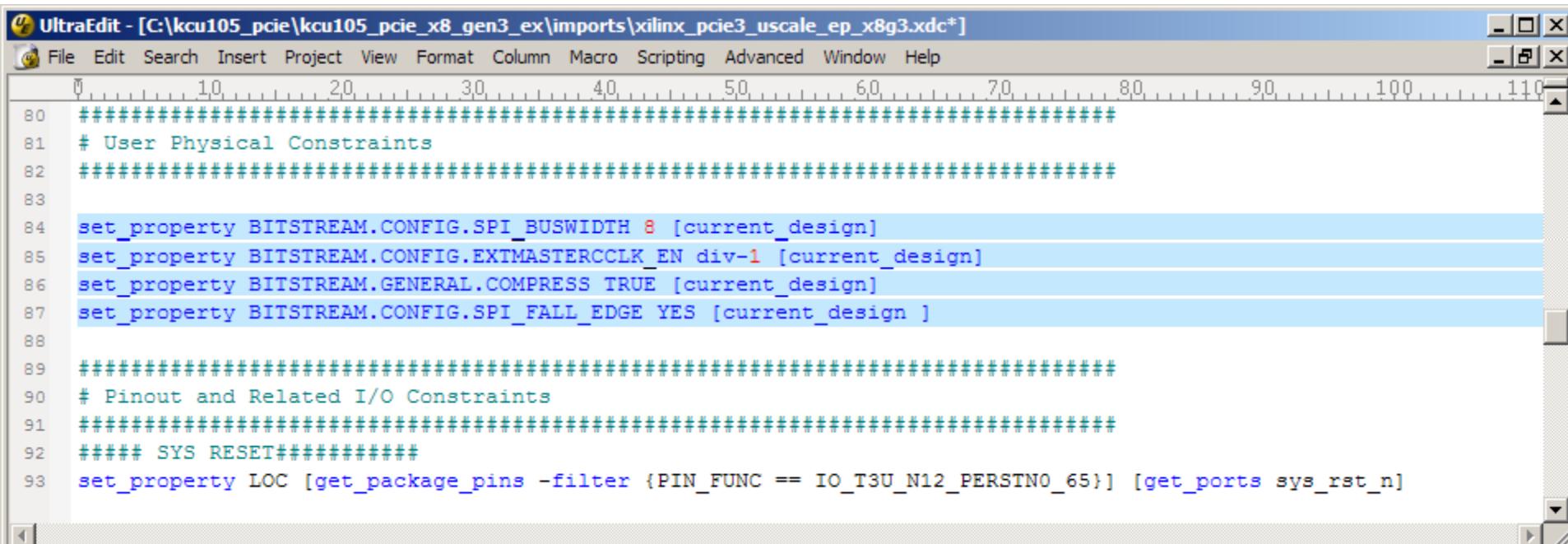
#####
# Pinout and Related I/O Constraints
#####
#####

#### SYS RESET#####
set_property LOC [get_package_pins -filter {PIN_FUNC == IO_T3U_N12_PERSTNO_65}] [get_ports sys_rst_n]
```

Modify PCIe Core

► Details on the XDC constraints :

- N25Q256 Maximum Frequency: 108 MHz; KCU105 EMCCLK Freq: 90 MHz
- **BITSTREAM.CONFIG.SPI_BUSWIDTH 8**: For Dual Quad SPI
BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1: Sets the EMCCLK in the FPGA to divide by 1
- **BITSTREAM.GENERAL.COMPRESS TRUE**: Shrinks the bitstream
- **BITSTREAM.CONFIG.SPI_FALL_EDGE YES**: Improves SPI loading speed

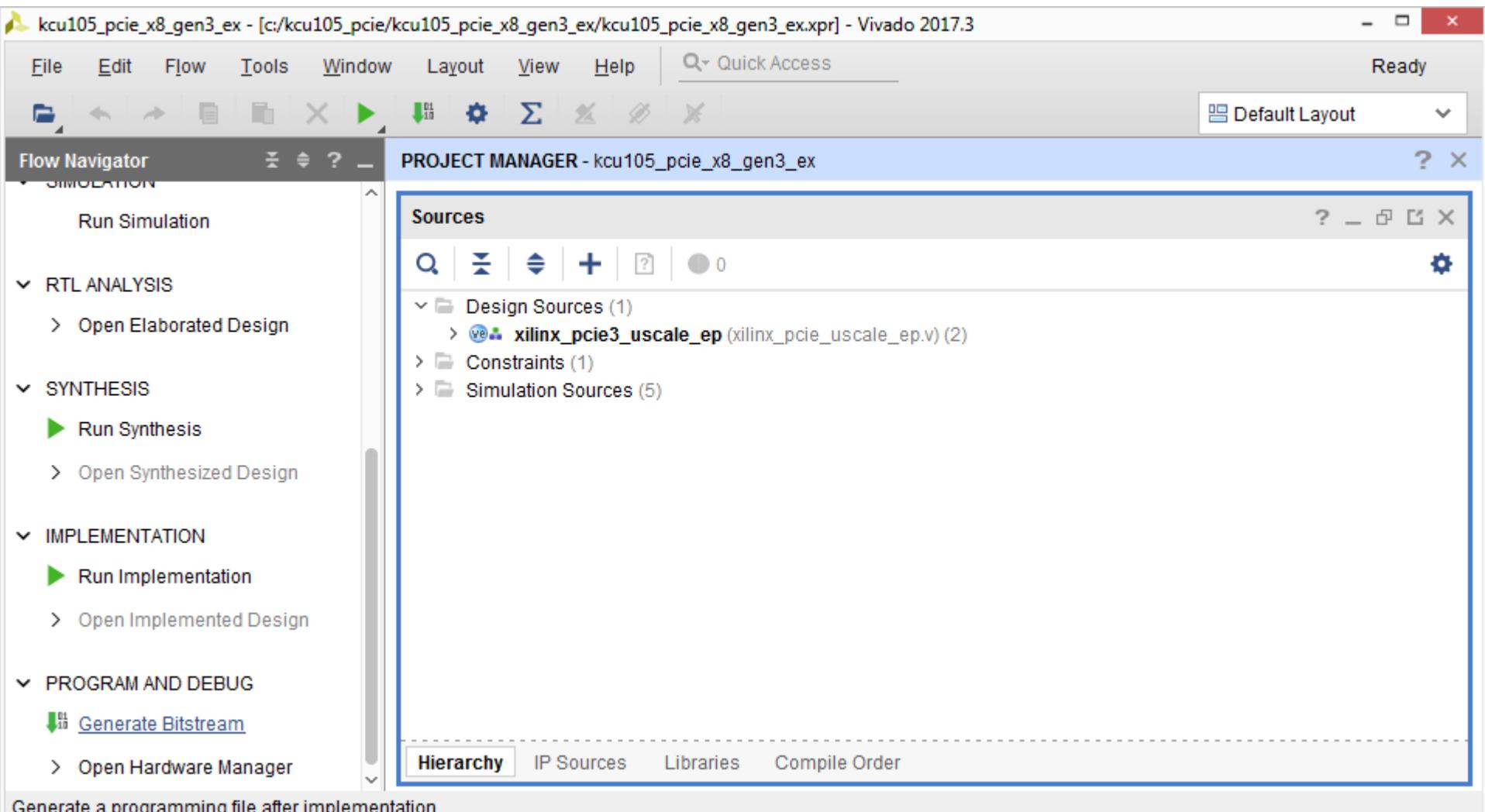


The screenshot shows the UltraEdit text editor displaying an XDC constraint file. The file contains several lines of configuration properties for a PCIe core. Lines 84 through 87 define physical constraints for the bitstream, while line 93 specifies a pinout constraint for a system reset pin.

```
UltraEdit - [C:\kcu105_PCIE\kcu105_PCIE_x8_gen3_ex\imports\xilinx_PCIE3_uscale_EP_X8g3.xdc*]
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
80 #####
81 # User Physical Constraints
82 #####
83
84 set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 8 [current_design]
85 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-1 [current_design]
86 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
87 set_property BITSTREAM.CONFIG.SPI_FALL_EDGE YES [current_design ]
88
89 #####
90 # Pinout and Related I/O Constraints
91 #####
92 ##### SYS RESET#####
93 set_property LOC [get_package_pins -filter {PIN_FUNC == IO_T3U_N12_PERSTNO_65}] [get_ports sys_rst_n]
```

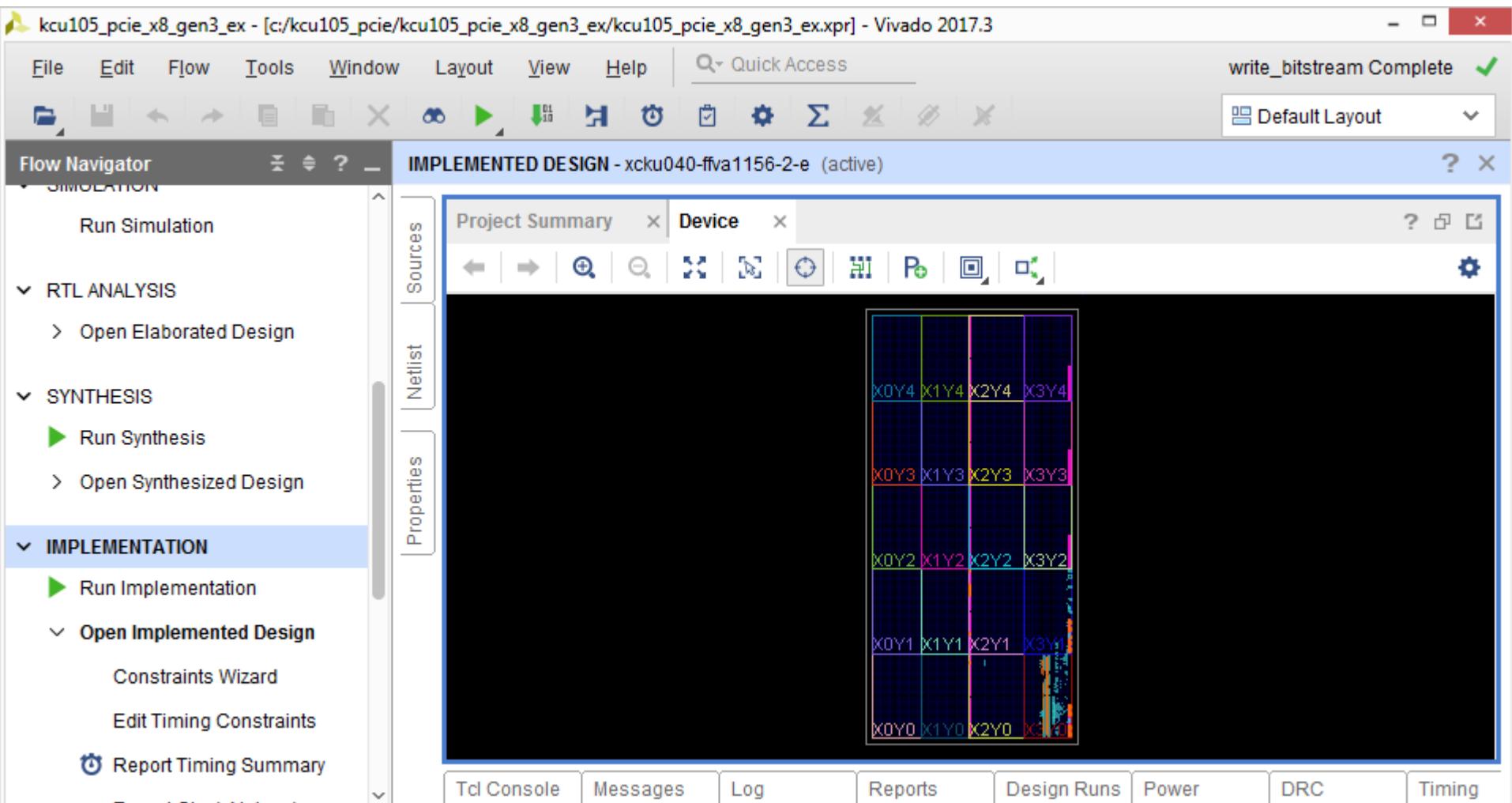
Compile Example Design

► Click on **Generate Bitstream**



Compile Example Design

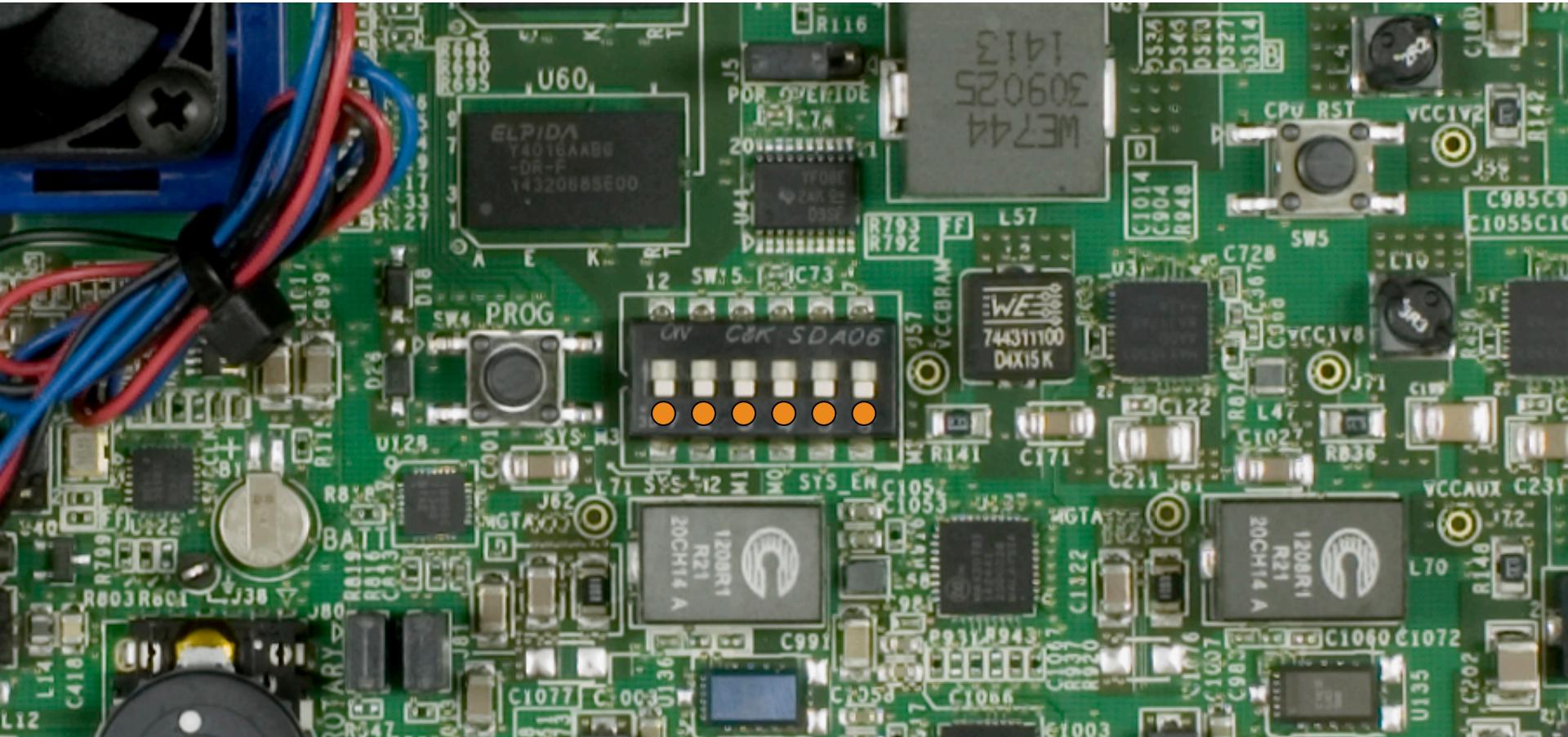
► Open and view the Implemented Design



Programming the Dual N25Q256 QSPI Flash

► Set S15 to 000000 (1 = on, Position 1 → Position 6)

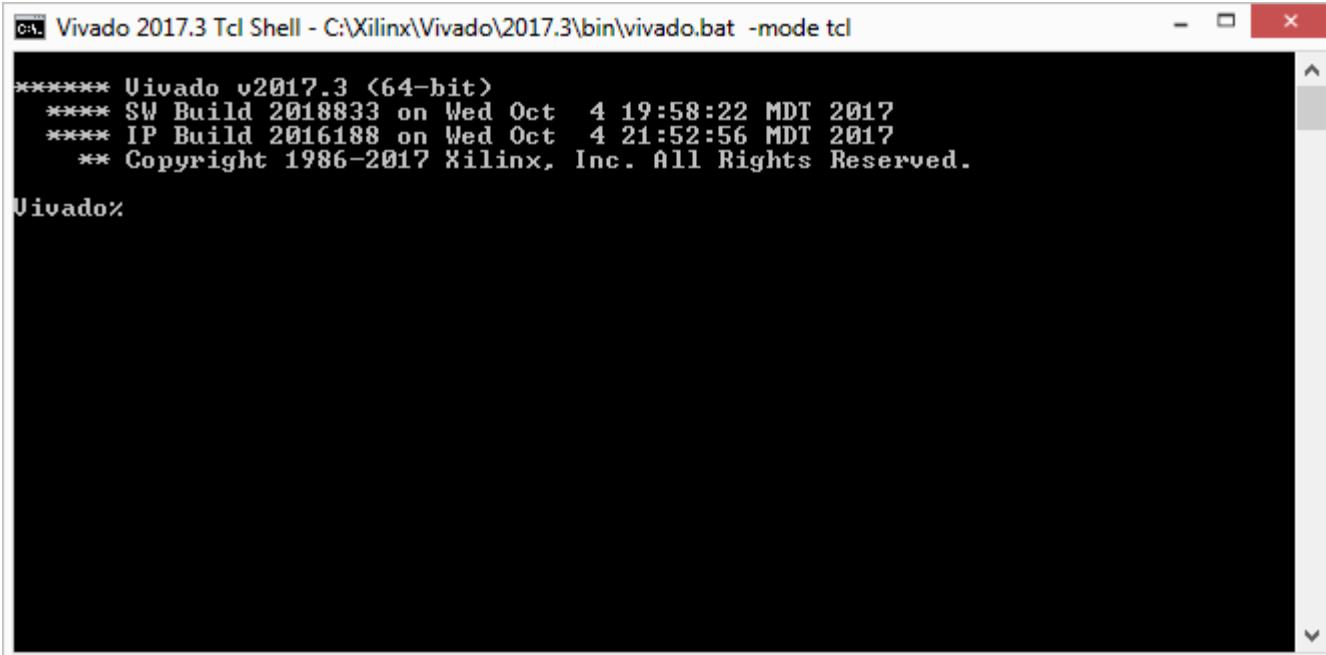
- This enables Master SPI configuration from the Dual N25Q256 QSPI Flash



Generate PCIe MCS File

► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2017.3 →
Vivado 2017.3 Tcl Shell**



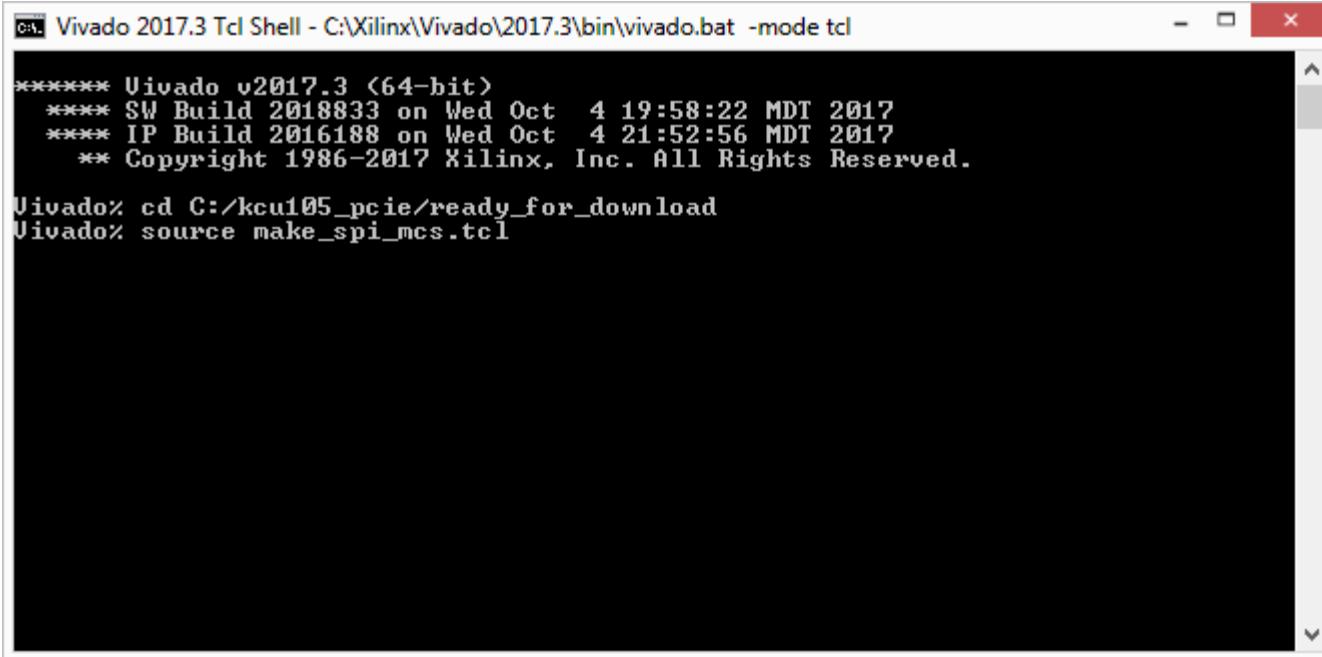
```
C:\> Vivado 2017.3 Tcl Shell - C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl
***** Vivado v2017.3 (64-bit)
***** SW Build 2018833 on Wed Oct  4 19:58:22 MDT 2017
***** IP Build 2016188 on Wed Oct  4 21:52:56 MDT 2017
** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

Vivado>
```

Program SPI Flash with PCIe Design

- Create the Dual QSPI PCIe MCS files
- In the Vivado Tcl Shell type:

```
cd C:/kcu105_pcie/ready_for_download  
source make_spi_mcs.tcl
```



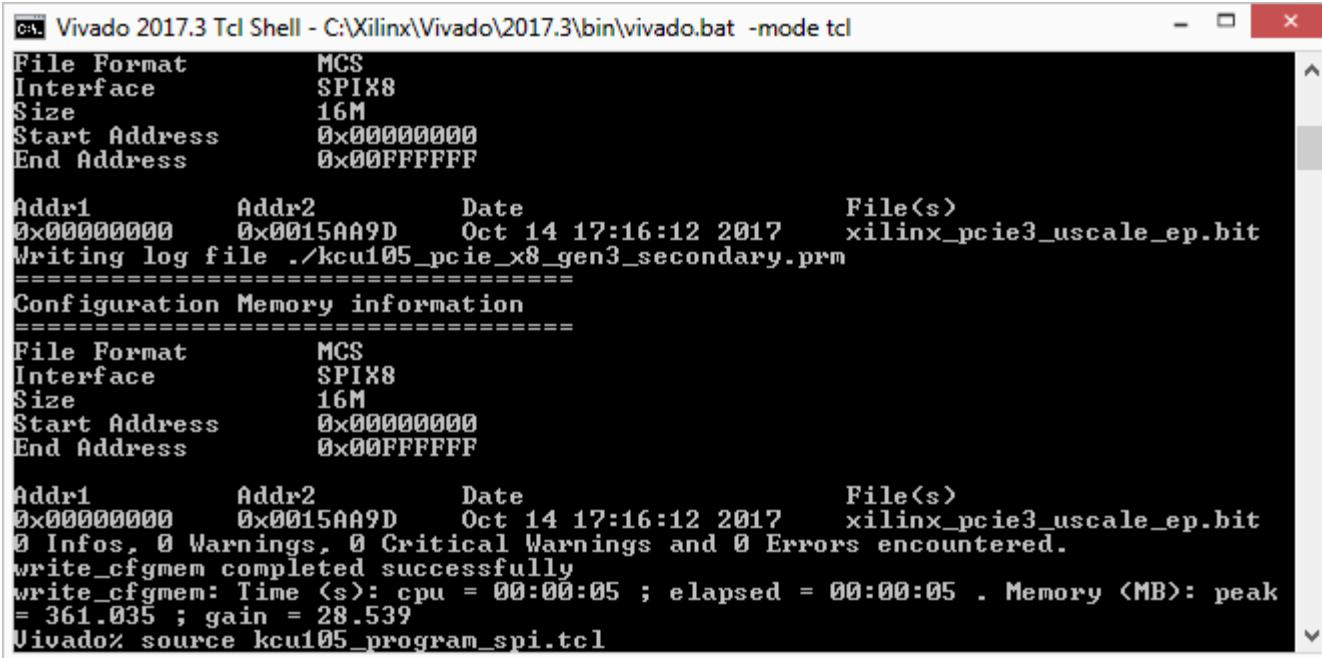
The screenshot shows a Windows command-line interface window titled "Vivado 2017.3 Tcl Shell - C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2017.3 (64-bit)  
***** SW Build 2018833 on Wed Oct 4 19:58:22 MDT 2017  
***** IP Build 2016188 on Wed Oct 4 21:52:56 MDT 2017  
** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.  
  
Vivado> cd C:/kcu105_pcie/ready_for_download  
Vivado> source make_spi_mcs.tcl
```

Program SPI Flash with PCIe Design

- Program the Dual QSPI Flash devices
- In the Vivado Tcl Shell type:

```
source kcu105_program_spi.tcl
```



```
C:\ Vivado 2017.3 Tcl Shell - C:\Xilinx\Vivado\2017.3\bin\vivado.bat -mode tcl
File Format      MCS
Interface        SPIx8
Size             16M
Start Address    0x00000000
End Address      0x00FFFFFF

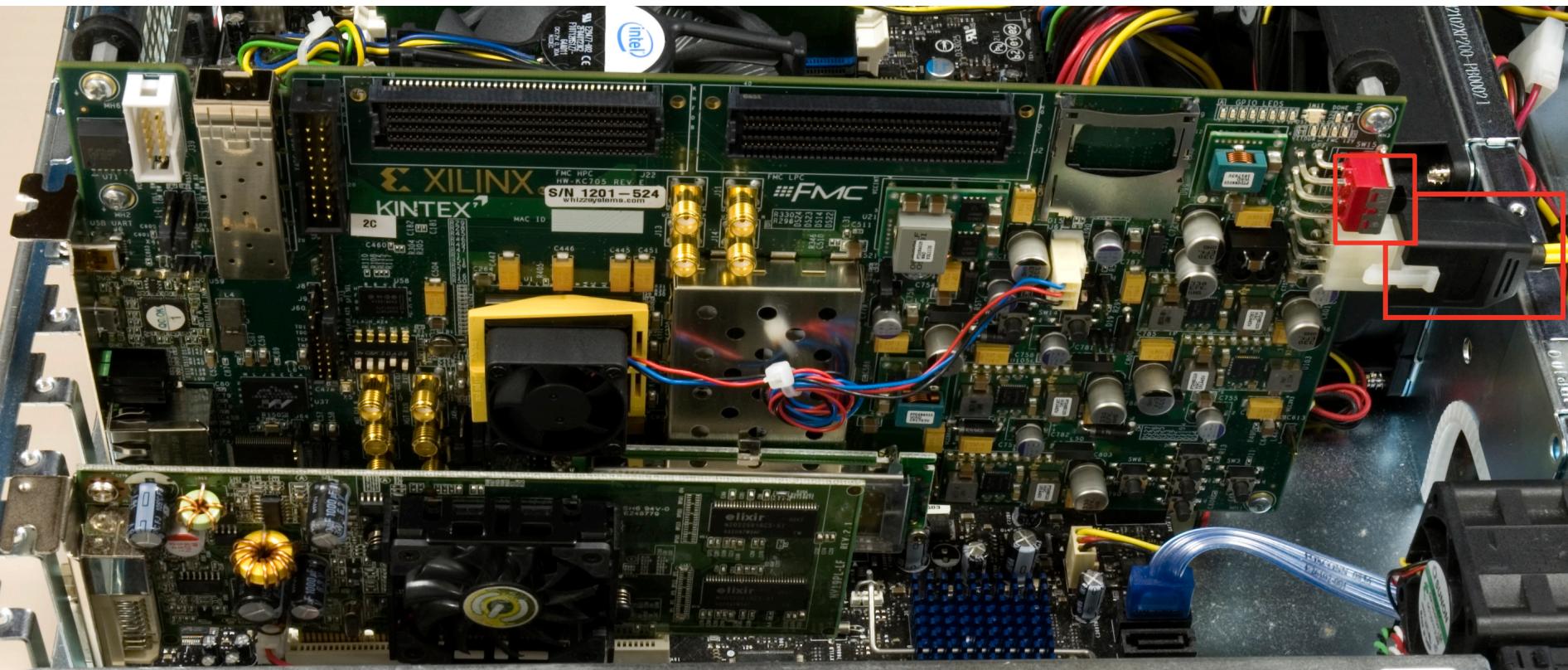
Addr1           Addr2           Date          File(s)
0x00000000     0x0015AA9D   Oct 14 17:16:12 2017  xilinx_pcie3_uscale_ep.bit
Writing log file ./kcu105_pcie_x8_gen3_secondary.prm
=====
Configuration Memory information
=====
File Format      MCS
Interface        SPIx8
Size             16M
Start Address    0x00000000
End Address      0x00FFFFFF

Addr1           Addr2           Date          File(s)
0x00000000     0x0015AA9D   Oct 14 17:16:12 2017  xilinx_pcie3_uscale_ep.bit
0 Infos, 0 Warnings, 0 Critical Warnings and 0 Errors encountered.
write_cfm completed successfully
write_cfm: Time <s>: cpu = 00:00:05 ; elapsed = 00:00:05 . Memory <MB>: peak
= 361.035 ; gain = 28.539
Vivado% source kcu105_program_spi.tcl
```

Hardware Setup

► Insert the KCU105 Board into a PCIe slot (KC705 shown)

- Use the included PC Power adapter; turn on Power Switch

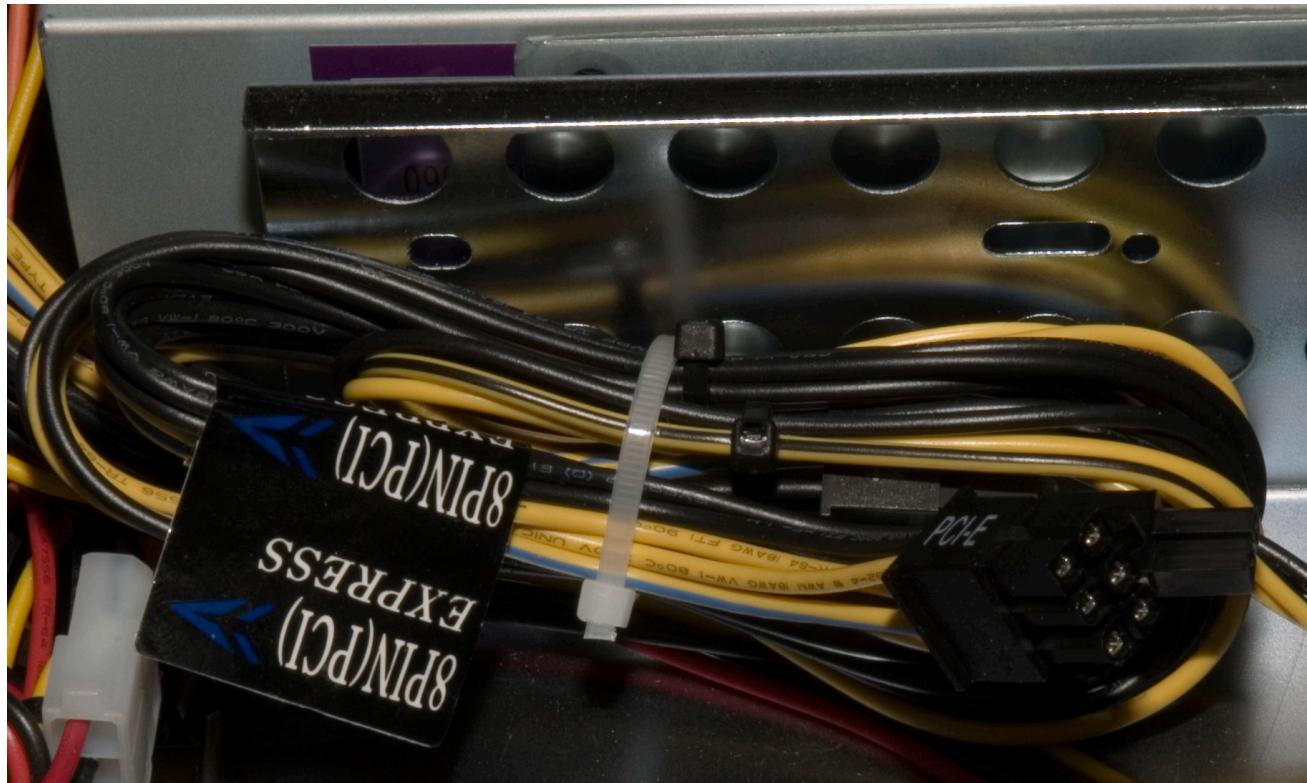


Note: As per AR64404, you may need to do a warm-reset

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Hardware Setup

- Do not use the PCIe connector from the PC power supply

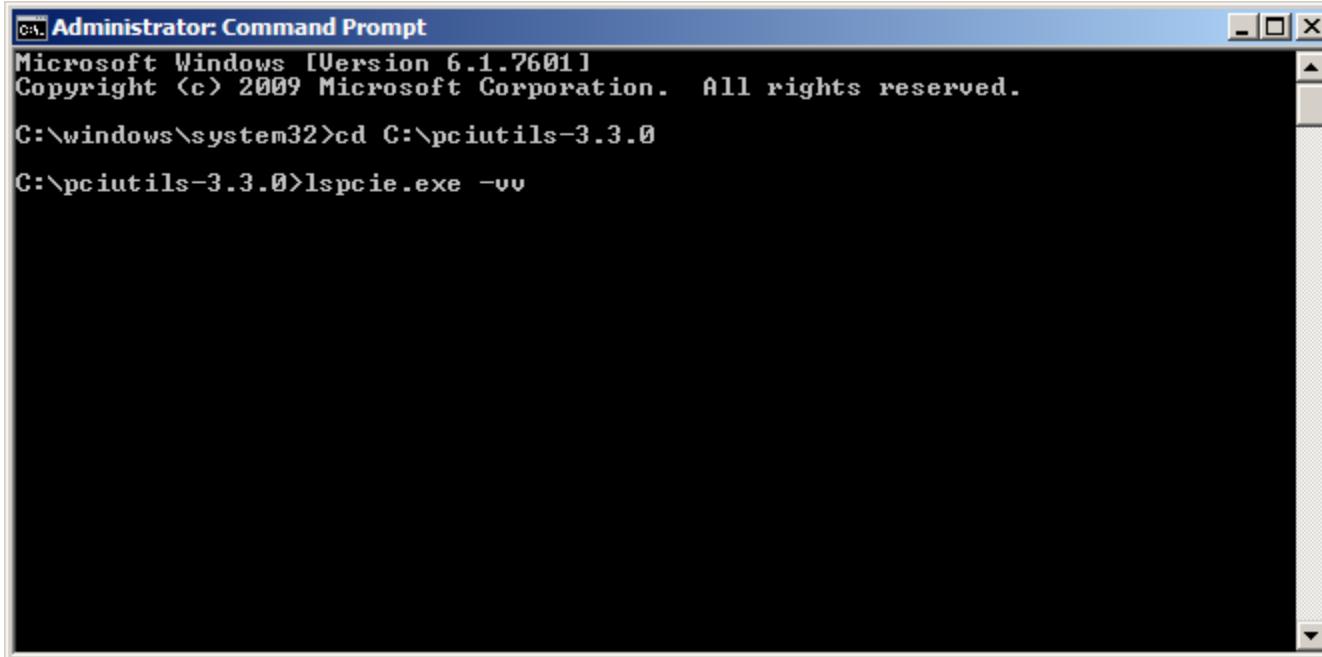


Running the PCIe x8 Gen3 Design

- Power on the PC
- Open an Administrator command prompt and type:

```
cd C:\pciutils-3.3.0
```

```
lspcie.exe -vv
```



The screenshot shows a Windows Command Prompt window titled "Administrator: Command Prompt". The window title bar is blue with white text. The main area of the window is black with white text. At the top, it displays the Windows version: "Microsoft Windows [Version 6.1.7601] Copyright (c) 2009 Microsoft Corporation. All rights reserved.". Below this, the command history shows two commands entered by the user: "C:\windows\system32>cd C:\pciutils-3.3.0" and "C:\pciutils-3.3.0>lspcie.exe -vv". The window has standard Windows-style scroll bars on the right side.

Running the PCIe x8 Gen3 Design

► View the Xilinx item in the results at 8GT/s (Gen3) and Width x8

```
c:\Administrator: Command Prompt
02:00.0 Memory controller: Xilinx Corporation Device 8038
    Subsystem: Xilinx Corporation Device 0007
    Control: I/O+ Mem+ BusMaster+ SpecCycle- MemWINV- UGASnoop- ParErr- Step
ping- SERR- FastB2B- DisINTx-
    Status: Cap+ 66MHz- UDF- FastB2B- ParErr- DEUSEL=fast >TAbsrt- <TAbsrt-
<MAbsrt- >SERR- <PERR- INTx-
    Latency: 0, Cache Line Size: 64 bytes
    Interrupt: pin A routed to IRQ 11
    Region 0: Memory at fbd00000 <32-bit, non-prefetchable>
    Capabilities: [80] Power Management version 3
        Flags: PMEClk- DSI- D1- D2- AuxCurrent=0mA PME<D0-,D1-,D2-,D3hot
-,D3cold->
        Status: D0 NoSoftRst+ PME-Enable- DSel=0 DScale=0 PME-
        Capabilities: [90] MSI: Enable- Count=1/1 Maskable- 64bit+
        Address: 0000000000000000 Data: 0000
        Capabilities: [c0] Express <v2> Endpoint, MSI 00
            DevCap: MaxPayload 512 bytes, PhantFunc 0, Latency L0s <64ns, L1
<1us
            ExtTag- AttnBtn- AttnInd- PwrInd- RBE+ FLReset-
d-
            DevCtl: Report errors: Correctable- Non-Fatal- Fatal- Unsupported
            R1xdOrd- ExtTag- PhantFunc- AuxPwr- NoSnoop+
            MaxPayload 256 bytes, MaxReadReq 512 bytes
            DevSta: CorrErr- UncorrErr- FatalErr- UnsuppReq- AuxPwr- TransPe
nd-
            LnkCap: Port #0, Speed 8GT/s, Width x8, ASPM unknown, Latency L0
unlimited, L1 unlimited
            ClockPM- Surprise- LLActRep- BwNot-
            LnkCtl: ASPM Disabled; RCB 64 bytes Disabled- Retrain- CommClk-
ExtSynch- ClockPM- 0.4WidDis- BWInt- AutBWInt-
            LnkSta: Speed 8GT/s, Width x8, TrErr- Train- SlotClk- DLActive-
BWmgmt- ABWmgmt-
            DevCap2: Completion Timeout: Range B, TimeoutDis+
            DevCtl2: Completion Timeout: 50us to 50ms, TimeoutDis-
            LnkCtl2: Target Link Speed: 8GT/s, EnterCompliance- SpeedDis-, S
electable De-emphasis: -6dB
            Transmit Margin: Normal Operating Range, EnterModifiedC
ompliance- ComplianceSOS-
            Compliance De-emphasis: -6dB
            LnkSta2: Current De-emphasis Level: -3.5dB, EqualizationComplete
+, EqualizationPhase1+
            EqualizationPhase2+, EqualizationPhase3+, LinkEqualizat
ionRequest-
```

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