Monte Carlo Algorithm for Leakage Optimization Based on Input Vector Control

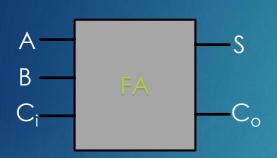
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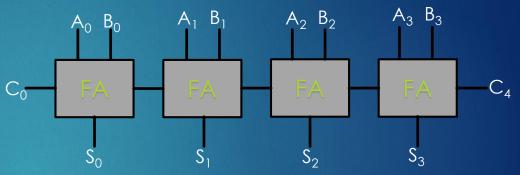
- Problem definition --- Input Vector Control
- Algorithm and implementation
- Results and Discussion
- Conclusion

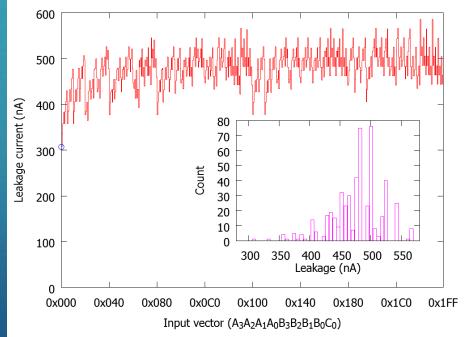
# Input Vector Control

A method for reducing leakage power consumption



Input vector(A,B,Ci)	Output(\$ ,Co)	Leakage/ nA
000	00	76.97
001	01	104.60
010	01	126.48
011	10	124.12
100	01	146.35
101	10	126.51
110	10	146.13
111	11	105.73





## Finding the best input vector

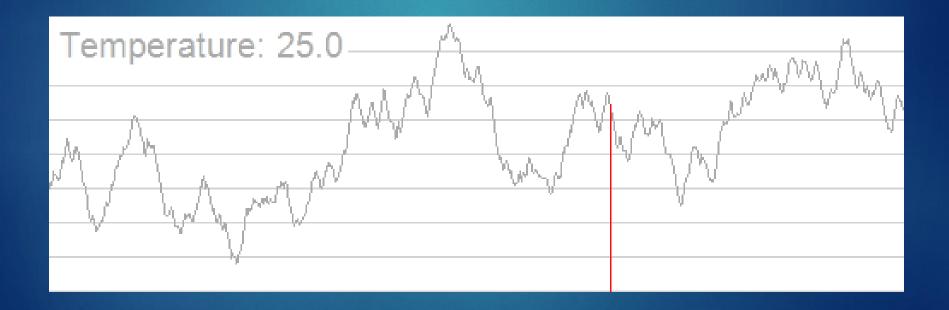
- NP-Complete problem
  - Heuristic algorithm
  - Random search
- Existing Algorithms
  - Linear programming
  - Dynamic programming
  - ▶ 2-SAT
  - Random searching
- Problems
  - Slow
  - Sub-optimal result

#### Random search

- A large class of algorithms based on random numbers
- Crude and simple, but can be sometimes effective
- Simplest random search:
  - ▶ n=64 inputs
  - Number of state N=1.845×10<sup>19</sup>
  - ► Random search ~10<sup>8</sup> states

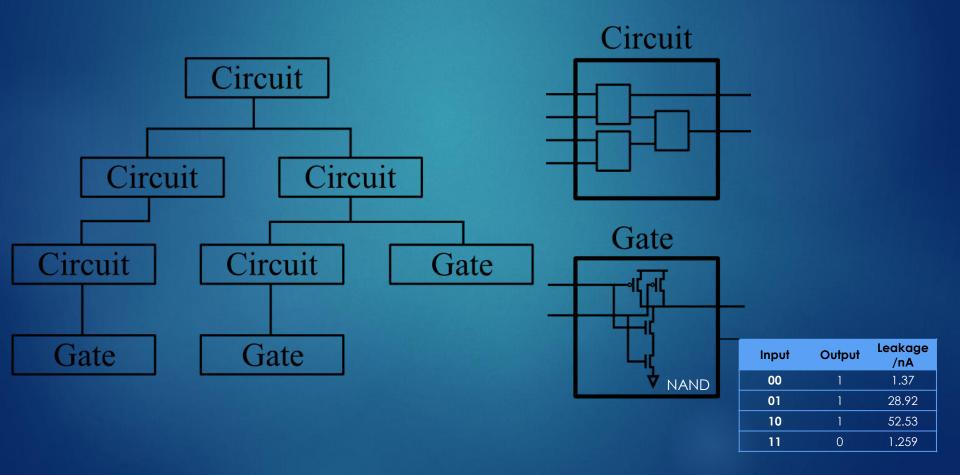
### Improvement: Simulated Annealing

- Analogue of thermodynamics problem
- Temperature T: characterizes the randomness

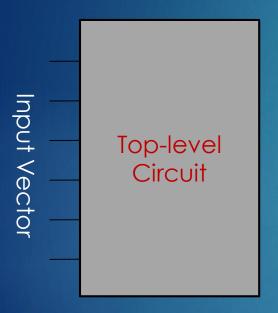


### Simulation model

Hierarchical model for simulating combinational logic



## Implementation



```
Minimize Leakage(C, n)
    input[] = random(n);
    leak = evaluate(input);
    T = T_0;
         index = random(n);
         input[index].flip();
         new leak = evaluate(input);
         if(new leak < leak){</pre>
              leak = new leak;
              // save input vector
         else{
              prob = e-(new_leak-leak)/T.
              if(random() < prob) {</pre>
                   leak = new leak;
              else{
                   // restore
                   input[index].flip();
                   continue;
```

#### Extra heuristics

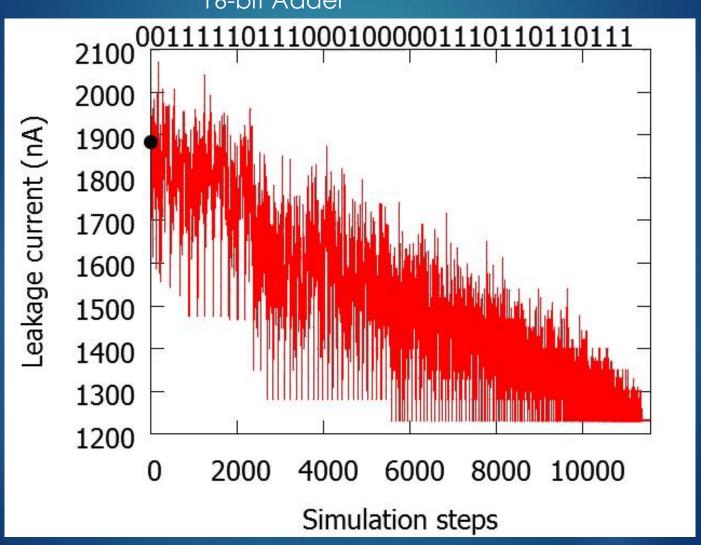
- Since only one bit is flipped, possibility of getting stuck
  - Example: T=0.5
  - > 0000000011000000
  - **>** 000000010000000 15
  - **>** 000000001000000 15
- Solution: Do relaxation after several iterations
  - ► Enumerate and try all possible two-bit flips

#### Results and Discussion

- Everything implemented in Java
  - > 2535 lines of code
- NOT, AND, OR, NAND, NOR, XOR, FA, etc. tens of gates extracted from GSCLIB090 technology library.
- Tested on a number of benchmark circuits

# Simulated Annealing

16-bit Adder



## Benchmark

Circuit	Inputs	Gate count	Min. Leakage(nA)	Time(s) (By bruteforcing)	Avg. annealing Leakage(nA)	Time(s) (By annealing)	Ratio
Adder-4	9	4	307.9	0.1	307.9	0.1	1.00
C17	5	6	35.4	0.1	35.4	0.1	1.00
C432	36	160	3360.6	-	3389.1	1.0	1.008
C880	60	383	9716.7	-	9815.9	6.0	1.010
C1355	41	546	11081.9	-	11081.9	5.0	1.00
C3540	50	1669	52588.5	-	52588.5	25.0	1.00
C6288	32	2416	75939.3	-	75939.3	22.0	1.00
C7552	207	3512	1.05×10 <sup>5</sup>	-	1.07×10 <sup>5</sup>	439.0	1.019

ISCAS85 Benchmark circuits

#### Conclusion

- An improved version of random search for input vector control is developed based on widely-used simulated annealing algorithm
- The effectiveness and validity of the algorithm is verified.
- Possible further improvements
  - Use more efficient programming language such as C++

### References

- Gao, Feng, and John P. Hayes. "Exact and heuristic approaches to input vector control for leakage power reduction." Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on 25.11 (2006): 2564-2571.
- Chang, Xiaotao, et al. "Fast algorithm for leakage power reduction by input vector control." ASIC, 2005. ASICON 2005. 6th International Conference On. Vol. 1. IEEE, 2005.
- Cheng, Lei, et al. "A fast simultaneous input vector generation and gate replacement algorithm for leakage power reduction." *Proceedings of the 43rd annual Design Automation Conference*. ACM, 2006.
- Aloul, Fadi A., et al. "Robust SAT-based search algorithm for leakage power reduction." Integrated Circuit Design. Power and Timing Modeling, Optimization and Simulation. Springer Berlin Heidelberg, 2002. 167-177.
- Halter, Jonathan P., and Farid N. Najm. "A gate-level leakage power reduction method for ultra-low-power CMOS circuits." Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997. IEEE, 1997.

# Thanks!