Heli_inner_loop

Design Description

bpotter

Heli_inner_loop: Design Description

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Chapter 1. Model Version

Version: 1.32

Last modified: Mon May 11 09:09:03 2020

Checksum: 1102282267 3300914420 1173054518 630799149

Chapter 2. Root System

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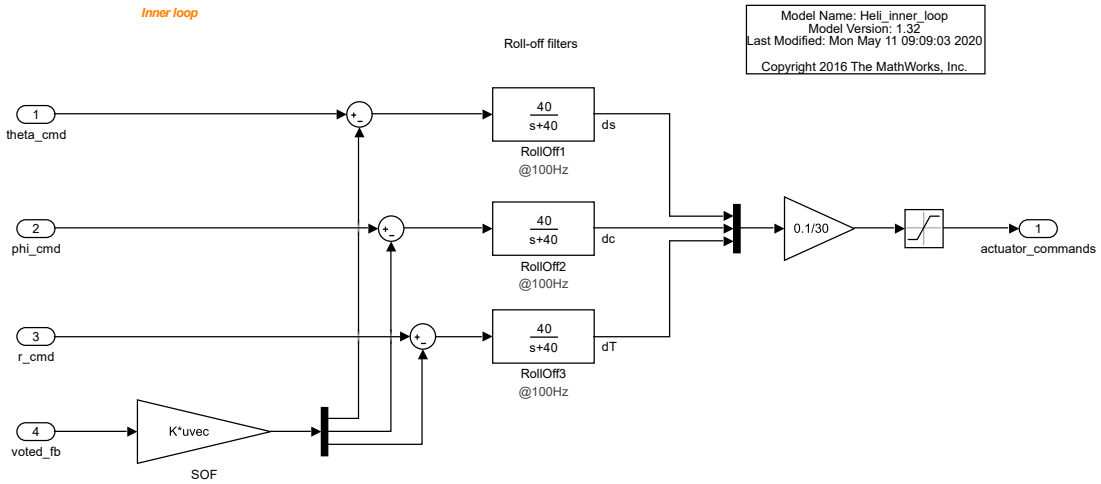
Figure 2.1. Heli_inner_loop



2.1. Description

This model implements a multi-variable inner loop control for a helicopter. The control loop stabilizes the pitch rate, roll rate and yaw rate of the helicopter.

2.2. Interface

2.2.1. Input Signals

Table 2.1.

Description:
Data Type: double
Width: 1
Dimensions: [1 1]

Table 2.2.

Description:
Data Type: double
Width: 1
Dimensions: [1 1]

Table 2.3.

Description:
Data Type: double
Width: 1
Dimensions: [1 1]

Table 2.4.

Description:
Data Type: double
Width: 5
Dimensions: [1 5]

2.2.2. Output Signals

Table 2.5.

Description:
Data Type: double
Width: 3
Dimensions: [1 3]

2.3. Blocks

2.3.1. Parameters

2.3.1.1. "actuator_commands" (Outport)

Table 2.6. "actuator_commands" Parameters

Parameter	Value
Port number	1
Icon display	Port number
Minimum	[]
Maximum	[]
Data type	Inherit: auto
Lock output data type setting against	off

Parameter	Value
changes by the fixed-point tools	
Output as nonvirtual bus in parent model	off
Unit (e.g., m, m/s^2, N*m)	inherit
Port dimensions (-1 for inherited)	-1
Variable-size signal	Inherit
Sample time (-1 for inherited)	-1
Ensure outport is virtual	off
Source of initial output value	Dialog
Output when disabled	held
Initial output	[]
MustResolveToSignalObject	off
Specify output when source is unconnected	off
Constant value	0
Interpret vector parameters as 1-D	off

2.3.1.2. "Demux2" (Demux)

Table 2.7. "Demux2" Parameters

Parameter	Value
Number of outputs	3
Display option	bar
Bus selection mode	off

2.3.1.3. "Gain" (Gain)

Table 2.8. "Gain" Parameters

Parameter	Value
Gain	0.1/30

Parameter	Value
Multiplication	Element-wise(K.*u)
Parameter minimum	[]
Parameter maximum	[]
Parameter data type	Inherit: Inherit via internal rule
Output minimum	[]
Output maximum	[]
Output data type	Inherit: Inherit via internal rule
Lock output data type setting against changes by the fixed-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

2.3.1.4. "Mux3" (Mux)

Table 2.9. "Mux3" Parameters

Parameter	Value
Number of inputs	3
Display option	bar

2.3.1.5. "phi_cmd" (Inport)

Table 2.10. "phi_cmd" Parameters

Parameter	Value
Port number	2
Port dimensions (-1 for inherited)	1
Sample time (-1 for inherited)	0.01
Minimum	-30
Maximum	30
Data type	double

2.3.1.6. "r_cmd" (Inport)

Table 2.11. "r_cmd" Parameters

Parameter	Value
Port number	3
Port dimensions (-1 for inherited)	1
Sample time (-1 for inherited)	0.01
Minimum	-30
Maximum	30
Data type	double

2.3.1.7. "Saturation" (Saturate)

Table 2.12. "Saturation" Parameters

Parameter	Value
Upper limit	0.1
Lower limit	-0.1
Treat as gain when linearizing	on
Enable zero-crossing detection	on
Sample time (-1 for inherited)	-1
Output minimum	[]
Output maximum	[]
Output data type	Inherit: Same as input
Lock output data type setting against changes by the fixed-point tools	off
Integer rounding mode	Floor

2.3.1.8. "SOF" (Gain)

Table 2.13. "SOF" Parameters

Parameter	Value
Gain	[2.395, -0.3609, -0.002145, 0.8087, -0.0205; -0.1427, -1.115, 0.04573, -0.04318, -0.1007; -0.02792, -0.02229, -2.025, -0.06152, 0.03151;]

Parameter	Value
Multiplication	Matrix(K*u) (u vector)
Parameter minimum	[]
Parameter maximum	[]
Parameter data type	Inherit: Inherit via internal rule
Output minimum	[]
Output maximum	[]
Output data type	Inherit: Inherit via internal rule
Lock output data type setting against changes by the fixed-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

2.3.1.9. "Sum4" (Sum)

Table 2.14. "Sum4" Parameters

Parameter	Value
Icon shape	round
List of signs	|+-
Sum over	All dimensions
Dimension	1
Require all inputs to have the same data type	off
Accumulator data type	Inherit: Inherit via internal rule
Output minimum	[]
Output maximum	[]
Output data type	Inherit: Inherit via internal rule
Lock data type settings against changes by the fixed-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off

Parameter	Value
Sample time (-1 for inherited)	-1

2.3.1.10. "Sum5" (Sum)

Table 2.15. "Sum5" Parameters

Parameter	Value
Icon shape	round
List of signs	|+-
Sum over	All dimensions
Dimension	1
Require all inputs to have the same data type	off
Accumulator data type	Inherit: Inherit via internal rule
Output minimum	[]
Output maximum	[]
Output data type	Inherit: Inherit via internal rule
Lock data type settings against changes by the fixed-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

2.3.1.11. "Sum6" (Sum)

Table 2.16. "Sum6" Parameters

Parameter	Value
Icon shape	round
List of signs	|+-
Sum over	All dimensions
Dimension	1
Require all inputs to have the same data type	off

Parameter	Value
Accumulator data type	Inherit: Inherit via internal rule
Output minimum	[]
Output maximum	[]
Output data type	Inherit: Inherit via internal rule
Lock data type settings against changes by the fixed-point tools	off
Integer rounding mode	Floor
Saturate on integer overflow	off
Sample time (-1 for inherited)	-1

2.3.1.12. "theta_cmd" (Inport)

Table 2.17. "theta_cmd" Parameters

Parameter	Value
Port number	1
Port dimensions (-1 for inherited)	1
Sample time (-1 for inherited)	0.01
Minimum	-30
Maximum	30
Data type	double

2.3.1.13. "voted_fb" (Inport)

Table 2.18. "voted_fb" Parameters

Parameter	Value
Port number	4
Port dimensions (-1 for inherited)	5
Sample time (-1 for inherited)	0.01
Minimum	-180
Maximum	180

Parameter	Value
Data type	double

2.3.2. Block Execution Order

"Heli_inner_loop" is a multitasking model. Block execution order is not available for multitasking models.

Chapter 3. Subsystems

Chapter 4. System Design Variables

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4.1. Design Variable Summary

Table 4.1. Functions used in Design Variable Expressions

Function Name	Parent Blocks	Calling character vector
dspFilterRealizedInBasicElemsAlgLoopErrFcnCallback	RollOff1 [6] RollOff2 [6] RollOff3 [6]	`dspFilterRealizedInBasicElemsAlgLoopErrFcnCallback` `dspFilterRealizedInBasicElemsAlgLoopErrFcnCallback` `dspFilterRealizedInBasicElemsAlgLoopErrFcnCallback`

Chapter 5. Requirements

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5.1. Model Information for "Heli_inner_loop"

Table 5.1. Heli_inner_loop Version Information

ModelVersion	1.32	*ConfigurationManager*	N/A
Created	Thu Feb 05 10:22:56 2015	*Creator*	bpotter
LastModifiedDate	Mon May 11 09:09:03 2020	*LastModifiedBy*	bpotter

5.2. Document Summary for "Heli_inner_loop"

Table 5.2. Requirements documents linked in model

ID	Artifact names stored by RMI	Last modified	# links
DOC1	HelicopterSoftwareRequirements.slreqx [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%22%22,%22Heli_inner_loop%22]]	Fri Dec 14 07:33:19 2018	16

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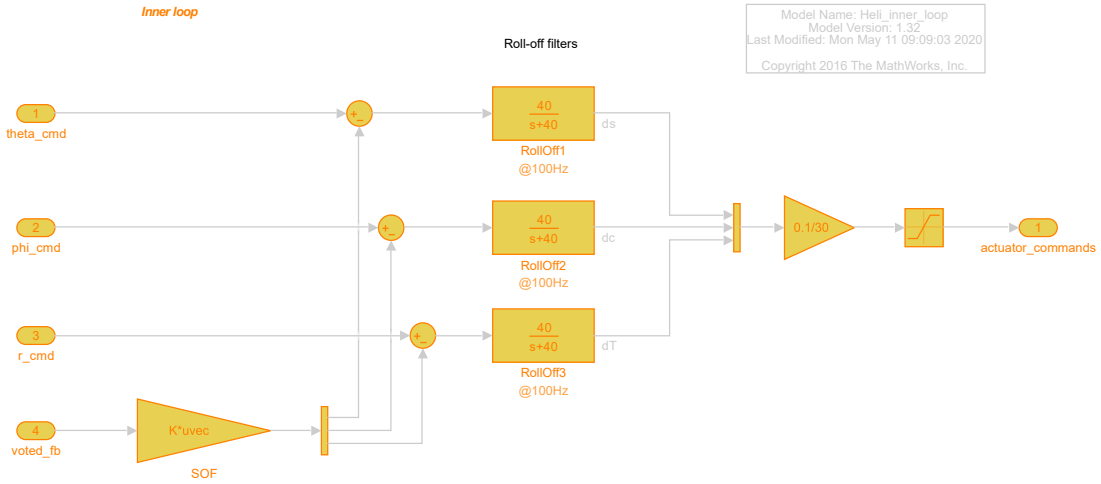
5.3. System - Heli_inner_loop



Show in Simulink [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22-Heli_inner_loop%22,%22%22]]

Table 5.3. Blocks in "Heli_inner_loop" that have requirements

Linked Object	Requirements Data	
actuator_commands [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:2%22]]	1.	"HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)" HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
Demux2 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:3%22]]	1.	"HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)" HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
Gain [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:23%22]]	1.	"HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)" HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
Mux3 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:4%22]]	1.	"HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)" HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwar-

Linked Object	Requirements Data	
		eRequirements.slreqx%22,%229-%22,%22Heli_inner_loop%22]]
phi_cmd [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:14%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229-%22,%22Heli_inner_loop%22]]
r_cmd [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:15%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229-%22,%22Heli_inner_loop%22]]
RollOff1 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:20%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229-%22,%22Heli_inner_loop%22]]
RollOff2 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:21%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229-%22,%22Heli_inner_loop%22]]
RollOff3 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:22%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229-%22,%22Heli_inner_loop%22]]
Saturation [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:25%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229-%22,%22Heli_inner_loop%22]]
SOF [http://localhost:31415/matlab/feval/rmiobjnavigate?argumen-	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigat-

Linked Object	Requirements Data	
ts=[%22Heli_inner_loop%22,%22:5%22]]		e?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
Sum4 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:6%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
Sum5 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:7%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
Sum6 [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:8%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
theta_cmd [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:1%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]
voted_fb [http://localhost:31415/matlab/feval/rmiobjnavigate?arguments=[%22Heli_inner_loop%22,%22:16%22]]	1. "HLR_5: Multi-Variable Inner Loop Control (HelicopterSoftwareRequirements#9)"	HelicopterSoftwareRequirements.slreqx, at "9" [http://localhost:31415/matlab/feval/rmi.navigate?arguments=[%22linktype_rmi_slreq%22,%22HelicopterSoftwareRequirements.slreqx%22,%229%22,%22Heli_inner_loop%22]]

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Table 5.4. Objects in "Heli_inner_loop" that are not linked to requirements

Name	Type
ModelInfo	SubSystem

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5.4. Systems in "Heli_inner_loop" that have no links to requirements

Table 5.5. Systems and subsystem blocks in "Heli_inner_loop" that have no links to requirements

Model or subsystem block	Children with links
Heli_inner_loop	16 out of 17

.

Chapter 6. System Model Configuration

Source: Model
Source Name: Heli_inner_loop

Table 6.1. Heli_inner_loop Configuration Set

Property	Value
Description	
Components	[Heli_inner_loop Configuration Set.Components(1) [18], Heli_inner_loop Configuration Set.Components(2) [19], Heli_inner_loop Configuration Set.Components(3)- [20], Heli_inner_loop Configuration Set.Components(4) [22], Heli_inner_loop Configuration Set.Components(5) [24], Heli_inner_loop Configuration Set.Components(6) [26], Heli_inner_loop Configuration Set.Components(7) [26], Heli_inner_loop Configuration Set.Components(8)- [27], Heli_inner_loop Configuration Set.Components(9) [29], Heli_inner_loop Configuration Set.Components(10) [30], Heli_inner_loop Configuration Set.Components(11) [30]]
Name	Configuration

Table 6.2. Heli_inner_loop Configuration Set.Components [18](1)

Property	Value
Name	Solver
Description	
Components	
StartTime	0.0
StopTime	10.0
AbsTol	auto
AutoScaleAbsTol	on
FixedStep	0.01
InitialStep	auto
MaxOrder	5
ZcThreshold	auto
ConsecutiveZCsStepRelTol	10*128*eps
MaxConsecutiveZCs	1000

ExtrapolationOrder	4
NumberNewtonIterations	1
MaxStep	auto
MinStep	auto
MaxConsecutiveMinStep	1
RelTol	1e-3
EnableMultiTasking	on
ConcurrentTasks	off
Solver	FixedStepDiscrete
SolverName	FixedStepDiscrete
SolverType	Fixed-step
SolverJacobianMethodControl	auto
ShapePreserveControl	DisableAll
ZeroCrossControl	UseLocalSettings
ZeroCrossAlgorithm	Nonadaptive
SolverResetMethod	Fast
PositivePriorityOrder	off
AutoInsertRateTranBlk	off
SampleTimeConstraint	Unconstrained
InsertRTBMode	Whenever possible
SampleTimeProperty	
DecoupledContinuousIntegration	off
MinimalZcImpactIntegration	off
SolverOrder	3

Table 6.3. Heli_inner_loop Configuration Set.Components [18](2)

Property	**Value**
Name	Data Import/Export
Description	
Components	
Decimation	1
ExternalInput	[t, u]
FinalStateName	xFinal
InitialState	xInitial
LimitDataPoints	on
MaxDataPoints	1000
LoadExternalInput	off
LoadInitialState	off
SaveFinalState	off

SaveOperatingPoint	off
SaveFormat	Array
SaveOutput	on
SaveState	off
SignalLogging	on
DSMLogging	on
InspectSignalLogs	off
SaveTime	on
ReturnWorkspaceOutputs	off
StateSaveName	xout
TimeSaveName	tout
OutputSaveName	yout
SignalLoggingName	logsout
DSMLoggingName	dsmout
OutputOption	RefineOutputTimes
OutputTimes	[]
ReturnWorkspaceOutputsName	out
Refine	1
LoggingToFile	off
DatasetSignalFormat	timeseries
LoggingFileName	out.mat
LoggingIntervals	[-inf, inf]

Table 6.4. Heli_inner_loop Configuration Set.Components [18](3)

Property	**Value**
Name	Optimization
Description	
Components	
BlockReduction	off
BooleanDataType	on
ConditionallyExecuteInputs	on
DefaultParameterBehavior	Inlined
InlineParams	on
UseDivisionForNetSlopeComputation	on
GainParamInheritBuiltInType	off
UseFloatMulNetSlope	off
DefaultUnderspecifiedDataType	double
UseSpecifiedMinMax	off
InlineInvariantSignals	off

OptimizeBlockIOStorage	on
BufferReuse	on
GlobalBufferReuse	on
GlobalVariableUsage	None
StrengthReduction	off
AdvancedOptControl	-SLCI
ExpressionFolding	on
BooleansAsBitfields	off
BitfieldContainerType	uint_T
EnableMemcpy	on
MemcpyThreshold	64
PassReuseOutputArgsAs	Individual arguments
PassReuseOutputArgsThreshold	12
LocalBlockOutputs	on
RollThreshold	5
StateBitsets	off
DataBitsets	off
ActiveStateOutputEnumStorageType	Native Integer
ZeroExternalMemoryAtStartup	on
ZeroInternalMemoryAtStartup	on
InitFltsAndDblsToZero	on
NoFixptDivByZeroProtection	off
EfficientFloat2IntCast	on
EfficientMapNaN2IntZero	off
LifeSpan	inf
EvaledLifeSpan	Inf
MaxStackSize	inf
BufferReusableBoundary	on
SimCompilerOptimization	off
AccelVerboseBuild	off
OptimizeBlockOrder	off
OptimizeDataStoreBuffers	on
BusAssignmentInplaceUpdate	on
DifferentSizesBufferReuse	off
UseRowMajorAlgorithm	off
OptimizationLevel	level2
OptimizationPriority	Balanced
OptimizationCustomize	on
LabelGuidedReuse	off

MultiThreadedLoops	off
DenormalBehavior	GradualUnderflow
EfficientTunableParamExpr	on

Table 6.5. Heli_inner_loop Configuration Set.Components [18](4)

Property	**Value**
Name	Diagnostics
Description	
Components	
RTPrefix	error
ConsistencyChecking	none
ArrayBoundsChecking	none
SignalInfNanChecking	error
StringTruncationChecking	error
SignalRangeChecking	error
ReadBeforeWriteMsg	EnableAllAsError
WriteAfterWriteMsg	EnableAllAsError
WriteAfterReadMsg	EnableAllAsError
AlgebraicLoopMsg	error
ArtificialAlgebraicLoopMsg	error
SaveWithDisabledLinksMsg	error
SaveWithParameterizedLinksMsg	error
CheckSSInitialOutputMsg	on
UnderspecifiedInitializationDetection	Simplified
MergeDetectMultiDrivingBlocksExec	error
CheckExecutionContextRuntimeOutputM-sg	off
SignalResolutionControl	UseLocalSettings
BlockPriorityViolationMsg	error
MinStepSizeMsg	warning
TimeAdjustmentMsg	none
MaxConsecutiveZCsMsg	error
MaskedZcDiagnostic	warning
IgnoredZcDiagnostic	warning
SolverPrmCheckMsg	error
InheritedTsInSrcMsg	error
MultiTaskDSMMsg	error
MultiTaskCondExecSysMsg	error
MultiTaskRateTransMsg	error

SingleTaskRateTransMsg	error
TasksWithSamePriorityMsg	error
SigSpecEnsureSampleTimeMsg	error
CheckMatrixSingularityMsg	error
IntegerOverflowMsg	error
Int32ToFloatConvMsg	warning
ParameterDowncastMsg	error
ParameterOverflowMsg	error
ParameterUnderflowMsg	error
ParameterPrecisionLossMsg	error
ParameterTunabilityLossMsg	error
FixptConstUnderflowMsg	none
FixptConstOverflowMsg	none
FixptConstPrecisionLossMsg	none
UnderSpecifiedDataTypeMsg	error
UnnecessaryDatatypeConvMsg	warning
VectorMatrixConversionMsg	error
InvalidFcnCallConnMsg	error
FcnCallInpInsideContextMsg	error
SignalLabelMismatchMsg	error
UnconnectedInputMsg	error
UnconnectedOutputMsg	error
UnconnectedLineMsg	error
UseOnlyExistingSharedCode	error
SFcnCompatibilityMsg	error
FrameProcessingCompatibilityMsg	error
UniqueDataStoreMsg	error
BusObjectLabelMismatch	error
RootOutportRequireBusObject	error
AssertControl	DisableAll
AllowSymbolicDim	off
ModelReferenceIOMsg	error
ModelReferenceVersionMismatchMessage	none
ModelReferenceIOMismatchMessage	error
UnknownTsInhSupMsg	error
ModelReferenceDataLoggingMessage	error
ModelReferenceSymbolNameMessage	warning
ModelReferenceExtraNoncontSigs	error
StateNameClashWarn	warning

OperatingPointInterfaceChecksumMismatchMsg	warning
NonCurrentReleaseOperatingPointMsg	error
PregeneratedLibrarySubsystemCodeDiagnostic	none
InitInArrayFormatMsg	warning
StrictBusMsg	ErrorOnBusTreatedAsVector
BusNameAdapt	WarnAndRepair
NonBusSignalsTreatedAsBus	error
SFUnusedDataAndEventsDiag	warning
SFUnexpectedBacktrackingDiag	error
SFInvalidInputDataAccessInChartInitDiag	error
SFNoUnconditionalDefaultTransitionDiag	error
SFTransitionOutsideNaturalParentDiag	error
SFUnreachableExecutionPathDiag	error
SFUndirectedBroadcastEventsDiag	error
SFTransitionActionBeforeConditionDiag	error
SFOutputUsedAsStateInMooreChartDiag	error
SFTemporalDelaySmallerThanSampleTimeDiag	warning
SFSelfTransitionDiag	warning
SFExecutionAtInitializationDiag	none
SFMachineParentedDataDiag	warning
IntegerSaturationMsg	error
AllowedUnitSystems	all
UnitsInconsistencyMsg	warning
AllowAutomaticUnitConversions	on
RCSCRenamedMsg	warning
RCSCObservableMsg	warning
ForceCombineOutputUpdateInSim	off
UnderSpecifiedDimensionMsg	none
DebugExecutionForFMUViaOutOfProcess	off
ArithmeticOperatorsInVariantConditions	warning

Table 6.6. Heli_inner_loop Configuration Set.Components [18](5)

Property	**Value**
Name	Hardware Implementation
Description	
Components	
ProdBitPerChar	8

ProdBitPerShort	16
ProdBitPerInt	32
ProdBitPerLong	32
ProdBitPerLongLong	64
ProdBitPerFloat	32
ProdBitPerDouble	64
ProdBitPerPointer	32
ProdBitPerSizeT	32
ProdBitPerPtrDiffT	32
ProdLargestAtomicInteger	Char
ProdLargestAtomicFloat	Float
ProdIntDivRoundTo	Zero
ProdEndianess	LittleEndian
ProdWordSize	32
ProdShiftRightIntArith	on
ProdLongLongMode	off
ProdHWDeviceType	Intel->x86-32 (Windows32)
TargetBitPerChar	8
TargetBitPerShort	16
TargetBitPerInt	32
TargetBitPerLong	32
TargetBitPerLongLong	64
TargetBitPerFloat	32
TargetBitPerDouble	64
TargetBitPerPointer	32
TargetBitPerSizeT	32
TargetBitPerPtrDiffT	32
TargetLargestAtomicInteger	Char
TargetLargestAtomicFloat	None
TargetShiftRightIntArith	on
TargetLongLongMode	off
TargetIntDivRoundTo	Zero
TargetEndianess	Unspecified
TargetWordSize	32
TargetPreprocMaxBitsSint	32
TargetPreprocMaxBitsUint	32
TargetHWDeviceType	Specified
TargetUnknown	off
ProdEqTarget	on

UseEmbeddedCoderFeatures	on
UseSimulinkCoderFeatures	on
HardwareBoardFeatureSet	EmbeddedCoderHSP

Table 6.7. Heli_inner_loop Configuration Set.Components [18](6)

Property	Value
Name	Model Referencing
Description	
Components	
UpdateModelReferenceTargets	IfOutOfDateOrStructuralChange
EnableRefExpFcnMdlSchedulingChecks	on
CheckModelReferenceTargetMessage	error
EnableParallelModelReferenceBuilds	off
ParallelModelReferenceErrorOnInvalidPool	on
ParallelModelReferenceMATLABWorkerInit	None
ModelReferenceNumInstancesAllowed	Single
PropagateVarSize	Infer from blocks in model
ModelDependencies	
ModelReferencePassRootInputsByReference	on
ModelReferenceMinAlgLoopOccurrences	off
PropagateSignalLabelsOutOfModel	off
SupportModelReferenceSimTargetCustomCode	off

Table 6.8. Heli_inner_loop Configuration Set.Components [18](7)

Property	Value
Name	Simulation Target
Description	
Components	
SimCustomSourceCode	
SimCustomHeaderCode	
SimCustomInitializer	
SimCustomTerminator	
SimReservedNameArray	
SimUserSources	
SimUserIncludeDirs	
SimUserLibraries	

SimUserDefines	
SFSimEnableDebug	off
SFSimEcho	on
SimCtrlC	on
SimIntegrity	on
SimUseLocalCustomCode	off
SimParseCustomCode	on
SimAnalyzeCustomCode	off
SimBuildMode	sf_incremental_build
SimGenImportedTypeDefs	off
CompileTimeRecursionLimit	0
EnableRuntimeRecursion	off
MATLABDynamicMemAlloc	off
MATLABDynamicMemAllocThreshold	65536
CustomCodeFunctionArrayLayout	
DefaultCustomCodeFunctionArrayLayout	NotSpecified
CustomCodeUndefinedFunction	UseInterfaceOnly

Table 6.9. Heli_inner_loop Configuration Set.Components [18](8)

Property	**Value**
Name	Code Generation
Description	Embedded Coder
SystemTargetFile	ert.tlc
HardwareBoard	None
ShowCustomHardwareApp	off
ShowEmbeddedHardwareApp	off
TLCOptions	
GenCodeOnly	off
MakeCommand	make_rtw
GenerateMakefile	on
PackageGeneratedCodeAndArtifacts	off
PackageName	
TemplateMakefile	ert_default_tmf
PostCodeGenCommand	
GenerateReport	on
RTWVerbose	on
RetainRTWFile	off
ProfileTLC	off
TLCDebug	off

TLCCoverage	off
TLCAssert	off
RTWUseLocalCustomCode	off
RTWUseSimCustomCode	off
CustomSourceCode	
CustomHeaderCode	
CustomInclude	
CustomSource	
CustomLibrary	
CustomDefine	
CustomBLASCallback	
CustomLAPACKCallback	
CustomFFTCallback	
CustomInitializer	
CustomTerminator	
Toolchain	Automatically locate an installed toolchain
BuildConfiguration	Faster Builds
CustomToolchainOptions	
IncludeHyperlinkInReport	on
LaunchReport	on
PortableWordSizes	on
GenerateErtSFunction	off
CreateSILPILBlock	None
CodeExecutionProfiling	off
CodeExecutionProfileVariable	executionProfile
CodeProfilingSaveOptions	SummaryOnly
CodeProfilingInstrumentation	off
CodeCoverageSettings	Heli_inner_loop Configuration Set.Components(8).CodeCoverageSettings [31]
SILDebugging	off
TargetLang	C
IncludeERTFirstTime	off
GenerateTraceInfo	on
GenerateTraceReport	on
GenerateTraceReportSl	on
GenerateTraceReportSf	on
GenerateTraceReportEml	on
GenerateWebview	off
GenerateCodeMetricsReport	off

GenerateCodeReplacementReport	off
RTWCompilerOptimization	off
ObjectivePriorities	
RTWCustomCompilerOptimizations	
CheckMdlBeforeBuild	Off
Components	[Heli_inner_loop Configuration Set.Components(8).Components(1) [31], Heli_inner_loop Configuration Set.Components(8).Components(2) [32]]

Table 6.10. Heli_inner_loop Configuration Set.Components [18](9)

Property	Value
Description	Simulink Coverage Configuration Component
Components	
Name	Simulink Coverage
CovEnable	off
CovScope	EntireSystem
CovIncludeTopModel	on
RecordCoverage	off
CovPath	/
CovSaveName	covdata
CovCompData	
CovMetricSettings	dw
CovFilter	
CovHTMLOptions	
CovNameIncrementing	off
CovHtmlReporting	on
CovForceBlockReductionOff	on
CovEnableCumulative	on
CovSaveCumulativeToWorkspaceVar	on
CovSaveSingleToWorkspaceVar	on
CovCumulativeVarName	covCumulativeData
CovCumulativeReport	off
CovSaveOutputData	on
CovOutputDir	slcov_output/$ModelName$
CovDataFileName	$ModelName$_cvdata
CovShowResultsExplorer	on
CovReportOnPause	on
CovModelRefEnable	off

CovModelRefExcluded	
CovExternalEMLEnable	off
CovSFcnEnable	off
CovBoundaryAbsTol	1.0000e-05
CovBoundaryRelTol	0.0100
CovUseTimeInterval	off
CovStartTime	0
CovStopTime	0
CovMetricStructuralLevel	Decision
CovMetricLookupTable	off
CovMetricSignalRange	off
CovMetricSignalSize	off
CovMetricObjectiveConstraint	off
CovMetricSaturateOnIntegerOverflow	off
CovMetricRelationalBoundary	off
CovLogicBlockShortCircuit	off
CovUnsupportedBlockWarning	on
CovHighlightResults	on
CovMcdcMode	Masking

Table 6.11. Heli_inner_loop Configuration Set.Components [18](10)

Property	Value
Description	HDL Coder custom configuration component
Components	
Name	HDL Coder

Table 6.12. Heli_inner_loop Configuration Set.Components [18](11)

Property	Value
Description	Polyspace Custom Configuration Component
Components	
Name	Polyspace
PSVerificationMode	BugFinder
PSVerificationSettings	PrjConfig
PSCxxVerificationSettings	PrjConfig
PSOpenProjectManager	off
PSResultDir	BugFinder_results_$ModelName$
PSAddSuffixToResultDir	off

PSEnableAdditionalFileList	off
PSAdditionalFileList	
PSModelRefVerifDepth	Current model only
PSModelRefByModelRefVerif	off
PSInputRangeMode	DesignMinMax
PSParamRangeMode	None
PSOutputRangeMode	None
PSAutoStubLUT	off
PSCheckConfigBeforeAnalysis	OnWarn
PSEnablePrjConfigFile	off
PSPrjConfigFile	
PSAddToSimulinkProject	off

Table 6.13. Heli_inner_loop Configuration Set.Components(8) [27].CodeCoverageSettings

Property	Value
TopModelCoverage	off
ReferencedModelCoverage	off
CoverageTool	None

Table 6.14. Heli_inner_loop Configuration Set.Components(8).Components [29](1)

Property	Value
Name	Code Appearance
Description	
Components	
ForceParamTrailComments	on
GenerateComments	on
CommentStyle	Auto
IgnoreCustomStorageClasses	off
IgnoreTestpoints	off
MaxIdLength	31
ShowEliminatedStatement	on
OperatorAnnotations	off
SimulinkDataObjDesc	off
SFDataObjDesc	off
MATLABFcnDesc	on
MangleLength	4
SharedChecksumLength	8

CustomSymbolStrGlobalVar	RN$M
CustomSymbolStrType	NR$M_T
CustomSymbolStrField	NM
CustomSymbolStrFcn	RNMF
CustomSymbolStrFcnArg	rt$I$N$M
CustomSymbolStrBlkIO	rtb_NM
CustomSymbolStrTmpVar	NM
CustomSymbolStrMacro	RN$M
CustomSymbolStrUtil	NC
CustomSymbolStrEmxType	emxArray_MN
CustomSymbolStrEmxFcn	emx$M$N
CustomUserTokenString	
CustomCommentsFcn	
DefineNamingRule	None
DefineNamingFcn	
ParamNamingRule	None
ParamNamingFcn	
SignalNamingRule	None
SignalNamingFcn	
InsertBlockDesc	off
InsertPolySpaceComments	off
SimulinkBlockComments	on
BlockCommentType	BlockPathComment
StateflowObjectComments	on
MATLABSourceComments	off
EnableCustomComments	off
InternalIdentifier	Shortened
InlinedPrmAccess	Literals
ReqsInCode	on
UseSimReservedNames	off
ReservedNameArray	
EnumMemberNameClash	error

Table 6.15. Heli_inner_loop Configuration Set.Components(8).Components [29](2)

Property	Value
Name	Target
Description	
Components	

IsERTTarget	on
TargetLibSuffix	
TargetPreCompLibLocation	
GenFloatMathFcnCalls	NOT IN USE
TargetLangStandard	C99 (ISO)
CodeReplacementLibrary	None
UtilityFuncGeneration	Shared location
MultiwordTypeDef	System defined
MultiwordLength	2048
DynamicStringBufferSize	256
GenerateFullHeader	on
InferredTypesCompatibility	off
ExistingSharedCode	
GenerateSampleERTMain	on
GenerateTestInterfaces	off
ModelReferenceCompliant	on
ParMdlRefBuildCompliant	on
CompOptLevelCompliant	on
ConcurrentExecutionCompliant	on
IncludeMdlTerminateFcn	off
CombineOutputUpdateFcns	on
CombineSignalStateStructs	off
GroupInternalDataByFunction	off
SuppressErrorStatus	on
IncludeFileDelimiter	Auto
ERTCustomFileBanners	on
SupportAbsoluteTime	off
LogVarNameModifier	rt_
MatFileLogging	off
MultiInstanceERTCode	off
CodeInterfacePackaging	Nonreusable function
PurelyIntegerCode	off
SupportNonFinite	off
SupportComplex	on
SupportContinuousTime	off
SupportNonInlinedSFcns	off
RemoveDisableFunc	off
RemoveResetFunc	on
SupportVariableSizeSignals	off

ParenthesesLevel	Maximum
CastingMode	Standards
PreserveStateflowLocalDataDimensions	off
ModelStepFunctionPrototypeControlCompliant	on
CPPClassGenCompliant	on
GRTInterface	off
GenerateAllocFcn	off
UseToolchainInfoCompliant	on
GenerateSharedConstants	off
LUTObjectStructOrderExplicitValues	Size,Breakpoints,Table
LUTObjectStructOrderEvenSpacing	Size,Breakpoints,Table
ArrayLayout	Column-major
UnsupportedSFcnMsg	error
ERTHeaderFileRootName	RE
ERTSourceFileRootName	RE
ERTDataFileRootName	$R_data
GenerateASAP2	off
DSAsUniqueAccess	off
ExtMode	off
ExtModeTransport	0
ExtModeStaticAlloc	off
ExtModeStaticAllocSize	1000000
ExtModeTesting	off
ExtModeMexFile	ext_comm
ExtModeMexArgs	
ExtModeIntrfLevel	Level1
TargetOS	BareBoardExample
MultiInstanceErrorCode	Error
RootIOFormat	Individual arguments
RTWCAPISignals	off
RTWCAPIParams	off
RTWCAPIStates	off
RTWCAPIRootIO	off
ERTSrcFileBannerTemplate	ert_code_template.cgt
ERTHdrFileBannerTemplate	ert_code_template.cgt
ERTDataSrcFileTemplate	ert_code_template.cgt
ERTDataHdrFileTemplate	ert_code_template.cgt
ERTCustomFileTemplate	example_file_process.tlc

EnableDataOwnership	off
SignalDisplayLevel	10
ParamTuneLevel	10
GlobalDataDefinition	Auto
DataDefinitionFile	global.c
GlobalDataReference	Auto
ERTFilePackagingFormat	Compact
RateTransitionBlockCode	Inline
DataReferenceFile	global.h
PreserveExpressionOrder	on
PreserveIfCondition	on
ConvertIfToSwitch	off
PreserveExternInFcnDecls	on
PreserveStaticInFcnDecls	on
SuppressUnreachableDefaultCases	off
EnableSignedLeftShifts	off
EnableSignedRightShifts	off
IndentStyle	K&R
IndentSize	2
NewlineStyle	Default
MaxLineWidth	80
EnableUserReplacementTypes	off
ReplacementTypes	Heli_inner_loop Configuration Set.Components(8).Components(2).ReplacementTypes [36]
MaxIdInt64	MAX_int64_T
MinIdInt64	MIN_int64_T
MaxIdUint64	MAX_uint64_T
MaxIdInt32	MAX_int32_T
MinIdInt32	MIN_int32_T
MaxIdUint32	MAX_uint32_T
MaxIdInt16	MAX_int16_T
MinIdInt16	MIN_int16_T
MaxIdUint16	MAX_uint16_T
MaxIdInt8	MAX_int8_T
MinIdInt8	MIN_int8_T
MaxIdUint8	MAX_uint8_T
BooleanTrueId	true
BooleanFalseId	false

TypeLimitIdReplacementHeaderFile	
MemSecPackage	--- None ---
MemSecDataConstants	Default
MemSecDataIO	Default
MemSecDataInternal	Default
MemSecDataParameters	Default
MemSecFuncInitTerm	Default
MemSecFuncExecute	Default
MemSecFuncSharedUtil	Default

Table 6.16. Heli_inner_loop Configuration Set.Components(8).Components(2) [32].ReplacementTypes

Field	Value
double	
single	
int32	
int16	
int8	
uint32	
uint16	
uint8	
boolean	
int	
uint	
char	
uint64	
int64	

Table 6.17. HDL Coder

Property	Value
HDLSubsystem	Heli_inner_loop
Workflow	Generic ASIC/FPGA
TargetPlatform	
ReferenceDesign	
ReferenceDesignPath	
CoeffPrefix	coeff
InputType	std_logic_vector
OutputType	Same as input type
ScalarizePorts	off

CoeffMultipliers	Multiplier
ResetType	Asynchronous
FIRAdderStyle	linear
MultiplierInputPipeline	0
MultiplierOutputPipeline	0
FoldingFactor	1
NumMultipliers	-1
OptimizeForHDL	off
TimingControllerPostfix	_tc
OptimizeTimingController	on
TimingControllerArch	default
CastBeforeSum	on
TCCounterLimitCompOp	>=
CheckHDL	off
EnablePrefix	enb
ClockEnableInputPort	clk_enable
ClockEnableOutputPort	ce_out
ClockInputPort	clk
ClockEdge	Rising
ResetInputPort	reset
SimulatorFlags	
HDLCompileFilePostfix	_compile.do
HDLCompileInit	vlib %s\n
HDLCompileTerm	
HDLCompileVerilogCmd	vlog %s %s\n
HDLCompileVHDLCmd	vcom %s %s\n
EnableForGenerateLoops	on
HDLMapFilePostfix	_map.txt
HDLMapSeparator	
HDLSimCmd	vsim -novopt %s.%s\n
HDLSimFilePostfix	_sim.do
HDLSimProjectFilePostfix	_init.do
HDLSimInit	onbreak resume\nonerror resume\n
HDLSimProjectCmd	project addfile %s\n
HDLSimProjectTerm	project compileall\n
HDLSimProjectInit	project new . %s work\n
HDLSimTerm	run -all\n
HDLSimViewWaveCmd	add wave sim:%s\n
HDLSynthTool	None

HDLSynthCmd	
HDLSynthFilePostfix	
HDLSynthInit	
HDLSynthLibCmd	
HDLSynthLibSpec	
HDLSynthTerm	
ReservedWordPostfix	_rsvd
BlockGenerateLabel	_gen
VHDLLibraryName	work
UseSingleLibrary	off
VHDLArchitectureName	rtl
ClockProcessPostfix	_process
ComplexImagPostfix	_im
ComplexRealPostfix	_re
EntityConflictPostfix	_block
InstancePrefix	u_
InstancePostfix	
InstanceGenerateLabel	_gen
OutputGenerateLabel	outputgen
PackagePostfix	_pkg
SplitEntityArch	off
SplitEntityFilePostfix	_entity
SplitArchFilePostfix	_arch
VectorPrefix	vector_of_
ClockInputs	Single
TriggerAsClock	off
ConditionalizePipeline	off
InferControlPorts	off
UseRisingEdge	off
TargetDirectory	hdlsrc
TargetSubdirectory	Model
EDAScriptGeneration	on
AddInputRegister	on
AddOutputRegister	on
AddPipelineRegisters	off
PipelinePostfix	_pipe
InputPort	filter_in
OutputPort	filter_out
FracDelayPort	filter_fd

Name	filter
RemoveResetFrom	None
ResetAssertedLevel	Active-high
ReuseAccum	off
ScaleWarnBits	3
SerialPartition	-1
DALUTPartition	-1
DARadix	2
CoefficientSource	Internal
CoefficientMemory	Registers
InputComplex	off
AddRatePort	off
InputDataType	
GenerateHDLCode	on
GenerateModel	on
GenerateTB	off
GenerateCEGenModel	off
ObfuscateGeneratedHDLCode	off
Traceability	off
ResourceReport	off
OptimizationReport	off
ErrorCheckReport	on
HDLGenerateWebview	off
IPCoreReport	off
Recommendations	off
RequirementComments	on
Backannotation	off
HierarchicalDistPipelining	off
PreserveDesignDelays	off
AcquireDesignDelaysForEMLOptimizations	off
ClockRatePipelining	on
CRPWithoutFlattening	on
UseCRPAlternativeStrategy	off
IncreaseCRPBudget	on
AdaptivePipelining	on
MinDelaysRequiredAtLocalMultirateOutput	1
ClockRatePipelineOutputPorts	off

CriticalPathEstimation	off
StaticLatencyPathAnalysis	off
optimizeserializer	on
shareequalwl	on
sharedmulsign	Signed
MultiplierPromotionThreshold	0
RoutingFudgeFactor	0.5000
OptimizationCompatibilityCheck	off
NumCriticalPathsEstimated	1
CriticalPathEstimationFile	criticalPathEstimated
SLPAFile	staticLatPathAnalysis
SLPALoopsFile	staticLatLoops
SLPABackEdgeFile	staticLatLoopBackEdge
SLPAGMMapMATFile	staticLatGMMap
HardwarePipeliningCharacterizationFile	
HighlightFeedbackLoops	on
HighlightFeedbackLoopsFile	highlightFeedbackLoop
HighlightClockRatePipeliningDiagnostic	on
HighlightClockRatePipeliningFile	highlightClockRatePipelining
DistributedPipeliningBarriers	on
DistributedPipeliningBarriersFile	highlightDistributedPipeliningBarriers
BlocksWithNoCharacterizationFile	highlightCriticalPathEstimationOffending-Blocks
AXIStreamingTransformFeatureControl	off
SerializerRatioThreshold	8192
RetimingCP	off
RetimingCPFile	highlightRetimingCP
ClearHighlightingFile	clearhighlighting
FunctionallyEquivalentRetiming	on
DistributedPipeliningPriority	Numerical Integrity
RetimingDetails	on
CriticalPathDetails	off
SignalNamesMangling	off
GuidedRetiming	off
LatencyConstraint	0
ReduceMatchingDelays	on
OptimizationData	
CPGuidanceFile	
CPAnnotationFile	

HandleAtomicSubsystem	on
OptimizeMdlGen	on
MulticyclePathInfo	off
MulticyclePathConstraints	off
FloatingPointTargetConfiguration	
GenerateTargetComps	on
NativeFloatingPoint	off
FPToleranceValue	1.0000e-07
FPToleranceStrategy	DEFAULT
nfpLatency	DEFAULT
nfpDenormals	DEFAULT
sschdlMatrixVectorProductEarlyElaborate	off
sschdlMatrixProductSumCustomLatency	-1
AlteraBackwardIncompatibleSinCosPipeline	off
FamilyDevicePackageSpeed	
ToolName	
SynthesisToolChipFamily	
SynthesisToolDeviceName	
SynthesisToolPackageName	
SynthesisToolSpeedValue	
SynthesisTool	
SynthesisProjectAdditionalFiles	
SimulationLibPath	
XilinxSimulatorLibPath	
AdderSharingMinimumBitwidth	0
MultiplierSharingMinimumBitwidth	0
MultiplyAddSharingMinimumBitwidth	0
ShareAdders	off
ShareMultipliers	on
ShareMultiplyAdds	on
ShareMATLABBlocks	on
ShareAtomicSubsystems	on
ShareFloatingPointIPs	on
PipelinedSharing	on
OptimizeCRPSharingRegisters	on
ClockRatePipeliningBudgetCheck	off
EnableFPGAWorkflow	off
FPGAWorkflowParameters	

GainMultipliers	Multiplier
ProductOfElementsStyle	linear
UserComment	
CustomFileHeaderComment	
CustomFileFooterComment	
DateComment	on
SafeZeroConcat	on
SumOfElementsStyle	linear
TargetLanguage	VHDL
Oversampling	1
ClockRatePipeliningFraction	1
Verbosity	1
TestBenchName	filter_tb
MultifileTestBench	off
IgnoreDataChecking	0
TestBenchPostfix	_tb
TestBenchDataPostfix	_data
TestBenchStimulus	
TestBenchUserStimulus	
TestBenchFracDelayStimulus	
TestBenchCoeffStimulus	
TestBenchRateStimulus	
ForceClockEnable	on
MinimizeClockEnables	off
MinimizeGlobalResets	off
NoResetInitializationMode	InsideModule
NoResetInitScript	noresetinitscript.tcl
ComplexMulElaboration	MultiplyAddBlock
FlattenBus	off
TestBenchClockEnableDelay	1
ForceClock	on
ClockHighTime	5
ClockLowTime	5
HoldTime	2
InputDataInterval	0
ForceReset	on
ErrorMargin	4
HoldInputDataBetweenSamples	on
InitializeTestBenchInputs	off

ResetLength	2
TestBenchReferencePostFix	_ref
GenerateValidationModel	off
RAMMappingThreshold	256
MapPipelineDelaysToRAM	off
RemoveRedundantCounters	on
ReplaceUnitDelayWithIntegerDelay	on
ConcatenateDelays	on
MergeDelaysOnFanouts	on
FoldDelaysToConstant	on
RAMArchitecture	WithClockEnable
InlineMATLABBlockCode	off
InlineHDLCode	off
MaskParameterAsGeneric	off
InlineSubsystems	on
StringTypeSupport	off
DeleteUnusedPorts	on
BalanceDelays	on
TargetFrequency	0
ExtraEffortMargin	1
MaxOversampling	Inf
MaxComputationLatency	1
MultiplierPartitioningThreshold	Inf
TreatDelayBalancingFailureAs	Error
TransformDelaysWithControlLogic	on
TransformNonZeroInitValDelay	on
DelayElaborationLimit	20
GenerateCoSimBlock	off
HDLCodeCoverage	off
GenerateHDLTestBench	on
GenerateCoSimModel	None
GenerateSVDPITestBench	None
SimulationTool	Mentor Graphics Modelsim
CoSimModelSetup	CosimBlockAndDut
SynthesisOnDirective	
SynthesisOffDirective	
LoopUnrolling	off
InlineConfigurations	on
UseAggregatesForConst	off

UseVerilogTimescale	on
Timescale	`timescale 1 ns / 1 ns
VerilogFileExtension	.v
SystemVerilogFileExtension	.sv
VHDLFileExtension	.vhd
CodeGenerationOutput	GenerateHDLCode
GeneratedModelName	
GeneratedModelNamePrefix	gm_
ValidationModelNameSuffix	_vnl
UseDotLayout	off
ShowCodeGenPIR	off
SerializeModel	0
SerializeIO	0
AutoRoute	on
AutoPlace	on
InterBlkHorzScale	1.7000
InterBlkVertScale	1.2000
CustomDotPath	
HighlightAncestors	on
HighlightColor	cyan
InitializeBlockRAM	on
InitializeRealPort	off
MapVectorPortToStream	off
UseFileIOInTestBench	on
TurnkeyWorkflow	off
AlteraWorkflow	off
GenerateFILBlock	off
CoSimLibPostfix	_cosim
TestBenchInitializeInputs	off
MinimizeIntermediateSignals	off
GenerateCodeInfo	off
GatewayoutWithDTC	off
IncrementalCodeGenForTopModel	off
HDLWFSmartbuild	on
HDLCodingStandard	None
HDLCodingStandardCustomizations	
ReferenceDesignParameter	
HDLLintTool	None
HDLLintInit	

HDLLintTerm	
HDLLintCmd	
ModulePrefix	
DetectBlackBoxNameCollision	Warning
PIRTB	on
PIRTC	off
EmitNetlist	off
UsePipelinedToolboxFunctions	on
savepirtoscript	off
ConcatenateHDLModules	off
AMS	off
ML2PIR	off
OptimBetweenMATLABAndSimulink	off
EnableTestpoints	off
TraceabilityStyle	Line Level
TreatRealsInGeneratedCodeAs	Error
EnumEncodingScheme	default
BuildToProtectModel	off
OptimizeConstants	on
StreamingMatrix	off
HDLDTO	off
UseArrangeSystem	off
TriggerAsClockWithoutSyncRegisters	off

Chapter 7. Glossary

Atomic Subsystem. A subsystem treated as a unit by an implementation of the design documented in this report. The implementation computes the outputs of all the blocks in the atomic subsystem before computing the next block in the parent system's block execution order (sorted list).

Block Diagram. A Simulink block diagram represents a set of simultaneous equations that relate a system or subsystem's inputs to its outputs as a function of time. Each block in the diagram represents an equation of the form y = f(t, x, u) where t is the current time, u is a block input, y is a block output, and x is a system state (see the Simulink documentation for information on the functions represented by the various types of blocks that make up the diagram). Lines connecting the blocks represent dependencies among the blocks, i.e., inputs whose current values are the outputs of other blocks. An implementation of a design described in this document computes a root or atomic system's outputs at each time step by computing the outputs of the blocks in an order determined by block input/output dependencies.

Block Parameter. A variable that determines the output of a block along with its inputs, for example, the gain parameter of a Gain block.

Block Execution Order. The order in which Simulink evaluates blocks during simulation of a model. The block execution order determined by Simulink ensures that a block executes only after all blocks on whose outputs it depends are executed.

Checksum. A number that indicates whether different versions of a model or atomic subsystem differ functionally or only cosmetically. Different checksums for different versions of the same model or subsystem indicate that the versions differ functionally.

Design Variable. A symbolic (MATLAB) variable or expression used as the value of a block parameter. Design variables allow the behavior of the model to be altered by altering the value of the design variable.

Signal. A block output, so-called because block outputs typically vary with time.

Virtual Subsystem. A subsystem that is purely graphical, i.e., is intended to reduce the visual complexity of the block diagram of which it is a subsystem. An implementation of the design treats the blocks in the subsystem as part of the first nonvirtual ancestor of the virtual subsystem (see Atomic Subsystem).

Chapter 8. About this Report

Table of Contents

8.1. Report Overview

This report describes the design of the Heli_inner_loop system. The report was generated automatically from a Simulink model used to validate the design. It contains the following sections:

Model Version. Specifies information about the version of the model from which this design description was generated. Includes the model checksum, a number that indicates whether different versions of the model differ functionally or only cosmetically. Different checksums for different versions indicate that the versions differ functionally.

Root System. Describes the design's root system.

Subsystems. Describes each of the design's subsystems.

Design Variables. Describes system design variables, i.e., MATLAB variables and expressions used as block parameter values.

System Model Configuration. Lists the configuration parameters, e.g., start and stop time, of the model used to simulate the system described by this report.

Requirements. Shows design requirements associated with elements of the design model. This section appears only if the design model contains requirements links.

Glossary. Defines Simulink terms used in this report.

8.2. Root System Description

This section describes a design's root system. It contains the following sections:

Diagram. Simulink block diagram that represents the algorithm used to compute the root system's outputs.

Description. Description of the root system. This section appears only if the model's root system has a Documentation property or a Doc block.

Interface. Name, data type, width, and other properties of the root system's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the root system has input or output ports.

Blocks. This section has two subsections:

- **Parameters.** Describes key parameters of blocks in the root system. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, i.e., blocks that use lookup tables to compute their outputs.
- **Block Execution Order.** Order in which blocks must be executed at each time step in order to ensure that each block's inputs are available when it executes.

State Charts. Describes state charts used in the root system. This section appears only if the root system contains Stateflow blocks.

8.3. Subsystem Descriptions

This section describes a design's subsystems. Each subsystem description contains the following sections:

Checksum. This section appears only if the subsystem is an atomic subsystem. The checksum indicates whether the version of the model subsystem used to generate this report differs functionally from other versions of the model subsystem. If two model checksums differ, the corresponding versions of the model differ functionally.

Diagram. Simulink block diagram that graphically represents the algorithm used to compute the subsystem's outputs.

Description. Description of the subsystem. This section appears only if the subsystem has a Documentation property or contains a Doc block.

Interface. Name, data type, width, and other properties of the subsystem's input and output signals. The number of the block port that outputs the signal appears in angle brackets appended to the signal name. This section appears only if the subsystem is atomic and has input or output ports.

Blocks. Blocks that this subsystem contains. This section has two subsections:

- **Parameters.** Key parameters of blocks in the subsystem. This section also includes graphical and/or tabular representations of lookup table data used by lookup table blocks, blocks that use lookup tables to compute their outputs.
- **Block Execution Order.** Order in which the subsystem's blocks must be executed at each time step in order to ensure that each block's inputs are available when the block executes .This section appears only if the subsystem is atomic. Note: in Acrobat(PDF) reports, the number in square brackets next to the block name is a hyperlink to the block parameter table. The number has no model significance.

State Charts. Describes state charts used in the subsystem. This section appears only if the root system contains Stateflow blocks.

8.4. State Chart Descriptions

This section describes the state machines used by Stateflow blocks to compute their outputs, i.e., Stateflow blocks. Each state machine description contains the following sections:

Chart. Diagram representing the state machine.

States. Describes the state machine's states. Each state description includes the state's diagram and diagrams and/or descriptions of graphical functions, Simulink functions, truth tables, and MATLAB functions parented by the state.

Transitions. Transitions between the state machine's states. Each transition description specifies the values of key transition properties. Appears only if a transition has properties that do not appear on the chart.

Junctions. Transition junctions. Each junction description specifies the values of key junction properties. Appears only if a junction has properties that do not appear on the chart.

Events. Events that trigger state transitions. Each event description specifies the values of key event properties.

Data. Data types and other properties of the Stateflow block's inputs, outputs, and other state machine data.

Targets. Executable implementations of the state machine used to compute the outputs of the corresponding Stateflow block.

MATLAB Supporting Functions. List of functions invoked by MATLAB functions defined in the chart.