Simulink Design Verifier Report

C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\FCC\verification\design_error_detections\dead_logic\FCC_replacement.slx

bpotter

Simulink Design Verifier Report: C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\FCC\verification\design_error_detections\dead_logic\FCC_replacement.slx

bpotter

Publication date 13-May-2020 15:23:23

Table of Contents

Chapter 1. Summary

Analysis Information.

Model:	FCC
Replacement Model:	C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\FCC\verification\design_error_detections\dead_logic\FCC_replacement.slx
Mode:	Design error detection
Model Representation:	Built on 13-May-2020 15:18:15
Status:	Exceeded time limit
PreProcessing Time:	13s
Analysis Time:	299s

Objectives Status.

Number of Objectives:	**135**
Objectives Valid:	10
Objectives Undecided:	4
Dead Logic:	6

Chapter 2. Analysis Information

Table of Contents

Model Information

File:	FCC
Version:	1.71
Time Stamp:	Mon May 11 08:00:40 2020
Author:	bpotter

Analysis Options

Mode:	DesignErrorDetection
Rebuild Model Representation:	IfChangeIsDetected
Detect dead logic:	on
Detect active logic:	off
Detect integer overflow:	on
Detect division by zero:	on
Detect specified minimum and maximum value violations:	on
Detect out of bound array access:	on
Detect non-finite and NaN floating-point values:	off
Detect subnormal floating-point values:	off
Detect data store access violations:	off
Maximum Analysis Time:	300s
Block Replacement:	off
Parameters Analysis:	off
Include expected output values:	off
Randomize data that do not affect the outcome:	off
Additional analysis to reduce instances of rational approximation:	on
Save Data:	on

Save Harness:	off
Save Report:	on

Constraints

Design Min Max Constraints

Name	Design Min Max Constraint
Act_Pos1	[-32768..32767]
Act_Pos2	[-32768..32767]
Act_Pos3	[-32768..32767]
AHRS1	[-180..180]
AHRS1	[-180..180]
AHRS1	[-180..180]
AHRS1	[-180..180]
AHRS1	[-180..180]
AHRS2	[-180..180]
AHRS2	[-180..180]
AHRS2	[-180..180]
AHRS2	[-180..180]
AHRS2	[-180..180]
AHRS3	[-180..180]
AHRS3	[-180..180]
AHRS3	[-180..180]
AHRS3	[-180..180]
AHRS3	[-180..180]
Pilot_theta_cmd	[-32768..32767]
Pilot_phi_cmd	[-32768..32767]
Pilot_r_cmd	[-32768..32767]

Approximations

Simulink Design Verifier performed the following approximations during analysis. These can impact the precision of the results generated by Simulink Design Verifier. Please see the product documentation for further details.

#	Type	Description
1	Multi-instance Model reference approximation	The model being analyzed references at least one model more than once. Simulink Design Verifier copies referenced model contents into the replacement model before analysis so that coverage objectives for each instance of a model are treated separately. This differs from Model Coverage reporting

#	Type	Description
		that combines instances for coverage. Coverage results from simulating test cases may differ from analysis results.

Chapter 3. Dead Logic

Simulink Design Verifier found that these decision and condition outcomes cannot occur and are dead logic in the model. Dead logic in the model can also be a side effect of parameter configurations or minimum and maximum constraints specified on input.

#	Type	Model Item	Description
1	Decision	ActuatorControl1/Saturation	input > lower limit **can only be true**
2	Decision	ActuatorControl1/Saturation	input >= upper limit **can never be true**
3	Decision	ActuatorControl2/Saturation	input > lower limit **can only be true**
4	Decision	ActuatorControl2/Saturation	input >= upper limit **can never be true**
5	Decision	ActuatorControl3/Saturation	input > lower limit **can only be true**
6	Decision	ActuatorControl3/Saturation	input >= upper limit **can never be true**

Chapter 4. Design Error Detection Objectives Status

Table of Contents

Objectives Valid

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
1	Design Range	RateTransition1	Design Range: [-0.1..0.1]	18	n/a
3	Design Range	RateTransition2	Design Range: [-0.1..0.1]	18	n/a
5	Design Range	RateTransition3	Design Range: [-0.1..0.1]	18	n/a
28	Division by zero	ActuatorControl1/TypeConversion6	Division by zero	18	n/a
53	Division by zero	ActuatorControl2/TypeConversion6	Division by zero	18	n/a
78	Division by zero	ActuatorControl3/TypeConversion6	Division by zero	18	n/a
101	Integer overflow	Model2/Sum	Overflow	18	n/a
219	Design Range	Model1/Saturation	Design Range: [-30..30]	18	n/a
226	Design Range	Model1/Saturation1	Design Range: [-30..30]	18	n/a
233	Design Range	Model1/Saturation2	Design Range: [-30..30]	18	n/a

Objectives Undecided

Simulink Design Verifier was not able to process these objectives with the current options.

#	Type	Model Item	Description	Analysis Time (sec)	Test Case
29	Integer overflow	ActuatorControl1/TypeConversion6	Overflow	-1	n/a
54	Integer overflow	ActuatorControl2/TypeConversion6	Overflow	-1	n/a
79	Integer overflow	ActuatorControl3/TypeConversion6	Overflow	-1	n/a
107	Design Range	Model2/MultiportSwitch	Design Range: [-180..180]	-1	n/a

Chapter 5. Derived Ranges

Signal	Derived Ranges
RateTransition1- Outport 1	[-0.1..0.1]
RateTransition2- Outport 1	[-0.1..0.1]
RateTransition3- Outport 1	[-0.1..0.1]
Act_Pos1- Outport 1	[-32768..32767]
ActuatorControl1/TypeConversion- Outport 1	[-32768..32767]
ActuatorControl1/Scaling- Outport 1	[-0.1..0.1]
ActuatorControl1/Sum- Outport 1	[-0.2..0.2]
ActuatorControl1/Difference/UD- Outport 1	[-0.2..0.2]
ActuatorControl1/Difference/Diff- Outport 1	[-0.4..0.4]
ActuatorControl1/Gain- Outport 1	[-0.0678..0.067801]
ActuatorControl1/Gain1- Outport 1	[-0.001088..0.001088]
ActuatorControl1/Gain2- Outport 1	[-0.546..0.54601]
ActuatorControl1/Integrator- Outport 1	[-0.1..0.1]
ActuatorControl1/Sum1- Outport 1	[-0.16889..0.16889]
ActuatorControl1/Saturation- Outport 1	[-0.16889..0.16889]
ActuatorControl1/Scaling6- Outport 1	[-18447..18447]
ActuatorControl1/TypeConversion6- Outport 1	[-18447..18446]
Actuator1- Outport 1	[-18447..18446]
Act_Pos2- Outport 1	[-32768..32767]
ActuatorControl2/TypeConversion- Outport 1	[-32768..32767]
ActuatorControl2/Scaling- Outport 1	[-0.1..0.1]
ActuatorControl2/Sum- Outport 1	[-0.2..0.2]
ActuatorControl2/Difference/UD- Outport 1	[-0.2..0.2]
ActuatorControl2/Difference/Diff- Outport 1	[-0.4..0.4]
ActuatorControl2/Gain- Outport 1	[-0.0678..0.067801]
ActuatorControl2/Gain1- Outport 1	[-0.001088..0.001088]
ActuatorControl2/Gain2- Outport 1	[-0.546..0.54601]
ActuatorControl2/Integrator- Outport 1	[-0.1..0.1]
ActuatorControl2/Sum1- Outport 1	[-0.16889..0.16889]
ActuatorControl2/Saturation- Outport 1	[-0.16889..0.16889]
ActuatorControl2/Scaling6- Outport 1	[-18447..18447]
ActuatorControl2/TypeConversion6- Outport 1	[-18447..18446]
Actuator2- Outport 1	[-18447..18446]
Act_Pos3- Outport 1	[-32768..32767]
ActuatorControl3/TypeConversion- Outport 1	[-32768..32767]
ActuatorControl3/Scaling- Outport 1	[-0.1..0.1]

Signal	Derived Ranges
ActuatorControl3/Sum- Outport 1	[-0.2..0.2]
ActuatorControl3/Difference/UD- Outport 1	[-0.2..0.2]
ActuatorControl3/Difference/Diff- Outport 1	[-0.4..0.4]
ActuatorControl3/Gain- Outport 1	[-0.0678..0.067801]
ActuatorControl3/Gain1- Outport 1	[-0.001088..0.001088]
ActuatorControl3/Gain2- Outport 1	[-0.546..0.54601]
ActuatorControl3/Integrator- Outport 1	[-0.1..0.1]
ActuatorControl3/Sum1- Outport 1	[-0.16889..0.16889]
ActuatorControl3/Saturation- Outport 1	[-0.16889..0.16889]
ActuatorControl3/Scaling6- Outport 1	[-18447..18447]
ActuatorControl3/TypeConversion6- Outport 1	[-18447..18446]
Actuator3- Outport 1	[-18447..18446]
Model2/Constant- Outport 1	0
AHRS1- Outport 1- Bus element AHRS_Bus.valid	[F..T]
AHRS1- Outport 1- Bus element AHRS_Bus.theta	[-180..180]
AHRS1- Outport 1- Bus element AHRS_Bus.phi	[-180..180]
AHRS1- Outport 1- Bus element AHRS_Bus.r	[-180..180]
AHRS1- Outport 1- Bus element AHRS_Bus.q	[-180..180]
AHRS1- Outport 1- Bus element AHRS_Bus.p	[-180..180]
AHRS2- Outport 1- Bus element AHRS_Bus.valid	[F..T]
AHRS2- Outport 1- Bus element AHRS_Bus.theta	[-180..180]
AHRS2- Outport 1- Bus element AHRS_Bus.phi	[-180..180]
AHRS2- Outport 1- Bus element AHRS_Bus.r	[-180..180]
AHRS2- Outport 1- Bus element AHRS_Bus.q	[-180..180]
AHRS2- Outport 1- Bus element AHRS_Bus.p	[-180..180]
AHRS3- Outport 1- Bus element AHRS_Bus.valid	[F..T]
AHRS3- Outport 1- Bus element AHRS_Bus.theta	[-180..180]
AHRS3- Outport 1- Bus element AHRS_Bus.phi	[-180..180]
AHRS3- Outport 1- Bus element AHRS_Bus.r	[-180..180]
AHRS3- Outport 1- Bus element AHRS_Bus.q	[-180..180]
AHRS3- Outport 1- Bus element AHRS_Bus.p	[-180..180]
Model2/Sum- Outport 1	[0..3]
Model2/MultiportSwitch- Outport 1	[-540..540]
Model2/Single_Value/Constant- Outport 1	0
Model2/Avg_Value/Constant- Outport 1	0
Model2/Single_Value/Switch- Outport 1	[-180..180]
Model2/Avg_Value/Switch- Outport 1	[-180..180]
Pilot_theta_cmd- Outport 1	[-32768..32767]

Signal	Derived Ranges
Model2/Mid_Value/MinMax- Outport 1	[-180..180]
Model1/TypeConversion- Outport 1	[-32768..32767]
Model2/Single_Value/Switch1- Outport 1	[-180..180]
Model2/Avg_Value/Switch1- Outport 1	[-180..180]
Model1/Scaling- Outport 1	[-30.001..30]
Model2/Mid_Value/MinMax1- Outport 1	[-180..180]
Model1/Sum- Outport 1	[-570..570]
Model2/Single_Value/Switch2- Outport 1	[-180..180]
Model2/Avg_Value/Switch2- Outport 1	[-180..180]
Model1/Gain- Outport 1	[-758.1..758.1]
Pilot_phi_cmd- Outport 1	[-32768..32767]
Model2/Mid_Value/MinMax2- Outport 1	[-180..180]
Model1/TypeConversion1- Outport 1	[-32768..32767]
Model2/Single_Value/Sum- Outport 1	[-360..540]
Model2/Avg_Value/Sum- Outport 1	[-540..540]
Model1/Scaling1- Outport 1	[-30.001..30]
Model2/Mid_Value/MinMax3- Outport 1	[-180..180]
Model2/Avg_Value/Gain- Outport 1	[-270..270]
Model1/Sum1- Outport 1	[-570..570]
Model1/Gain1- Outport 1	[-49.02..49.02]
Model1/Gain2- Outport 1	[-1282.5..1282.5]
Model1/Gain3- Outport 1	[-678.3..678.3]
Pilot_r_cmd- Outport 1	[-32768..32767]
Model1/TypeConversion2- Outport 1	[-32768..32767]
Model1/Scaling2- Outport 1	[-15..15]
Model1/Sum2- Outport 1	[-555..555]
Model1/Gain4- Outport 1	[-73.815..73.815]
Model1/Gain5- Outport 1	[-1293.2..1293.2]
Model1/Integrator- Outport 1	[-10..10]
Model1/Integrator1- Outport 1	[-10..10]
Model1/Integrator2- Outport 1	[-10..10]
Model1/Sum3- Outport 1	[-768.1..768.1]
Model1/Saturation- Outport 1	[-30..30]
Model1/Sum4- Outport 1	[-59.02..59.02]
Model1/Saturation1- Outport 1	[-30..30]
Model1/Sum5- Outport 1	[-83.815..83.815]
Model1/Saturation2- Outport 1	[-30..30]
Model/SOF- Outport 1	[-1937.1..1937.1]

Signal	Derived Ranges
Model/Sum5- Outport 1	[-1967.1..1967.1]
Model/RollOff1/s_1- Outport 1	[-331.27..331.27]
Model/RollOff1/UnitDelay- Outport 1	[-Inf..Inf]
Model/RollOff1/a_2_1- Outport 1	[-Inf..Inf]
Model/RollOff1/SumA21- Outport 1	[-Inf..Inf]
Model/RollOff1/SumB21- Outport 1	{ [-Inf..Inf] NaN }
Model/Sum4- Outport 1	[-811.55..811.55]
Model/RollOff2/s_1- Outport 1	[-136.67..136.67]
Model/RollOff2/UnitDelay- Outport 1	[-Inf..Inf]
Model/RollOff2/a_2_1- Outport 1	[-Inf..Inf]
Model/RollOff2/SumA21- Outport 1	[-Inf..Inf]
Model/RollOff2/SumB21- Outport 1	{ [-Inf..Inf] NaN }
Model/Sum6- Outport 1	[-1200.8..1200.8]
Model/RollOff3/s_1- Outport 1	[-202.23..202.23]
Model/RollOff3/UnitDelay- Outport 1	[-Inf..Inf]
Model/RollOff3/a_2_1- Outport 1	[-Inf..Inf]
Model/RollOff3/SumA21- Outport 1	[-Inf..Inf]
Model/RollOff3/SumB21- Outport 1	{ [-Inf..Inf] NaN }
Model/Gain- Outport 1	{ [-Inf..Inf] NaN }
Model/Saturation- Outport 1	[-0.1..0.1]

Chapter 6. Design Errors

Table of Contents

ActuatorControl1/TypeConversion6

Summary.

Model Item:	ActuatorControl1/TypeConversion6
Type:	Overflow
Status:	Undecided

ActuatorControl2/TypeConversion6

Summary.

Model Item:	ActuatorControl2/TypeConversion6
Type:	Overflow
Status:	Undecided

ActuatorControl3/TypeConversion6

Summary.

Model Item:	ActuatorControl3/TypeConversion6
Type:	Overflow
Status:	Undecided

Model2/MultiportSwitch

Summary.

Model Item:	Model2/MultiportSwitch
Type:	Design Range: [-180..180]
Status:	Undecided