

Report Generated by Test Manager

Title: AHRS_voter SIL Low-Level Tests

Author:






Date: 14-May-2020 12:50:07

Test Environment

Platform: PCWIN64

MATLAB: (R2019b)


Summary

| Name | Outcome | Duration (Seconds) |
|--|---------|-----------------------|
| Results: 2020-May-14 12:49:33 | 2✔ | 30.038 |
|  AHRs_voter_SLDV_Based_Test | 2✔ | 30.037 |
|  SLDV-Based Test | 2✔ | 30.038 |
|  LLR_SLDV | 2✔ | 30.037 |
|  Test Case:1 | ✔ | 21.085 |
|  Test Case:2 | ✔ | 8.946 |

Results: 2020-May-14 12:49:33

Result Type: Result Set
Parent: None
Start Time: 14-May-2020 12:49:33
End Time: 14-May-2020 12:50:03
Outcome: Total: 2, **Passed: 2**

Aggregated Coverage Results

| Analyzed Model | Sim Mode | Complexity | Decision | Function | Function call | Execution |
|--|-------------|------------|----------|----------|---------------|-----------|
|  AHRS voter | ModelRefSIL | 23 | 25% | 100% | 100% | 28% |

[Back to Report Summary](#)

AHRS_voter_SLDV_Based_Test

Test Result Information

Result Type: Test File Result
Parent: [Results: 2020-May-14 12:49:33](#)
Start Time: 14-May-2020 12:49:33
End Time: 14-May-2020 12:50:03
Outcome: Total: 2, **Passed: 2**
Description:

Checksum when compiled as referenced model: 274277033 2770558437
1049845676 2563622565

Checksum when compiled as top model: 1951542874 3450456451 46553782
3275149564

Test Suite Information

Name: AHRS_voter_SLDV_Based_Test

[Back to Report Summary](#)

SLDV-Based Test

Test Result Information

Result Type: Test Suite Result
Parent: [AHRS_voter_SLDV_Based_Test](#)
Start Time: 14-May-2020 12:49:33
End Time: 14-May-2020 12:50:03

Outcome: Total: 2, **Passed: 2**

Test Suite Information

Name: SLDV-Based Test

[Back to Report Summary](#)

LLR_SLDV

Test Result Information

Result Type: Test Case Result
Parent: [SLDV-Based Test](#)
Start Time: 14-May-2020 12:49:33
End Time: 14-May-2020 12:50:03
Outcome: **Passed**
Description:

SIL test for LLR from SLDV.

Test Case Information

Name: LLR_SLDV
Type: Baseline Test

Test Case:1

Test Result Information

Result Type: Test Iteration Result
Parent: [LLR_SLDV](#)
Start Time: 14-May-2020 12:49:33
End Time: 14-May-2020 12:49:54
Outcome: **Passed**

Test Case Information

Name: Test Case:1
Type: Baseline Test
Baseline Name: TestCases_1.mat
Baseline File: C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\verification\simulation_tests\low_level_tests\sl_test_baselines\TestCases_1.mat

Iteration Settings

Test Overrides

| Parameter Name | Value |
|----------------|---|
| ExternalInput | C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\verification\simulation_tests\low_level_tests\AHRS_voter_sldvdata.mat : Test Case:1 |
| Baseline | C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\verification\simulation_tests\low_level_tests\sl_test_baselines\TestCases_1.mat |

Baseline Comparison

| Name | Abs Tol | Rel Tol | Lead Tol | Lag Tol | Max Diff | Data Type 1 | Units 1 | Sample Time 1 | Data Type 2 | Units 2 | Sample Time 2 | Interp | Sync |
|------------------|---------|---------|----------|---------|----------|-------------|---------|---------------|-------------|---------|---------------|--------|-------|
| ✓ voted_fb: 1(1) | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | double | | 0.01 | zoh | union |
| ✓ voted_fb: 1(2) | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | double | | 0.01 | zoh | union |
| ✓ voted_fb: 1(3) | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | double | | 0.01 | zoh | union |
| ✓ voted_fb: 1(4) | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | double | | 0.01 | zoh | union |
| ✓ voted_fb: 1(5) | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | double | | 0.01 | zoh | union |

Simulation

System Under Test Information

Model: AHRS_voter
Harness: AHRS_voter_Harness_SLDV
Harness Owner: AHRS_voter
Simulation Mode: software-in-the-loop (sil)
Override SIL or PIL Mod 0
e:
Configuration Set: ModelReferencing
External Input Name: Test Case:1

External Input File: C:\Users\bpotter\MATLAB\Projects\ARP_DO_Proje
ct\DO_03_Design\AHRS_voter\verification\simulat
ion_tests\low_level_tests\AHRS_voter_sldvdata.m
at : Test Case:1

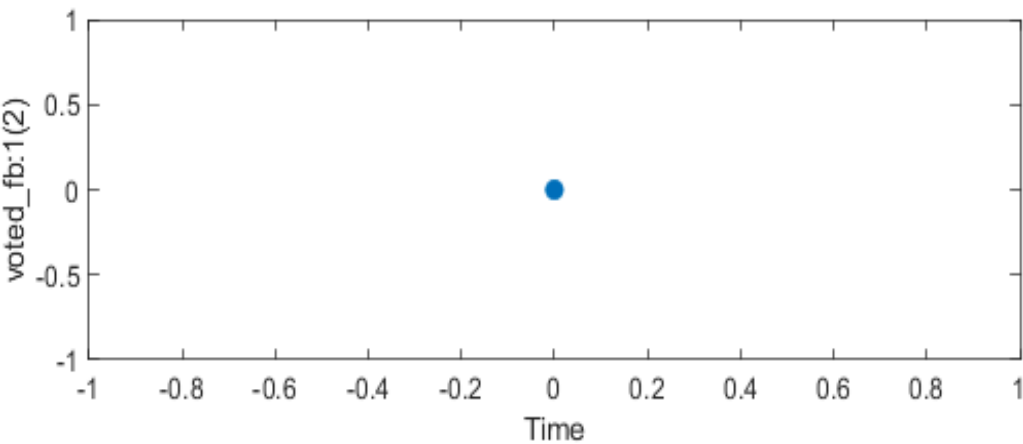
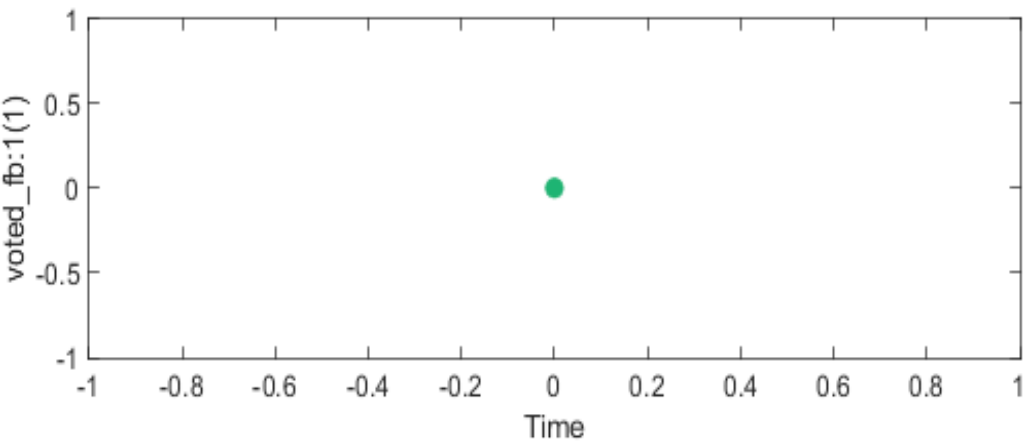
Start Time: 0
Stop Time: 0
Checksum: 1011840354 2562472742 2334803822 1338428446
Simulink Version: 10.0
Model Version: 1.72
Model Author: bpotter
Date: Wed May 13 13:30:04 2020
User ID: bpotter
Model Path: C:\Users\bpotter\MATLAB\Projects\ARP_DO_Proje
ct\DO_03_Design\AHRS_voter\specification\AHRS_
voter_Harness_SLDV.slx

Machine Name: AH-BPOTTER
Solver Name: FixedStepDiscrete
Solver Type: Fixed-Step
Fixed Step Size: 0.01
Simulation Start Time: 2020-05-14 12:49:34
Simulation Stop Time: 2020-05-14 12:49:52
Platform: PCWIN64

Simulation Output

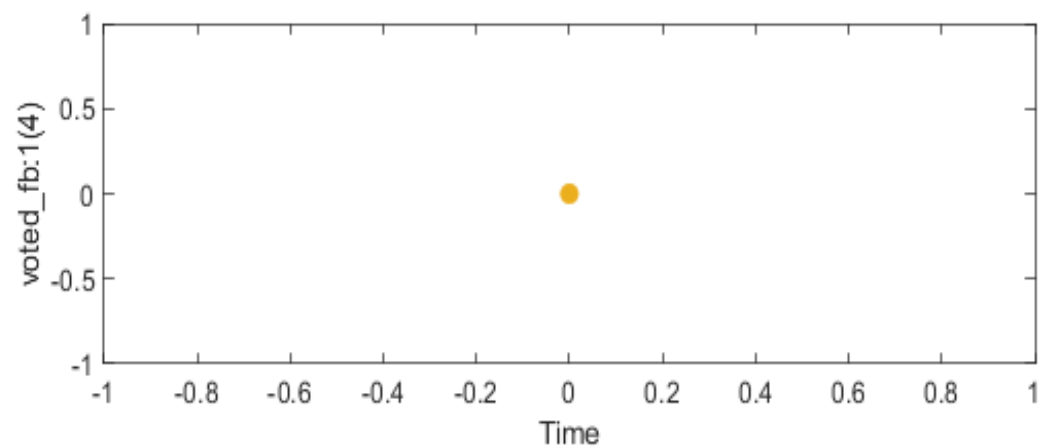
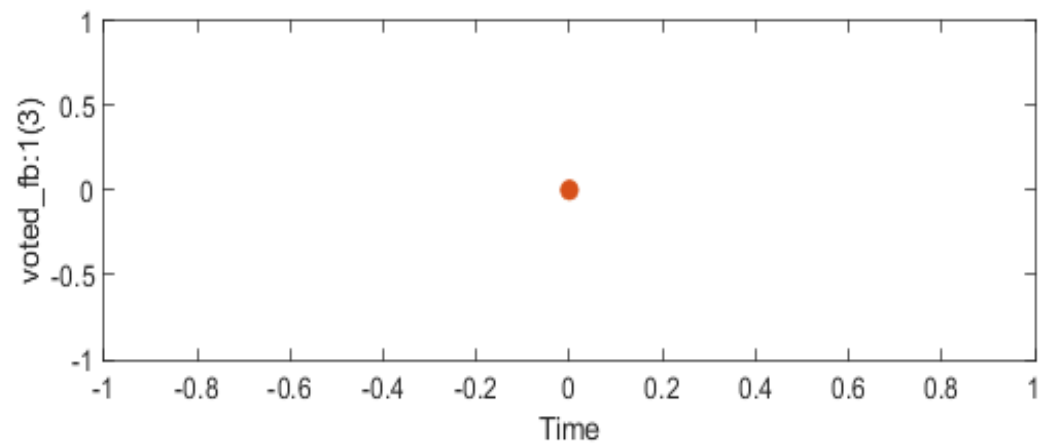
| Name | Data Type | Units | Sample Time | Interp | Sync | Link to Plot |
|---------------|-----------|-------|-------------|--------|-------|----------------------|
| voted_fb:1(1) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(2) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(3) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(4) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(5) | double | | 0.01 | zoh | union | Link |

| Name | Data Type | Units | Sample Time | Interp | Sync |
|---------------|-----------|-------|-------------|--------|-------|
| voted_fb:1(1) | double | | 0.01 | zoh | union |
| voted_fb:1(2) | double | | 0.01 | zoh | union |



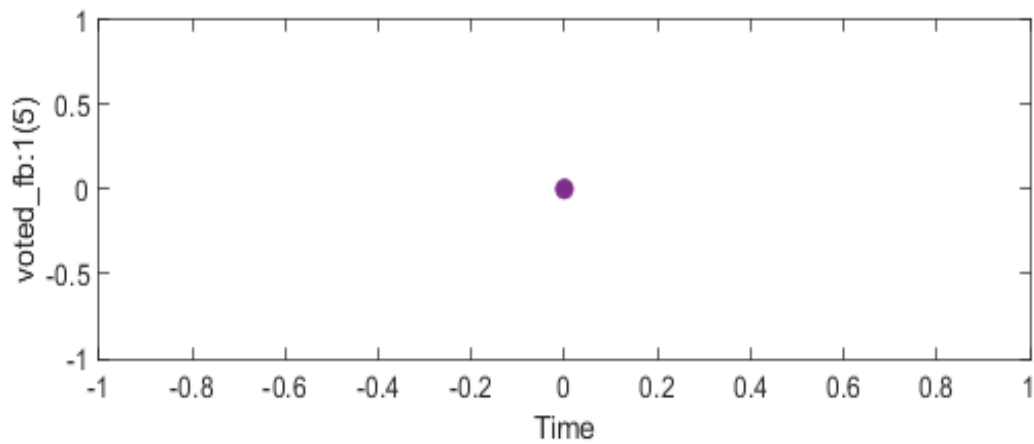
[Back to Report Summary](#)[Back to Signal Summary](#)

| Name | Data Type | Units | Sample Time | Interp | Sync |
|---------------|-----------|-------|-------------|--------|-------|
| voted_fb:1(3) | double | | 0.01 | zoh | union |
| voted_fb:1(4) | double | | 0.01 | zoh | union |



[Back to Report Summary](#)[Back to Signal Summary](#)

| Name | Data Type | Units | Sample Time | Interp | Sync |
|---------------|-----------|-------|-------------|--------|-------|
| voted_fb:1(5) | double | | 0.01 | zoh | union |



[Back to Report Summary](#)[Back to Signal Summary](#)

Simulation Logs:
Inputs are not mapped. Test results might not be accurate.

[Back to Report Summary](#)

Test Case:2

Test Result Information

Result Type: Test Iteration Result
Parent: [LLR_SLDV](#)
Start Time: 14-May-2020 12:49:54
End Time: 14-May-2020 12:50:03
Outcome: **Passed**

Test Case Information

Name: Test Case:2
Type: Baseline Test
Baseline Name: TestCases_2.mat
Baseline File: C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\verification\simulation_tests\low_level_tests\sl_test_baselines\TestCases_2.mat

Iteration Settings

Test Overrides

| Parameter Name | Value |
|----------------|---|
| ExternalInput | C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\verification\simulation_tests\low_level_tests\AHRS_voter_sldvdata.mat : Test Case:2 |
| Baseline | C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\verification\simulation_tests\low_level_tests\sl_test_baselines\TestCases_2.mat |

Baseline Comparison

| Name | Abs Tol | Rel Tol | Lead Tol | Lag Tol | Max Diff | Data Type 1 | Units 1 | Sample Time 1 | Data Type 2 | Units 2 | Sample Time 2 | Interp | Sync |
|------------------|---------|---------|----------|---------|----------|-------------|---------|---------------|-------------|---------|---------------|--------|-------|
| ✓ voted_fb: 1(1) | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | double | | 0.01 | zoh | union |
| ✓ voted_fb: 1(2) | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | double | | 0.01 | zoh | union |

| | | | | | | | | | | | | | | | |
|------|-----------|-------|-------|---|---|---|--------|--|--|--|--------|--|------|-----|-------|
| ✓ | voted_fb: | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | | double | | 0.01 | zoh | union |
| 1(3) | | | | | | | | | | | | | | | |
| ✓ | voted_fb: | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | | double | | 0.01 | zoh | union |
| 1(4) | | | | | | | | | | | | | | | |
| ✓ | voted_fb: | 1e-06 | 0.001 | 0 | 0 | 0 | double | | | | double | | 0.01 | zoh | union |
| 1(5) | | | | | | | | | | | | | | | |

Simulation

System Under Test Information

Model: AHRS_voter
 Harness: AHRS_voter_Harness_SLDV
 Harness Owner: AHRS_voter
 Simulation Mode: software-in-the-loop (sil)
 Override SIL or PIL Mod 0
 e:
 Configuration Set: ModelReferencing
 External Input Name: Test Case:2
 External Input File: C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\verification\simulation_tests\low_level_tests\AHRS_voter_sldvdata.mat : Test Case:2

 Start Time: 0
 Stop Time: 0
 Checksum: 1011840354 2562472742 2334803822 1338428446
 Simulink Version: 10.0
 Model Version: 1.72
 Model Author: bpotter
 Date: Wed May 13 13:30:04 2020
 User ID: bpotter
 Model Path: C:\Users\bpotter\MATLAB\Projects\ARP_DO_Project\DO_03_Design\AHRS_voter\specification\AHRS_voter_Harness_SLDV.slx

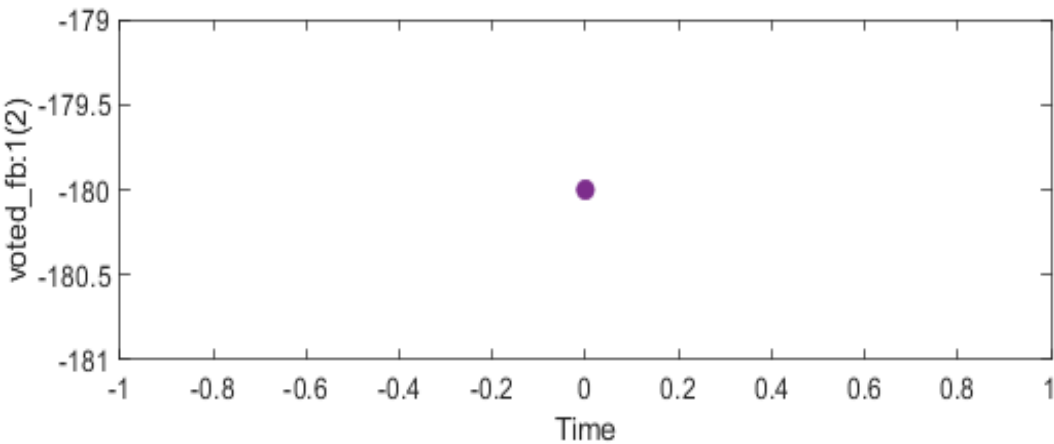
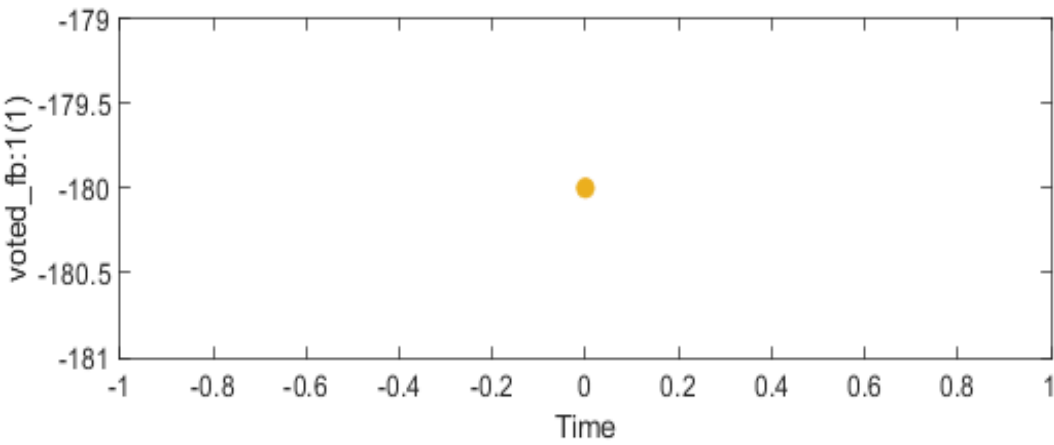
 Machine Name: AH-BPOTTER
 Solver Name: FixedStepDiscrete
 Solver Type: Fixed-Step
 Fixed Step Size: 0.01
 Simulation Start Time: 2020-05-14 12:49:54
 Simulation Stop Time: 2020-05-14 12:50:02

Platform: PCWIN64

Simulation Output

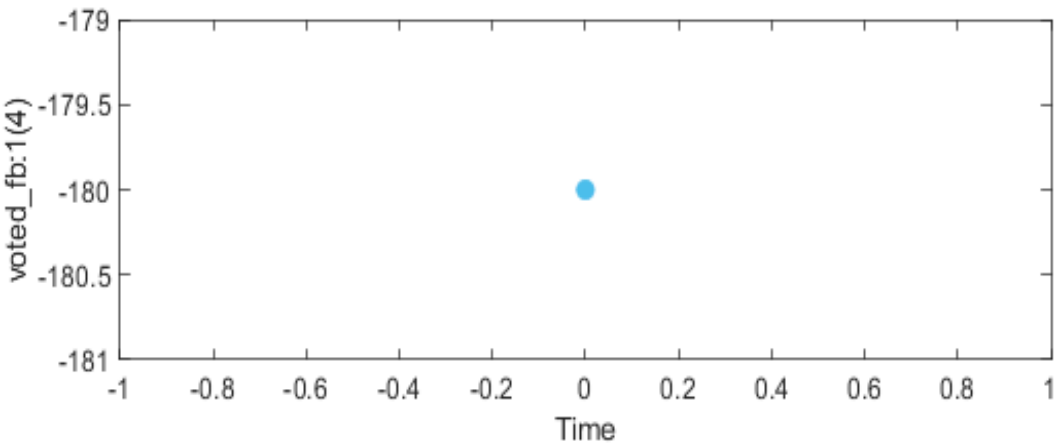
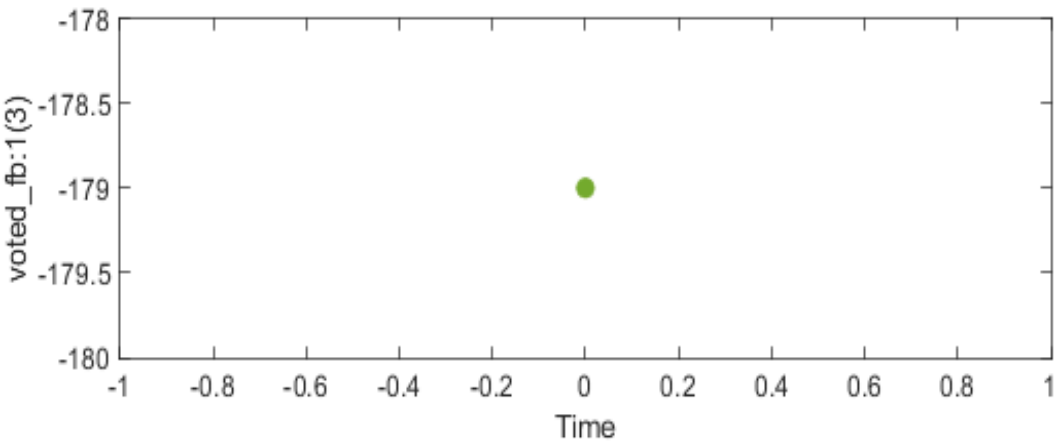
| Name | Data Type | Units | Sample Time | Interp | Sync | Link to Plot |
|---------------|-----------|-------|-------------|--------|-------|----------------------|
| voted_fb:1(1) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(2) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(3) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(4) | double | | 0.01 | zoh | union | Link |
| voted_fb:1(5) | double | | 0.01 | zoh | union | Link |

| Name | Data Type | Units | Sample Time | Interp | Sync |
|---------------|-----------|-------|-------------|--------|-------|
| voted_fb:1(1) | double | | 0.01 | zoh | union |
| voted_fb:1(2) | double | | 0.01 | zoh | union |



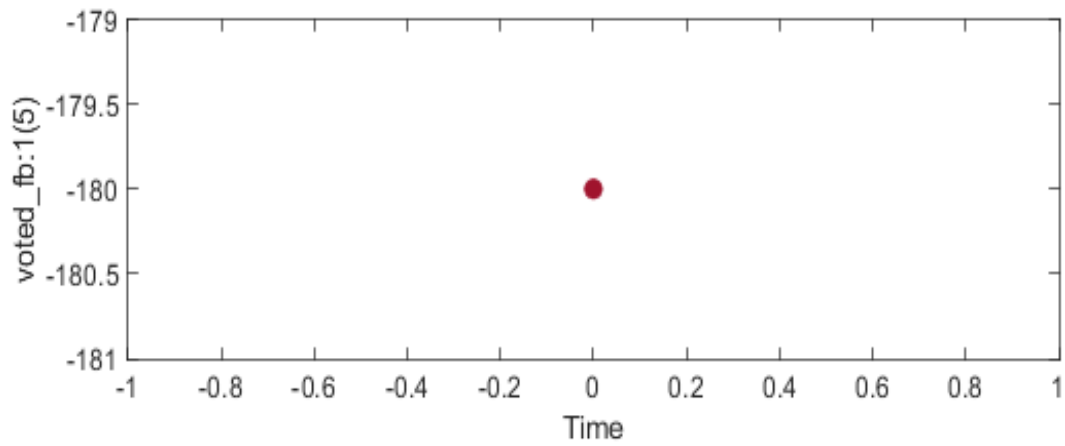
[Back to Report Summary](#)[Back to Signal Summary](#)

| Name | Data Type | Units | Sample Time | Interp | Sync |
|---------------|-----------|-------|-------------|--------|-------|
| voted_fb:1(3) | double | | 0.01 | zoh | union |
| voted_fb:1(4) | double | | 0.01 | zoh | union |



[Back to Report Summary](#)[Back to Signal Summary](#)

| Name | Data Type | Units | Sample Time | Interp | Sync |
|---------------|-----------|-------|-------------|--------|-------|
| voted_fb:1(5) | double | | 0.01 | zoh | union |



[Back to Report Summary](#)[Back to Signal Summary](#)

Simulation Logs:
Inputs are not mapped. Test results might not be accurate.

[Back to Report Summary](#)
