

# N-Channel Logic Level Enhancement Mode Field Effect Transistor

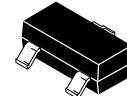
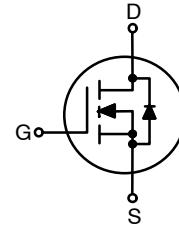
## BSS138

### General Description

These N-Channel enhancement mode field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance. These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

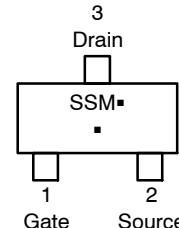
### Features

- 0.22 A, 50 V
  - ◆  $R_{DS(on)} = 3.5 \Omega$  @  $V_{GS} = 10 \text{ V}$
  - ◆  $R_{DS(on)} = 6.0 \Omega$  @  $V_{GS} = 4.5 \text{ V}$
- High Density Cell Design for Extremely Low  $R_{DS(on)}$
- Rugged and Reliable
- Compact Industry Standard SOT-23 Surface Mount Package
- HBM Class 0A, MM Class M2 (Note 3)
- This Device is Pb-Free and Halogen Free



SOT-23-3  
CASE 318-08

### MARKING DIAGRAM



SS = Specific Device Code  
M = Date Code\*  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation and/or position may vary depending upon manufacturing location.

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
BSS138, BSS138-G	SOT-23-3 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ABSOLUTE MAXIMUM RATINGS**  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain–Source Voltage	50	V
$V_{GSS}$	Gate–Source Voltage	$\pm 20$	
$I_D$	Drain Current – Continuous (Note 1)	0.22	A
	Drain Current – Pulsed (Note 1)	0.88	
$P_D$	Maximum Power Dissipation (Note 1)	0.36	W
	Derate Above $25^\circ\text{C}$	2.8	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	−55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purposes, 1/16" from Case for 10 s	300	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	350	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS**  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	50	—	—	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	—	72	—	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	0.5	$\mu\text{A}$
		$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 125^\circ\text{C}$	—	—	5	
		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	—	—	100	nA
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	—	—	$\pm 100$	

**ON CHARACTERISTICS**

$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 1 \text{ mA}$	0.8	1.3	1.5	V
$\frac{\Delta V_{GS(\text{th})}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 1 \text{ mA}$ , Referenced to $25^\circ\text{C}$	—	−2	—	$\text{mV}/^\circ\text{C}$
$R_{DS(\text{on})}$	Static Drain–Source On–Resistance	$V_{GS} = 10 \text{ V}, I_D = 0.22 \text{ A}$	—	0.7	3.5	$\Omega$
		$V_{GS} = 4.5 \text{ V}, I_D = 0.22 \text{ A}$	—	1.0	6.0	$\Omega$
		$V_{GS} = 10 \text{ V}, I_D = 0.22 \text{ A}, T_J = 125^\circ\text{C}$	—	1.1	5.8	
$I_{D(\text{on})}$	On–State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 5 \text{ V}$	0.2	—	—	A
$g_{FS}$	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 0.22 \text{ A}$	0.12	0.5	—	S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	—	27	—	pF
$C_{oss}$	Output Capacitance		—	13	—	pF
$C_{rss}$	Reverse Transfer Capacitance		—	6	—	pF
$R_G$	Gate Resistance	$V_{GS} = 15 \text{ mV}, f = 1.0 \text{ MHz}$	—	9	—	$\Omega$



ELECTRICAL CHARACTERISTICS  $T_A = 25^\circ\text{C}$  unless otherwise noted. (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, I_D = 0.29 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	-	2.5	5	ns
$t_r$	Turn-On Rise Time		-	9	18	ns
$t_{d(off)}$	Turn-Off Delay Time		-	20	36	ns
$t_f$	Turn-Off Fall Time		-	7	14	ns
$Q_g$	Total Gate Charge	$V_{DS} = 25 \text{ V}, I_D = 0.22 \text{ A}, V_{GS} = 10 \text{ V}$	-	1.7	2.4	nC
$Q_{gs}$	Gate-Source Charge		-	0.1	-	nC
$Q_{gd}$	Gate-Drain Charge		-	0.4	-	nC

## DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	-	-	0.22	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 0.44 \text{ A}$ (Note 2)	-	0.8	1.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.

a)  $350^\circ\text{C}/\text{W}$  when mounted on a minimum pad.



2. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$

3. ESD between the gate and source serves only, no gate overvoltage rating is implied.

## TYPICAL CHARACTERISTICS

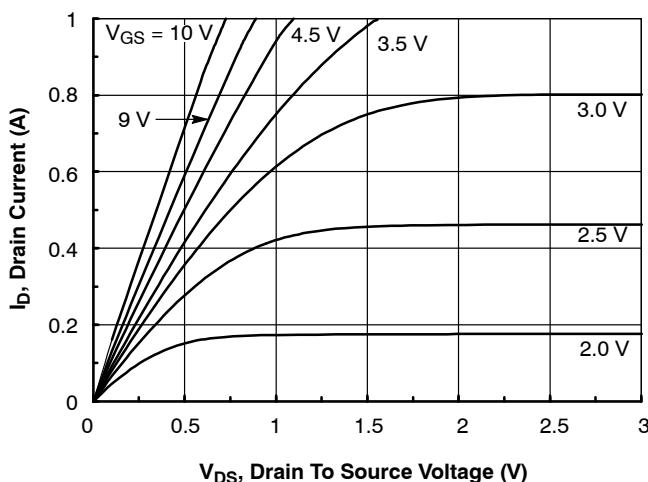


Figure 1. On-Region Characteristics

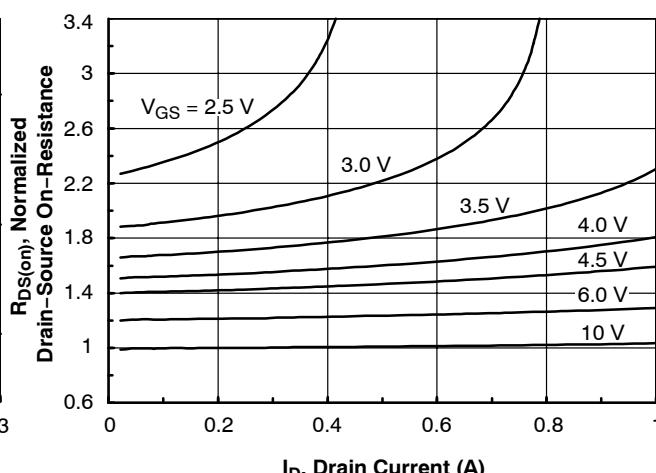


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

## TYPICAL CHARACTERISTICS (continued)

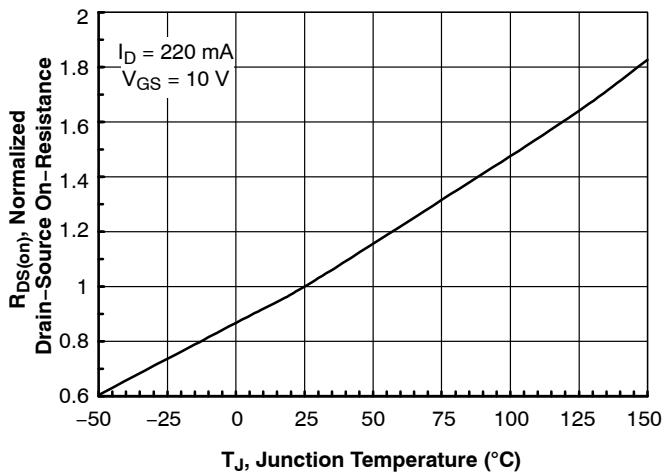


Figure 3. On-Resistance Variation with Temperature

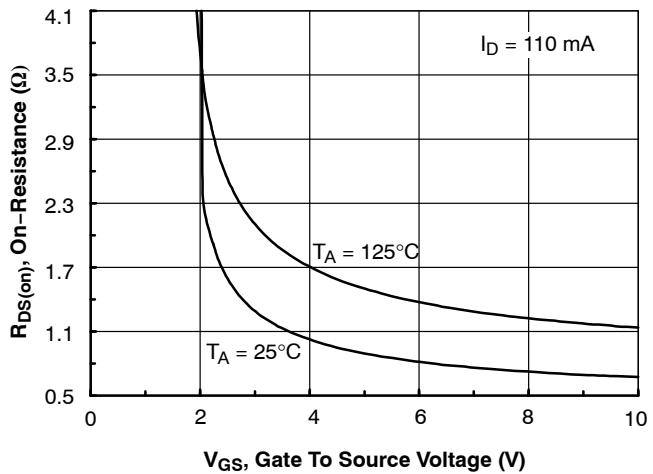


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

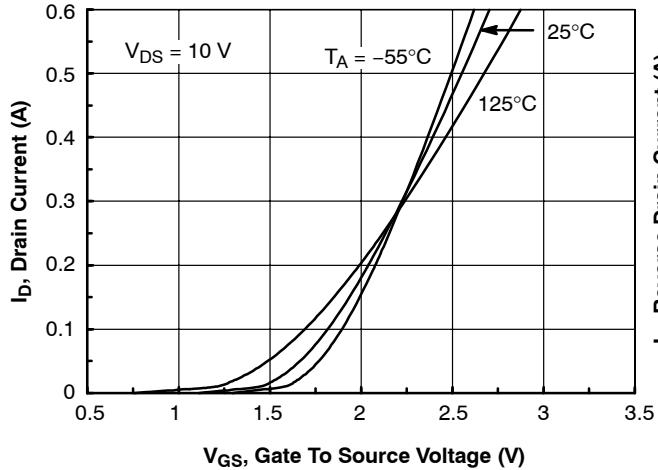


Figure 5. Transfer Characteristics

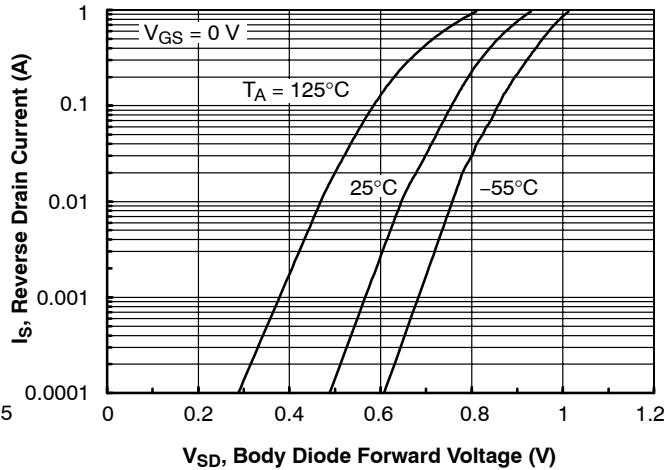


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

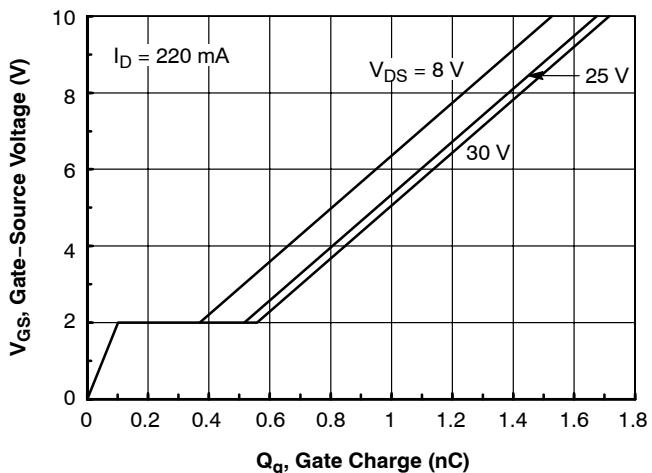


Figure 7. Gate Charge Characteristics

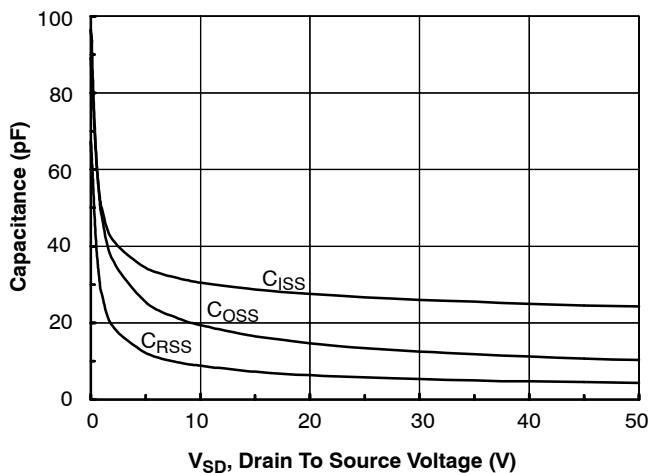


Figure 8. Capacitance Characteristics

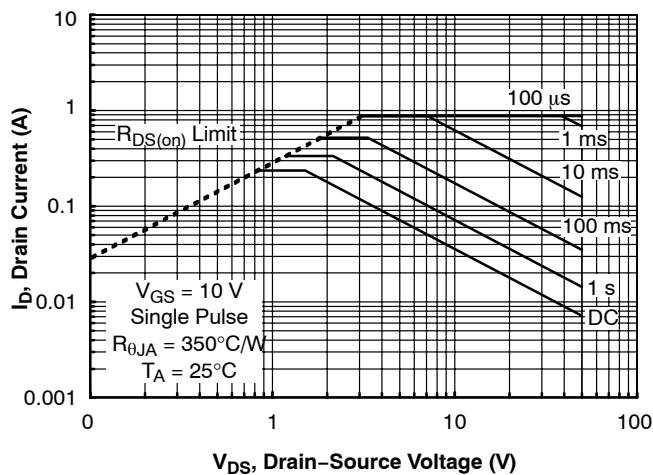


Figure 9. Maximum Safe Operating Area

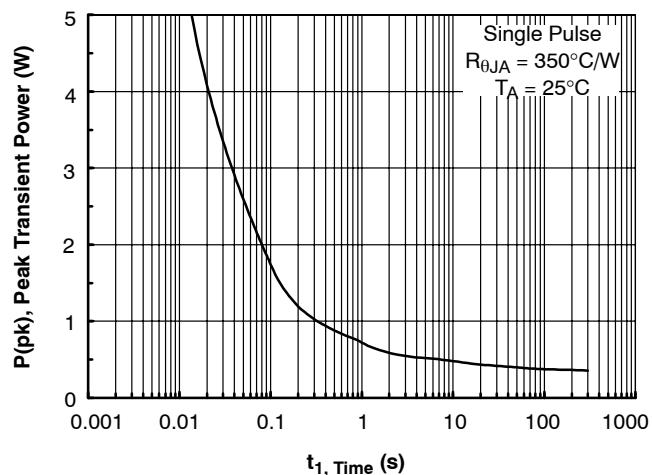


Figure 10. Single Pulse Maximum Power Dissipation

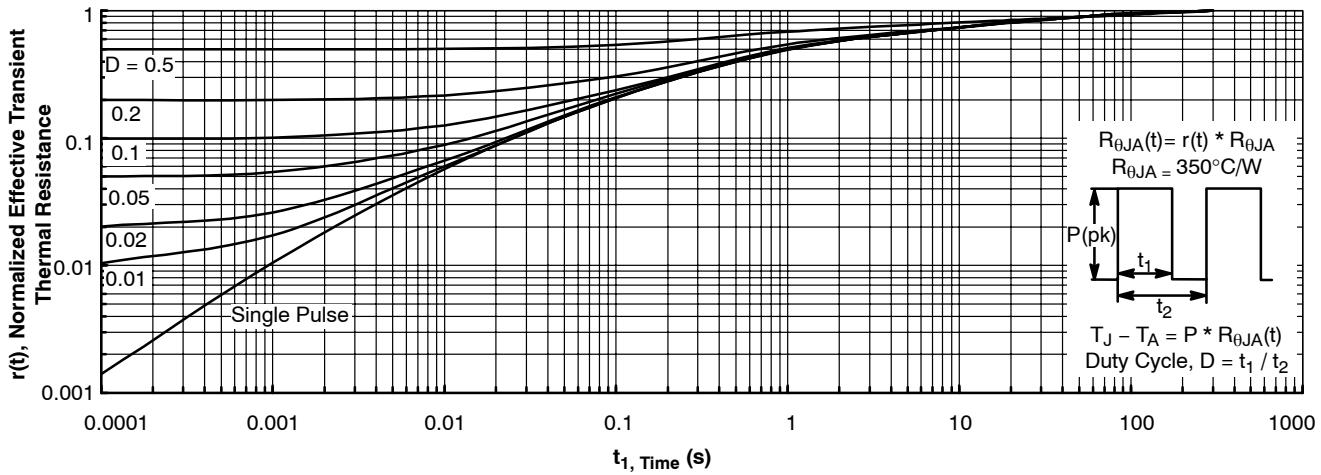
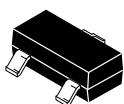


Figure 11. Transient Thermal Response Curve

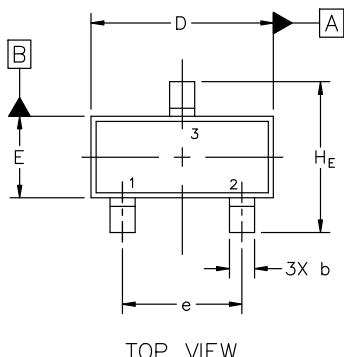
Thermal characterization performed using the conditions described in Note 1a.  
Transient thermal response will change depending on the circuit board design.



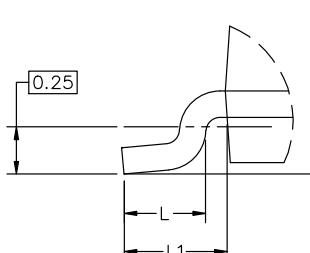
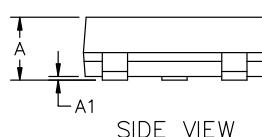
SCALE 4:1

SOT-23 (TO-236) 2.90x1.30x1.00 1.90P  
CASE 318  
ISSUE AU

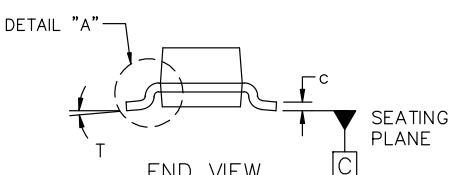
DATE 14 AUG 2024



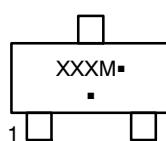
TOP VIEW

DETAIL "A"  
Scale 3:1

SIDE VIEW



END VIEW

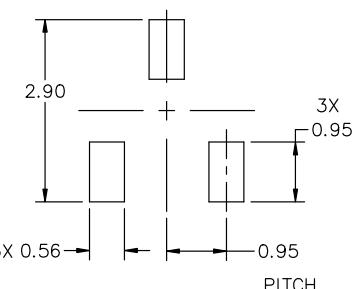
GENERIC  
MARKING DIAGRAM\*

XXX = Specific Device Code

M = Date Code

- = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED  
MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	---	10°

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

## STYLES ON PAGE 2

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**SOT-23 (TO-236) 2.90x1.30x1.00 1.90P**

CASE 318

ISSUE AU

DATE 14 AUG 2024

**STYLE 1 THRU 5:**  
CANCELLED

**STYLE 6:**  
PIN 1. BASE  
2. Emitter  
3. Collector

**STYLE 7:**  
PIN 1. Emitter  
2. Base  
3. Collector

**STYLE 8:**  
PIN 1. Anode  
2. No Connection  
3. Cathode

**STYLE 9:**  
PIN 1. Anode  
2. Anode  
3. Cathode

**STYLE 10:**  
PIN 1. Drain  
2. Source  
3. Gate

**STYLE 11:**  
PIN 1. Anode  
2. Cathode  
3. Cathode-Anode

**STYLE 12:**  
PIN 1. Cathode  
2. Cathode  
3. Anode

**STYLE 13:**  
PIN 1. Source  
2. Drain  
3. Gate

**STYLE 14:**  
PIN 1. Cathode  
2. Gate  
3. Anode

**STYLE 15:**  
PIN 1. Gate  
2. Cathode  
3. Anode

**STYLE 16:**  
PIN 1. Anode  
2. Cathode  
3. Cathode

**STYLE 17:**  
PIN 1. No Connection  
2. Anode  
3. Cathode

**STYLE 18:**  
PIN 1. No Connection  
2. Cathode  
3. Anode

**STYLE 19:**  
PIN 1. Cathode  
2. Anode  
3. Cathode-Anode

**STYLE 20:**  
PIN 1. Cathode  
2. Anode  
3. Gate

**STYLE 21:**  
PIN 1. Gate  
2. Source  
3. Drain

**STYLE 22:**  
PIN 1. Return  
2. Output  
3. Input

**STYLE 23:**  
PIN 1. Anode  
2. Anode  
3. Cathode

**STYLE 24:**  
PIN 1. Gate  
2. Drain  
3. Source

**STYLE 25:**  
PIN 1. Anode  
2. Cathode  
3. Gate

**STYLE 26:**  
PIN 1. Cathode  
2. Anode  
3. No Connection

**STYLE 27:**  
PIN 1. Cathode  
2. Cathode  
3. Cathode

**STYLE 28:**  
PIN 1. Anode  
2. Anode  
3. Anode

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