EPICS Test Report
SN0013 lab{3}
2025-10-29T10:37:48.082382

Device configuration
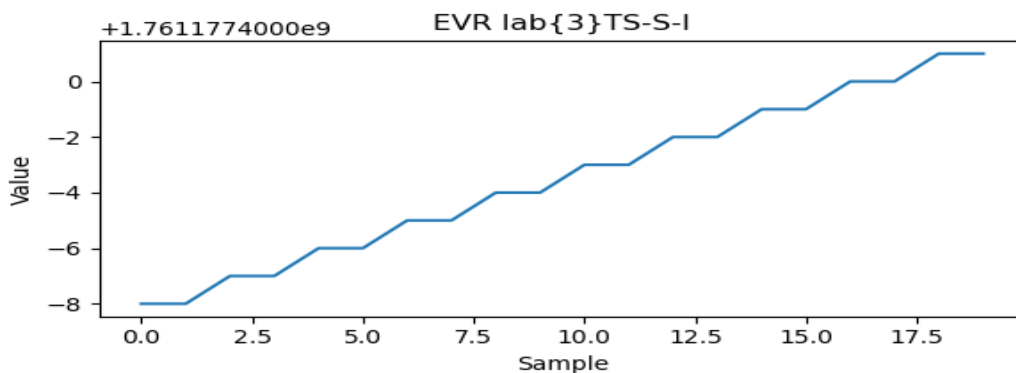
PV	Value
lab{3}NumChannels-Mode	4 Channel
lab{3}Resolution-Mode	MS (18bit)
lab{3}Bandwidth-Mode	Slow
lab{3}Polarity-Mode	Bipolar

Section 1: DAC loopback test

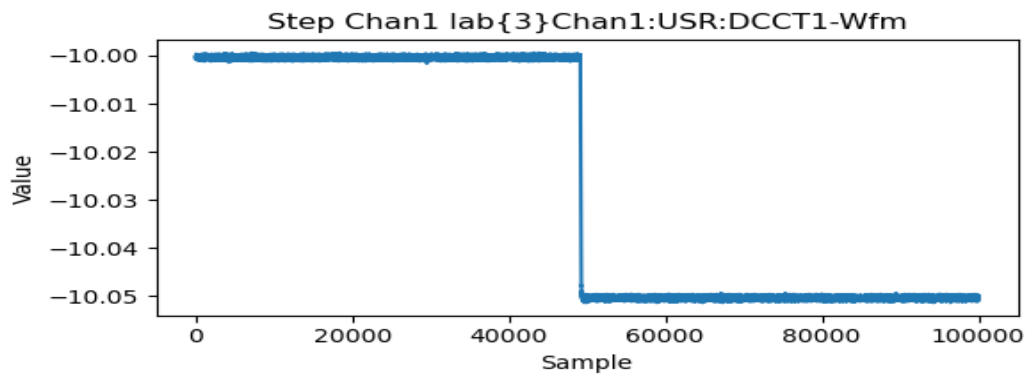| Channel	Readback	Pass/Fail
Chan1	1.00067138671875	PASS
Chan2	0.999755859375	PASS
Chan3	1.0015869140625	PASS
Chan4	0.999755859375	PASS

Section 2: EVR monotonicity test
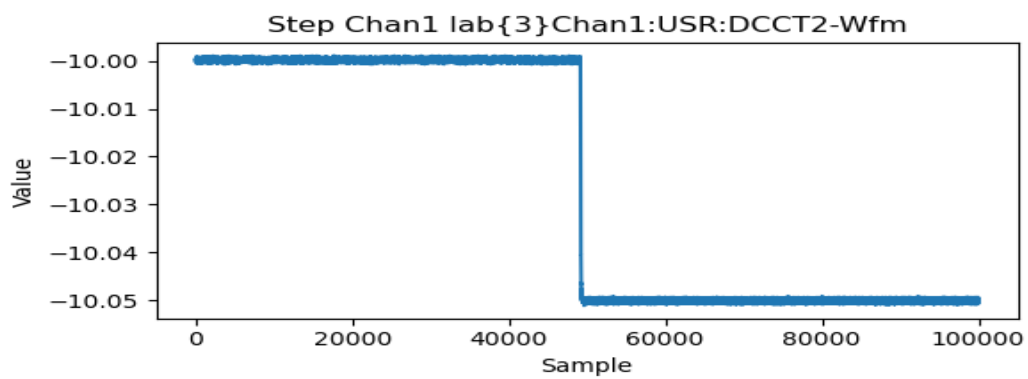
EVR PV: lab{3}TS-S-I monotonic test -> **PASS**

Section 3: Test Data

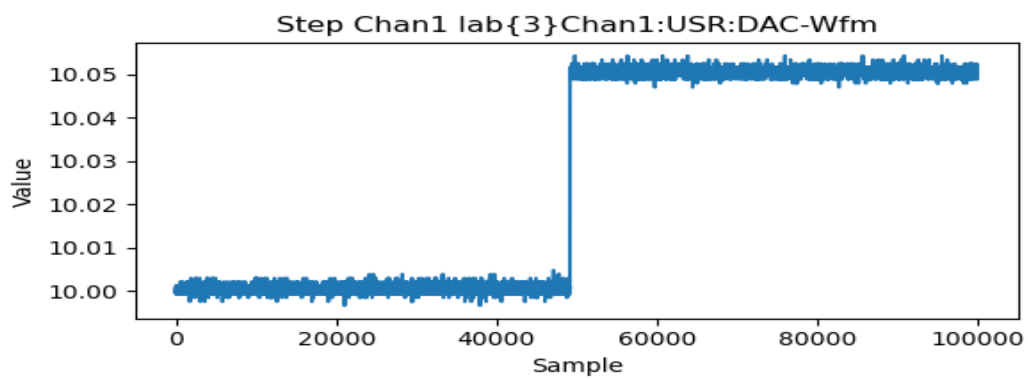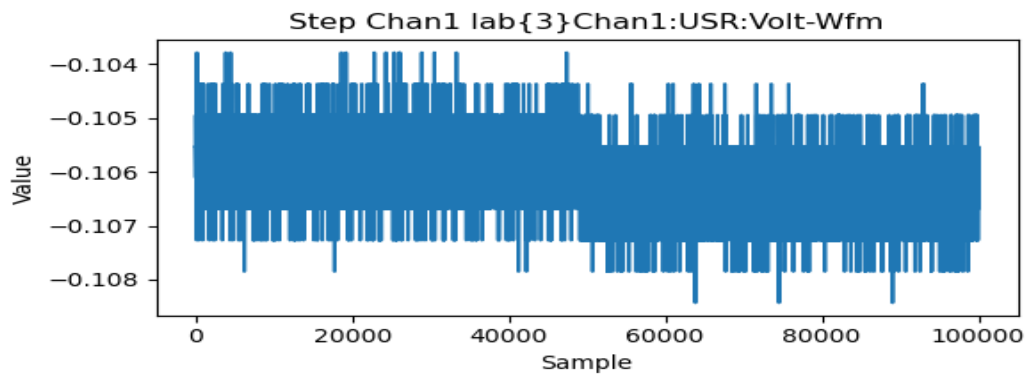Step Chan1 PV: lab{3}Chan1:USR:DCCT1-Wfm

Step Chan1 lab{3}Chan1:USR:DCCT1-Wfm

Step Chan1 PV: lab{3}Chan1:USR:DCCT2-Wfm

Step Chan1 lab{3}Chan1:USR:DCCT2-Wfm

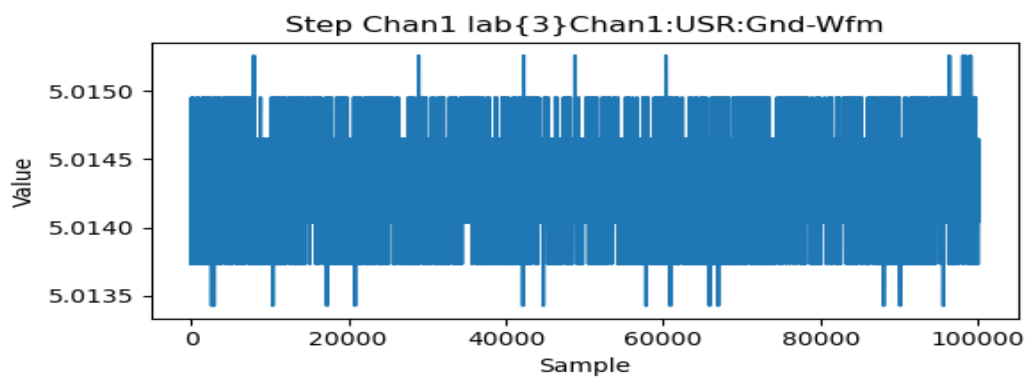Step Chan1 PV: lab{3}Chan1:USR:DAC-Wfm

Step Chan1 lab{3}Chan1:USR:DAC-Wfm

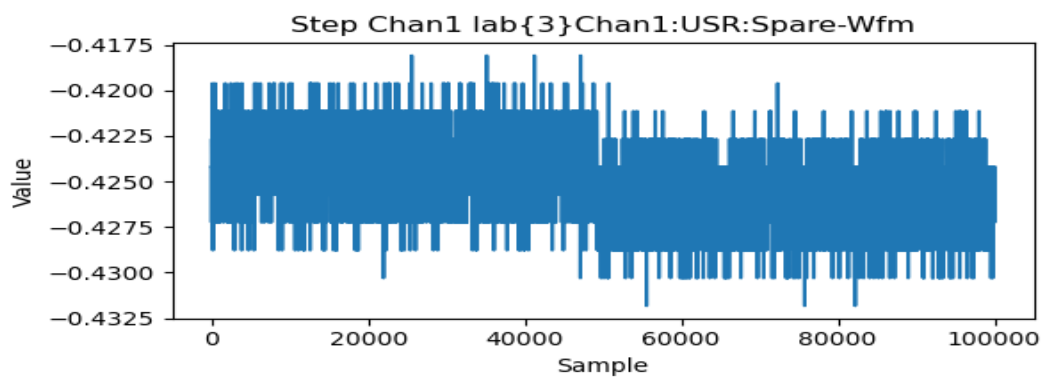Step Chan1 PV: lab{3}Chan1:USR:Volt-Wfm

Step Chan1 lab{3}Chan1:USR:Volt-Wfm

Step Chan1 PV: lab{3}Chan1:USR:Gnd-Wfm

Step Chan1 lab{3}Chan1:USR:Gnd-Wfm

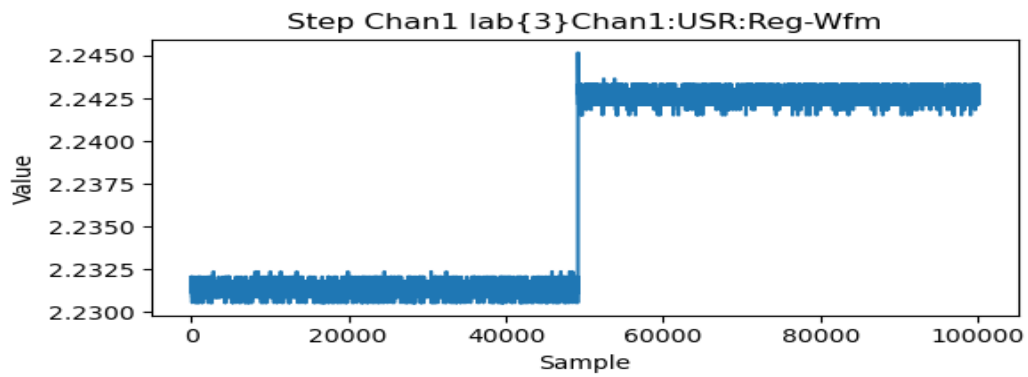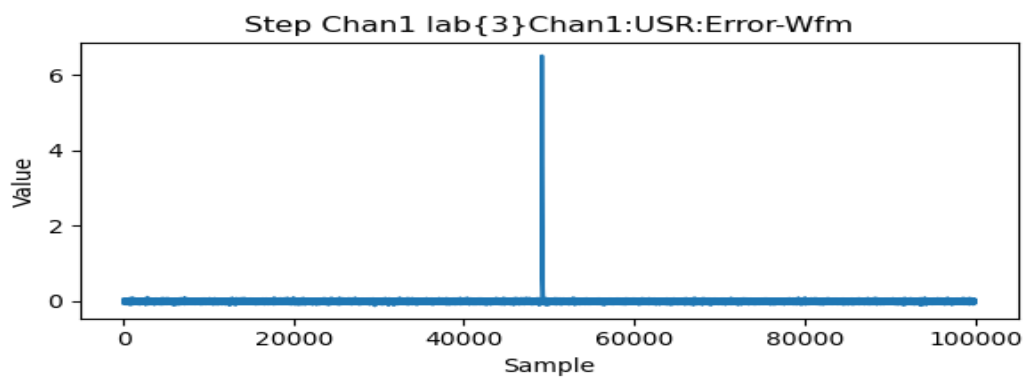Step Chan1 PV: lab{3}Chan1:USR:Spare-Wfm
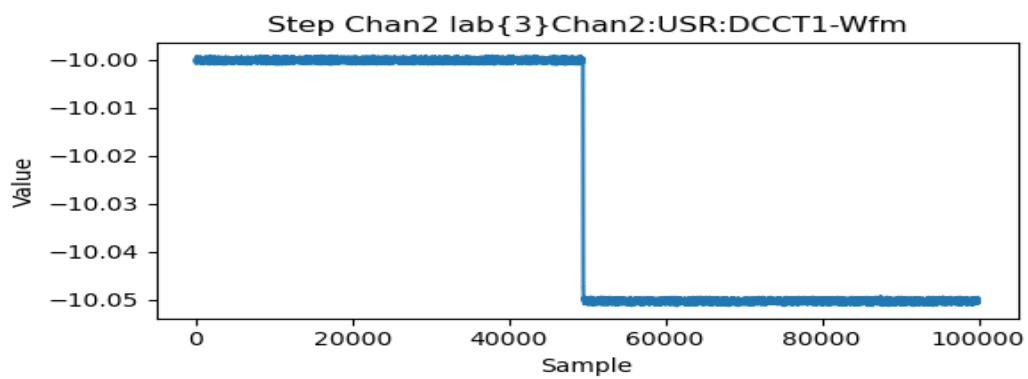

Step Chan1 lab{3}Chan1:USR:Spare-Wfm

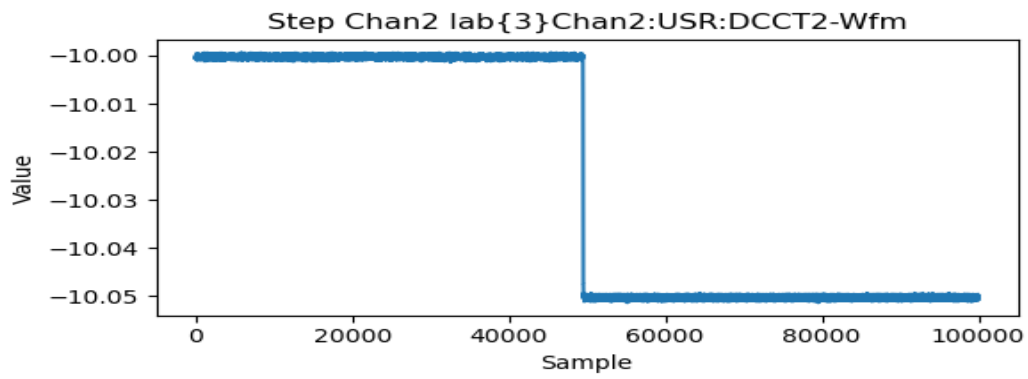Step Chan1 PV: lab{3}Chan1:USR:Reg-Wfm

Step Chan1 PV: lab{3}Chan1:USR:Error-Wfm

Step Chan2 PV: lab{3}Chan2:USR:DCCT1-Wfm
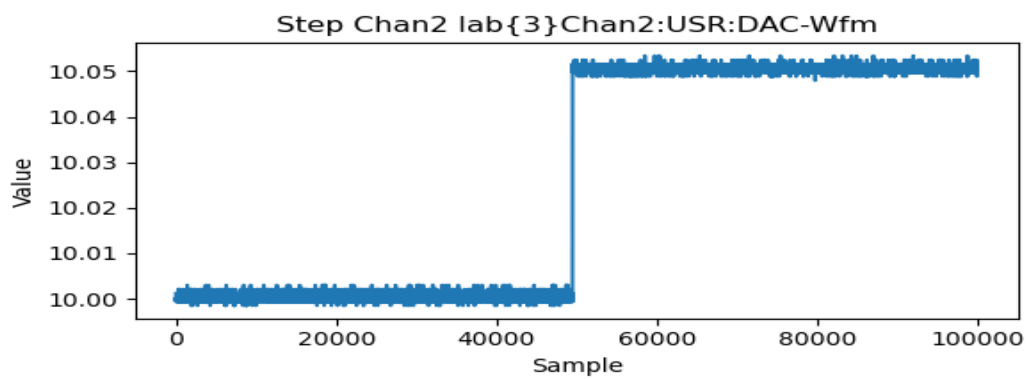

Step Chan2 PV: lab{3}Chan2:USR:DCCT2-Wfm

Step Chan2 lab{3}Chan2:USR:DCCT2-Wfm
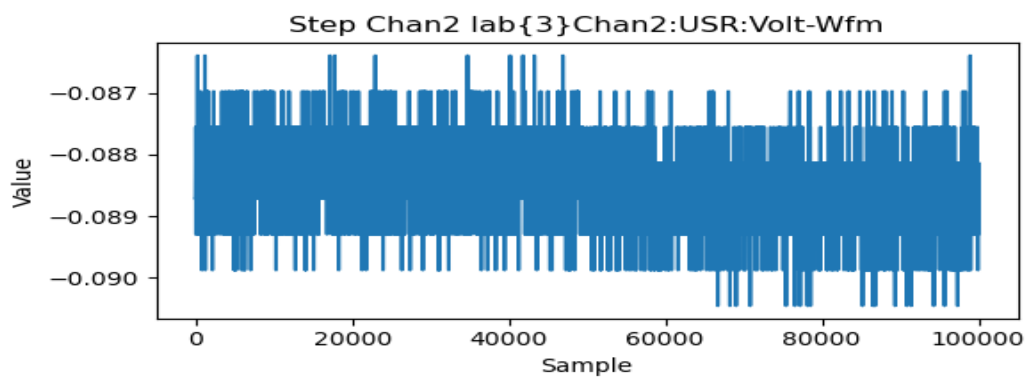
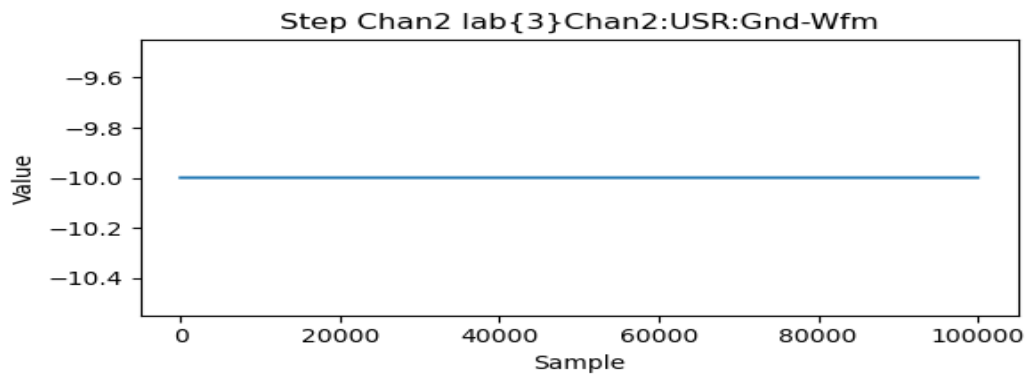Step Chan2 PV: lab{3}Chan2:USR:DAC-Wfm

Step Chan2 lab{3}Chan2:USR:DAC-Wfm

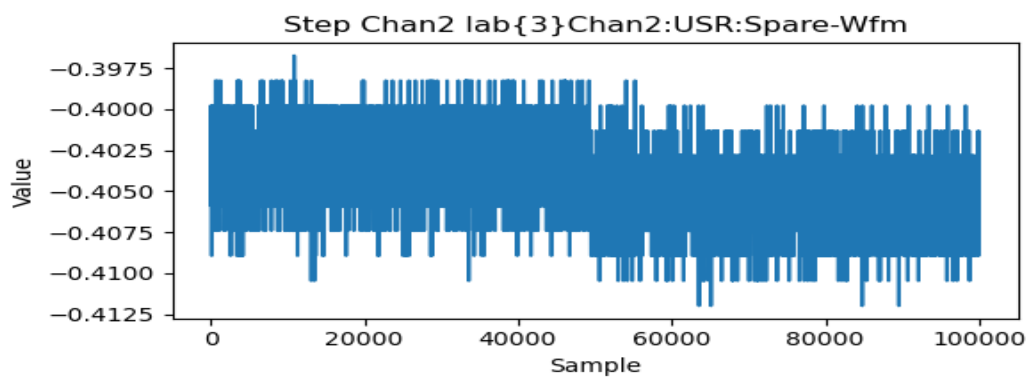Step Chan2 PV: lab{3}Chan2:USR:Volt-Wfm

Step Chan2 lab{3}Chan2:USR:Volt-Wfm

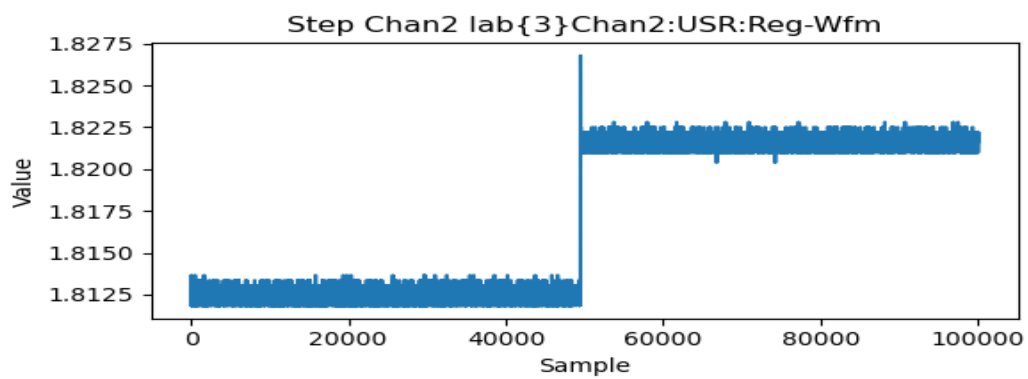Step Chan2 PV: lab{3}Chan2:USR:Gnd-Wfm

Step Chan2 lab{3}Chan2:USR:Gnd-Wfm

Step Chan2 PV: lab{3}Chan2:USR:Spare-Wfm
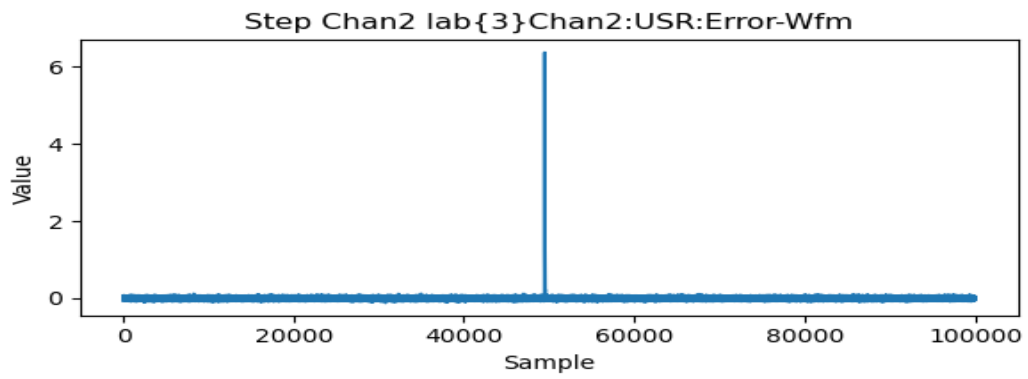

Step Chan2 lab{3}Chan2:USR:Spare-Wfm

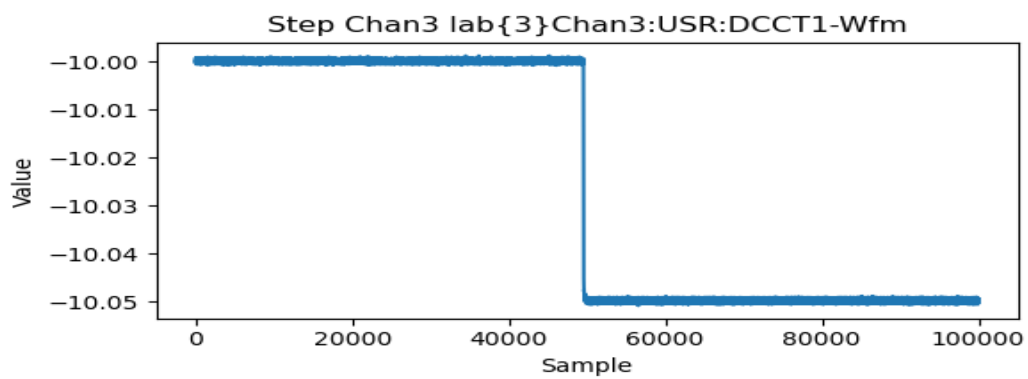Step Chan2 PV: lab{3}Chan2:USR:Reg-Wfm

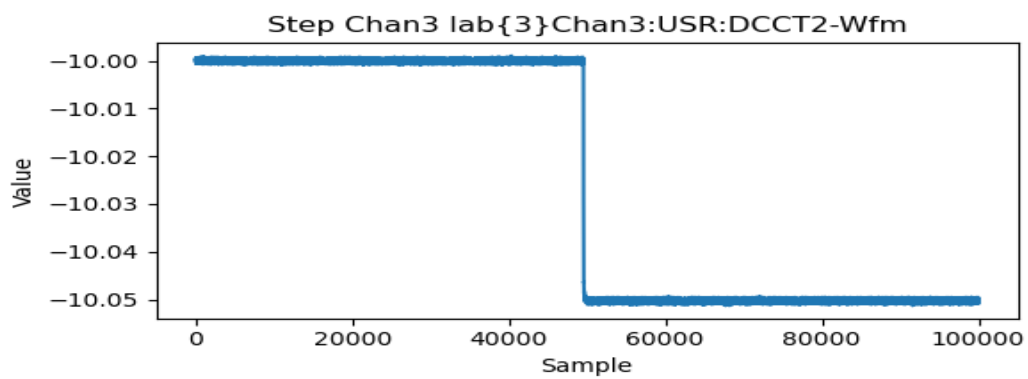Step Chan2 lab{3}Chan2:USR:Reg-Wfm

Step Chan2 PV: lab{3}Chan2:USR:Error-Wfm

Step Chan2 lab{3}Chan2:USR:Error-Wfm

Step Chan3 PV: lab{3}Chan3:USR:DCCT1-Wfm
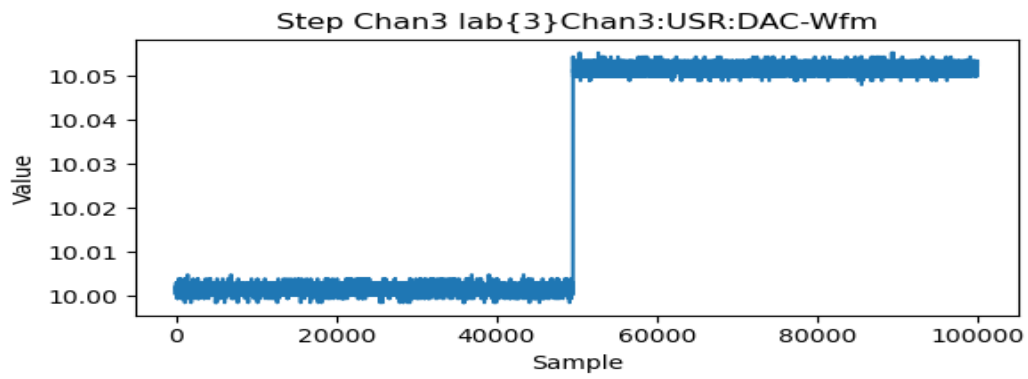

Step Chan3 lab{3}Chan3:USR:DCCT1-Wfm

Step Chan3 PV: lab{3}Chan3:USR:DCCT2-Wfm
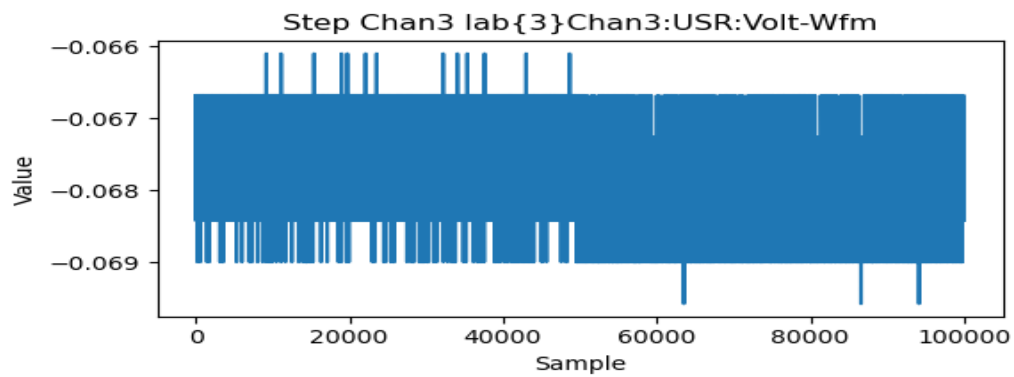

Step Chan3 lab{3}Chan3:USR:DCCT2-Wfm

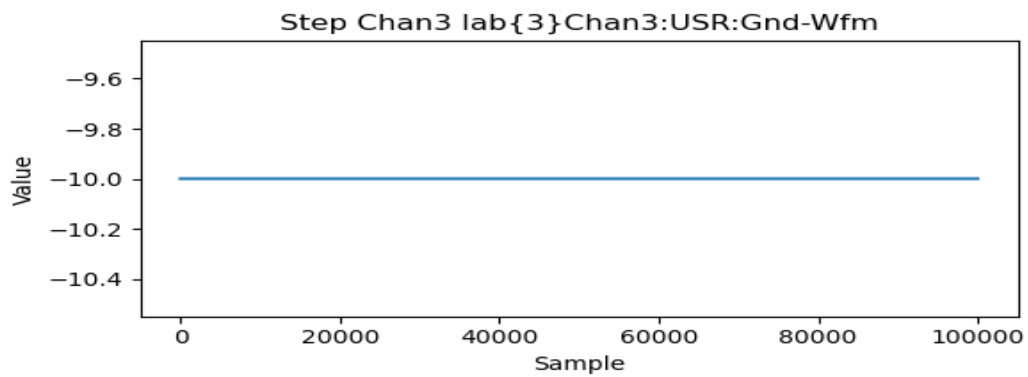Step Chan3 PV: lab{3}Chan3:USR:DAC-Wfm

Step Chan3 lab{3}Chan3:USR:DAC-Wfm

Step Chan3 PV: lab{3}Chan3:USR:Volt-Wfm
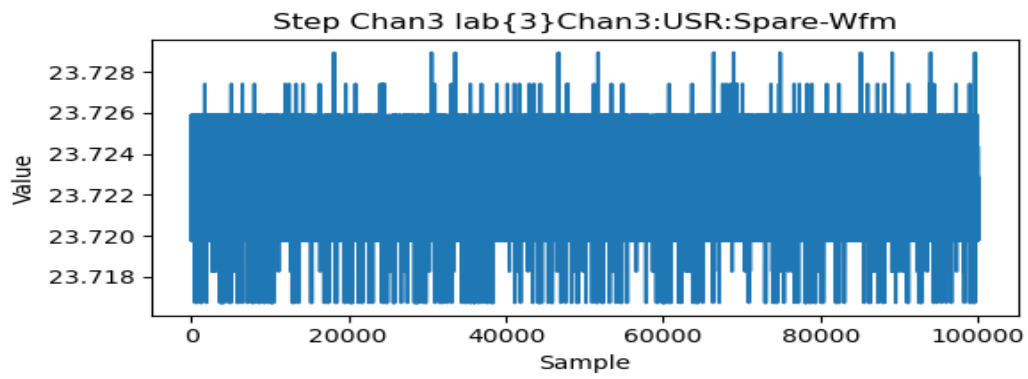

Step Chan3 lab{3}Chan3:USR:Volt-Wfm

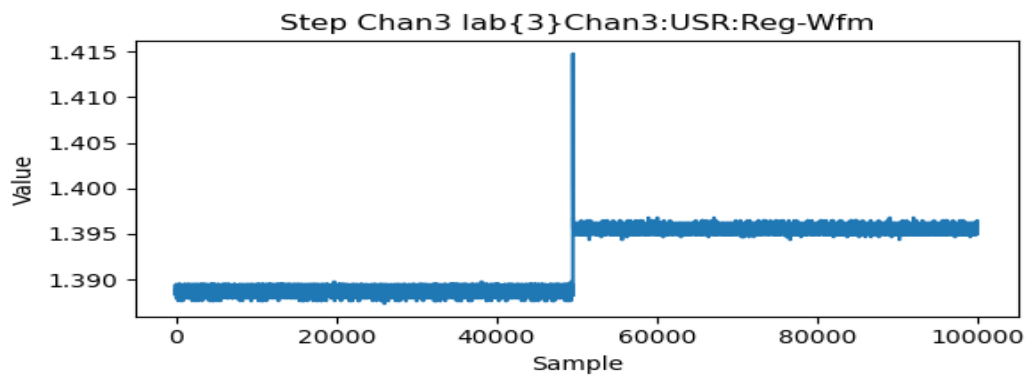Step Chan3 PV: lab{3}Chan3:USR:Gnd-Wfm

Step Chan3 lab{3}Chan3:USR:Gnd-Wfm

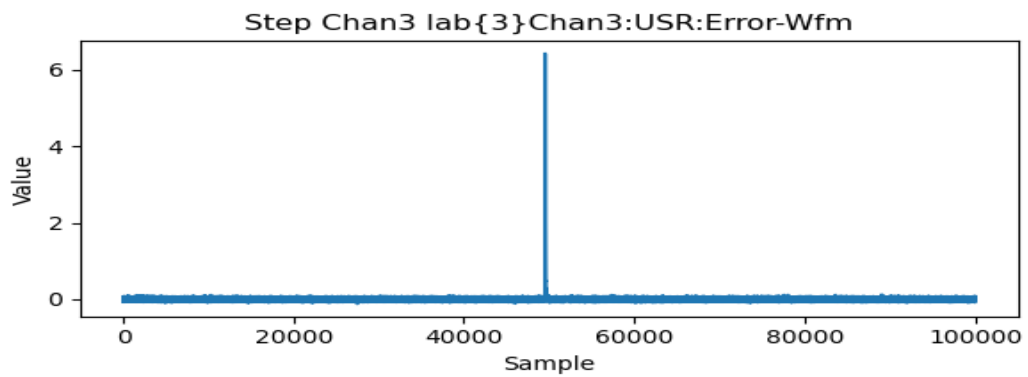Step Chan3 PV: lab{3}Chan3:USR:Spare-Wfm

Step Chan3 lab{3}Chan3:USR:Spare-Wfm

Step Chan3 PV: lab{3}Chan3:USR:Reg-Wfm

Step Chan3 lab{3}Chan3:USR:Reg-Wfm
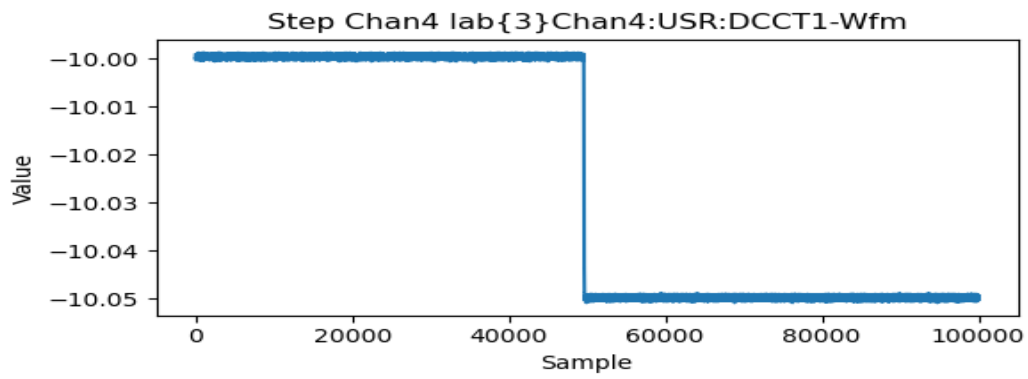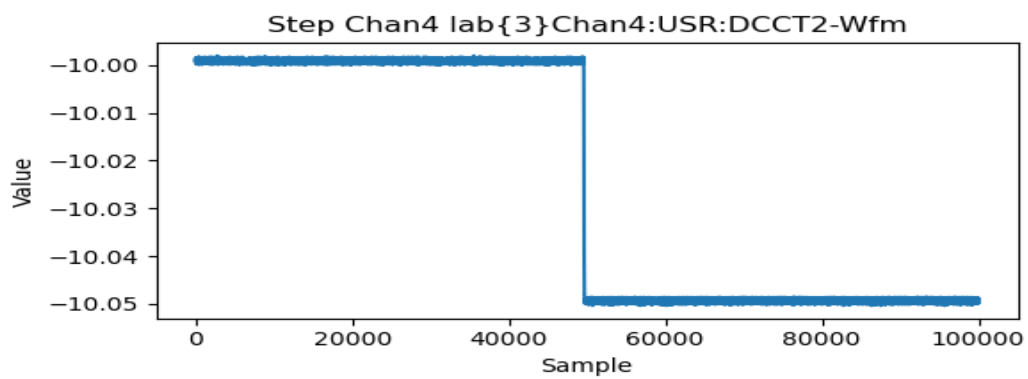
Step Chan3 PV: lab{3}Chan3:USR:Error-Wfm

Step Chan3 lab{3}Chan3:USR:Error-Wfm

Step Chan4 PV: lab{3}Chan4:USR:DCCT1-Wfm
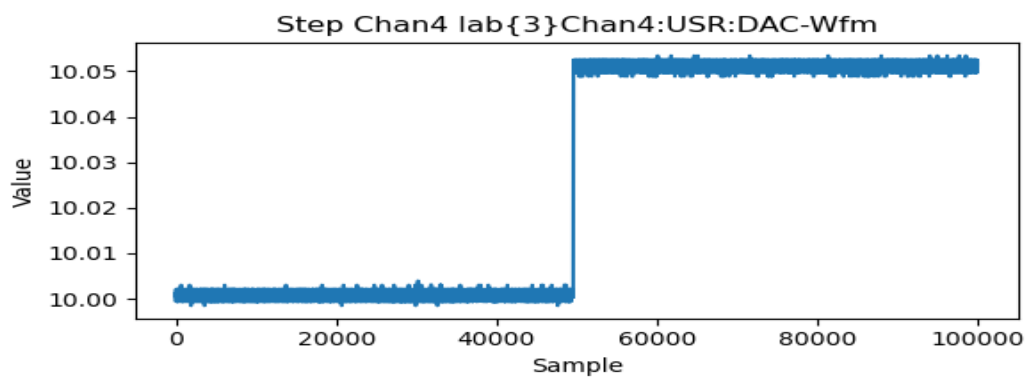
Step Chan4 lab{3}Chan4:USR:DCCT1-Wfm

Step Chan4 PV: lab{3}Chan4:USR:DCCT2-Wfm
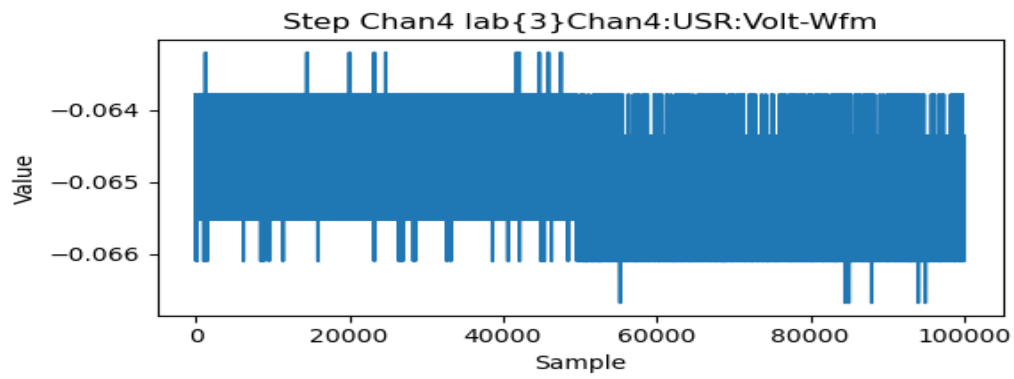

Step Chan4 lab{3}Chan4:USR:DCCT2-Wfm

Step Chan4 PV: lab{3}Chan4:USR:DAC-Wfm
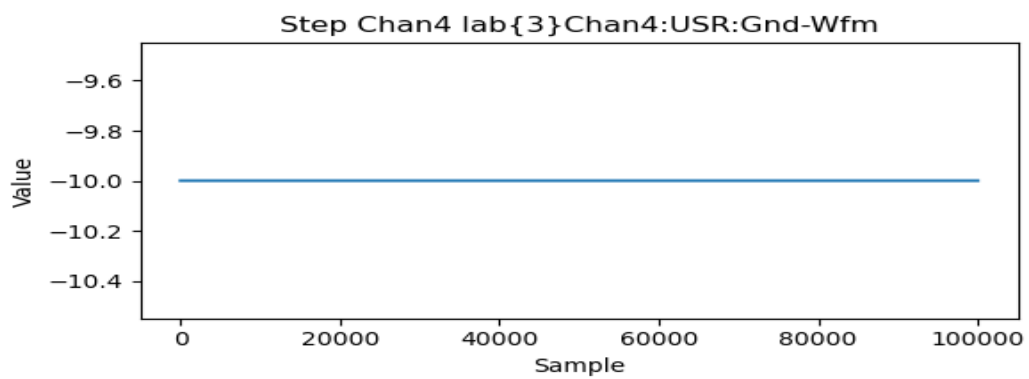

Step Chan4 lab{3}Chan4:USR:DAC-Wfm

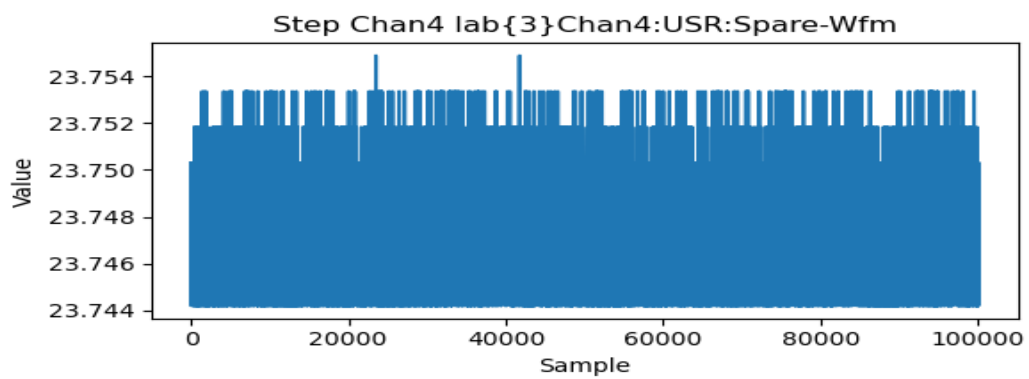Step Chan4 PV: lab{3}Chan4:USR:Volt-Wfm

Step Chan4 lab{3}Chan4:USR:Volt-Wfm

Step Chan4 PV: lab{3}Chan4:USR:Gnd-Wfm
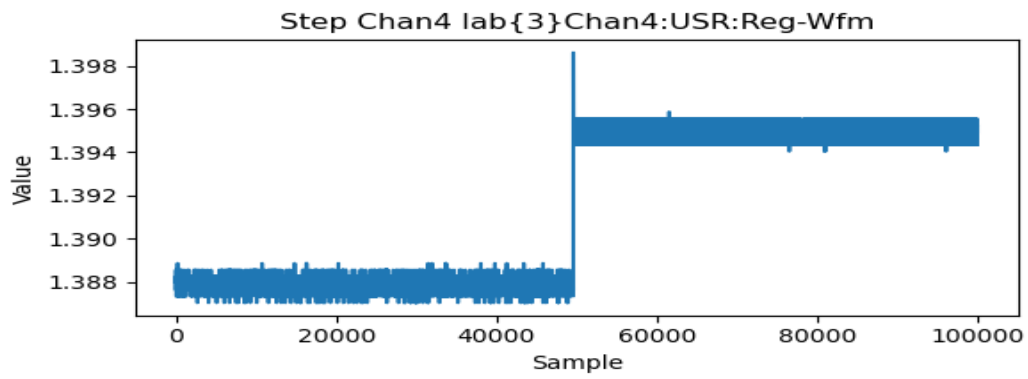

Step Chan4 lab{3}Chan4:USR:Gnd-Wfm

Step Chan4 PV: lab{3}Chan4:USR:Spare-Wfm

Step Chan4 lab{3}Chan4:USR:Spare-Wfm
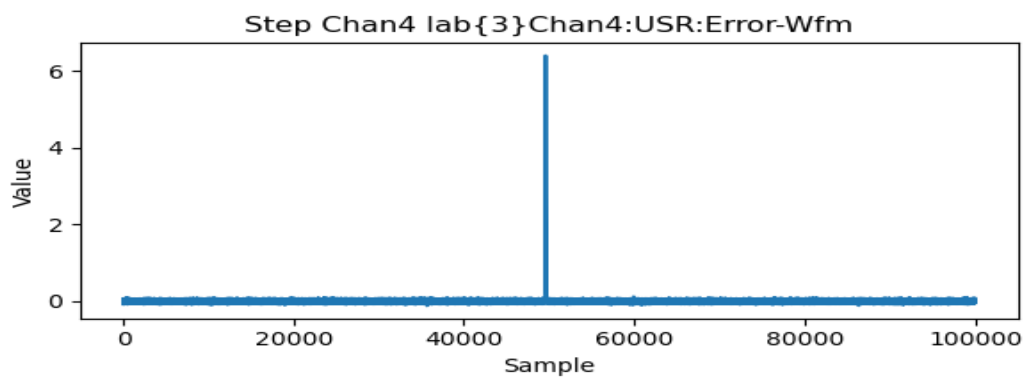
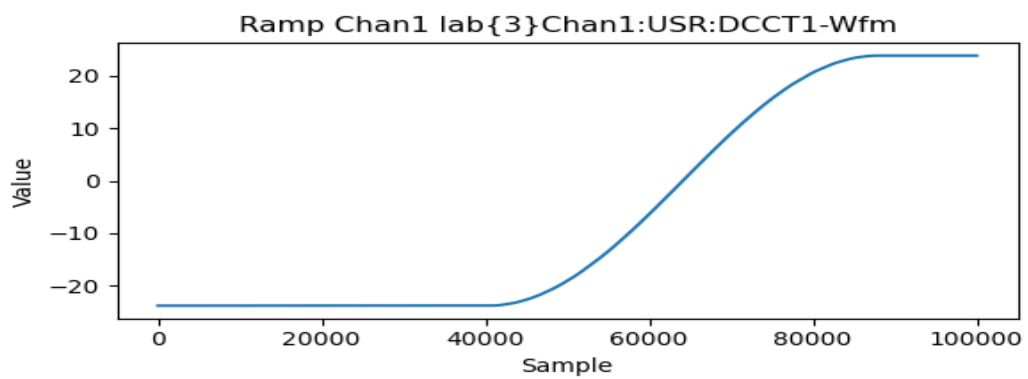Step Chan4 PV: lab{3}Chan4:USR:Reg-Wfm

Step Chan4 lab{3}Chan4:USR:Reg-Wfm

Step Chan4 PV: lab{3}Chan4:USR:Error-Wfm
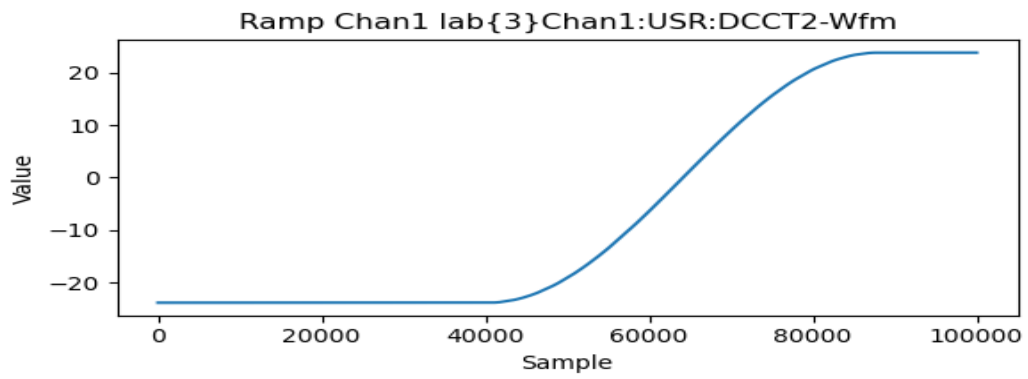

Step Chan4 lab{3}Chan4:USR:Error-Wfm

Ramp Chan1 PV: lab{3}Chan1:USR:DCCT1-Wfm
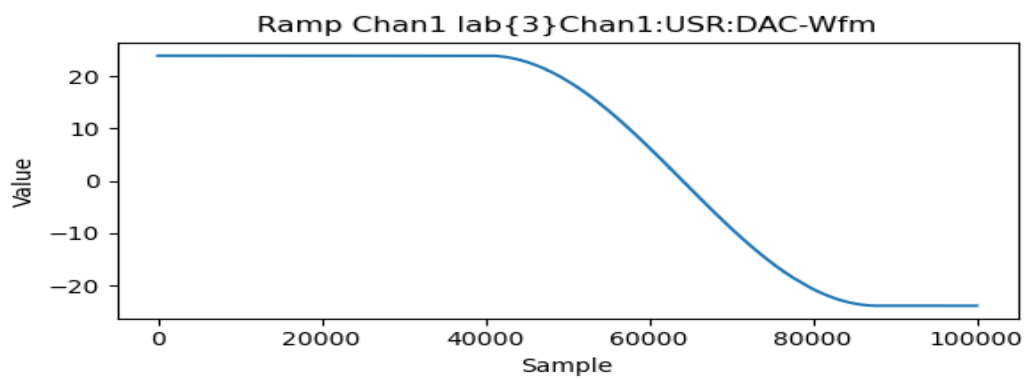

Ramp Chan1 lab{3}Chan1:USR:DCCT1-Wfm

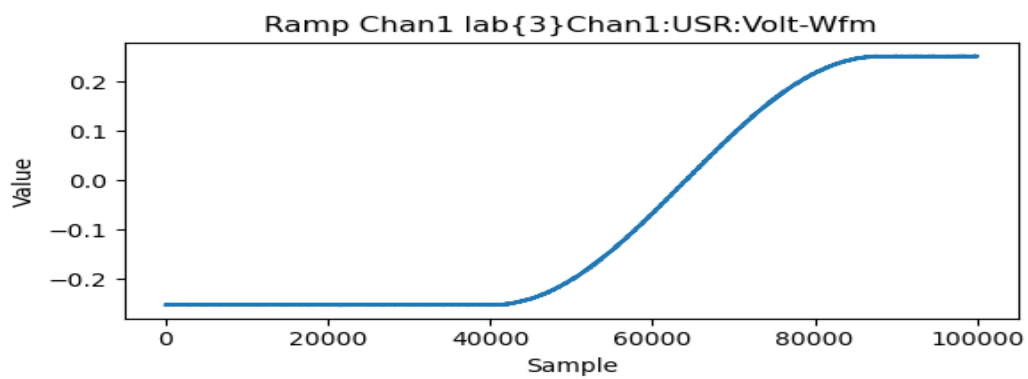Ramp Chan1 PV: lab{3}Chan1:USR:DCCT2-Wfm

Ramp Chan1 lab{3}Chan1:USR:DCCT2-Wfm

Ramp Chan1 PV: lab{3}Chan1:USR:DAC-Wfm
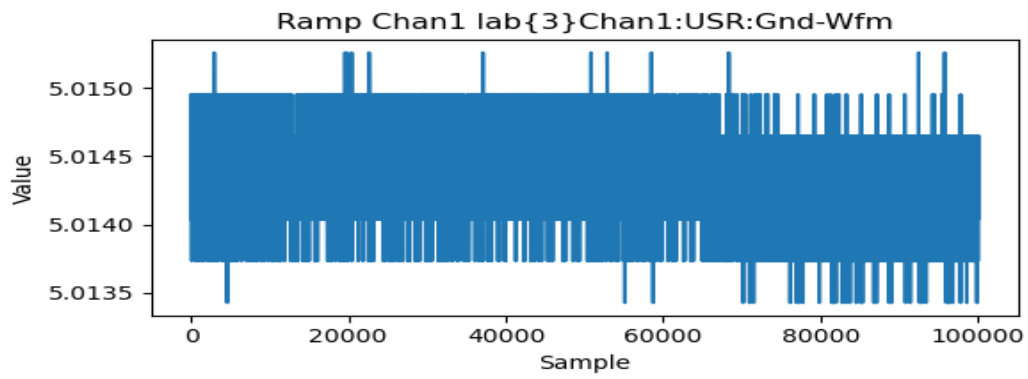

Ramp Chan1 lab{3}Chan1:USR:DAC-Wfm

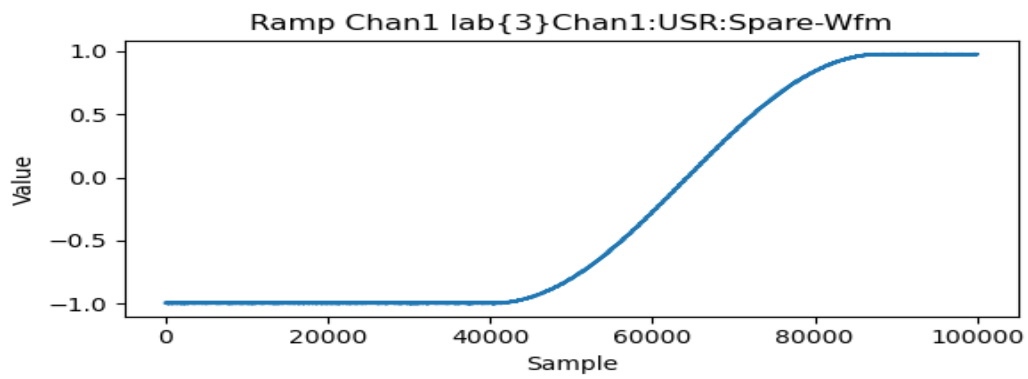Ramp Chan1 PV: lab{3}Chan1:USR:Volt-Wfm

Ramp Chan1 lab{3}Chan1:USR:Volt-Wfm

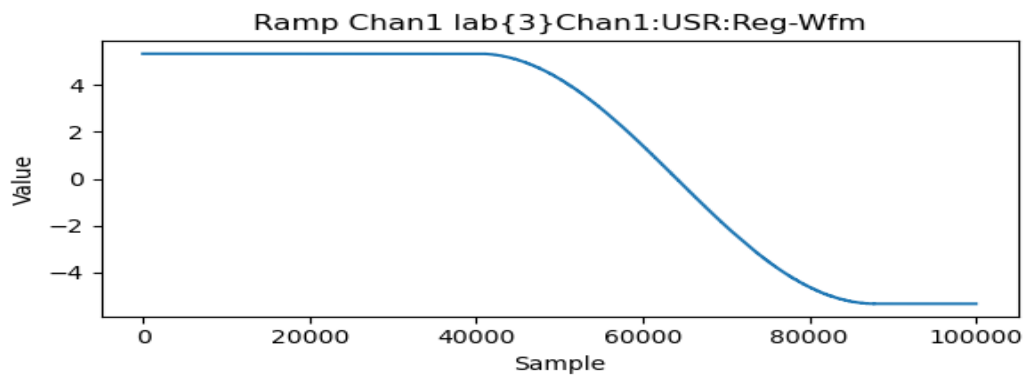Ramp Chan1 PV: lab{3}Chan1:USR:Gnd-Wfm

Ramp Chan1 lab{3}Chan1:USR:Gnd-Wfm

Ramp Chan1 PV: lab{3}Chan1:USR:Spare-Wfm
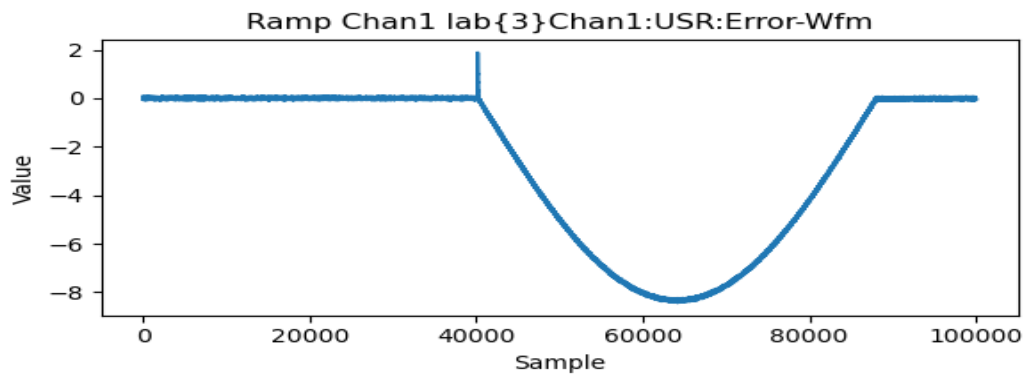

Ramp Chan1 lab{3}Chan1:USR:Spare-Wfm

Ramp Chan1 PV: lab{3}Chan1:USR:Reg-Wfm
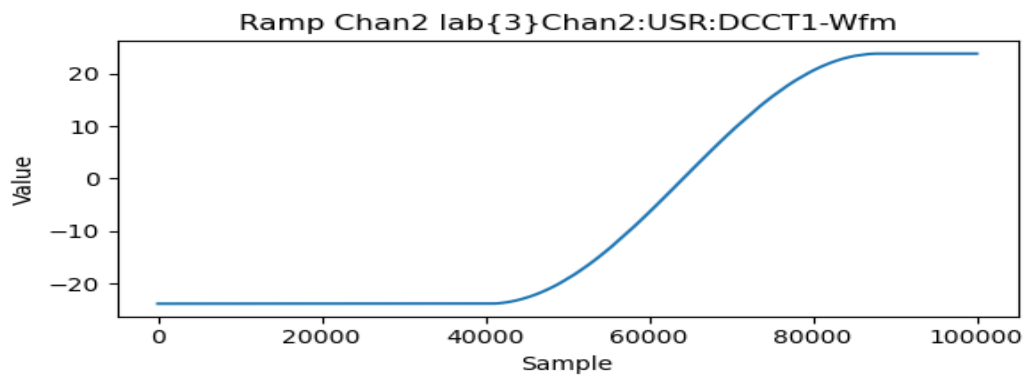

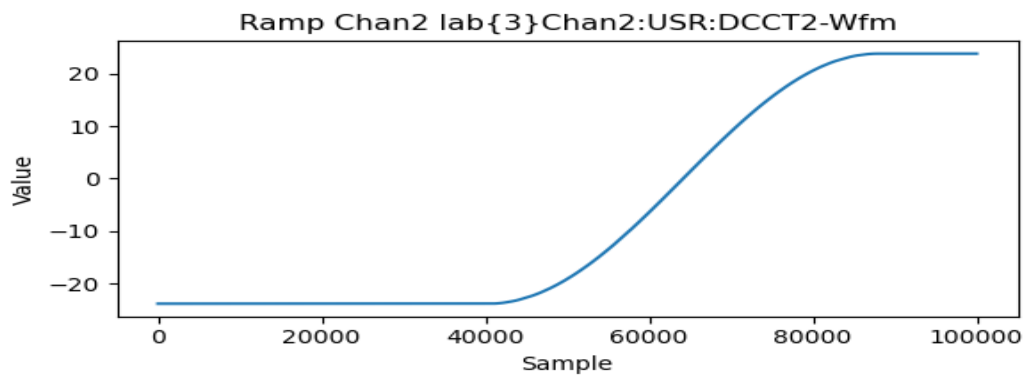Ramp Chan1 lab{3}Chan1:USR:Reg-Wfm

Ramp Chan1 PV: lab{3}Chan1:USR:Error-Wfm

Ramp Chan1 lab{3}Chan1:USR:Error-Wfm

Ramp Chan2 PV: lab{3}Chan2:USR:DCCT1-Wfm
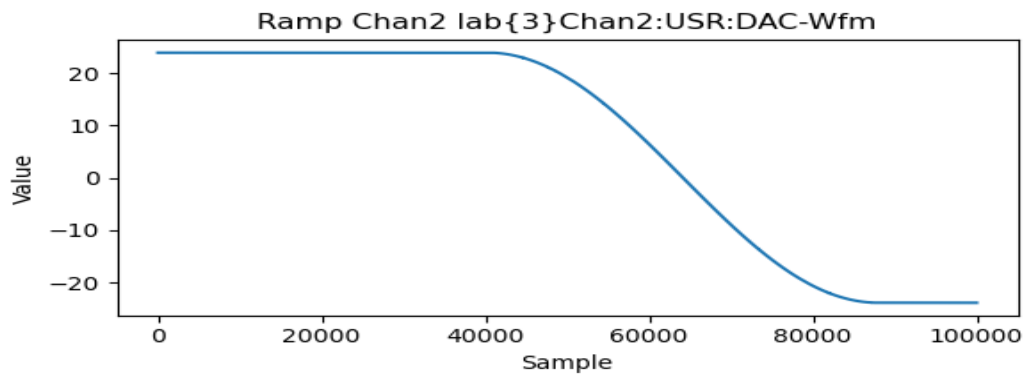

Ramp Chan2 lab{3}Chan2:USR:DCCT1-Wfm

Ramp Chan2 PV: lab{3}Chan2:USR:DCCT2-Wfm
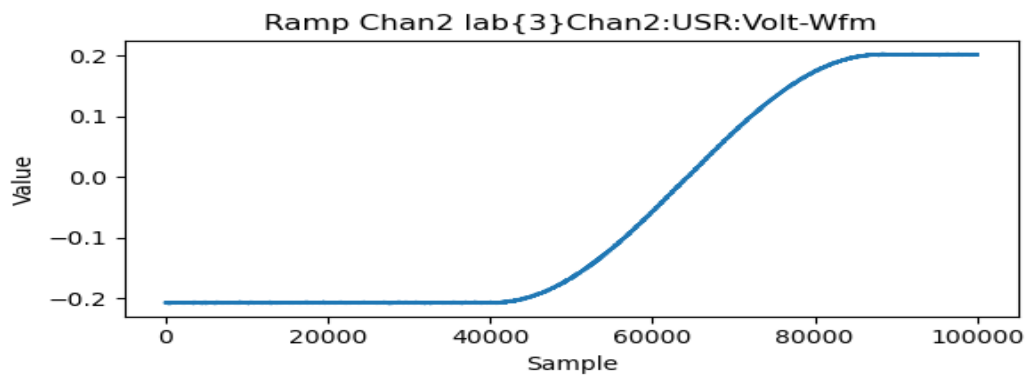

Ramp Chan2 lab{3}Chan2:USR:DCCT2-Wfm

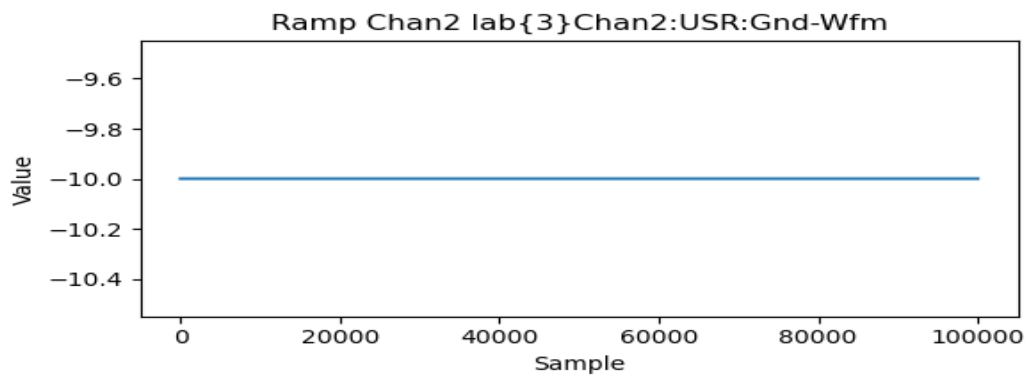Ramp Chan2 PV: lab{3}Chan2:USR:DAC-Wfm

Ramp Chan2 lab{3}Chan2:USR:DAC-Wfm

Ramp Chan2 PV: lab{3}Chan2:USR:Volt-Wfm
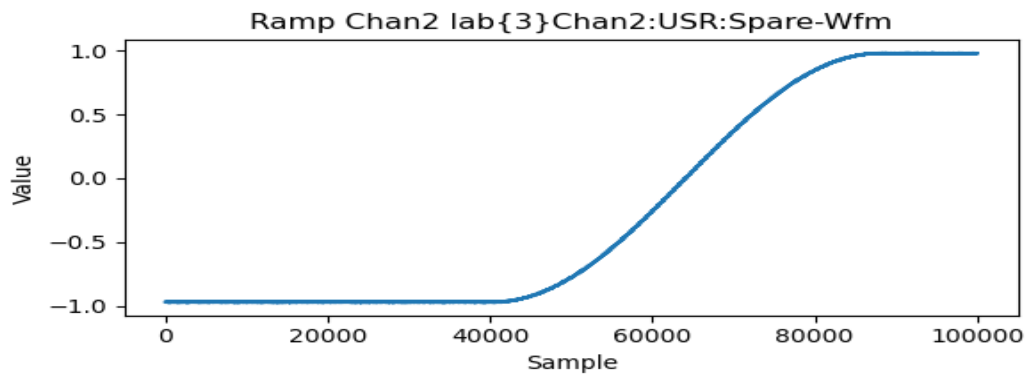

Ramp Chan2 lab{3}Chan2:USR:Volt-Wfm

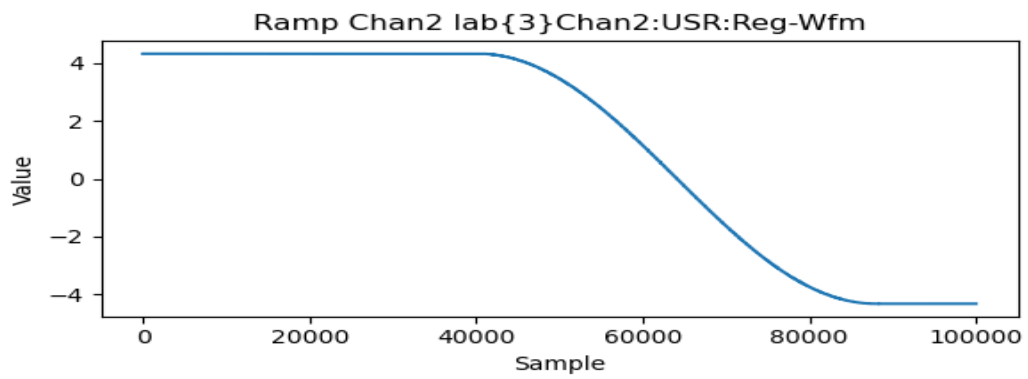Ramp Chan2 PV: lab{3}Chan2:USR:Gnd-Wfm

Ramp Chan2 lab{3}Chan2:USR:Gnd-Wfm

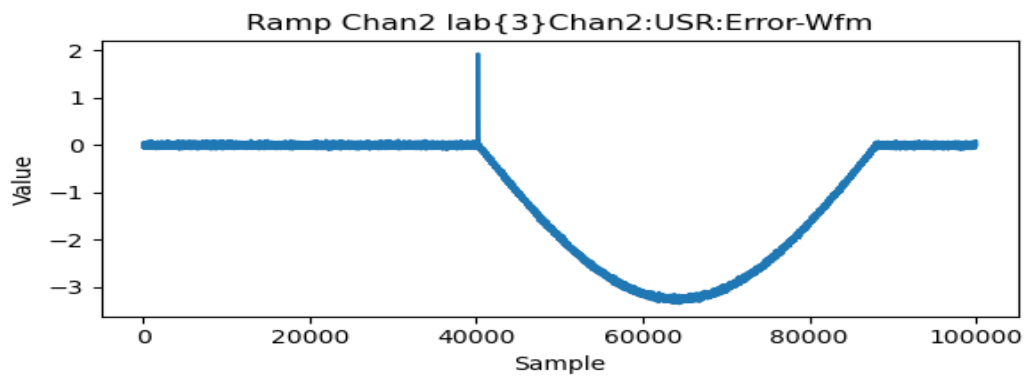Ramp Chan2 PV: lab{3}Chan2:USR:Spare-Wfm

Ramp Chan2 lab{3}Chan2:USR:Spare-Wfm

Ramp Chan2 PV: lab{3}Chan2:USR:Reg-Wfm
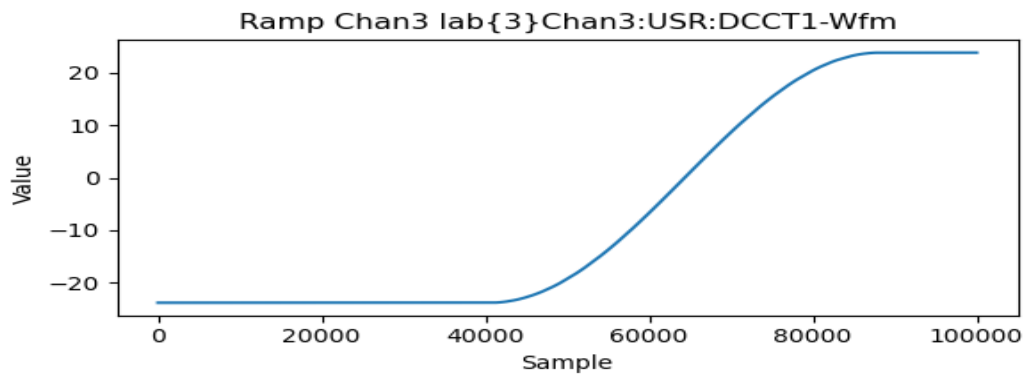

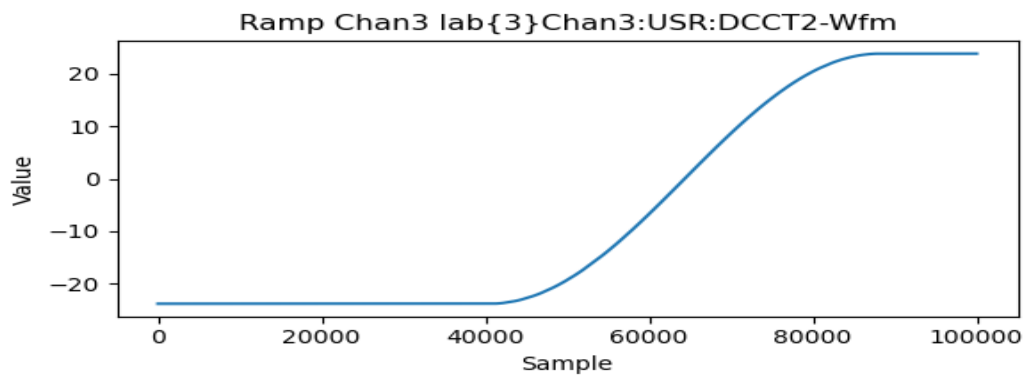Ramp Chan2 lab{3}Chan2:USR:Reg-Wfm

Ramp Chan2 PV: lab{3}Chan2:USR:Error-Wfm

Ramp Chan2 lab{3}Chan2:USR:Error-Wfm

Ramp Chan3 PV: lab{3}Chan3:USR:DCCT1-Wfm
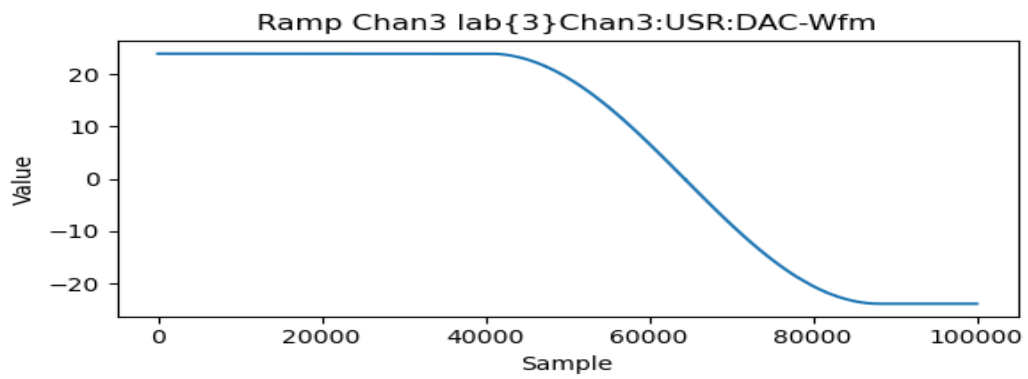
Ramp Chan3 lab{3}Chan3:USR:DCCT1-Wfm

Ramp Chan3 PV: lab{3}Chan3:USR:DCCT2-Wfm
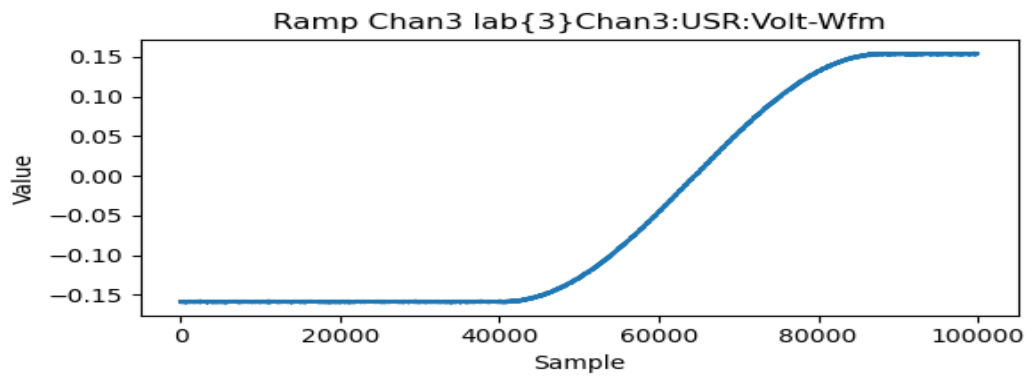

Ramp Chan3 lab{3}Chan3:USR:DCCT2-Wfm

Ramp Chan3 PV: lab{3}Chan3:USR:DAC-Wfm
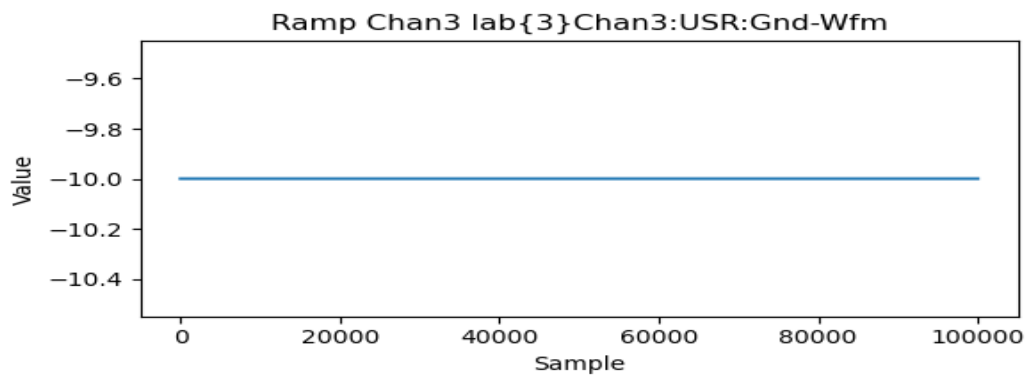

Ramp Chan3 lab{3}Chan3:USR:DAC-Wfm

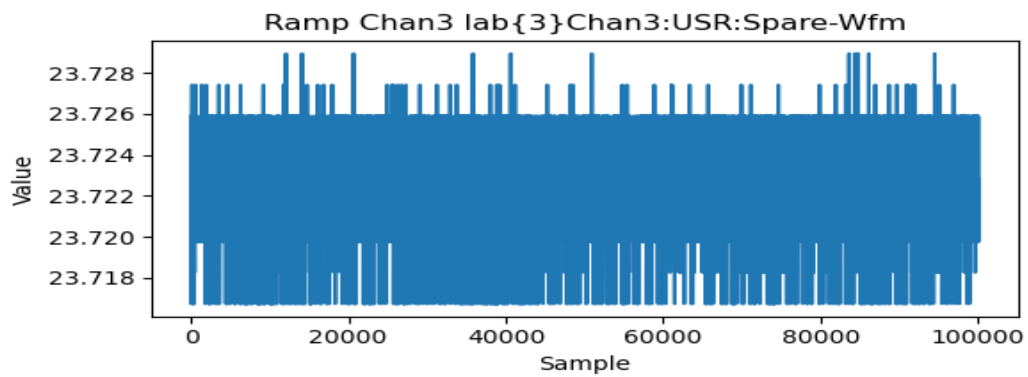Ramp Chan3 PV: lab{3}Chan3:USR:Volt-Wfm

Ramp Chan3 lab{3}Chan3:USR:Volt-Wfm

Ramp Chan3 PV: lab{3}Chan3:USR:Gnd-Wfm
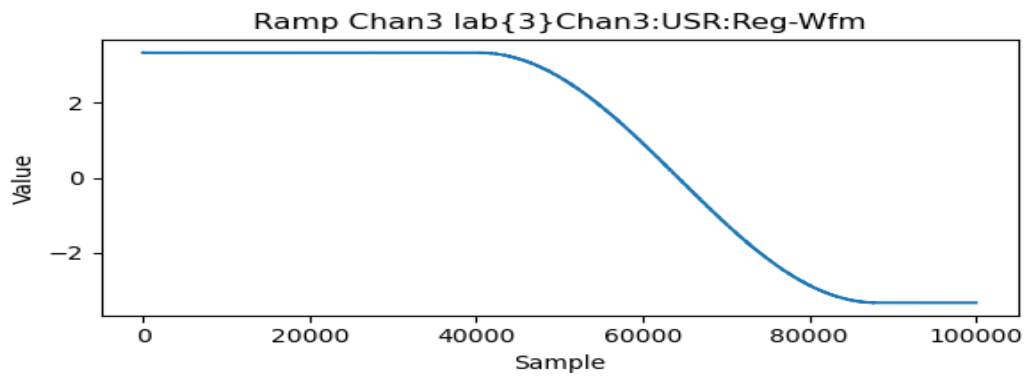

Ramp Chan3 lab{3}Chan3:USR:Gnd-Wfm

Ramp Chan3 PV: lab{3}Chan3:USR:Spare-Wfm

Ramp Chan3 lab{3}Chan3:USR:Spare-Wfm
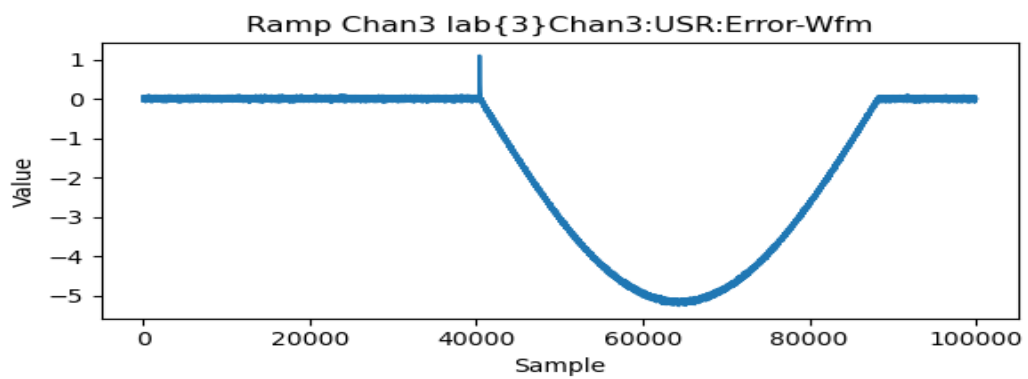
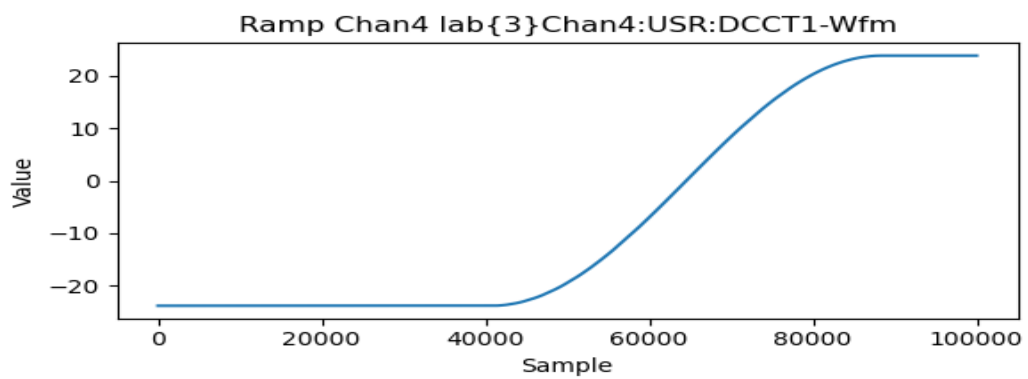Ramp Chan3 PV: lab{3}Chan3:USR:Reg-Wfm

Ramp Chan3 lab{3}Chan3:USR:Reg-Wfm

Ramp Chan3 PV: lab{3}Chan3:USR:Error-Wfm
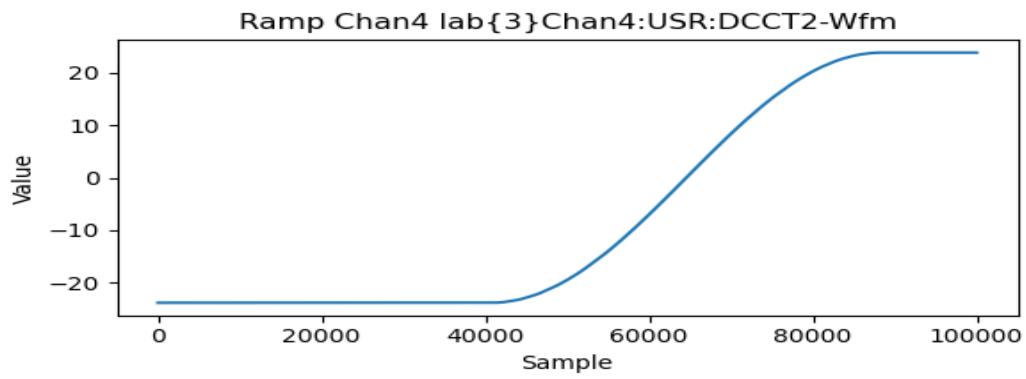

Ramp Chan3 lab{3}Chan3:USR:Error-Wfm

Ramp Chan4 PV: lab{3}Chan4:USR:DCCT1-Wfm
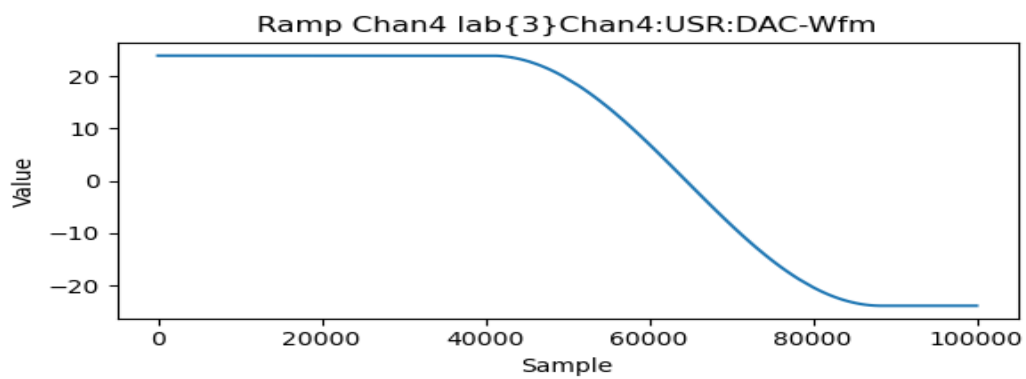

Ramp Chan4 lab{3}Chan4:USR:DCCT1-Wfm

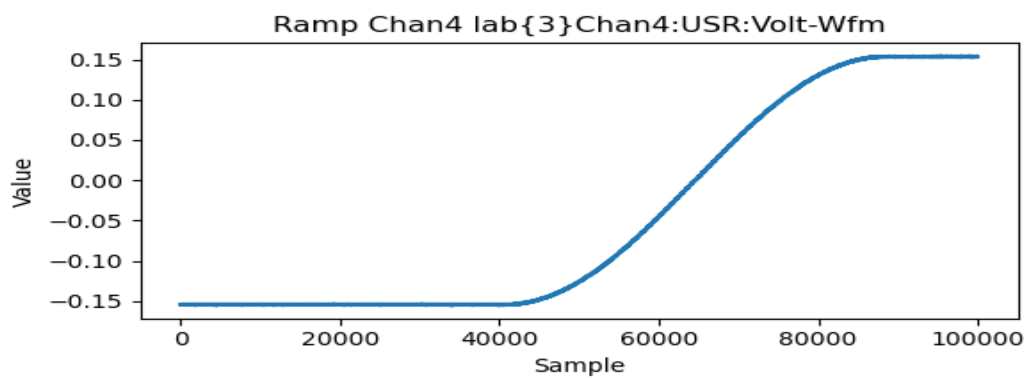Ramp Chan4 PV: lab{3}Chan4:USR:DCCT2-Wfm

Ramp Chan4 lab{3}Chan4:USR:DCCT2-Wfm

Ramp Chan4 PV: lab{3}Chan4:USR:DAC-Wfm
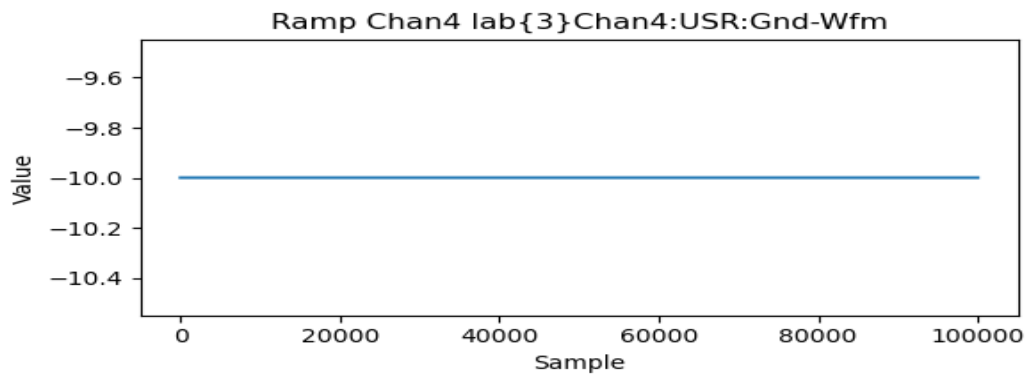

Ramp Chan4 lab{3}Chan4:USR:DAC-Wfm

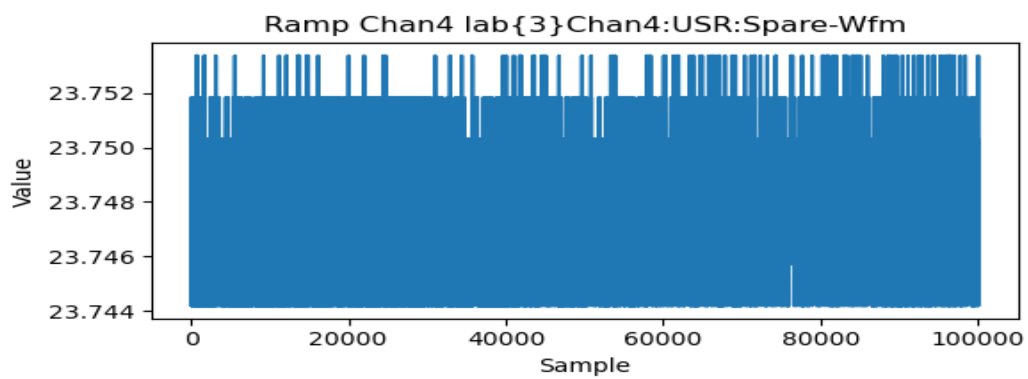Ramp Chan4 PV: lab{3}Chan4:USR:Volt-Wfm

Ramp Chan4 lab{3}Chan4:USR:Volt-Wfm

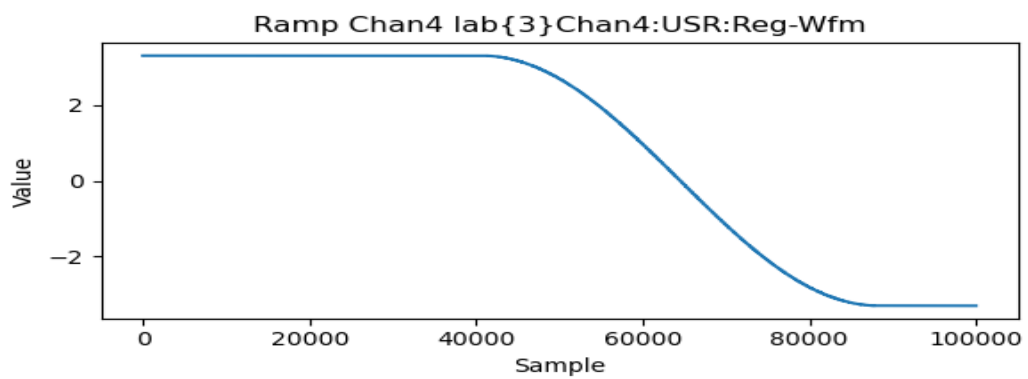Ramp Chan4 PV: lab{3}Chan4:USR:Gnd-Wfm

Ramp Chan4 lab{3}Chan4:USR:Gnd-Wfm

Ramp Chan4 PV: lab{3}Chan4:USR:Spare-Wfm
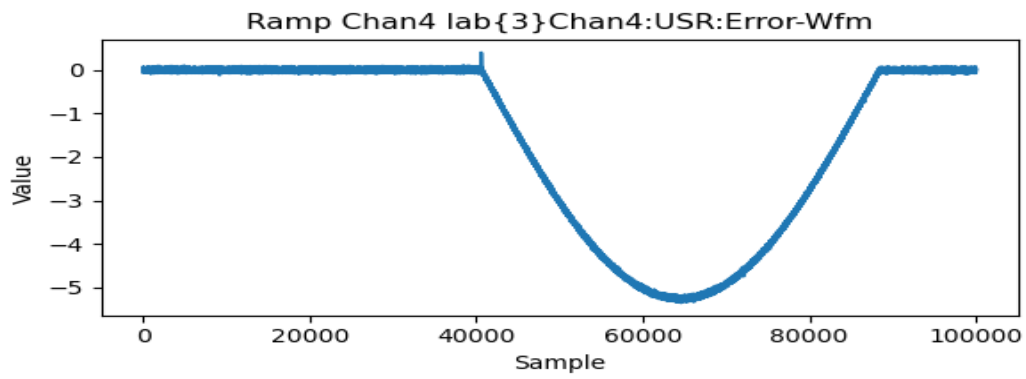

Ramp Chan4 lab{3}Chan4:USR:Spare-Wfm

Ramp Chan4 PV: lab{3}Chan4:USR:Reg-Wfm
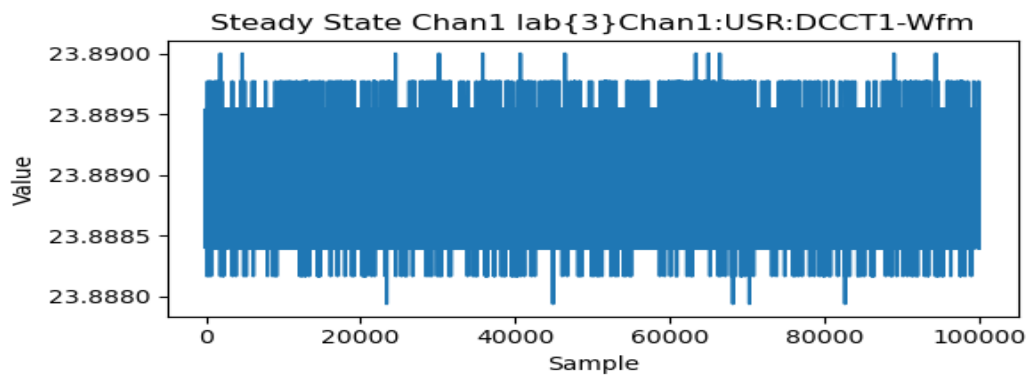

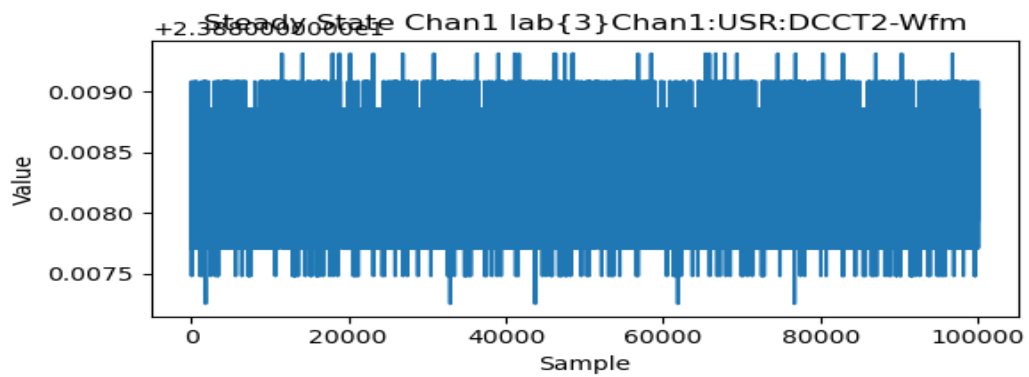Ramp Chan4 lab{3}Chan4:USR:Reg-Wfm

Ramp Chan4 PV: lab{3}Chan4:USR:Error-Wfm

Ramp Chan4 lab{3}Chan4:USR:Error-Wfm

Steady State Chan1 PV: lab{3}Chan1:USR:DCCT1-Wfm
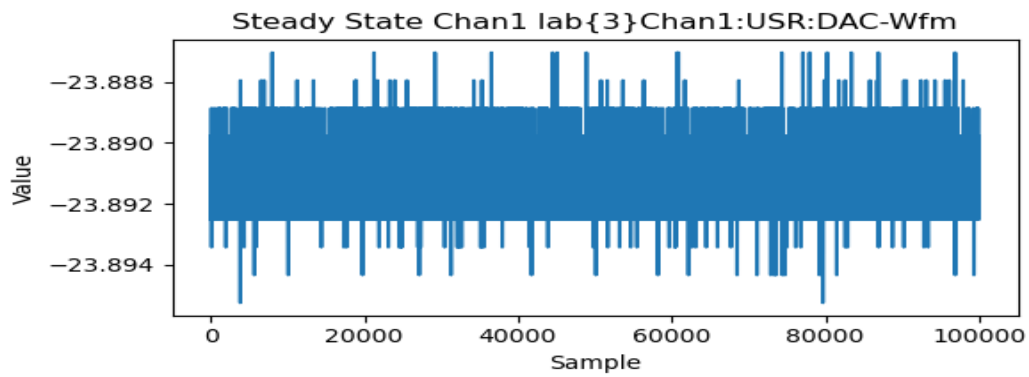

Steady State Chan1 lab{3}Chan1:USR:DCCT1-Wfm

Steady State Chan1 PV: lab{3}Chan1:USR:DCCT2-Wfm
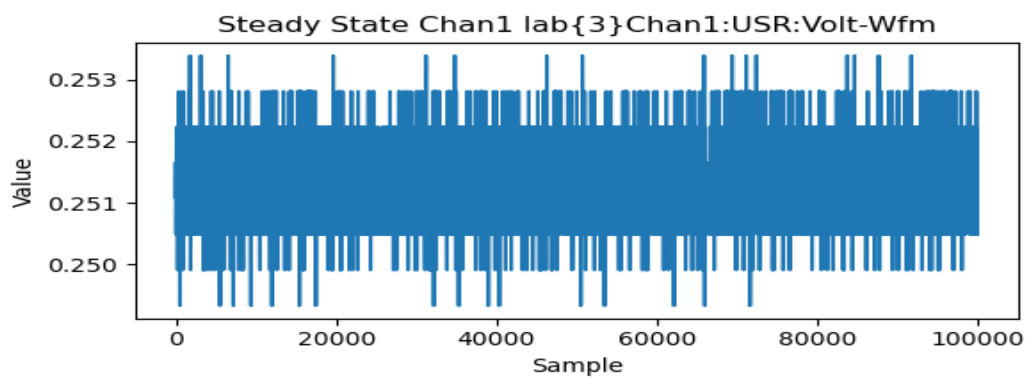

Steady State Chan1 lab{3}Chan1:USR:DCCT2-Wfm

Steady State Chan1 PV: lab{3}Chan1:USR:DAC-Wfm
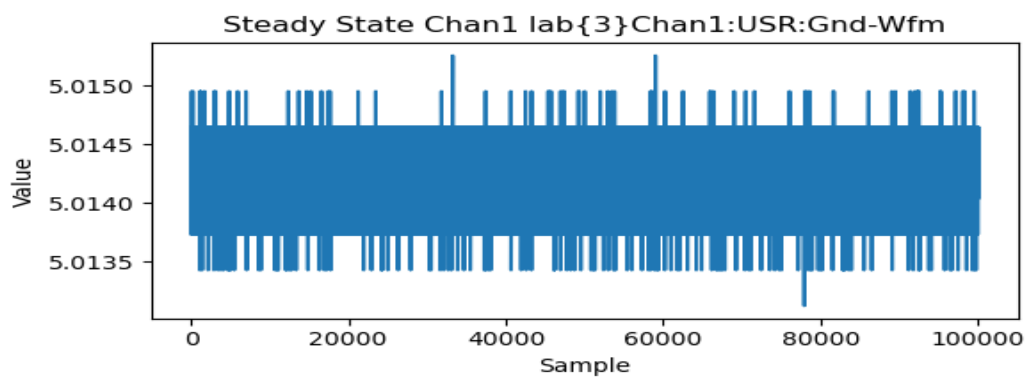
Steady State Chan1 lab{3}Chan1:USR:DAC-Wfm

Steady State Chan1 PV: lab{3}Chan1:USR:Volt-Wfm

Steady State Chan1 lab{3}Chan1:USR:Volt-Wfm
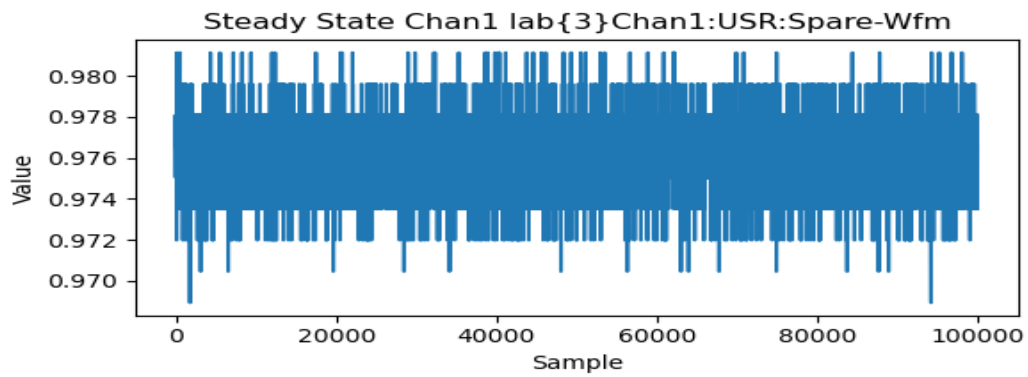
Steady State Chan1 PV: lab{3}Chan1:USR:Gnd-Wfm

Steady State Chan1 lab{3}Chan1:USR:Gnd-Wfm
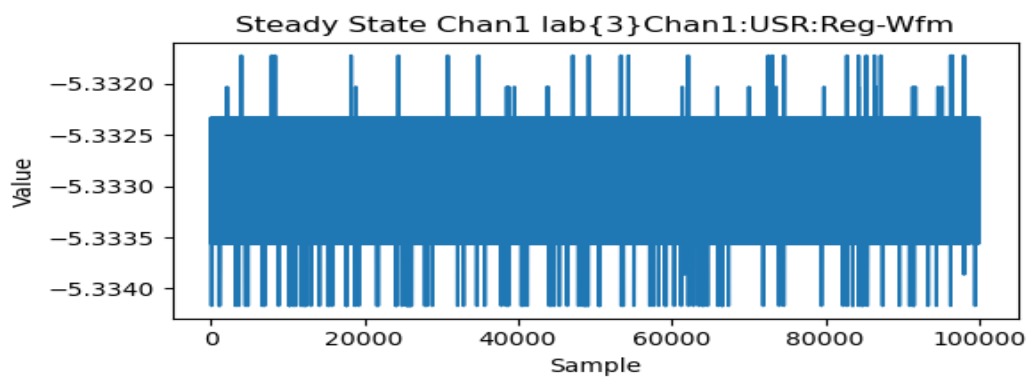
Steady State Chan1 PV: lab{3}Chan1:USR:Spare-Wfm
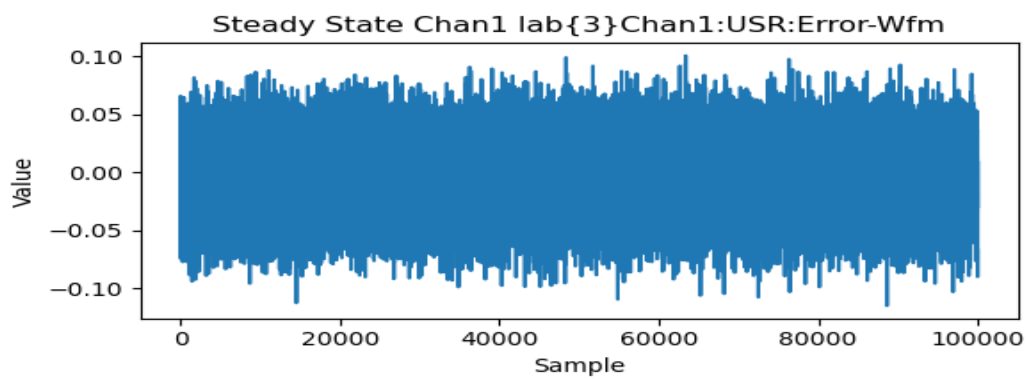
Steady State Chan1 lab{3}Chan1:USR:Spare-Wfm

Steady State Chan1 PV: lab{3}Chan1:USR:Reg-Wfm
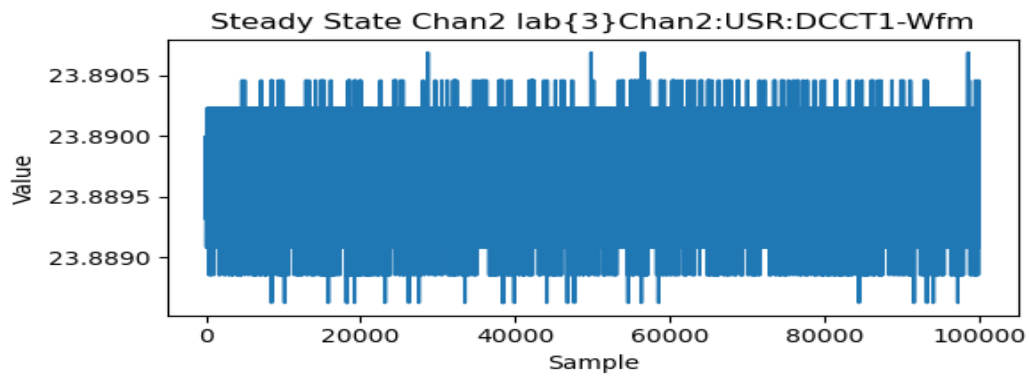

Steady State Chan1 lab{3}Chan1:USR:Reg-Wfm
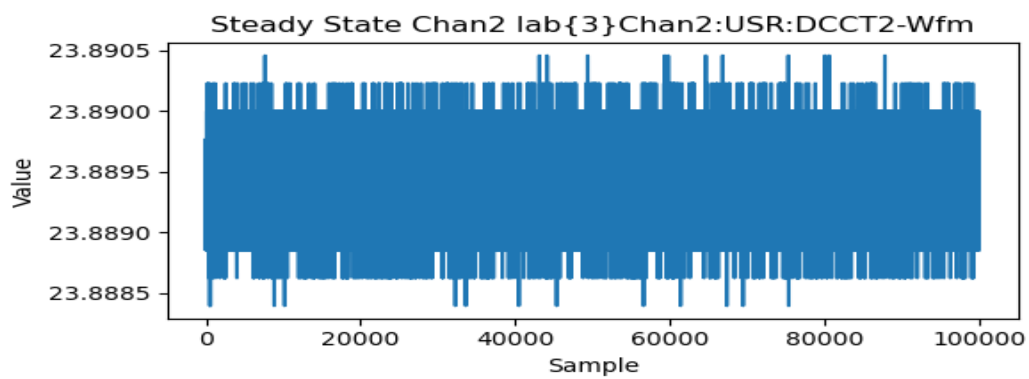
Steady State Chan1 PV: lab{3}Chan1:USR:Error-Wfm

Steady State Chan1 lab{3}Chan1:USR:Error-Wfm

Steady State Chan2 PV: lab{3}Chan2:USR:DCCT1-Wfm
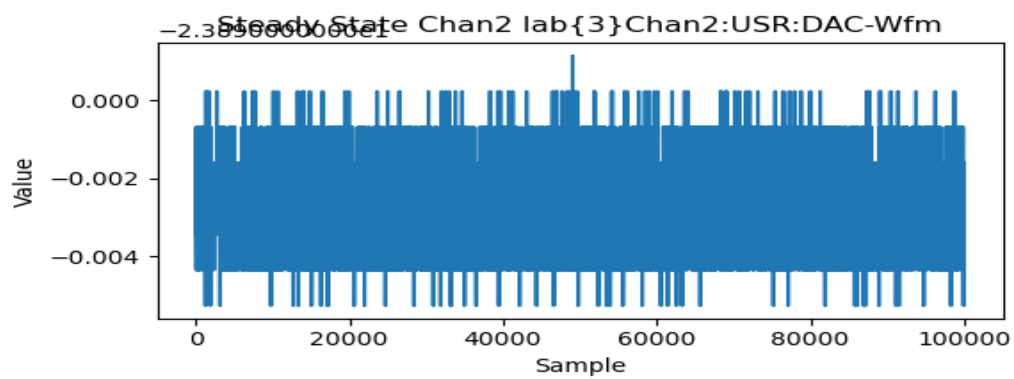
Steady State Chan2 lab{3}Chan2:USR:DCCT1-Wfm

Steady State Chan2 PV: lab{3}Chan2:USR:DCCT2-Wfm
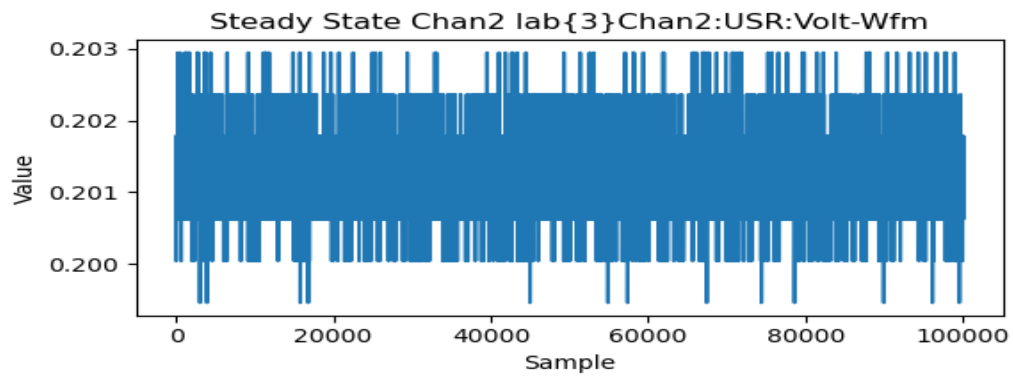

Steady State Chan2 lab{3}Chan2:USR:DCCT2-Wfm
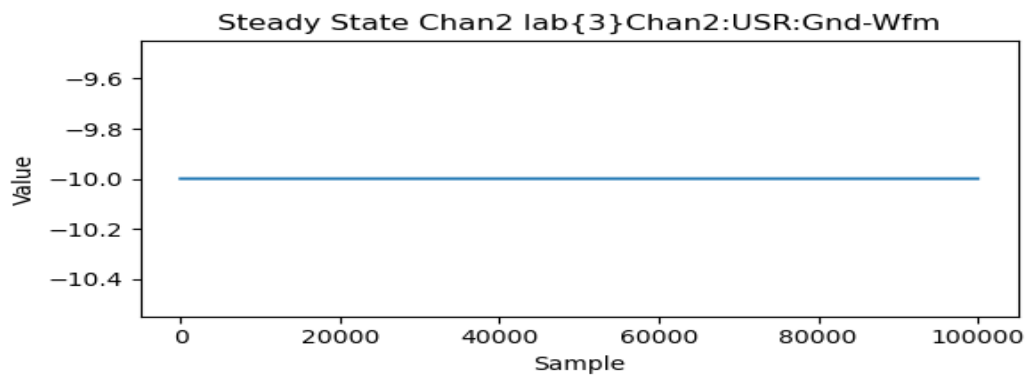
Steady State Chan2 PV: lab{3}Chan2:USR:DAC-Wfm

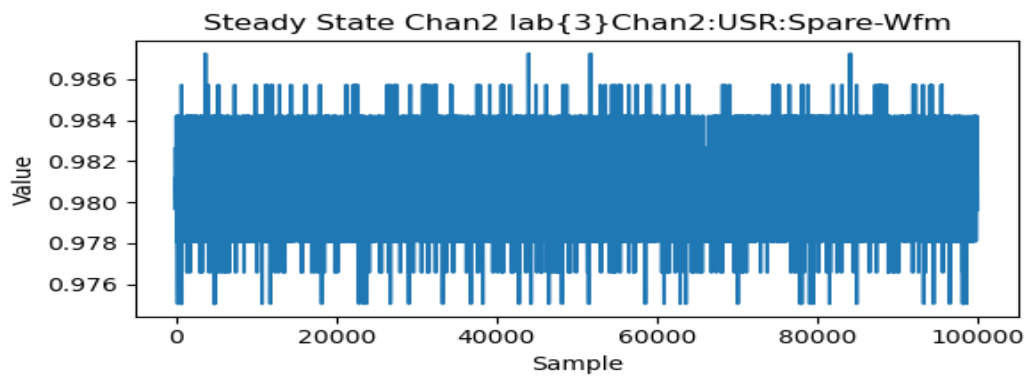Steady State Chan2 lab{3}Chan2:USR:DAC-Wfm

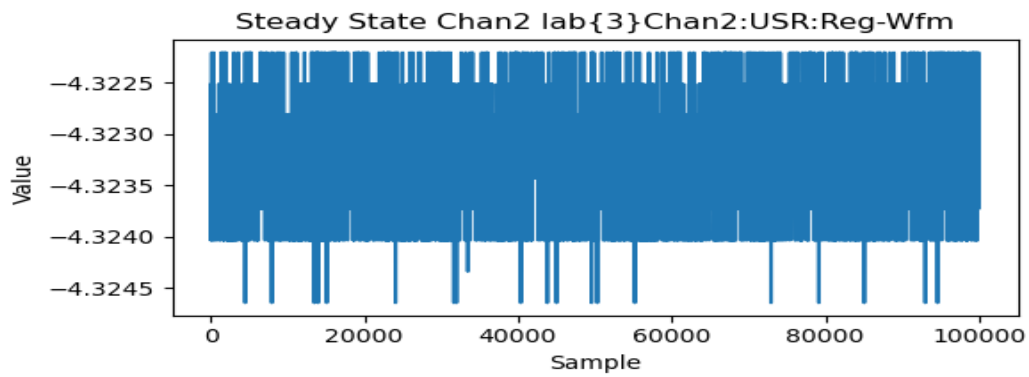Steady State Chan2 PV: lab{3}Chan2:USR:Volt-Wfm

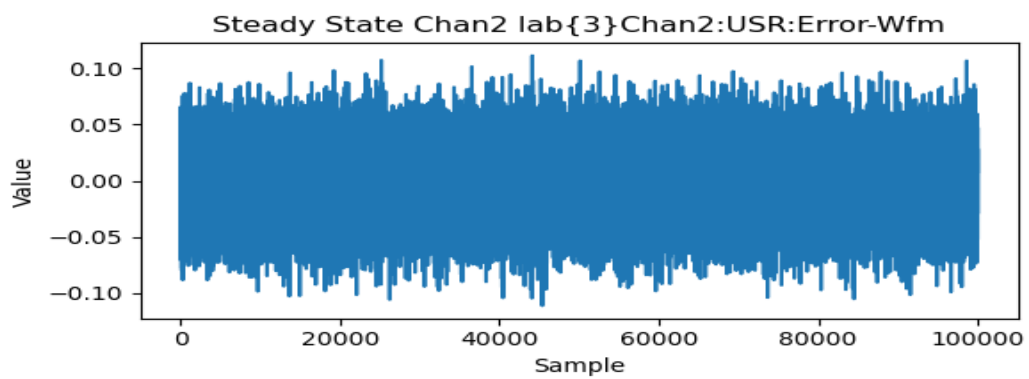Steady State Chan2 PV: lab{3}Chan2:USR:Gnd-Wfm

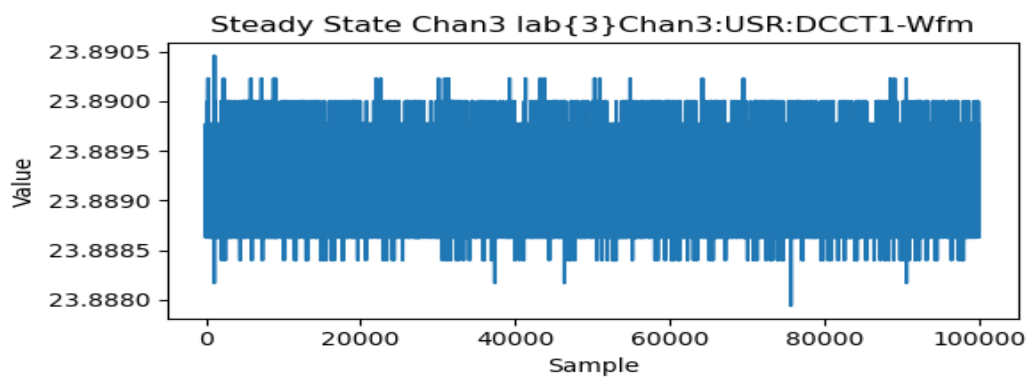Steady State Chan2 PV: lab{3}Chan2:USR:Spare-Wfm

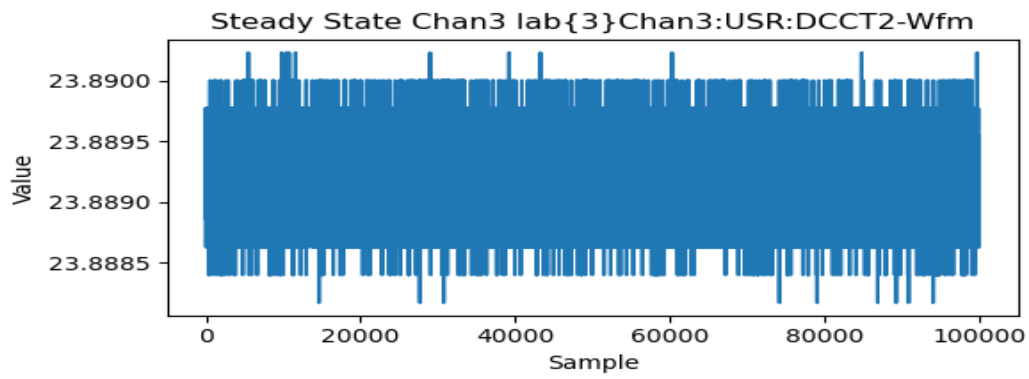Steady State Chan2 PV: lab{3}Chan2:USR:Reg-Wfm

Steady State Chan2 PV: lab{3}Chan2:USR:Error-Wfm
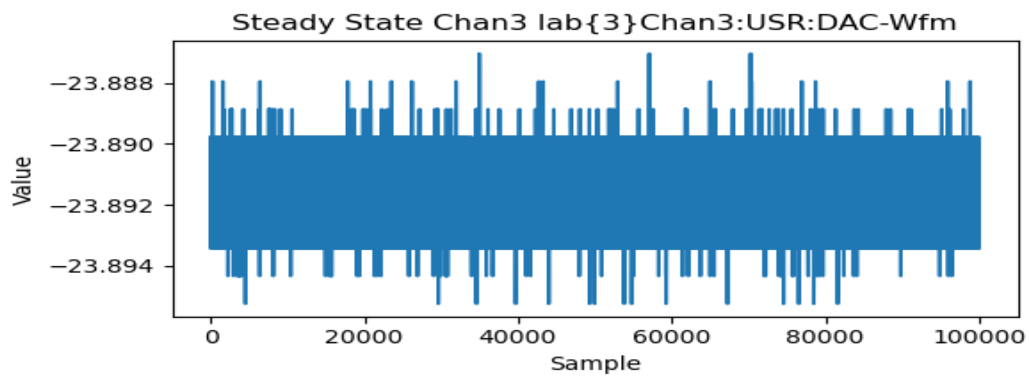

Steady State Chan3 PV: lab{3}Chan3:USR:DCCT1-Wfm

Steady State Chan3 PV: lab{3}Chan3:USR:DCCT2-Wfm

Steady State Chan3 lab{3}Chan3:USR:DCCT2-Wfm
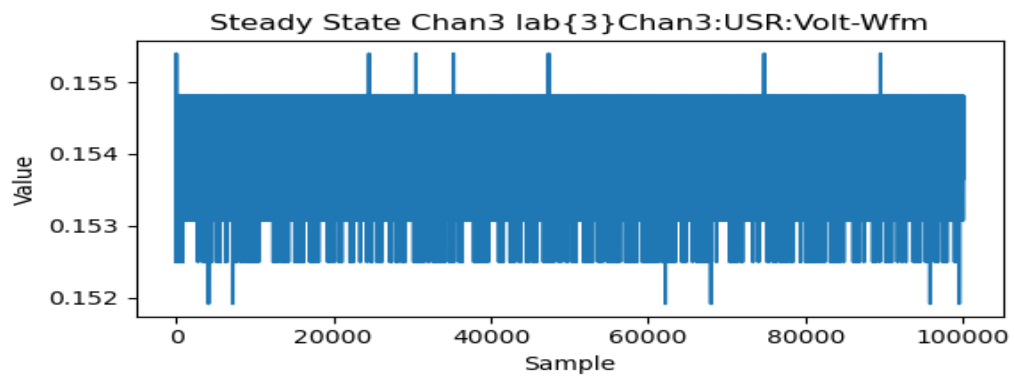
Steady State Chan3 PV: lab{3}Chan3:USR:DAC-Wfm
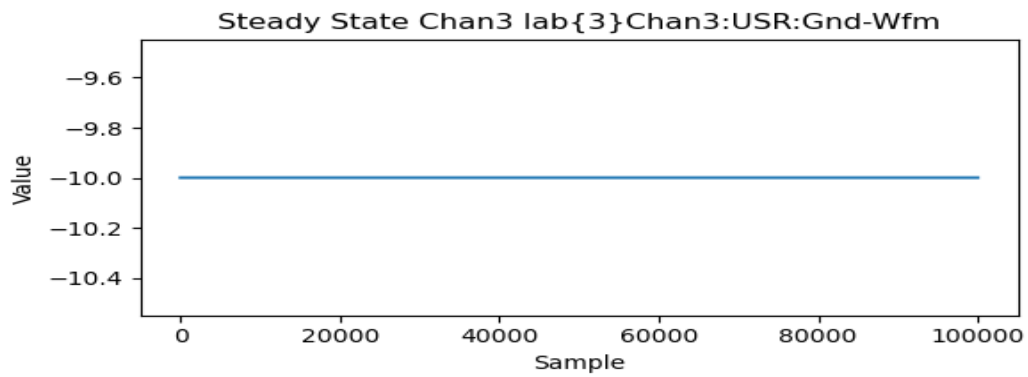

Steady State Chan3 lab{3}Chan3:USR:DAC-Wfm
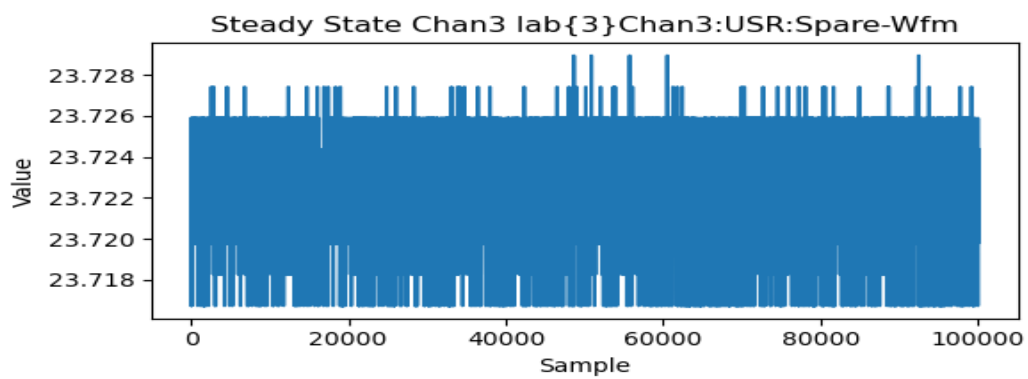
Steady State Chan3 PV: lab{3}Chan3:USR:Volt-Wfm

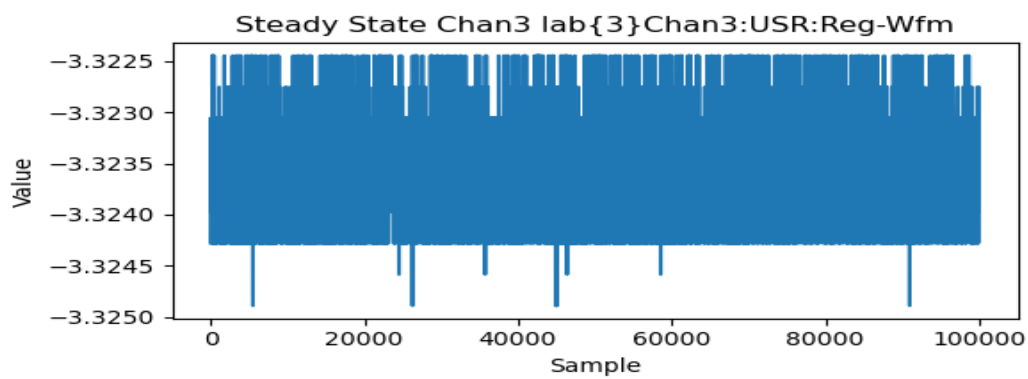Steady State Chan3 lab{3}Chan3:USR:Volt-Wfm

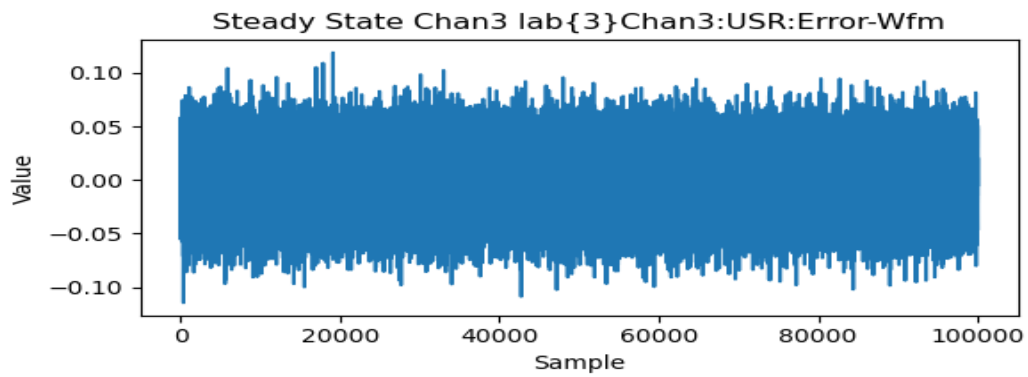Steady State Chan3 PV: lab{3}Chan3:USR:Gnd-Wfm

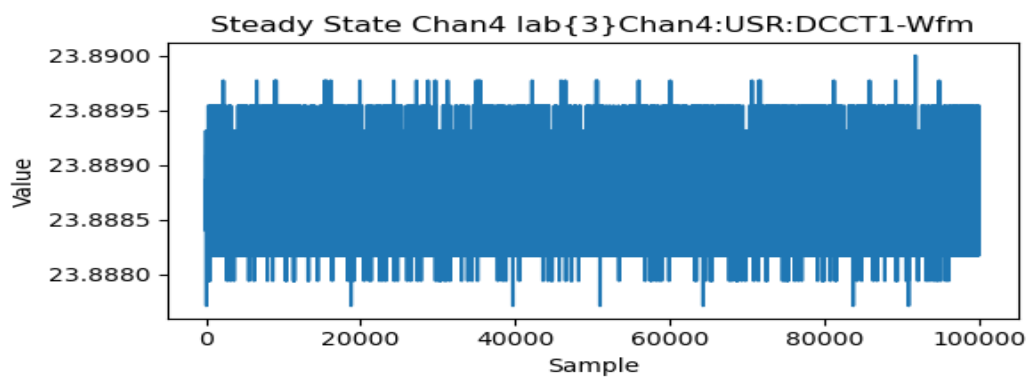Steady State Chan3 PV: lab{3}Chan3:USR:Spare-Wfm

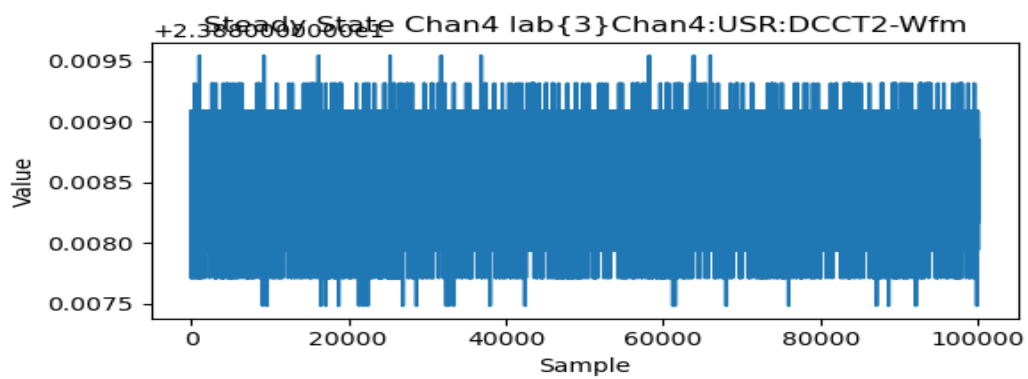Steady State Chan3 PV: lab{3}Chan3:USR:Reg-Wfm

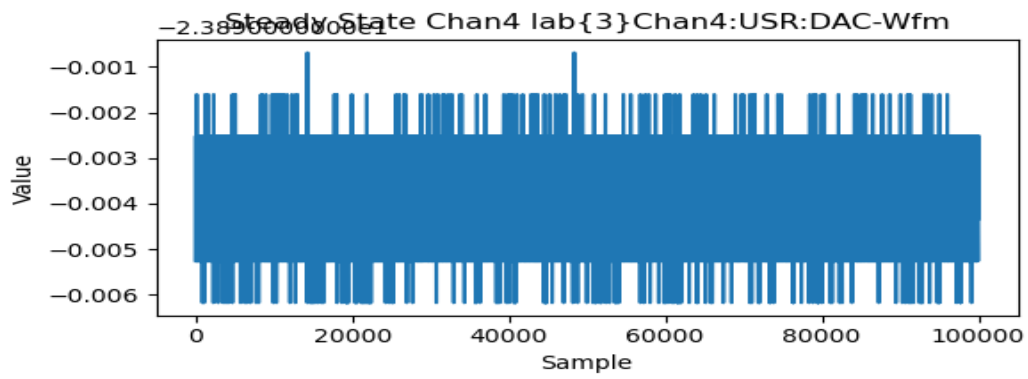Steady State Chan3 PV: lab{3}Chan3:USR:Error-Wfm
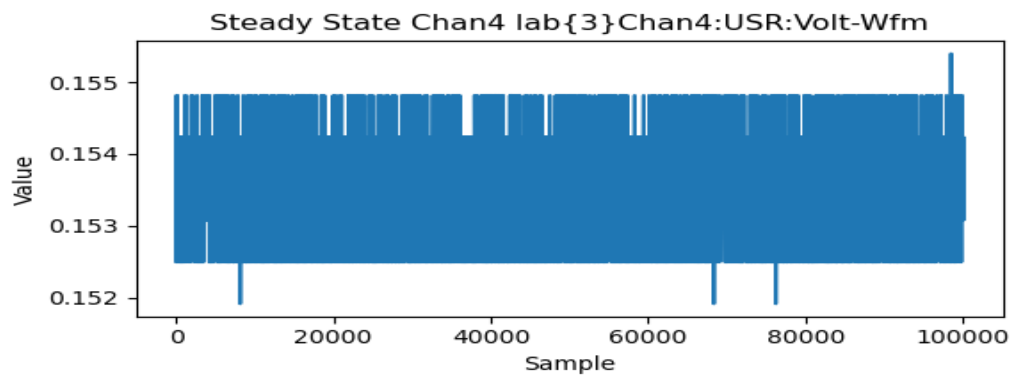
Steady State Chan4 PV: lab{3}Chan4:USR:DCCT1-Wfm
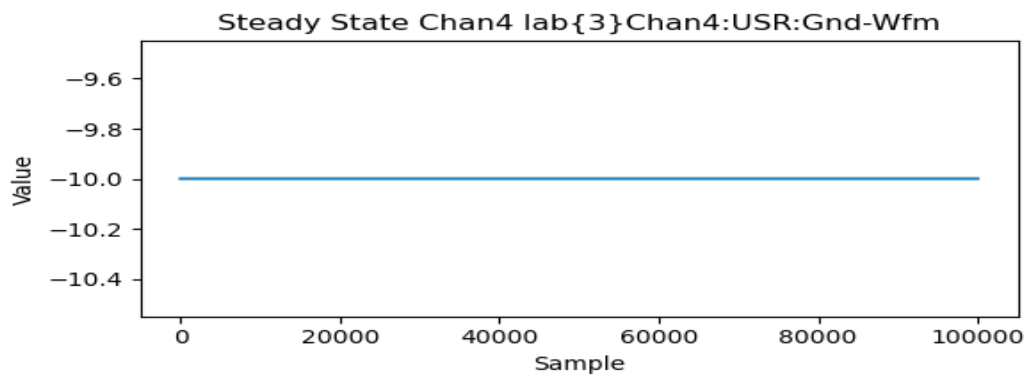

Steady State Chan4 PV: lab{3}Chan4:USR:DCCT2-Wfm
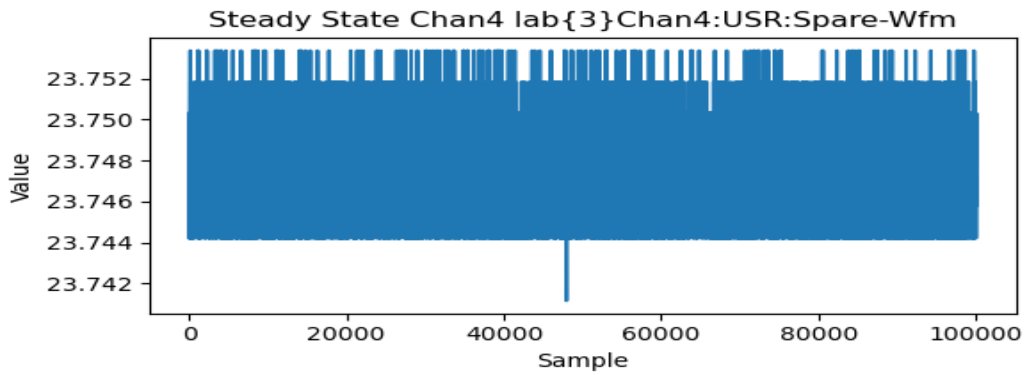

Steady State Chan4 PV: lab{3}Chan4:USR:DAC-Wfm

Steady State Chan4 lab{3}Chan4:USR:DAC-Wfm

Steady State Chan4 PV: lab{3}Chan4:USR:Volt-Wfm

Steady State Chan4 lab{3}Chan4:USR:Volt-Wfm

Steady State Chan4 PV: lab{3}Chan4:USR:Gnd-Wfm
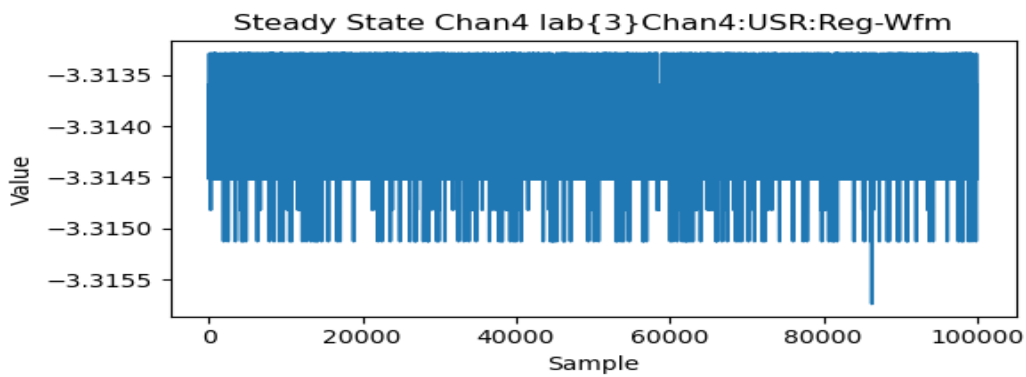

Steady State Chan4 lab{3}Chan4:USR:Gnd-Wfm

Steady State Chan4 PV: lab{3}Chan4:USR:Spare-Wfm

Steady State Chan4 lab{3}Chan4:USR:Spare-Wfm
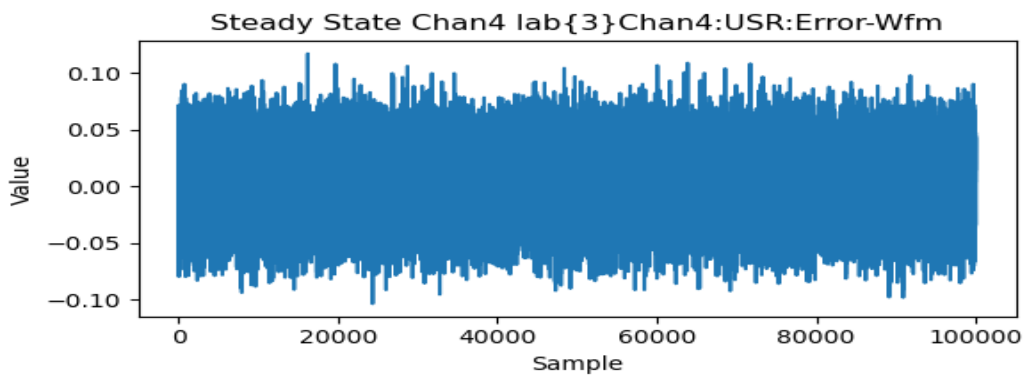
Steady State Chan4 PV: lab{3}Chan4:USR:Reg-Wfm

Steady State Chan4 lab{3}Chan4:USR:Reg-Wfm
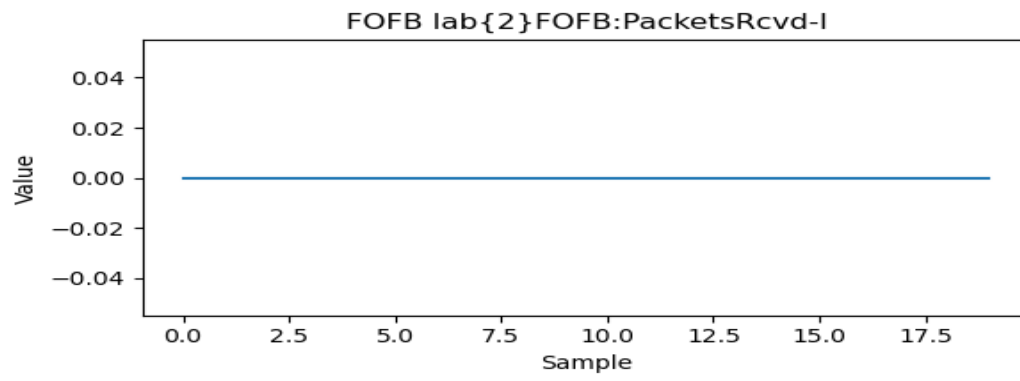
Steady State Chan4 PV: lab{3}Chan4:USR:Error-Wfm

Steady State Chan4 lab{3}Chan4:USR:Error-Wfm

Section 2: FOFB Packet test

FOFB PV: lab{2}FOFB:PacketsRcvd-I monotonic test -> **PASS**

FOFB lab{2}FOFB:PacketsRcvd-I

FOFB test: SKIPPED (Bandwidth-Mode != Fast)