[FATIH EMRE SIMSEK]

CURRICULUM VITAE

PERSONAL DETAILS

Surname   : Simsek
First name   : Fatih Emre
Date of birth   : 15.01.1987
Place of residence : Ankara/Turkey
Nationality   : Turkish

PROFILE & AMBITION

As highly motivated and future potential electronics engineer, with strong analytical and research skills, I am seeking for FPGA design engineering positions. I mostly worked in FPGA business by designing PCBs and FPGAs. My areas of interests are Video and Image processing on FPGA, high speed data transfer on XAUI and Ethernet protocols on FPGA, Microprocessors & Embedded Systems. My ultimate career goal is to be a part of world's leading technology suppliers in which I can work with highly qualified engineers while making effective and significant contribution to my company.

EDUCATION & COURSES

Education

	Period	Education & Projects	Diploma
	2017-Present	**Philosophy of Doctorate:** ● Main subject: Video image processing ● Potential thesis: Motion estimation algorithm for H.264 video compression	No
	2010-2013	**Master of Science in Electrical and Electronics Engineering:** ● Main subjects: Electromagnetic fields & Analog circuits ● Master thesis: Finite Element Method Based Simulations of Low Frequency Magnetic Field in Seawater	Yes
	2005-2010	**Bachelor of Science in Electrical and Electronics Engineering:** ● Senior project: Underwater electro-acoustic telephony system	Yes

Courses

Period	Description course	Institute	Certificate
02/2018	Incremental Compilation on Altera/Intel QuartusII	Kuantek	No
02/2018	Static Timing Analysis on Altera/Intel QuartusII Timequest Timing Analyzer	Kuantek	No
10/2017	C Programming for Embedded Systems	Doulos	Yes
04/2017	Embedded Design for Intel SoC FPGAs	Doulos	Yes
01/2017	Verilog, System Verilog & UVM Fundamentals	Anka-Sys	Yes
09/2016	The Intel SoC FPGA Developer Forum (ISDF)	Intel	No
02/2016	DO-254 Based FPGA Digital Design Flow	PLC2	No
04/2015	Building Gigabit Interfaces in Altera Transciever Devices	EBV	No
01/2014	Introduction to QuartusII	EBV	Yes
04/2014	Mentor Graphics DxDesigner Training	CDT	Yes

WORK EXPERIENCE & ADDITIONAL QUALIFICATIONS

Work experience:

	Period	Department and function
aselsan	2013-Present	Electronics Design Department • Digital Design Engineer
	2010-2013	Bilkent Underwater Acoustics Technologies Research Center • Design and Test Engineer of a torpedo which is activated according to change in Electric field

The position is described in more detail in the appendix

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ADDITIONAL QUALIFICATIONS (WORK EXPERIENCE):

Internship:

	Period	Department and function
HAVELSAN	06/2009	Network System Administration ● Network switch maintenance of the campus ● Design of a chat program in Java by using socket programming
aselsan	06/2008	Electronics Design Department ● Pic programming in C: Reading an analog temperature sensor and displaying the result on a 7-segment

EXPERTISE

	Average	Good	Very Good
Operating Systems			
Microsoft Windows			X
GNU/Linux (Raspbian)		X	
macOS		X	
Programming/Software/Design			
Java		X	
Assembly	X		
C	X		
Python	X		
Matlab, GNU/Octave		X	
Hardware Description Language			
VHDL			X
Verilog	X		
FPGA Brand & Model			
Intel/Altera Cyclone V			X
Intel/Altera Stratix V		X	
Intel/Altera Cyclone III	X		
Xilinx Spartan 6	X		
Xilinx Spartan 3E		X	
Design Software			
Intel/Altera QuartusII			X
Xilinx Vivado	X		
Xilinx ISE		X	
Modelsim			X
Mentor Graphics HDL Designer			X
Tortoise SVN		X	

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Comsol Multiphysics	X		
PSpice/5Spice	X		
Equipment/Hardware/Tools			
Multimeter			X
Oscilloscope		X	
Microsoft and other office applications			
MS Office		X	
MS Visio		X	
Open/Libre Office	X		

LANGUAGE SKILLS

	SPEAKING	WRITING
Turkish	Native Speaker	Native Speaker
English	Fluent	Fluent
German	Beginner	Beginner

HOBBIES

- Building projects with Raspberry Pi and Arduino Uno at home. These projects include video camera, sensors such as temperature and humidity. These are projects of hobby electronics.
- Table tennis
- Bowling
- Running

PORTFOLIO

Aselsan Inc, Digital Design Engineer

2013-Present

- Owned full-cycle development of FPGAs including implementation, functional simulation, synthesis, static timing analysis, board level integration:

  - Designed, simulated and tested ITU-R BT.656 digital video encoder and decoder block for PAL and PAL Square videos
  - Designed, simulated and tested a video clock domain crosser block
  - Designed, simulated and tested a video deinterlacer block
  - Designed,simulated and tested a video affine transformer IP
  - Designed, simulated and tested an Exponential-Golomb encoder for H.264/AVC
  - Designed, simulated and tested a block of fusion of thermal and night vision videos
  - Designed, simulated and tested a video histogram calculator
  - Designed, simulated and tested a color space converter block
  - Designed, simulated and tested a camera-link TX/RX block using SERDES IP
  - Designed, simulated and tested a separable 9x9 filter to have HF and LF components of video
  - Designed, simulated and tested a linear image optimization block to stretch the content of night vision video due to low dynamic range
  - Designed, simulated and tested a video electronic zoom and freeze block
  - Designed, simulated and tested video vertical and horizontal flip blocks
  - Designed, simulated and tested an interface to capture analog video via ADC
  - Designed, simulated and tested a video test pattern generator block
  - Designed, simulated and tested a multiport arbiter interface for XAUI PHY and Ethernet MAC to stream data via fiber optic interfaces.
  - Designed, simulated and tested a multiport arbiter interface for DDR3 SDRAM and LPDDR2 SDRAM
  - Designed, simulated and tested an Avalon Memory Mapped to UART interface
  - Designed, simulated and tested an Avalon Memory Mapped to mutiport XAUI interface. This interface has two dual-port BRAM
  - Designed, simulated and tested an Avalon Memory Mapped to Xilinx MCB adaptor interface
  - Designed, simulated and tested a packet filter of ethernet stream
  - Designed, simulated and tested low speed communication interfaces such as UART, USART, I2C, SPI and BISS.
  - Integrated thermal and night vision video processing algorithms on FPGAs.
  - Integrated SDI IP block
  - Designed, simulated and tested RSA algorithm in cryptography: modulo exponentiation, modulo multiplication

2013-2015

- High speed electronic board design including schematic and PCB layout:

  - ❖ Joined hardware design for 18-20 layer PCB boards consisting of at least 100 different individual components.
  - ❖ Performed hardware design of an electronic board which is used to test the interfaces of an electronic board which has Cyclone V FPGA on it.
  - ❖ Board level debug of high speed transceivers SFP, XFP and high speed interfaces 10G/XAUI, XFI, SFI.
  - ❖ Board level debug of a camera interface board containing Cyclone V FPGA, LVDS transceivers, RS422 transceivers, DDR3 SDRAM.
  - ❖ Board level debug of fiber optic interface board containing Spartan-6 FPGA, LPDDR2 SDRAM, Camera Link receivers, clock generators.

2013-Present

- Experience on some Detectors, ICs, Cameras and Display:

  - ❖ SOFRADIR Cooled Thermal Sensor
  - ❖ ULIS PICO Gen 2 Uncooled Thermal Sensor
  - ❖ ULIS Gen 1 Uncooled Thermal Sensor
  - ❖ FLIR MUON Uncooled Thermal Sensor
  - ❖ NIT Night Vision Sensor
  - ❖ SONY DayTV Camera (FCB-EX 15EP)
  - ❖ ANALOG DEVICES Analog Video Encoder (ADV7393)
  - ❖ ANALOG DEVICES Analog Video Decoder (ADV7180)
  - ❖ OLIGHTEC 800x600 Low-power Amoled Microdisplay
  - ❖ ANALOG DEVICES ADC (LTC2263-14)
  - ❖ TEXAS INSTRUMENTS DAC (DAC124S085)
  - ❖ KVH 1750 IMU
  - ❖ RENISHAW Rotary Optical Encoder

Bilkent Underwater Acoustic Technologies Research Center, Design and Test Engineer

My assignment on this center was to design and test a torpedo which is activated according to change in Electric field. The following tasks were accomplished:

- ❖ Design and simulation of coils via COMSOL Multiphysics, and realization of the coils.
- ❖ Design and realization of a D-type amplifier.
- ❖ Measuring the magnetic field via Bartington Spectramag-6 magnetometer and filtering on MATLAB.
- ❖ Environmental condition tests of the coils and PCBs.