TUSB2046x 4-Port Hub for the Universal Serial Bus With Optional Serial EEPROM Interface

1 Features

- Fully Compliant With the USB Specification as a Full-Speed Hub: TID #30220231
- 32-Pin LQFP (1) Package With a 0.8-mm Terminal Pitch or QFN Package With a 0.5-mm Pin Pitch
- 3.3-V Low-Power ASIC Logic
- Integrated USB Transceivers
- State Machine Implementation Requires No Firmware Programming
- One Upstream Port and Four Downstream Ports
- All Downstream Ports Support Full-Speed and Low-Speed Operations
- Two Power Source Modes
  - Self-Powered Mode
  - Bus-Powered Mode
- Power Switching and Overcurrent Reporting Is Provided Ganged or Per Port
- Supports Suspend and Resume Operations
- Supports Programmable Vendor ID and Product ID With External Serial EEPROM
- 3-State EEPROM Interface Allows EEPROM Sharing
- Push-Pull Outputs for $\overline{\text{PWRON}}$ Eliminate the Need for External Pullup Resistors
- Noise Filtering on $\overline{\text{OVRCUR}}$ Provides Immunity to Voltage Spikes
- Package Pinout Allows 2-Layer PCB
- Low EMI Emission Achieved by a 6-MHz Crystal Input
- Migrated From Proven TUSB2040 Hub
- Lower Cost Than the TUSB2040 Hub
- Enhanced System ESD Performance
- No Special Driver Requirements; Works Seamlessly With Any Operating System With USB Stack Support
- Supports 6-MHz Operation Through a Crystal Input or a 48-MHz Input Clock

(1) JEDEC descriptor S-PQFP-G for low-profile quad flatpack (LQFP).

2 Applications

- Computer Systems
- Docking Stations

3 Description

The TUSB2046x is a 3.3-V CMOS hub device that provides one upstream port and four downstream ports in compliance with the Universal Serial Bus (USB) specification as a full-speed hub. Because this device is implemented with a digital state machine instead of a microcontroller, no firmware programming is required. Fully compliant USB transceivers are integrated into the ASIC for all upstream and downstream ports. The downstream ports support full-speed and low-speed devices by automatically setting the slew rate according to the speed of the device attached to the ports. The configuration of the BUSPWR pin selects either the bus-powered or the self-powered mode.

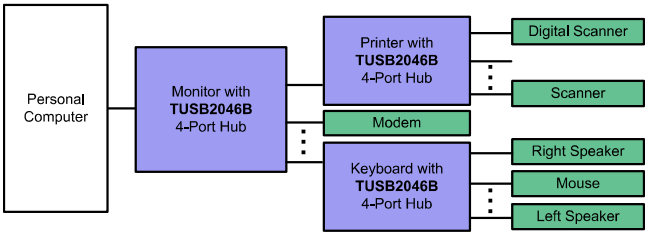
Configuring the GANGED input determines the power switching and overcurrent detection modes for the downstream ports. If GANGED is high, all $\overline{\text{PWRON}}$ outputs switch together and if any $\overline{\text{OVRCUR}}$ is activated, all ports transition to the power-off state. If GANGED is low, the $\overline{\text{PWRON}}$ outputs and $\overline{\text{OVRCUR}}$ inputs operate on a per-port basis.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TUSB2046B TUSB2046BI TUSB2046I	VQFN (32)	5.00 mm × 5.00 mm
	LQFP (32)	7.00 mm × 7.00 mm

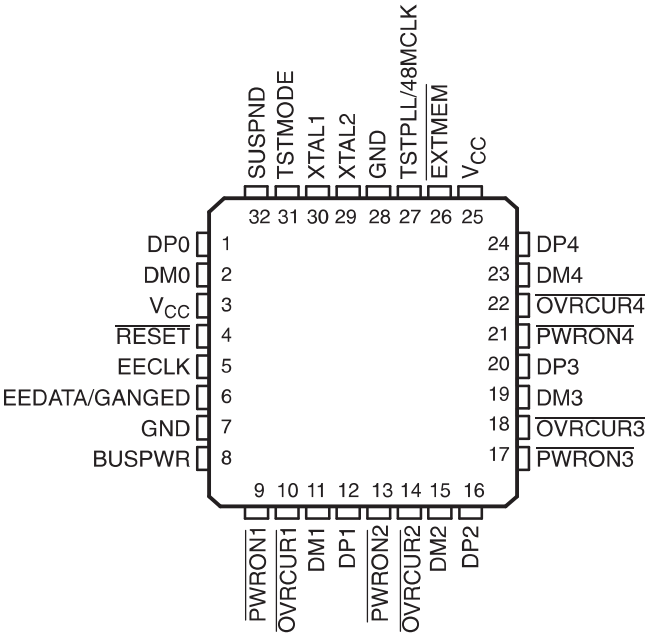
(1) For all available packages, see the orderable addendum at the end of the data sheet.

USB-Tiered Configuration Example

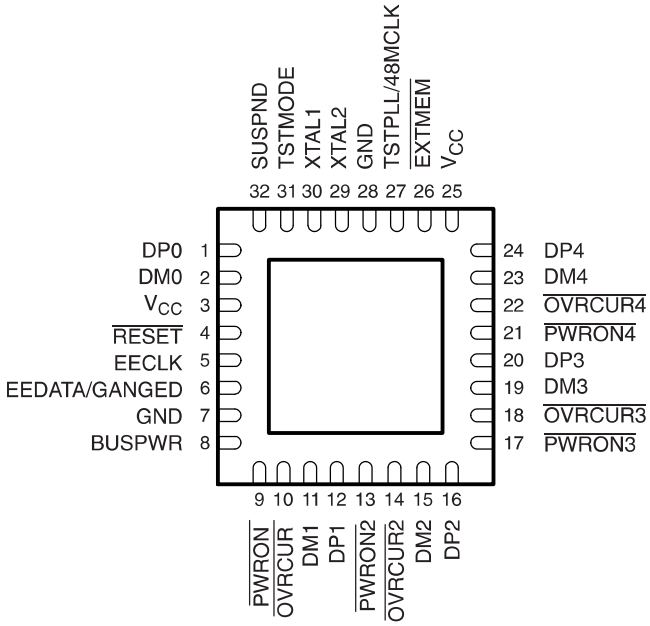


6 Pin Configuration and Functions

VF Package
32-Pin LQFP
Top View



RHB Package
32-Pin VQFN With Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BUSPWR	8	I	Power source indicator. BUSPWR is an active-high input that indicates whether the downstream ports source their power from the USB cable or a local power supply. For the bus-power mode, this terminal must be pulled to 3.3 V, and for the self-powered mode, this terminal must be pulled low. Input must not change dynamically during operation.
DM0	2	I/O	Root port USB differential data minus. DM0 paired with DP0 constitutes the upstream USB port.
DM1	11	I/O	USB differential data minus. DM1–DM4 paired with DP1–DP4 support up to four downstream USB ports.
DM2	15		
DM3	19		
DM4	23		
DP0	1	I/O	Root port USB differential data plus. DP0 paired with DM0 constitutes the upstream USB port.
DP1	12	I/O	USB differential data plus. DP1–DP4 paired with DM1–DM4 support up to four downstream USB ports.
DP2	16		
DP3	20		
DP4	24		
EECLK	5	O	EEPROM serial clock. When $\overline{\text{EXTMEM}}$ is high, the EEPROM interface is disabled. The EECLK terminal is disabled and must be left floating (unconnected). When $\overline{\text{EXTMEM}}$ is low, EECLK acts as a 3-state serial clock output to the EEPROM with a 100-μA internal pulldown.
EEDATA/GANGED	6	I/O	EEPROM serial data/power-management mode indicator. When $\overline{\text{EXTMEM}}$ is high, EEDATA/GANGED selects between ganged or per-port power overcurrent detection for the downstream ports. When $\overline{\text{EXTMEM}}$ is low, EEDATA/GANGED acts as a serial data I/O for the EEPROM and is internally pulled down with a 100-μA pulldown. This standard TTL input must not change dynamically during operation.
$\overline{\text{EXTMEM}}$	26	I	When $\overline{\text{EXTMEM}}$ is high, the serial EEPROM interface of the device is disabled. When $\overline{\text{EXTMEM}}$ is low, terminals 5 and 6 are configured as the clock and data terminals of the serial EEPROM interface, respectively.
GND	7, 28		GND terminals must be tied to ground for proper operation.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	3.6	V
V_I	Input voltage range		–0.5	V_{CC} + 0.5	V
V_O	Output voltage range		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 V or V_I < V_{CC}		±20	mA
I_{OK}	Output clamp current	V_O < 0 V or V_O < V_{CC}		±20	mA
T_A	Operating free-air temperature	TUSB2046B	0	70	°C
		TUSB2046BI, TUSB2046I	–40	85	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage levels are with respect to GND.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

PARAMETER			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	TUSB2046B	3	3.3	3.6	V
		TUSB2046BI, TUSB2046I	3.3		3.6	
V_I	Input voltage, TTL/LVCMOS		0		V_{CC}	V
V_O	Output voltage, TTL/LVCMOS		0		V_{CC}	V
$V_{IH(REC)}$	High-level input voltage, signal-ended receiver		2		V_{CC}	V
$V_{IL(REC)}$	Low-level input voltage, signal-ended receiver				0.8	V
$V_{IH(TTL)}$	High-level input voltage, TTL/LVCMOS		2		V_{CC}	V
$V_{IL(TTL)}$	Low-level input voltage, TTL/LVCMOS		0		0.8	V
T_A	Operating free-air temperature	TUSB2046B	0		70	°C
		TUSB2046BI, TUSB2046I	–40		85	
$R_{(DRV)}$	External series, differential driver resistor		22 (–5%)		22 (5%)	Ω
$f_{(OPRH)}$	Operating (dc differential driver) high speed mode				12	Mb/s
$f_{(OPRL)}$	Operating (dc differential driver) low speed mode				1.5	Mb/s
V_{ICR}	Common mode, input range, differential receiver		0.8		2.5	V
t_t	Input transition times, TTL/LVCMOS		0		25	ns
T_J	Junction temperature range		–40		115	°C

7.4 Thermal Information

THERMAL METRIC[1]		TUSB2046x RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.7	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	28.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	9.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL/LVCMOS	I_{OH} = –4 mA	V_{CC} – 0.5		V
		USB data lines	$R_{(DRV)}$ = 15 kΩ to GND	2.8		
			I_{OH} = –12 mA (without $R_{(DRV)}$)	V_{CC} – 0.5		
V_{OL}	Low-level output voltage	TTL/LVCMOS	I_{OL} = 4 mA		0.5	V
		USB data lines	$R_{(DRV)}$ = 1.5 kΩ to 3.6 V		0.3	
			I_{OL} = 12 mA (without $R_{(DRV)}$)		0.5	
V_{IT+}	Positive input threshold	TTL/LVCMOS			1.8	V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V		1.8	
V_{IT-}	Negative-input threshold	TTL/LVCMOS		0.8		V
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	1		
V_{hys}	Input hysteresis[1] ($V_{T+} - V_{T-}$)	TTL/LVCMOS		0.3	0.7	mV
		Single-ended	0.8 V ≤ V_{ICR} ≤ 2.5 V	300	500	
I_{OZ}	High-impedance output current	TTL/LVCMOS	V = V_{CC} or GND[2]		±10	µA
		USB data lines	0 V ≤ V_O ≤ V_{CC}		±10	
I_{IL}	Low-level input current	TTL/LVCMOS	V_I = GND		–1	µA
I_{IH}	High-level input current	TTL/LVCMOS	V_I = V_{CC}		1	µA
$z_{0(DRV)}$	Driver output impedance	USB data lines	Static V_{OH} or V_{OL}	7.1	19.9	Ω
V_{ID}	Differential input voltage	USB data lines	0.8 V ≤ V_{ICR} ≤ 2.5 V	0.2		V
I_{CC}	Input supply current		Normal operation		40	mA
			Suspend mode		1	µA

(1) Applies for input buffers with hysteresis.
(2) Applies for open-drain buffers.

7.6 Differential Driver Switching Characteristics (Full Speed Mode)

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_r	Transition rise time for DP or DM	See Figure 1 and Figure 2	4	20	ns
t_f	Transition fall time for DP or DM	See Figure 1 and Figure 2	4	20	ns
$t_{(RFM)}$	Rise/fall time matching[1]	(t_r/t_f) × 100	90%	110%	
$V_{O(CRS)}$	Signal crossover output voltage[1]		1.3	2.0	V

(1) Characterized only. Limits are approved by design and are not production tested.

7.7 Differential Driver Switching Characteristics (Low Speed Mode)

over recommended ranges of operating free-air temperature and supply voltage, C_L = 50 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
t_r	Transition rise time for DP or DM(1)	C_L = 200 pF to 600 pF,	See Figure 1 and Figure 2	75	300	ns
t_f	Transition fall time for DP or DM(1)	C_L = 200 pF to 600 pF,	See Figure 1 and Figure 2	75	300	ns
$t_{(RFM)}$	Rise/fall time matching(1)	$(t_r/t_f) \times 100$		80%	120%	
$V_{O(CRS)}$	Signal crossover output voltage(1)	C_L = 200 pF to 600 pF		1.3	2.0	V

(1) Characterized only. Limits are approved by design and are not production tested.

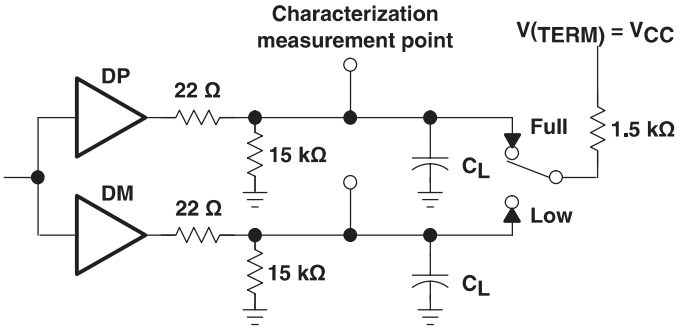
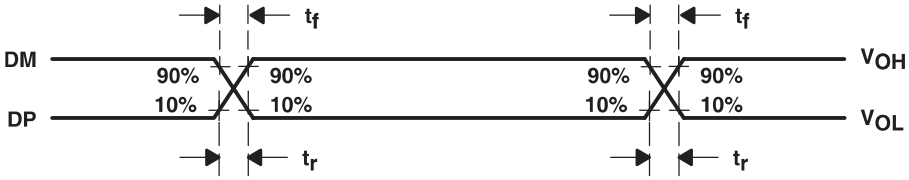


Figure 1. Differential Driver Switching Load



NOTE: The t_r/t_f ratio is measured as $t_{r(DP)}/t_{f(DM)}$ and $t_{r(DM)}/t_{f(DP)}$ at each crossover point.

Figure 2. Differential Driver Timing Waveforms

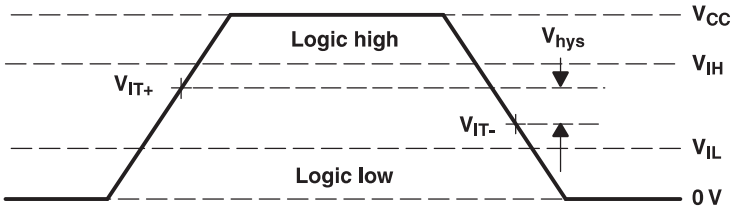


Figure 3. Single-Ended Receiver Input Signal Parameter Definitions

Typical Application (continued)

9.2.1 Design Requirements

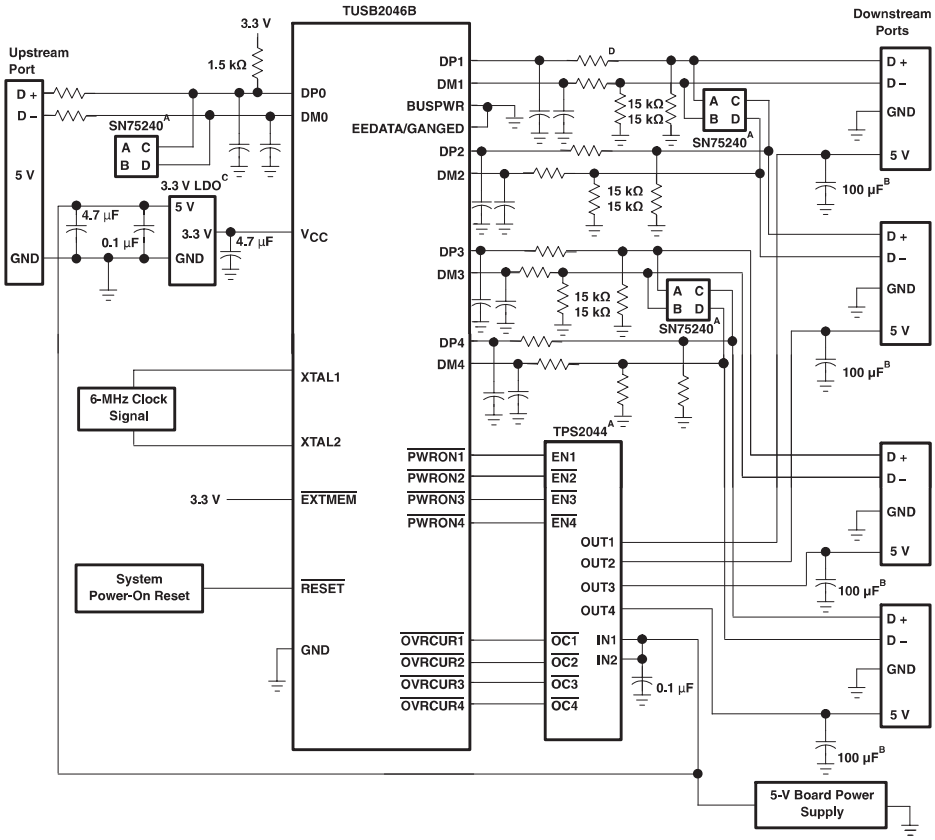
For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

DESIGN PARAMETERS	VALUE
VCC Supply	3.3-V
Downstream Ports	4
Power Management	Individual-Port
Clock Source	6-MHz Crystal
External EEPROM	No
Power Source Mode	Self-Powered

9.2.2 Detailed Design Procedure

In a self-powered configuration, the TUSB2046x can be implemented for individual-port power management when used with the TPS2044 because it is capable of supplying 500 mA of current to each downstream port and can provide current limiting on a per-port basis. When the hub detects a fault on a downstream port, power is removed from only the port with the fault and the remaining ports continue to operate normally. Self-powered hubs are required to implement overcurrent protection and report overcurrent conditions. The SN75240 transient suppressors reduce inrush current and voltage spikes on the data lines.



NOTES: A. TPS2044, TPS2042, and SN75240 are Texas Instruments devices. Two TPS2042 devices can be substituted for the TPS2044. The $\overline{OCn}$ outputs of the TPS204n are open drain. A 10-kΩ pullup is recommended.
B. 120 µF per hub is the minimum required per the USB specification. However, TI recommends a 100-µF, low ESR, tantalum capacitor per port for immunity to voltage droop.
C. LDO is a 5-V-to-3.3-V voltage regulator
D. All USB DP, DM signal pairs require series resistors of approximately 27Ω to ensure proper termination. An optional filter capacitor of about 22 pF is recommended for EMI suppression. This capacitor, if used, must be placed between the hub terminal and the series resistor, as per section 7.1.6 of the USB specification.

Figure 11. TUSB2046x Self-Powered Hub, Individual-Port Power-Management Application