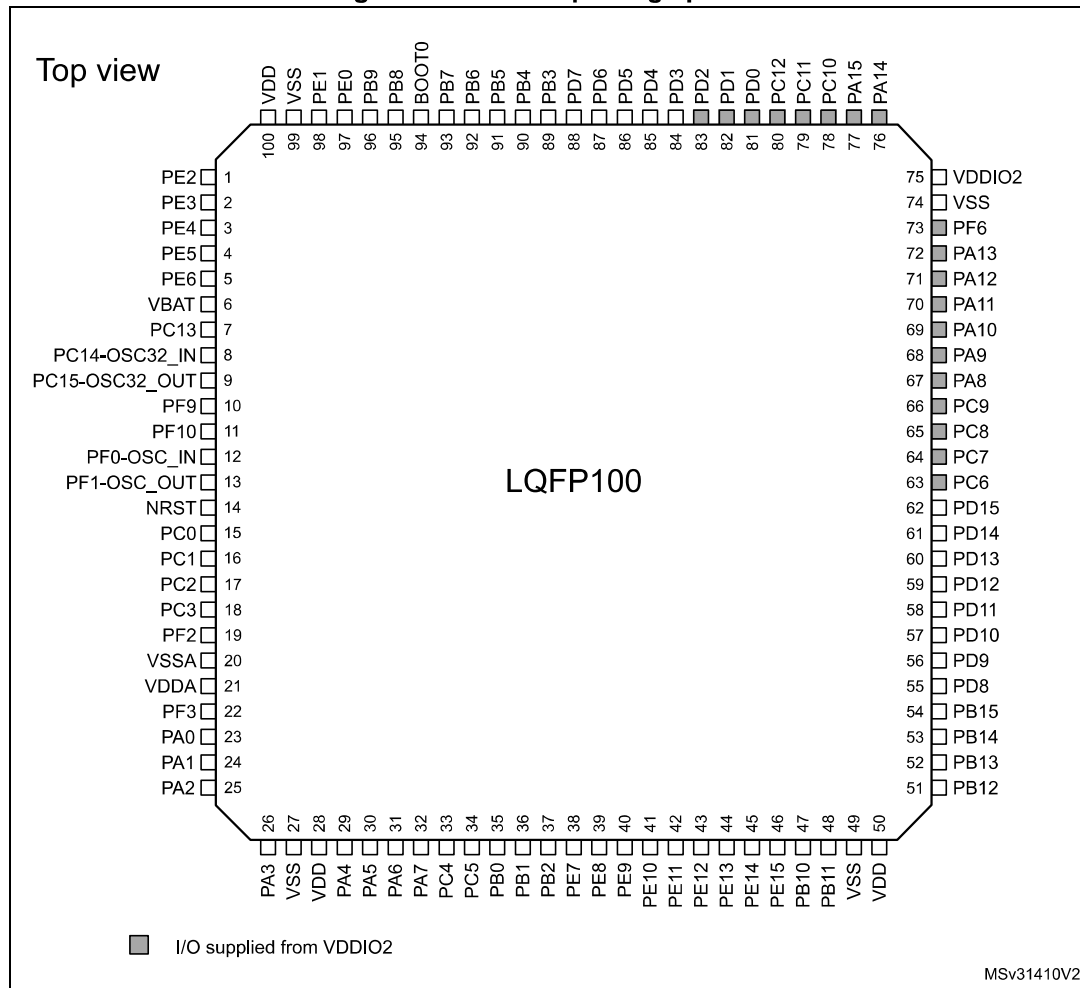


Figure 5. LQFP100 package pinout



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 21: Voltage characteristics](#), [Table 22: Current characteristics](#) and [Table 23: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 21. Voltage characteristics⁽¹⁾

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage	- 0.3	4.0	V
$V_{DDIO2}-V_{SS}$	External I/O supply voltage	- 0.3	4.0	V
$V_{DDA}-V_{SS}$	External analog supply voltage	- 0.3	4.0	V
$V_{DD}-V_{DDA}$	Allowed voltage difference for $V_{DD} > V_{DDA}$	-	0.4	V
$V_{BAT}-V_{SS}$	External backup supply voltage	- 0.3	4.0	V
$V_{IN}^{(2)}$	Input voltage on FT and FTf pins	$V_{SS} - 0.3$	$V_{DDIOx} + 4.0^{(3)}$	V
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	V
	BOOT0	0	9.0	V
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	V
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ V_{SSx} - V_{SS} $	Variations between all the different ground pins	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.12: Electrical sensitivity characteristics		-

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 22: Current characteristics](#) for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

6.3 Operating conditions

6.3.1 General operating conditions

Table 24. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
f_{PCLK}	Internal APB clock frequency	-	0	48	
V_{DD}	Standard operating voltage	-	2.0	3.6	V
V_{DDIO2}	I/O supply voltage	Must not be supplied if V_{DD} is not present	1.65	3.6	V
V_{DDA}	Analog operating voltage (ADC and DAC not used)	Must have a potential equal to or higher than V_{DD}	V_{DD}	3.6	V
	Analog operating voltage (ADC and DAC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.65	3.6	V
V_{IN}	I/O input voltage	TC and RST I/O	-0.3	$V_{DDIOx}+0.3$	V
		TTa I/O	-0.3	$V_{DDA}+0.3^{(1)}$	
		FT and FTf I/O	-0.3	$5.5^{(1)}$	
		BOOT0	0	5.5	
P_D	Power dissipation at $T_A = 85\text{ }^{\circ}\text{C}$ for suffix 6 or $T_A = 105\text{ }^{\circ}\text{C}$ for suffix 7 ⁽²⁾	UFBGA100	-	364	mW
		LQFP100	-	476	
		UFBGA64	-	308	
		LQFP64	-	455	
		LQFP48	-	370	
		UFQFPN48	-	625	
		WLCSP49	-	408	
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	-40	85	$^{\circ}\text{C}$
		Low power dissipation ⁽³⁾	-40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	-40	105	$^{\circ}\text{C}$
		Low power dissipation ⁽³⁾	-40	125	
T_J	Junction temperature range	Suffix 6 version	-40	105	$^{\circ}\text{C}$
		Suffix 7 version	-40	125	

- For operation with a voltage higher than $V_{DDIOx} + 0.3\text{ V}$, the internal pull-up resistor must be disabled.
- If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} . See [Section 7.8: Thermal characteristics](#).
- In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see [Section 7.8: Thermal characteristics](#)).

6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 25](#) are derived from tests performed under the ambient temperature condition summarized in [Table 24](#).

Table 25. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	$\mu\text{s/V}$
	V_{DD} fall time rate		20	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		20	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 26](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 26. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{POR/PDR}^{(1)}$	Power on/power down reset threshold	Falling edge ⁽²⁾	1.80	1.88	1.96 ⁽³⁾	V
		Rising edge	1.84 ⁽³⁾	1.92	2.00	V
$V_{PDRhyst}$	PDR hysteresis	-	-	40	-	mV
$t_{RSTTEMPO}^{(4)}$	Reset temporization	-	1.50	2.50	4.50	ms

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD} .
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Table 27. Programmable voltage detector characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD0}	PVD threshold 0	Rising edge	2.1	2.18	2.26	V
		Falling edge	2	2.08	2.16	V
V_{PVD1}	PVD threshold 1	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVD2}	PVD threshold 2	Rising edge	2.28	2.38	2.48	V
		Falling edge	2.18	2.28	2.38	V
V_{PVD3}	PVD threshold 3	Rising edge	2.38	2.48	2.58	V
		Falling edge	2.28	2.38	2.48	V

Table 27. Programmable voltage detector characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD4}	PVD threshold 4	Rising edge	2.47	2.58	2.69	V
		Falling edge	2.37	2.48	2.59	V
V_{PVD5}	PVD threshold 5	Rising edge	2.57	2.68	2.79	V
		Falling edge	2.47	2.58	2.69	V
V_{PVD6}	PVD threshold 6	Rising edge	2.66	2.78	2.9	V
		Falling edge	2.56	2.68	2.8	V
V_{PVD7}	PVD threshold 7	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
$V_{PVDhyst}^{(1)}$	PVD hysteresis	-	-	100	-	mV
$I_{DD(PVD)}$	PVD current consumption	-	-	0.15	0.26 ⁽¹⁾	μ A

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in [Table 28](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 24: General operating conditions](#).

Table 28. Embedded internal reference voltage

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	$-40\text{ }^{\circ}\text{C} < T_A < +105\text{ }^{\circ}\text{C}$	1.2	1.23	1.25	V
t_{START}	ADC_IN17 buffer startup time	-	-	-	10 ⁽¹⁾	μ s
t_{S_refint}	ADC sampling time when reading the internal reference voltage	-	4 ⁽¹⁾	-	-	μ s
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	$V_{DDA} = 3\text{ V}$	-	-	10 ⁽¹⁾	mV
T_{Coeff}	Temperature coefficient	-	- 100 ⁽¹⁾	-	100 ⁽¹⁾	ppm/ $^{\circ}\text{C}$

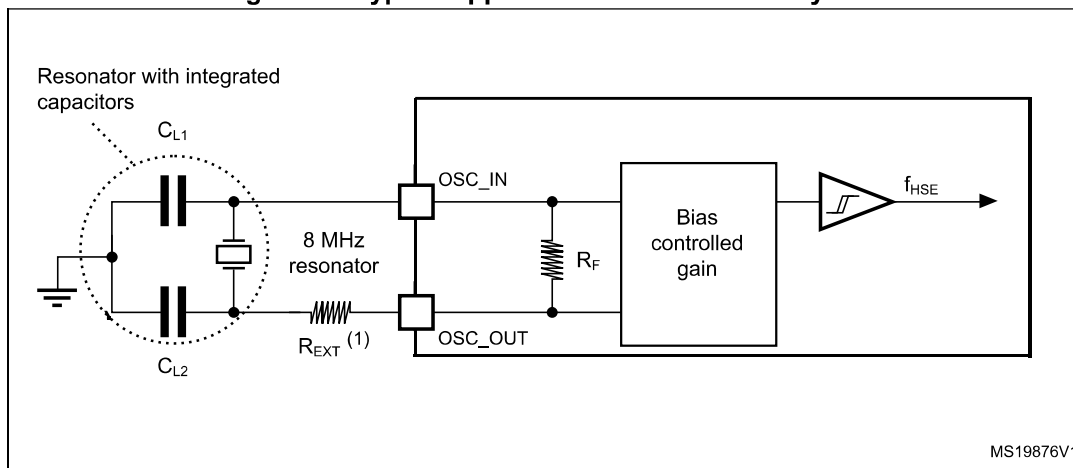
1. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 14: Current consumption measurement scheme](#).

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 40](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 40. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)

Symbol	Parameter	Conditions ⁽¹⁾	Min ⁽²⁾	Typ	Max ⁽²⁾	Unit
I_{DD}	LSE current consumption	low drive capability	-	0.5	0.9	μA
		medium-low drive capability	-	-	1	
		medium-high drive capability	-	-	1.3	
		high drive capability	-	-	1.6	
g_m	Oscillator transconductance	low drive capability	5	-	-	$\mu A/V$
		medium-low drive capability	8	-	-	
		medium-high drive capability	15	-	-	
		high drive capability	25	-	-	
$t_{SU(LSE)}^{(3)}$	Startup time	V_{DDIOX} is stabilized	-	2	-	s

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer