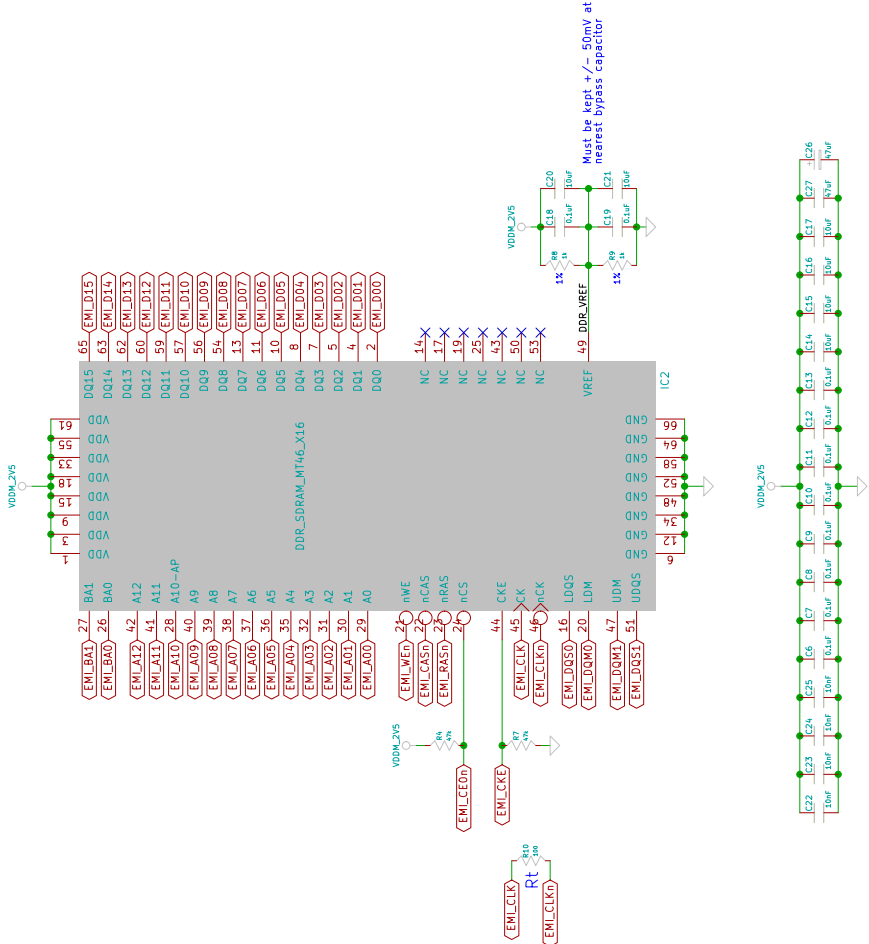


64Mbytes DDR SDRAM



- Notes:
- All capacitors are X5R, 6.3V, 20%, ESR < 300mOhm or better unless otherwise noted
 - All resistors are 5% unless otherwise noted
 - Assuming 2-layer standard 1/16" FR4 (Dk=4.4, Df=0.02) and 7mil-15mil trace-space-drill design
 - Per Micron TN-46-02, need about 7 0.1uF bypass caps but to fake TN-46-14 layout guidelines of GND planes use a lot more and consider external copper foil reference planes
 - Cannot meet DDR routing guidelines (TN-46-14) on 2-layers so just keep all signals as short as possible to limit effects on Signal Integrity (SI) of incorrect inter/intra-pair spacing and characteristic trace impedance
 - On 2-layer boards impedance of the lines is large so termination resistors should be used per TN-46-06.
 - However, all the traces are < 0.8" long and therefore have an electrical length of <8deg at 200MHz.
 - Also, most signals have only one via. Only UDQS (EMI_DQS1) has three vias. Since there is very little room anyway, do not use termination resistors.
 - Only using one DDR device so should not require Rt and cannot fit it near i.MX233 IC anyway
 - For additional design and layout notes see TN-46-11
 - TN AppNotes are available at www.micron.com

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Id: 3/8