Table 1: Summary of recent Intel x86 ISA extensions

		Year of		Instructions		Other ISA changes
Extension		spec	launch	new	chg.	(excl. feature test bits, XSAVE/VMCS context)
SMEP	Block kernel exec. of user pg.	2011	2012	0	0	
RDRAND	Hardware random numbers	2011	2012	1	0	
FSGSBASE	FS/GS access instructions	2011	2012	4	0	
AVX2	256-bit vector ops.	2011	2013	30	0	wider vector registers
INVPCID	Tagged TLB invalidation	2011	2013	1	0	
VMFUNC	VM optimisations	2011	2013	1	0	
TSX	Transactional mem.	2012	2013[a]	4	0	2 new instr. prefixes, transaction aborts
ADX	Arbitrary-precision arithmetic	2012	2014	2	0	
RDSEED	Hardware random numbers	2012	2014	1	0	
PREFETCHW	Prefetch memory for write	2012	2014	1	0	
SMAP	Block kernel access to user pg.	2012	2014	2	0	
CAT	Cache partitioning	2013	2014	0	0	new model-specific registers
CLFLUSHOPT	Optimised cache flush	2013	2015	1	0	
XSAVEC/XSAVES/XRSTORS	Context switch	2014	2015	3	0	
MPX	Bounds checking	2013	2015	8	4	new instr. prefix, 7 new regs., bound table
SGX1	Secure enclaves	2013	2015	18	2	mem. access rights, exceptions, . . . (see §3)
PT	Processor trace	2013	2015	1	0	9 new model-specific registers, trace buffer
SHA	SHA crypto accel.	2013	2016	7	0	
CLWB	Cache line write-back	2013		1	0	
AVX-512	512-bit vector ops.	2013/14		129	0	wider vector registers
SGX2	Enclave dynamic mem. mgmt.	2014		8	0	
MPK	Protection keys for user-mode	2015		2	0	new register, alters page table format
CET [21]	Code-reuse attack defences	2016		10	9	control transfers, new exception, pg. table

[a] TSX launched with "Haswell" in 2013 but was later disabled due to a bug. "Broadwell" CPUs with the bug fix shipped in late 2014.

part, ignore such changes. Vector extensions (MMX, SSE, and AVX) added data processing instructions, and sometimes widened vector registers, but didn't substantially change systems interfaces. With the notable exception of 64-bit mode and virtualisation extensions, OS developers on x86 were occasionally given tweaks to improve performance (e.g., fast system calls) or correct glaring shortcomings (e.g., [redacted]) but otherwise ignored [29]. Even 64-bit mode didn't substantially increase architectural complexity—registers were added and widened and the page table format changed, but there were only a handful of new instructions. Indeed, some features were effectively removed: segmentation, task switching, and 16-bit modes.

But this has changed. Figure 1 plots the transistor count of Intel x86 CPU implementations (on a log scale), as well as the number of words in the Intel architecture software developer's manual (on a linear scale). Transistor counts were sourced from Wikipedia [40]; manuals from various sources were counted using `pdftotext|wc`. The two data sets are not comparable, but some trends are evident. First, we see Moore's Law; the recently-announced slowdown in Intel's cadence [36] does not yet appear, and aside from a recent 22-core Xeon, Intel has stopped publicising transistor counts. Second is the steady growth, and recent 2015–2016 jump in the general complexity of x86. [redacted], and dwarfs even 64-bit mode and virtual-machine extensions (both added in 2007).

Table 1 summarises x86 ISA extensions specified and implemented by Intel since the 2012 launch of "Ivy Bridge" CPUs. For each extension we report the year of the first public specification, year of first CPU implementation, number of new instructions, number of instructions whose behaviour was non-trivially changed, and any other significant ISA changes. Prior to 2015, the most complex additions were the AVX2 vector extensions and TSX transactional memory, both introduced with 2013's "Haswell" microarchitecture. TSX was evidently a complex feature to implement—the first implementation turned out to be buggy, and was later disabled via a microcode patch—but had relatively low ISA-level complexity, with only 4 new instructions. Other pre-Skylake extensions were minor, adding single instructions or tweaking protection (e.g., the SMEP/SMAP features).

However, Skylake introduces substantial complexity, including MPX bounds-checking instructions and registers, the processor trace (PT) feature, and SGX enclaves. In total, it adds 31 instructions and a raft of associated changes: new registers, a new instruction prefix, many new processor-level data structures, changes to page ac-