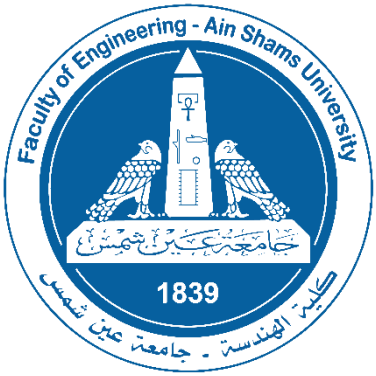
Project 1

ATM Banking System



CSE312– Electronic Design Automation

Faculty of Engineering, Ain-Shams University

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1. Introduction

ATM module implemented in Verilog. It's a state machine that simulates the operation of an ATM.

1.1 Inputs

The system takes several inputs including language selection, service type (deposit, withdraw, check balance), amount of money to deposit or withdraw, card number, PIN, and a flag indicating if another service is required.

1.2 Outputs

The system outputs a flag indicating if it's in operation, the current balance, and a flag indicating if the operation is taking too long.

1.3 States

The system has several states including idle, language selection, PIN input, deposit, withdraw, service selection, balance check, and another service selection. The system transitions between these states based on the inputs and the current state.

1.4 Operation

The system starts in the idle state. When a card number is input, it transitions to the language selection state. After language selection, it moves to the PIN input state. If the correct PIN is entered, it moves to the service selection state. Depending on the service selected, it moves to the deposit, withdraw, or balance check state. After completing a service, it can either return to the service selection state for another service or return to the idle state.

1.5 Timers

The system includes a timer that increments on each clock cycle. If the system stays in the same state for too long (indicated by the timer reaching a certain value), it transitions back to the idle state and resets the inputs.

1.6 Registers

The system uses registers to store the current state, next state, and inputs. The registers are updated on the positive edge of the clock for state transitions and on the negative edge of the clock for input updates.

1.7 Balance Updates

In the deposit state, the balance is increased by the deposit amount. In the withdraw state, the balance is decreased by the withdraw amount if it is less than or equal to the current balance. The balance is also output in the balance check state.

2. Design

2.1 State Diagram

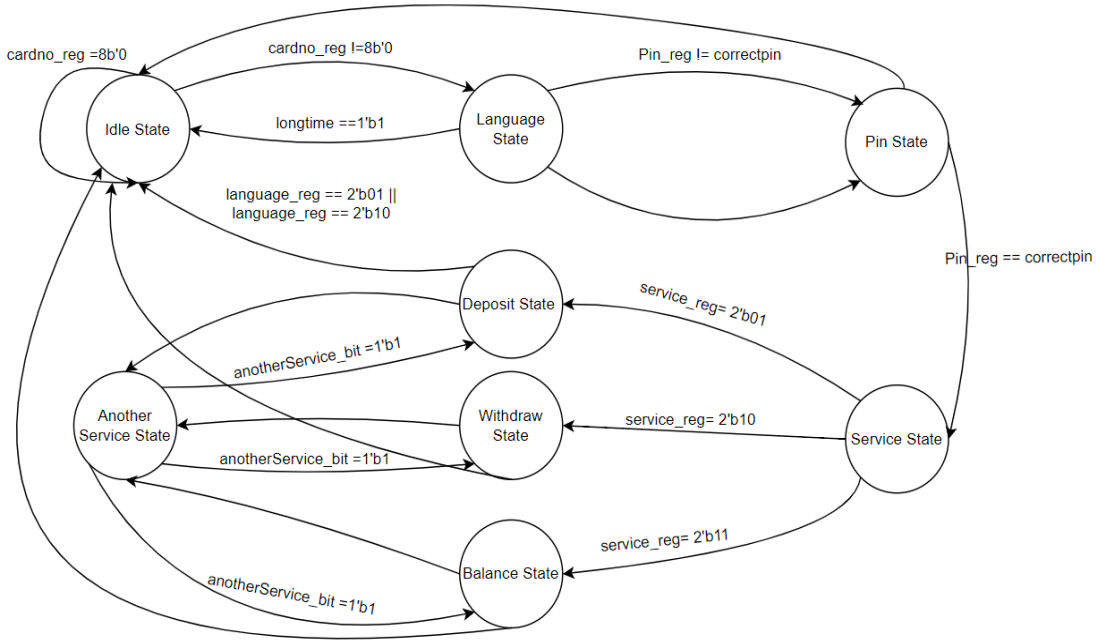

Figure 1 State Diagram (Visio)

2.2 State Table

Table 1 State Table

Current State	Card Number	Language Selection	Entered PIN	Correct PIN	Service Selection	Valid Deposit Amount	Valid Withdrawal Amount	Another Service Request	Next State	
Idle (0000)	cardno_reg								**Language (0001)**	**Idle (0000)**
Language (0001)		language_reg							**PIN (0010)**	
PIN (0010)			pin_reg	correctPin					**Service (0011)**	
Service (0011)					service_reg				**Corresponding State**	
Deposit (0100)						amount_reg			**Another Service (0101)**	
Withdraw (1000)							amount_reg		**Another Service (0101)**	
Balance (0110)									**Another Service (0101)**	
Another Service (0101)								anotherServiceBit_reg	**Service (0011)**	

3. Verification:

3.1 Verification plan

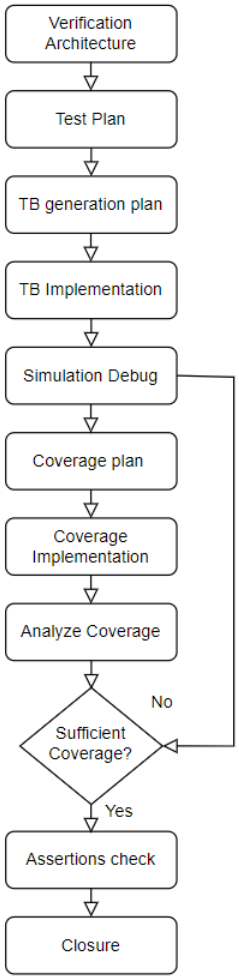

Figure 2 Verification Plan

3.2 Verification result

3.2.1 Coverage of ATMmodule

Branch Coverage: **Overall** Branch Coverage: 100.00%

```
================================================================================
=== File: ATMmodule.v
================================================================================
Branch Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Branches                        36        36         0   100.00%
```

Condition Coverage:

```
Condition Coverage:
    Enabled Coverage              Bins   Covered    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Conditions                      8         8         0   100.00%
```

Overall Condition Coverage: 100.00%

Covered Conditions: 8

Missed Conditions: 0

Statement Coverage: Overall Statement Coverage: 100.00%

```
Statement Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Statements                      57        57         0   100.00%
```

Toggle Coverage:

```
Toggle Coverage:
    Enabled Coverage              Bins      Hits    Misses  Coverage
    ----------------              ----      ----    ------  --------
    Toggles                        174       174         0   100.00%
```

Overall Toggle Coverage: 100.00%