<https://www.youtube.com/watch?v=CsnZ9K0fPl8>

<https://stackoverflow.com/questions/25607124/test-bench-for-writing-verilog-output-to-a-text-file>

<https://www.accellera.org/about>

code must be synthesizable...at RTL level

don’t want RTL code that can’t be targeted at ASIC or FPGA level

LET YOSIS’s ABC tell you if it can map

should have a net list/cell library or VTR 7.0 [should be better]

has logic synthesis on front end and place and route on back end

also uses recommended architecture

\*ODIN doesn’t support the new port decleration

best to make sure it works on both

module TBencrypt;

reg [7:0] a;

initial

begin

a = 8'b01000001;

$display ("%s" , a);

#10 $finish;

end

endmodule

`timescale 1ns / 100ps // unit in ns....#1 is a 1ns delay