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# Welcome to 3Ts The tutorial will start on time

## Everyone is on mute, but feel free to send questions using the chat window.

2022-05-31

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# The 3 Tees Agenda

- Short technical sessions – up to 20min
- DC Measurements in patterns
  - Guest speaker Carl Elmen
- Q&A
- You can send questions throughout the meeting using chat

# DC Measurements in Patterns

## The Motivation and challenge

- Inserting DC measurements into patterns
  - Very common usage, IDDQ, supply currents
  - Often a manual process done directly on the tester
    - Splitting patterns,  hard to automate
    - Using tester specific frameworks, SmartRDI, in-house tooling, generate DC events inside testmethod.
    - Have to compile, manage first run, tester generates lots of small patterns that are difficult to manage with version control
    - New patterns -  repeat the process

## Solution: STIL IEEE-1450.2 + ATEGen

- STIL standard extensions allows adding DC specs and measurements directly in the STIL file
  - Patterns can be processed by software ***outside*** of the tester environment
  - Advantages:
    - Same pattern source for multiple tester platforms
    - DC measurements are inserted "upstream", i.e. before conversion
    - Patterns with DC code works "out of the box" - no patching in features on the tester.
  - Uses existing level and timing specs

# DC Measurements in Patterns

- Example STIL File
- Need to include DCLevels 2002;

```
// Stil header DC Levels need to be included
STIL 1.0 {
  Design 2005;
  DCLevels 2002;
}

// Pin definitions
Signals {
  clk In;     // Digital input
  d1 In;      // Digital input
  VDD Supply;  // Power Supply (DPS) pin
}
```

- Define a minimal pin list, two digital pins and one supply
- Define DC and timing specs

```
  Spec all_specs {
    Category all_cats {
      per1 = '100ns';
      vdd_low = '1.5V';
      vdds_low = '2.7V';
      vdd_hi = '1.8V';
      vdds_hi = '3.3V';
      iddmax = '100mA';
      vih_hi = '3.3V';
      vil_hl = '0.0V';
      custom_vdd_low = 'vdd_low + 0.1V' ;

    }
  }
```

# DC Measurements in Patterns

- 93kDynamicDC_Events defines the test points
- Values can be used directly
- Use of defined specs also allowed

```
// Definition of the DC measurements
 NameMaps "93kDynamicDC_Events" {
  AllNames {
      VF_vdd_3p3V     "signal=VDD, force=voltage, value = 3.3";
      VF_vdd_low     "signal=VDD, force=voltage, value =LEV:vdd_low";
      VF_vdd_hi     "signal=VDD, force=voltage, value =LEV:vdd_hi";
      IM_idd     "signal=VDD, measure=current, samples=16,  limitmode=on,  limitLow=0.2, limitHigh=LEV:iddmax";
  }
}
```

# DC Measurements in Patterns

- “name” : IddqTestPoint

links the definition of a DC measurement with a place in the pattern.

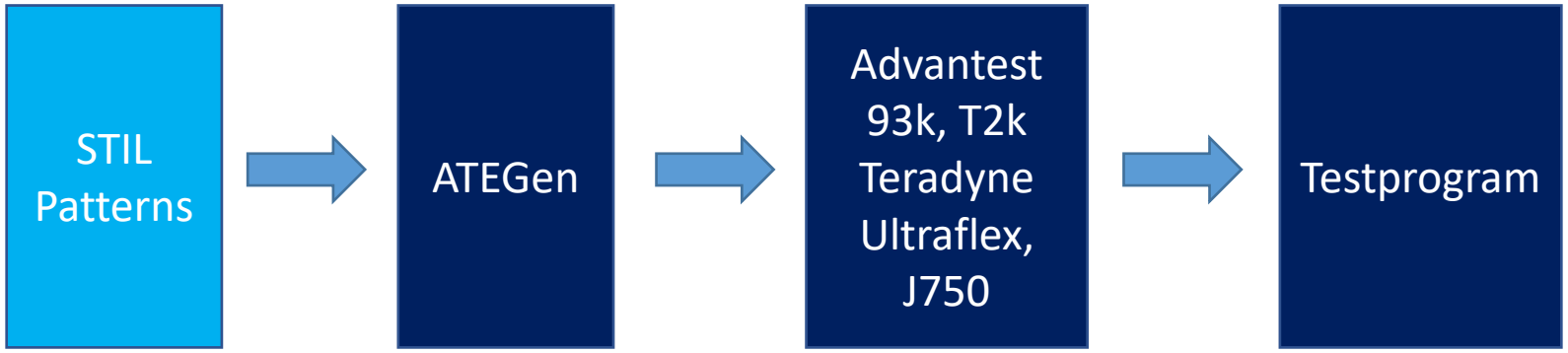
You will need to manage settling time yourself (Loop)

```
V { d1 =1;}
V { d1 =0;}
"<DC_EVENT_1>VF_vdd_3p3V":IddqTestPoint;
V { d1 =0;}
V { d1 =1;}
```

```
V { d1 =0;}
"<DC_EVENT_1>VF_vdd_3p3V":IddqTestPoint;
V { d1 =0;}
V { d1 =0; LP:=8789;}
Loop LP { V { Ann {* Settling time*}}}
V { d1 =1;}
```

# DC Measurements in Patterns

## Conversion flow



# Live Demo

- Convert a STIL file with DC measurements to Advantest 93k
  - Insertion of test points
  - Using specs
  - View result

# Links

- Demo program
  - https://github.com/carelmen/stil_with_dc
- ATEGen / TDL
  - https://www.testinsight.com/tdl-test-pattern-conversion/

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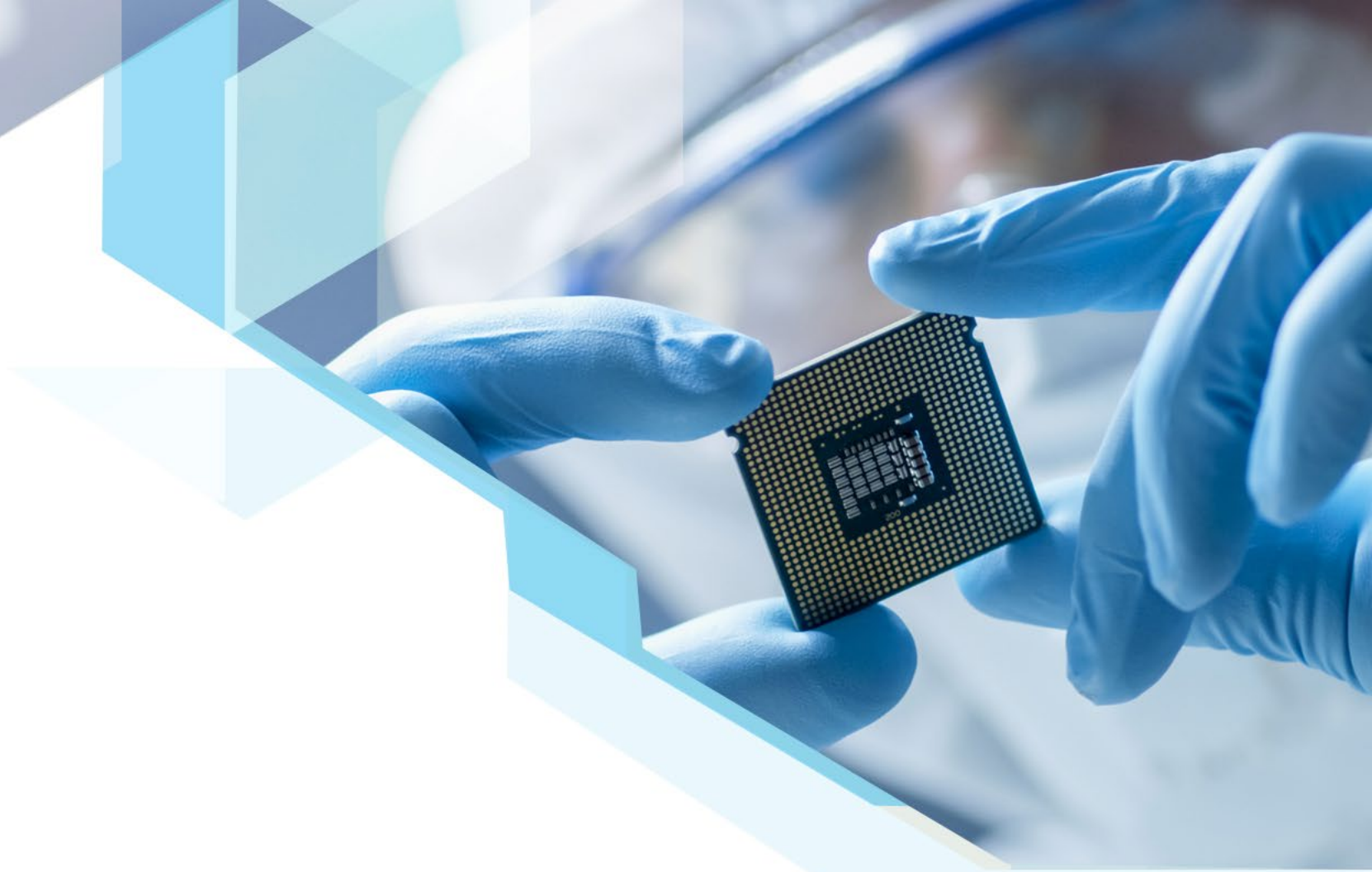
# Thank You



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