



Oregon Institute of Technology

CST456 Embedded System Testing

Midterm

In this homework you are going to write a UVM based testbench for your FSM sequence detector, you designed for HW1. If you remember FSM sequence detector has the following properties: one-input one-output sequence detector that produces an output value 1 every time the sequences 1100 or 1011 is detected and an output value 0 at all other times. Overlapping sequences are accepted; for example, if the input sequence is **11110000101101100** then the corresponding output sequence is **00000100000100101**. FSM sequence detector **must be mealy type** and It must have the following port structure:

```
module duv (input logic clk,  
            input logic reset,  
            input logic inp,  
            output logic outp );
```

Under source directory (SRC) you will see the following files:

```
02/15/2024 11:04 PM <DIR> .  
02/15/2024 11:04 PM <DIR> ..  
02/14/2024 05:51 PM      773 agent.sv  
02/15/2024 10:47 PM    2,105 base_test.sv  
02/14/2024 05:47 PM    1,070 driver.sv  
02/14/2024 06:10 PM    2,383 duv-org.sv  
02/15/2024 11:39 PM    1,265 duv.sv  
02/14/2024 05:52 PM      856 env.sv  
02/14/2024 05:44 PM      729 gen_item_seq.sv  
02/14/2024 05:53 PM      267 interface.sv  
02/14/2024 05:43 PM      346 item.sv  
02/14/2024 05:48 PM    1,316 monitor.sv  
02/16/2024 12:21 AM    2,287 scoreboard.sv  
02/15/2024 11:47 PM      667 tb.sv  
12 File(s)      14,064 bytes
```

These are the files for reference design. Reference design is a FSM sequence detector. It only detects **1011** and it is a Moore machine. Replace reference duv.sv with your own design and modify the other files to make it work for your design. Do not forget your design can detect two sequences and both sequences must be tested.

After a successful run your UVM report summary should look like as follows:

```

--- UVM Report Summary ---

** Report counts by severity
UVM_INFO : 541
UVM_WARNING : 0
UVM_ERROR : 0
UVM_FATAL : 0
** Report counts by id
[RNTST] 1
[SCBD] 536
[SEQ] 1
[TEST_DONE] 1
[UVM/COMP/NAMECHECK] 1
[UVM/RELNOTES] 1

```

Also configure the UVM info to have the following response after a sequence detection(1011 or 1100):

```

uvm_test_top.e0.sb0 [SCBD] Pattern found to match
uvm_test_top.e0.sb0 [SCBD] PASS ! out=1 exp=1

```

Note: In your simulation use **Vivado** in command line mode. Under HW2 directory you will find two more directories: SRC and SIM.

Now open up a command prompt (cmd) and change directory to SIM. In cmd, under SIM directory run the following commands:

```
call C:\Xilinx\Vivado\2023.2\bin\xvlog --sv ../SRC/duv.sv ../SRC/tb.sv -L UVM
```

```
call C:\Xilinx\Vivado\2023.2\bin\xelab -debug typical -top tb -snapshot duv_tb_snapshot
```

```
call C:\Xilinx\Vivado\2023.2\bin\xsim duv_tb_snapshot -R
```

```
call C:\Xilinx\Vivado\2023.2\bin\xsim duv_tb_snapshot --tclbatch xsim_cfg.tcl
```

```
call C:\Xilinx\Vivado\2023.2\bin\xsim --gui duv_tb_snapshot.wdb
```

Submit your Midterm directory