

# 1. Description

## 1.1. Project

Project Name	SDMMC
Board Name	NUCLEO-L4A6ZG
Generated with:	STM32CubeMX 6.5.0
Date	04/04/2022

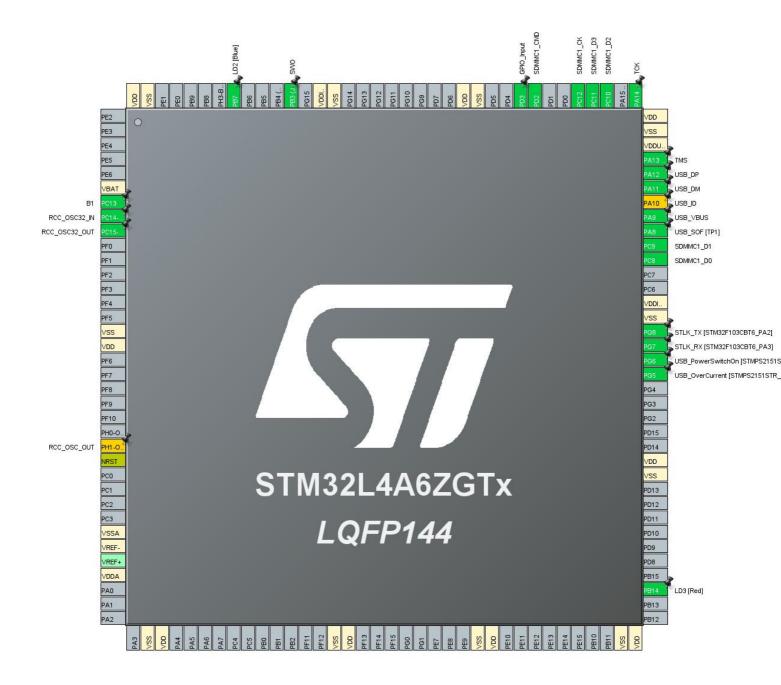
## 1.2. MCU

MCU Series	STM32L4
MCU Line	STM32L4x6
MCU name	STM32L4A6ZGTx
MCU Package	LQFP144
MCU Pin number	144

## 1.3. Core(s) information

Core(s)	Arm Cortex-M4

# 2. Pinout Configuration



# 3. Pins Configuration

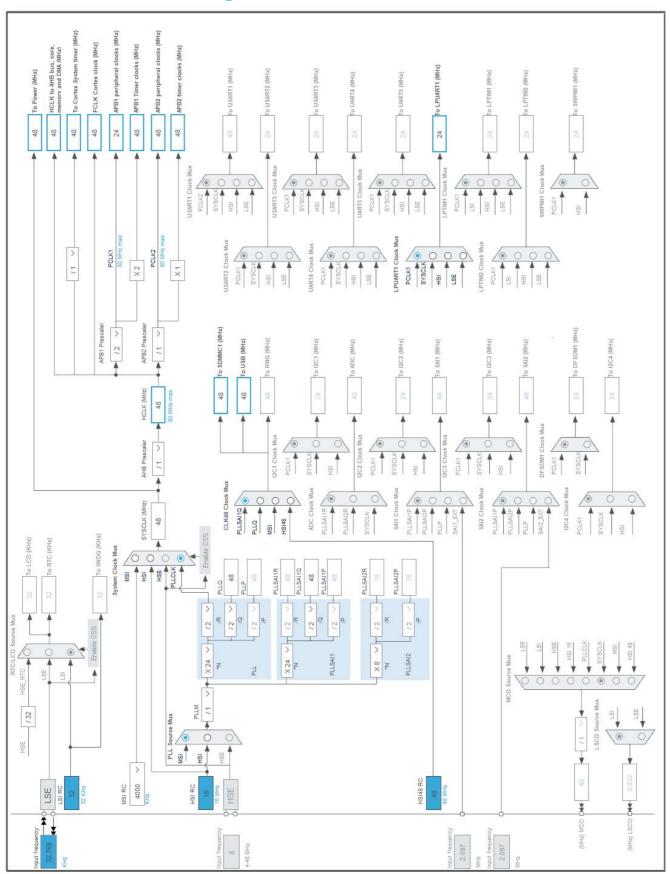
Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP144	(function after		Function(s)	
	reset)			
6	VBAT	Power		
7	PC13	I/O	GPIO_EXTI13	B1
8	PC14-OSC32_IN (PC14)	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT (PC15)	I/O	RCC_OSC32_OUT	
16	VSS	Power		
17	VDD	Power		
24	PH1-OSC_OUT (PH1) *	I/O	RCC_OSC_OUT	
25	NRST	Reset		
30	VSSA	Power		
31	VREF-	Power		
33	VDDA	Power		
38	VSS	Power		
39	VDD	Power		
51	VSS	Power		
52	VDD	Power		
61	VSS	Power		
62	VDD	Power		
71	VSS	Power		
72	VDD	Power		
75	PB14 **	I/O	GPIO_Output	LD3 [Red]
83	VSS	Power		
84	VDD	Power		
90	PG5 **	I/O	GPIO_Input	USB_OverCurrent [STMPS2151STR_FAULT]
91	PG6 **	I/O	GPIO_Output	USB_PowerSwitchOn [STMPS2151STR_EN]
92	PG7	I/O	LPUART1_TX	STLK_RX [STM32F103CBT6_PA3]
93	PG8	I/O	LPUART1_RX	STLK_TX [STM32F103CBT6_PA2]
94	VSS	Power		
95	VDDIO2	Power		
98	PC8	I/O	SDMMC1_D0	
99	PC9	I/O	SDMMC1_D1	
100	PA8	I/O	USB_OTG_FS_SOF	USB_SOF [TP1]
101	PA9	I/O	USB_OTG_FS_VBUS	USB_VBUS

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
102	PA10 *	I/O	USB_OTG_FS_ID	USB_ID
103	PA11	I/O	USB_OTG_FS_DM	USB_DM
104	PA12	I/O	USB_OTG_FS_DP	USB_DP
105	PA13 (JTMS/SWDIO)	I/O	SYS_JTMS-SWDIO	TMS
106	VDDUSB	Power		
107	VSS	Power		
108	VDD	Power		
109	PA14 (JTCK/SWCLK)	I/O	SYS_JTCK-SWCLK	TCK
111	PC10	I/O	SDMMC1_D2	
112	PC11	I/O	SDMMC1_D3	
113	PC12	I/O	SDMMC1_CK	
116	PD2	I/O	SDMMC1_CMD	
117	PD3 **	I/O	GPIO_Input	
120	VSS	Power		
121	VDD	Power		
130	VSS	Power		
131	VDDIO2	Power		
133	PB3 (JTDO/TRACESWO)	I/O	SYS_JTDO-SWO	swo
137	PB7 **	I/O	GPIO_Output	LD2 [Blue]
143	VSS	Power		
144	VDD	Power		

<sup>\*\*</sup> The pin is affected with an I/O function

<sup>\*</sup> The pin is affected with a peripheral function but no peripheral mode is activated

## 4. Clock Tree Configuration



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# 5. Software Project

## 5.1. Project Settings

Name	Value
Project Name	SDMMC
Project Folder	C:\Users\carlk\STM32CubeIDE\workspace_1.8.0\SDMMC
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_L4 V1.17.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x400
Minimum Stack Size	0x800

## 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_LPUART1_UART_Init	LPUART1
4	MX_USB_OTG_FS_PCD_Init	USB_OTG_FS
5	MX_DMA_Init	DMA
6	MX_FATFS_Init	FATFS
7	MX_SDMMC1_SD_Init	SDMMC1

# 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32L4
Line	STM32L4x6
мси	STM32L4A6ZGTx
Datasheet	DS11584_Rev2

### 6.2. Parameter Selection

Temperature	25
Vdd	3.0

## 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

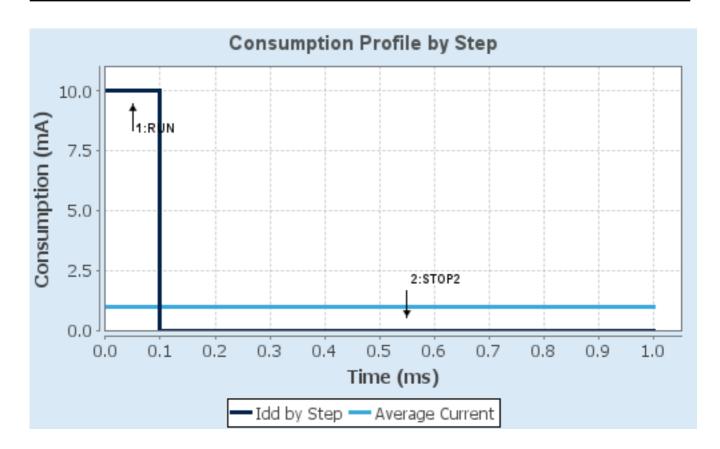
## 6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP2
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	Range1-High	NoRange
Fetch Type	FLASH	n/a
CPU Frequency	80 MHz	0 Hz
Clock Configuration	HSE BYP PLL Flash-ON	ALL CLOCKS OFF
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	10 mA	2.69 µA
Duration	0.1 ms	0.9 ms
DMIPS	100.0	0.0
Ta Max	104.04	105
Category	In DS Table	In DS Table

### 6.5. Results

Sequence Time	1 ms	Average Current	1 mA
Battery Life	4 months, 19	Average DMIPS	100.0 DMIPS
	days, 3 hours		

## 6.6. Chart



## 7. Peripherals and Middlewares Configuration

#### **7.1. LPUART1**

#### **Mode: Asynchronous**

#### 7.1.1. Parameter Settings:

#### **Basic Parameters:**

Baud Rate 115200 \*

Word Length 8 Bits (including Parity) \*

Parity None Stop Bits 1

**Advanced Parameters:** 

Data Direction Receive and Transmit

Single Sample Disable

**Advanced Features:** 

Auto Baudrate Mode Disable TX Pin Active Level Inversion Disable **RX Pin Active Level Inversion** Disable **Data Inversion** Disable TX and RX pins Swapping Disable Overrun Enable DMA on RX Error Enable MSB First Disable

#### 7.2. RCC

#### Low Speed Clock (LSE): Crystal/Ceramic Resonator

#### 7.2.1. Parameter Settings:

#### **System Parameters:**

VDD voltage (V) 3.3
Instruction Cache Enabled
Prefetch Buffer Disabled
Data Cache Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

**RCC Parameters:** 

HSI Calibration Value 64

MSI Calibration Value 0

MSI Auto Calibration Enabled

HSE Startup Timout Value (ms) 100

LSE Startup Timout Value (ms) 5000

LSE Drive Capability

LSE oscillator low drive capability

**Power Parameters:** 

Power Regulator Voltage Scale Power Regulator Voltage Scale 1

#### 7.3. SDMMC1

Mode: SD 4 bits Wide bus

### 7.3.1. Parameter Settings:

#### **SDMMC** parameters:

Clock transition on which the bit capture is made Rising transition

SDMMC Clock divider bypass Disable

SDMMC Clock output enable when the bus is idle 
Disable the power save for the clock

SDMMC hardware flow control

The hardware control flow is enabled \*

SDMMCCLK clock divide factor 0

#### 7.4. SYS

**Debug: Trace Asynchronous Sw** 

**Timebase Source: TIM17** 

7.5. USB\_OTG\_FS

Mode: Device\_Only

Activate\_VBUS: VBUS sensing

mode: Activate\_SOF

7.5.1. Parameter Settings:

Speed Full Speed 12MBit/s

Low powerDisabledBattery chargingEnabledLink Power ManagementDisabledUse dedicated end point 1 interruptDisabledVBUS sensingEnabledSignal start of frameEnabled

#### **7.6. FATFS**

#### mode: SD Card

#### 7.6.1. Set Defines:

Version:

FATFS version R0.12c

**Function Parameters:** 

FS\_READONLY (Read-only mode) Disabled
FS\_MINIMIZE (Minimization level) Disabled

USE\_STRFUNC (String functions) Enabled with LF -> CRLF conversion

USE\_FIND (Find functions) Enabled \*

USE\_MKFS (Make filesystem function)

USE\_FASTSEEK (Fast seek function)

USE\_EXPAND (Use f\_expand function)

USE\_CHMOD (Change attributes function)

Disabled

USE\_LABEL (Volume label functions)

Disabled

USE\_FORWARD (Forward function)

Disabled

**Locale and Namespace Parameters:** 

CODE\_PAGE (Code page on target) Latin 1

USE\_LFN (Use Long Filename) Enabled with dynamic working buffer on the STACK \*

MAX\_LFN (Max Long Filename) 255

LFN\_UNICODE (Enable Unicode) ANSI/OEM STRF\_ENCODE (Character encoding) UTF-8

FS\_RPATH (Relative Path) Enabled with f\_getcwd \*

**Physical Drive Parameters:** 

VOLUMES (Logical drives) 1

MAX\_SS (Maximum Sector Size) 512

MIN\_SS (Minimum Sector Size) 512

MULTI\_PARTITION (Volume partitions feature) Disabled

USE\_TRIM (Erase feature) Disabled

FS\_NOFSINFO (Force full FAT scan) 0

**System Parameters:** 

FS\_TINY (Tiny mode) Disabled
FS\_EXFAT (Support of exFAT file system) Disabled

FS\_NORTC (Timestamp feature) Dynamic timestamp

FS\_REENTRANT (Re-Entrancy)

FS\_TIMEOUT (Timeout ticks)

Disabled

1000

FS\_LOCK (Number of files opened simultaneously)

2

## 7.6.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance SDMMC1
Use dma template Enabled \*
BSP code for SD Generic

## 7.6.3. Platform Settings:

Detect\_SDIO PD3

<sup>\*</sup> User modified value

# 8. System Configuration

## 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
LPUART1	PG7	LPUART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLK_RX [STM32F103CBT6_PA3]
	PG8	LPUART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High	STLK_TX [STM32F103CBT6_PA2]
RCC	PC14- OSC32_IN (PC14)	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15- OSC32_OU T (PC15)	RCC_OSC32_O UT	n/a	n/a	n/a	
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC9	SDMMC1_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC10	SDMMC1_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC11	SDMMC1_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
SYS	PA13 (JTMS/SWDI O)	SYS_JTMS- SWDIO	n/a	n/a	n/a	TMS
	PA14 (JTCK/SWC LK)	SYS_JTCK- SWCLK	n/a	n/a	n/a	тск
	PB3 (JTDO/TRA CESWO)	SYS_JTDO- SWO	n/a	n/a	n/a	SWO
USB_OTG_ FS	PA8	USB_OTG_FS_ SOF	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_SOF [TP1]
	PA9	USB_OTG_FS_ VBUS	Input mode	No pull-up and no pull-down	n/a	USB_VBUS
	PA11	USB_OTG_FS_ DM	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_DM
	PA12	USB_OTG_FS_ DP	Alternate Function Push Pull	No pull-up and no pull-down	Very High	USB_DP
Single Mapped Signals	PH1- OSC_OUT (PH1)	RCC_OSC_OUT	n/a	n/a	n/a	
	PA10	USB_OTG_FS_I D	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	USB_ID

## SDMMC Project Configuration Report

IP	Pin	Signal	GPIO mode	GPIO pull/up pull	Max	User Label
				down	Speed	
GPIO	PC13	GPIO_EXTI13	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	B1
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD3 [Red]
	PG5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OverCurrent [STMPS2151STR_FAULT]
	PG6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_PowerSwitchOn [STMPS2151STR_EN]
	PD3	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LD2 [Blue]

### 8.2. DMA configuration

DMA request	Stream	Direction	Priority
SDMMC1_TX	DMA2_Channel4	Memory To Peripheral	High *
SDMMC1_RX	DMA2_Channel5	Peripheral To Memory	High *

### SDMMC1\_TX: DMA2\_Channel4 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Word \*
Memory Data Width: Word

### SDMMC1\_RX: DMA2\_Channel5 DMA request Settings:

Mode: Normal
Peripheral Increment: Disable
Memory Increment: Enable \*
Peripheral Data Width: Word \*
Memory Data Width: Word

## 8.3. NVIC configuration

## 8.3.1. NVIC

Into wount Table	Fachle	Dragonmention Drievity	Cub Deionita	
Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	15	0	
TIM1 trigger and commutation interrupts and TIM17 global interrupt	true	15	0	
SDMMC1 global interrupt	true	0	0	
DMA2 channel4 global interrupt	true	0	0	
DMA2 channel5 global interrupt	true	0	0	
LPUART1 global interrupt	true	0	0	
PVD/PVM1/PVM2/PVM3/PVM4 interrupts through EXTI lines 16/35/36/37/38		unused		
Flash global interrupt	unused			
RCC global interrupt	unused			
EXTI line[15:10] interrupts	unused			
USB OTG FS global interrupt	unused			
FPU global interrupt	unused			

## 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Prefetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
TIM1 trigger and commutation interrupts and TIM17 global interrupt	false	true	true
SDMMC1 global interrupt	false	true	true

Enabled interrupt Table	Select for init	Generate IRQ	Call HAL handler
	sequence ordering	handler	
DMA2 channel4 global interrupt	false	true	true
DMA2 channel5 global interrupt	false	true	true
LPUART1 global interrupt	false	true	true

<sup>\*</sup> User modified value

# 9. System Views

9.1. Category view

9.1.1. Current



## 10. Docs & Resources

Type Link

Presentations https://www.st.com/resource/en/product\_presentation/stm32-

stm8\_embedded\_software\_solutions.pdf

Presentations https://www.st.com/resource/en/product\_presentation/stm32\_eval-

tools\_portfolio.pdf

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Application Notes https://www.st.com/resource/en/application\_note/an1181-electrostatic-

discharge-sensitivity-measurement-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application\_note/an1709-emc-design-

- guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an2548-using-the-stm32f0f1f3gxlx-series-dma-controller-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an2639-soldering-recommendations-and-package-information-for-leadfree-ecopack-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an2834-how-to-get-the-best-adc-accuracy-in-stm32-microcontrollers-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application\_note/an3154-can-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf
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- stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application\_note/an4616-migrating-from-stm32f401-and-stm32f411-lines-to-stm32l4-series-and-stm32l4-series-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application\_note/an4621-stm32l4-and-stm32l4-ultralowpower-features-overview-stmicroelectronics.pdf

- Application Notes https://www.st.com/resource/en/application\_note/an4629-adc-hardwareoversampling-for-microcontrollers-of-the-stm32-l0-and-l4-seriesstmicroelectronics.pdf
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