Wishbone Block RAM

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1 Specifications

This core creates 32-bit storage RAM on the Wishbone bus by using FPGA Block RAM.

Byte-wide writes are supported. Burst access is not supported.

The typical use case is to provide initial memory for softcore CPUs.

2 Using the core

You should specify the block RAM storage depth, in bytes, by using the `adr_width` parameter.

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