Frequency Agile Monolithic GaN Doherty Power Amplifier

A.M. Mahmoud Mohamed [(1)], S. Boumaiza [(1)], I. Zine-El-Abidine [(2)] and R. Mansour [(1)]

(1) University of Waterloo, Waterloo, ON, N2L 3G1, Canada, +1 (519) 888- 4567

(2) CMC Microsystems Canada, Kingston, ON, K7L 3N6, Canada, +1 (613) 530- 8104

a5mahmou@uwaterloo.ca, sboumaiz@uwaterloo.ca, zine-el-abidine@cmc.ca, rrmansou@uwaterloo.ca

***Abstract* — This paper proposes a monolithic GaN Doherty power amplifier (DPA) capable of efficiently amplifying communication signals located in multiple widely spaced wireless frequency bands. The proposed monolithic DPA incorporates a number of microelectromechanical systems switches which were used to mitigate the variation of the DPA circuit parameters within the operating frequency. A systematic design methodology was used to optimize the size and complexity of the frequency agile DPA thus locating the reconfigurability out of the combining network so that this latter can be kept off-chip. A monolithic DPA was designed and fabricated using the Canadian Photonics Fabrication Centre GaN500 monolithic microwave integrated circuit (MMIC) process (0.5 um gate length) which was operated at 1.7GHz, 2.14GHz and 2.6GHz. The preliminary measurement results demonstrated drain efficiency higher than 50% for power levels up to 6dB back-off from the peak output power.**

***Index Terms* — Reconfigurable Power Amplifiers, Monolithically Integrated Power Amplifiers, Doherty Amplifiers, MEMS RF switches.**

I. Introduction

During the last three decades, wireless communication has progressed from an exclusive voice service to support broadband mobile applications. At present a large spectrum of communication standards are deployed or are in development. These standards involve challenging communication signals scattered over widely spaced frequency bands and characterized by highly varying envelopes. This context has prompted a shift from dedicated to adaptive radio systems to cope with dissimilar signals requirements (e.g. centre frequency, modulation schemes, and average powers) while maintaining competitive performance. This paper focuses on the development of high power amplifiers (PA) which are capable of efficiently amplifying communication signals located in widely spaced communication bands.

Several techniques have been devised to enhance the efficiency of PAs when driven with single band communication signals of high peak to average power ratio (PAPR). Among those techniques, the load modulation based Doherty technique [1] has demonstrated excellent power efficiency and currently is widely adopted for single band base stations. This success prompted the investigation of new approaches for realizing broadband and multi-band Doherty power amplifiers (DPA) [2- 4]. These latter yielded relatively reduced efficiencies compared with single band DPAs, especially when operated in back-off regions. Alternatively, authors in [5] proposed a reconfigurable DPA architecture that allowed for proper load modulation over multiple bands using electronically tunable devices. This architecture was applied to design frequency-agile DPA using packaged Gallium Nitride (GaN) transistors and off the shelf microelectromechanical systems (MEMS) RF switches.

This paper aims to combine the strengths of the GaN transistor and the flexibility of MEMS devices to build a frequency agile, monolithically integrated DPA. The authors begin by describing the design methodology and then provide a detailed description of the realization of the fully integrated GaN MMIC DPA capable of operating over three widely spaced frequencies with enhanced efficiency at 6dB back-off power levels. The GaN MEMS switch that was developed to enable the full integration of the DPA is also described.

II. Frequency-Agile DPA Design Methodology

Fig. 1 demonstrates a generic DPA schematic, which includes main and auxiliary transistors, input and output matching networks (IMN and OMN), and two quarter wavelength inverters with characteristic impedances R_T and Z_{T1}. The main transistor is usually Class AB biased and matched to ensure peak efficiency at a predetermined input voltage level of $V_{in,\max}/p$. The parameter p is directly related to the PAPR of the input signal. The auxiliary transistor is biased at Class C and is required to start conducting at the input voltage level $V_{in,\max}/p$. For proper Doherty operation, the combining network parameters are given by

$$R_T = R_{opt}, \qquad Z_{T1} = \frac{R_{opt}}{\sqrt{p}} \tag{1}$$

where R_{opt} denotes the optimum load impedance for the main transistor at peak input power.

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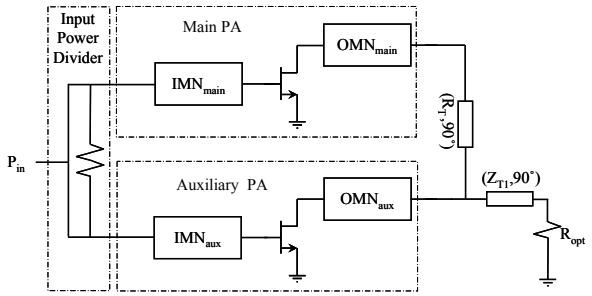


Fig. 1. Generic DPA schematic

In Fig. 1, the change of the electrical lengths, θ, of the quarter wavelength impedance inverters with frequency directly results in improper load modulation and consequently efficiency deterioration. In addition, the combining network parameters R_T and Z_{T1} change with the PAPR of the input signal. Hence, to ensure proper load modulation when the input signal carrier frequency and PAPR change, the combining network lengths and characteristic impedances must be adjusted. Discrete electronically tunable devices such as varactors and RF MEMS switches were used in [6, 7] to maintain high performance over different operating conditions (e.g., frequency, input power level). Motivated by the need for monolithically integrated DPAs using GaN technology, the current work opted to use MEMS RF switches to adjust the parameters of the combining network to maintain proper load modulation at widely spaced frequencies. MEMS tunable devices were favoured for this application due to their ultra-linearity, low losses and amenability to integration on commercially available GaN MMIC process as demonstrated in [8]. Attention was

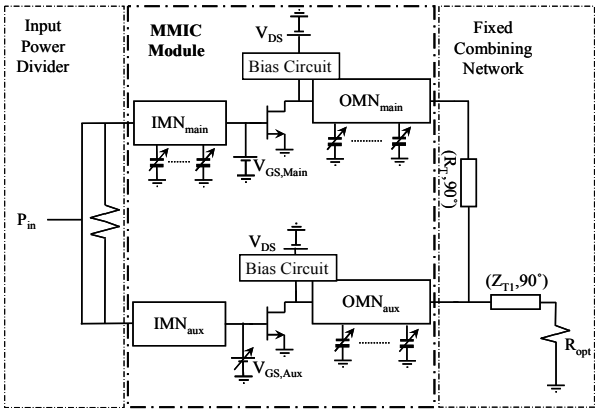


Fig. 3. The proposed reconfigurable DPA architecture

given in this work to minimizing both the size and sources of loss therefore a fixed combining network located off chip was used. The dimensions of the transmission lines of the combining network were chosen to satisfy the load modulation condition, Eq. 1, at a given reference frequency. To satisfy the load modulation condition at frequencies other than the reference frequency, two reconfigurable OMNs were added to the two paths in the DPA circuit. The reconfigurable OMNs were carefully designed so that when combined with the fixed combining network, the resulting network satisfied the load modulation condition at each targeted frequency as shown in Fig. 2. The resulting frequency agile DPA architecture is depicted in Fig. 3. It includes the two typical transistors, two reconfigurable OMNs in the main and auxiliary paths, a reconfigurable IMN in the main path (to ensure phase balance between the two paths) and finally a fixed IMN.

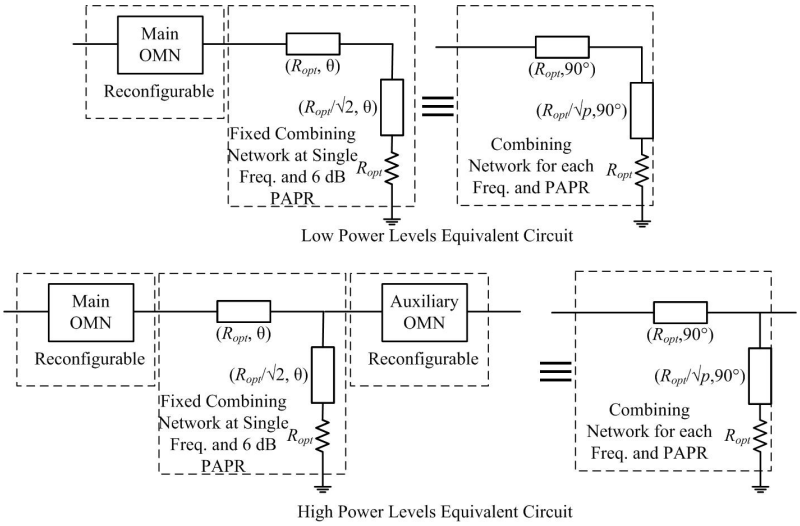


Fig. 2. The equivalent combining network circuitry

IV. Frequency-Agile GaN MMIC DPA Design

The Canadian Photonics Fabrication Centre (CPFC) GaN500 MMIC process (0.5 um gate length), described in detail in [8], was used to implement the MMIC module in Fig. 3. The input power divider and the fixed combining networks were implemented off chip using a printed circuit board to minimize the overall size, and consequently the cost, and to limit the additional losses associated with the integrated passives. The DPA was designed to achieve a second efficiency at 6dB back-off, $p = 6dB$, and to operate at 1.7, 2.14 and 2.6GHz.

A. High Power Monolithic RF MEMS Switch

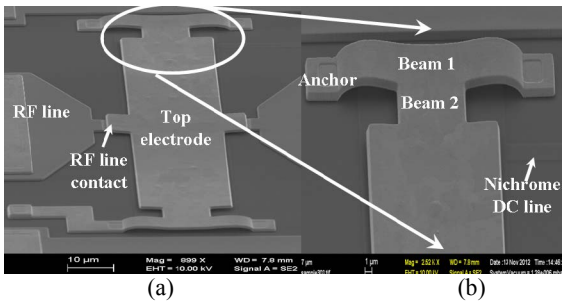
The main challenge in designing a frequency-agile monolithically integrated DPA was the integration of tunable devices on the selected MMIC process. In fact, the MEMS switch was designed by exploiting the air gap layer in the GaN process while respecting the process design rules. The switch length and width were limited to 100 and 20um respectively. In addition, special attention was given to lower the needed actuation voltage. A recess was placed in the top plate, resulting in beams 1 and 2, to reduce the stiffness of the bridge. The beam dimensions were optimized so that the actuation voltage value was higher than the expected RF voltage swing (actuation voltage > $3V_{DD}$). In this design, the switch actuation voltage was equal to 77.5V and V_{DD}=24V. Fig. 4 shows a scanning electron microscope (SEM) image of the designed GaN MEMS switch. As can be seen in Fig. 5, the switch insertion loss did not exceed 0.4dB whereas; the return loss and the isolation were higher than 18 and 15dB respectively. The monolithic GaN MEMS switch was tested for power handling as well as yield. It handled 3.6W RF power under hot switching conditions with a third order intercept point (IIP3) of more than 68dBm.

B. DPA MMIC Module Design

The successful realization of the GaN MEMS switch using the GaN MMIC process paved the way for the implementation of the frequency agile DPA on the same process. The design of the integrated DPA was carried out using the switch model extracted from measurement data and the large signal models of the transistors provided in the GaN process design kit.

The main and auxiliary transistors were composed of 4 and 8 fingers each with widths of 300um. The sizes were selected based on the target of 5W peak output power. The drain supply voltage was set to be equal to 24V. The gate biasing voltages were set to 2.8V and 5.3V, for the main and auxiliary transistors, respectively so proper classes of operation are obtained.

Load pull analysis was conducted on both transistors to identify the optimum impedances that need to be presented to the input and output of both transistors at



(a) (b)

Fig. 4. (a) SEM of a GaN integrated switch (b) Switch design (only part of the top plate is shown)

Fig. 5. Switch extracted and measured insertion and return losses and isolation

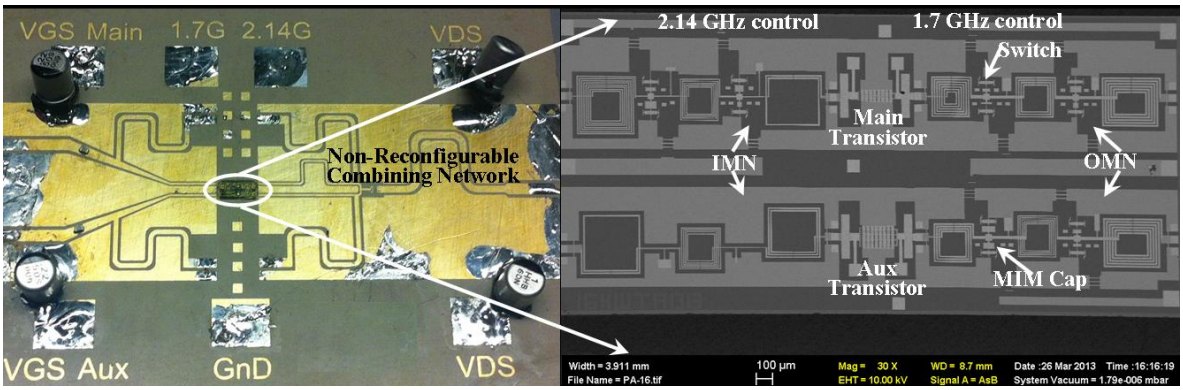


Fig. 6. Frequency agile monolithic GaN DPA

Fig. 7. The measured drain efficiency at 1.7GHz, 2.14GHz and 2.6GHz

different frequencies and power levels. Those impedances were used in the synthesis of the reconfigurable OMNs and IMNs. The reconfigurable matching network design employed MMIC inductors with enhanced insertion loss, supported by the process, in the main signal line rather than distributed elements in order to reduce chip size and cost. Each inductor was capacitively loaded by two shunt MEMS switches connected to fixed Metal-Insulator-Metal capacitors to shift the DPA centre frequency from the initial value of 2.6GHz to one of the other two bands, 1.7 or 2.14GHz. Simulations proved that six pairs of MEMS switches, two in each OMN and two in the main transistor IMN, were needed to satisfy the conditions required for the DPA to enhance the efficiency in the last 6dB back off at 1.7, 2.14 and 2.6GHz. The non-tunable distributed element impedance inverters were fabricated off-chip. Fig 6 shows a picture of the frequency agile demonstrator including the MMIC module attached to the off chip fixed combining network.

C. MMIC DPA Measurement Results

The measured gain and peak output power of the DPA were higher than 10dB and 36dBm, respectively, at the three frequencies. As can be seen in Fig 7, the designed demonstrator satisfied Doherty load modulation requirements in the three operating frequencies (deduced from the significant efficiency improvement in the back off region). In fact, drain efficiency in excess of 50% was maintained in the last 6dB power range for the three operating frequencies.

V. CONCLUSION

A monolithically integrated reconfigurable GaN DPA capable of efficiently amplifying signals with wide spread centre frequencies, based on a systematic design methodology, was presented. The proposed methodology helped with optimizing the size and cost of the MMIC module of the frequency agile DPA, by substituting the required tunable combining network with two integrated matching networks and one off-chip fixed combining network. An integrated MEMS switch is designed using the same GaN process to implement the integrated tunable matching networks at a minimum performance overhead. The 37dBm DPA demonstrator operated at the three desired centre frequencies and confirmed drain efficiencies at 6dB back-off of more than 53% at all the targeted bands with a small signal gain of about 10dB.

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