Lab 3 Report
ECE 532

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Introduction

In this lab a 2.4GHz LNA is designed, simulated and a PCB layout is produced. The network that provides a DC bias is analyzed to see how component variability affects bias. Then a comparison of the S-Parameter files from the manufacturer is compared to the non-linear device model in ADS. Using the LNA design guide in ADS, an LNA is designed and stabilized using stabilizing resistors, and finally a layout is produced.

DC Bias Network

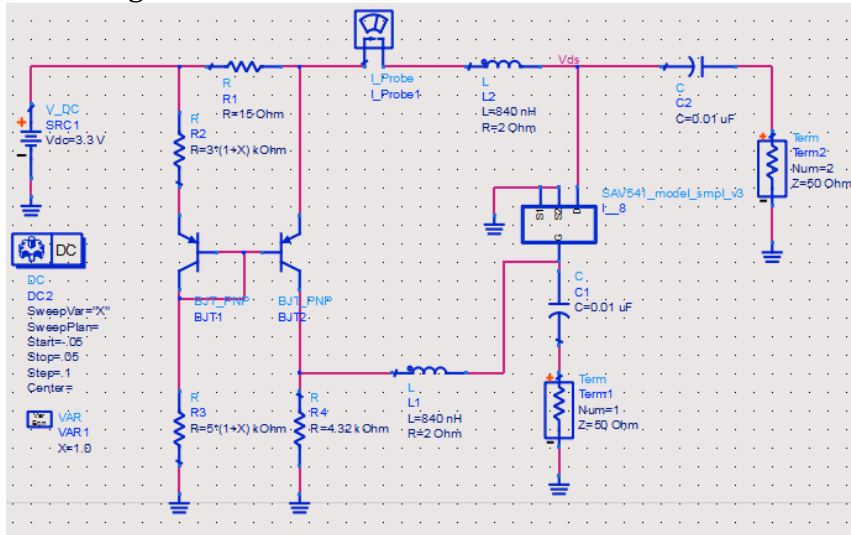The chosen DC bias network was an active network, which can be seen in figure 1. This design was found in the datasheet for the SAV-541+ transistor. The purpose of an active bias network is that it provides stable voltage levels over a wide range of temperature levels. Simulation in ADS was done to check to see how component variability affects bias voltages. Over a +/- 5% component variation, there was about a 0.1mA change in device current, which is shown in figure 1. Some difficulty may arise from choosing a DC bias circuit with a more component when it comes to PCB layout, however there are only 3 or 4 additional components that must be accounted for, and that seems reasonable considering the gain in temperature stability.

Figure 1: DC Bias Schematic

Figure 2: Current
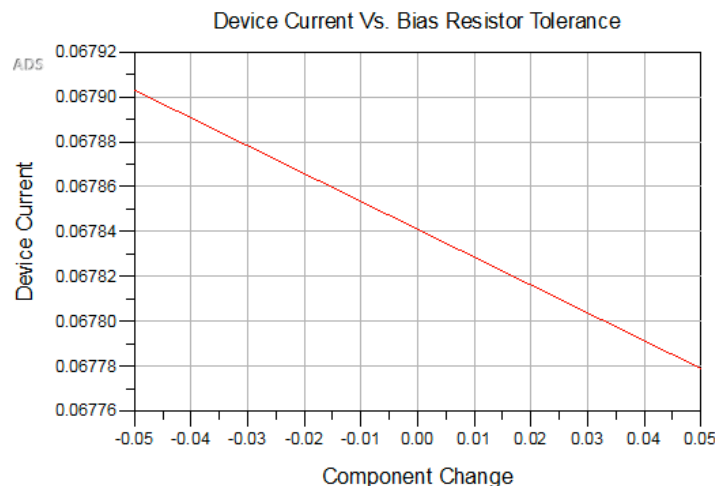
Device Change

S-Parameter Comparison

There are 2 ways that the device can be simulated in ADS. One way is to use the non-linear device model, which requires a biasing network to be set up, like in figure 1. There are also a variety of 2 port S-Parameter files provided by the manufacturer that model the divide at different device voltages and currents. Below is a plot of
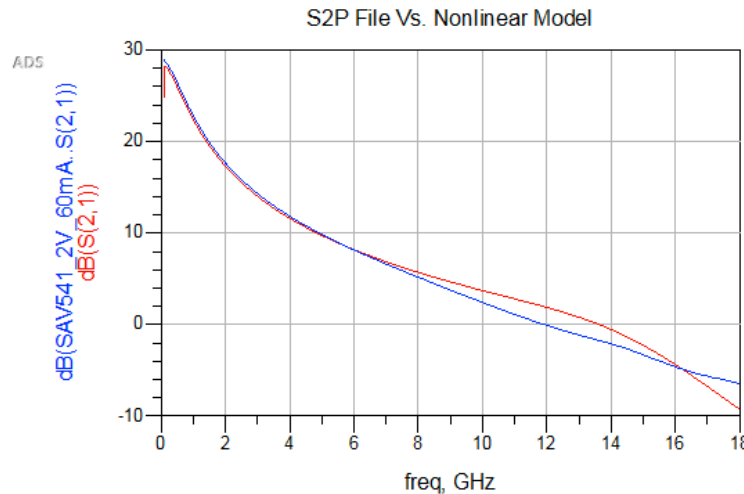
|S21| generated by the non-linear device model and the S-Parameter file provided by the manufacturer at an equivalent device bias. It can be seen that the non-linear model and the S2P file are very close, especially up to 6GHz.

Figure 3: |S21| Comparison

LNA Design

Using the amplifier design guide in ADS, the beginning design of the LNA was formed. To start, the S-Parameter file at the chosen bias level (which is Vgs = 2V, Id = 60mA) was used in the amplifier design guide. This showed that the transistor was not stable at frequencies below 4GHz, which means that using the transistor alone could result in oscillations on the input or the output. To compensate for this, stabilizing resistors were added in shunt to the drain and gate to make the amplifier stable up to 6GHz and have over 10dB gain up to 4.5GHz. However, this decreased the gain to about 13dB at 2.4GHz. Show below are the gain, noise, and stability plots using a 50ohm gate resistor and a 100ohm drain resistor.
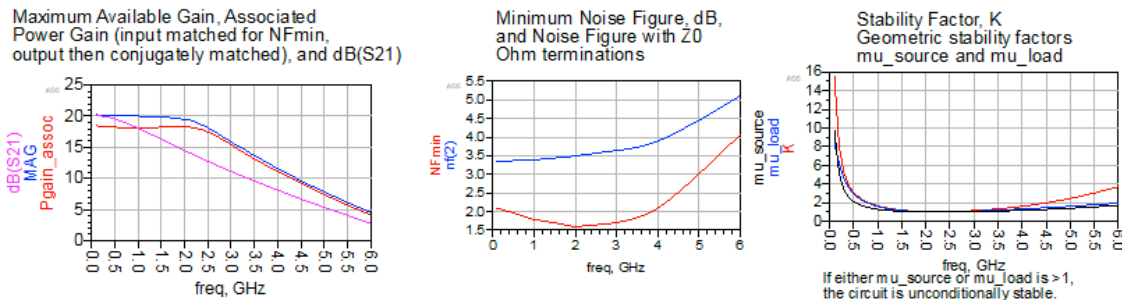

Figure 4: Gain, Noise, and Stability

Using these resistors, the impedances for a conjugate match were found to be:

$$Zsource = 2.416 + j3.189$$
$$Zload = 6.884 + j25.335$$

This supposedly should give a maximum available power gain of 18.5dB. Using the Smith chart tool in ADS, equivalent electrical lengths were found for a open circuit stub and transmission line to transform the source and load impedances to the ones listed above. Next, ideal transmission lines were used to check that there was indeed a match at the desired frequency. Initially the results were close, and using the tune feature in ADS, an almost perfect was achieved. The plot of S11 and S22 on a smith chart can be seen in Figure 5.
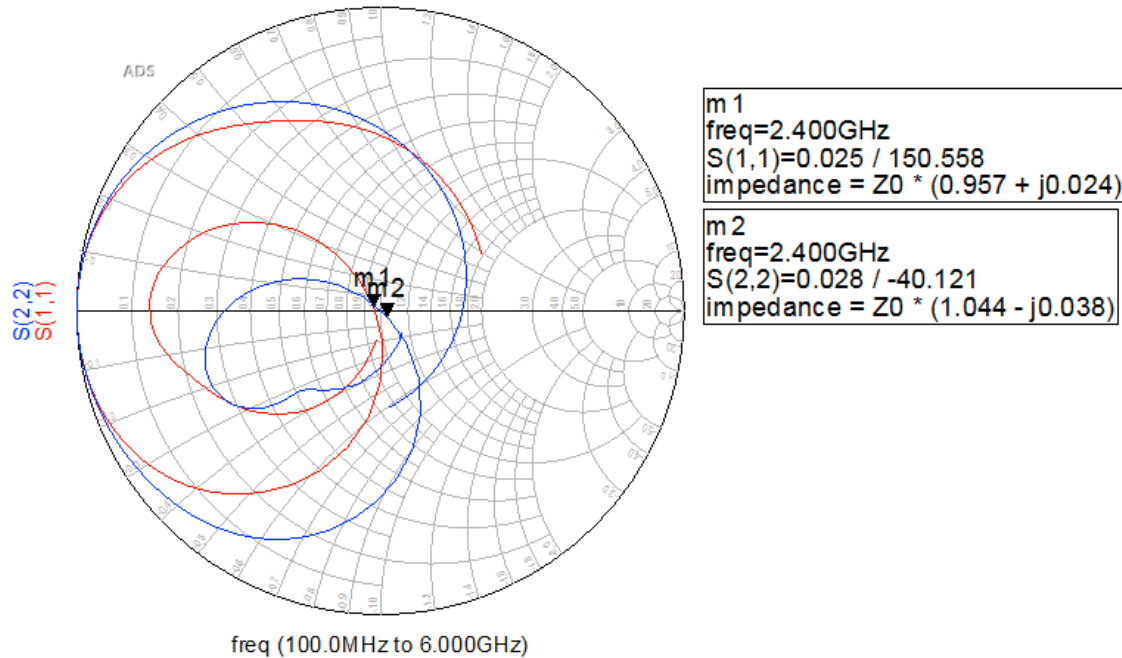

Figure 5: Input and Output Matched

A gain of 18dB was achieved in simulation once the input and output were matched. Finally, the ideal electrical lengths were converted into physical lengths for a particular substrate using the LineCalc tool in ADS. Additional tuning was required to adjust stub and transmission line lengths to re-match the input and output.

Parasitic Effects
In the next phase of the design, realistic components from the Murata library were added to the schematic. Replacing the DC blocking capacitors and RF chokes with real models did not seem to have much affect on the performance of the amplifier. However what did have a noticeable affect was when inductance was added to the source lead of the transistor. This increased the stability of the amplifier, however it decreased overall gain. This is because the inductance on the source lead is a form of negative feedback.

LNA PCB Layout
To accommodate real components, some additional transmission line elements were added to the schematic, such as a Tees and Tapers. These allow the transmission lines to be connected to other elements and components. However they alter the matching network. Again, the tuning feature was used to achieve a

match on the input and the output of the device. Initially, a layout was generated using ADS but after hours of research and tinkering, it proved to be too difficult. Instead, the line lengths were recorded and transferred to Eagle CAD, which was much easier to work with. Shown in figure 6 is the layout that was generated in Eagle.
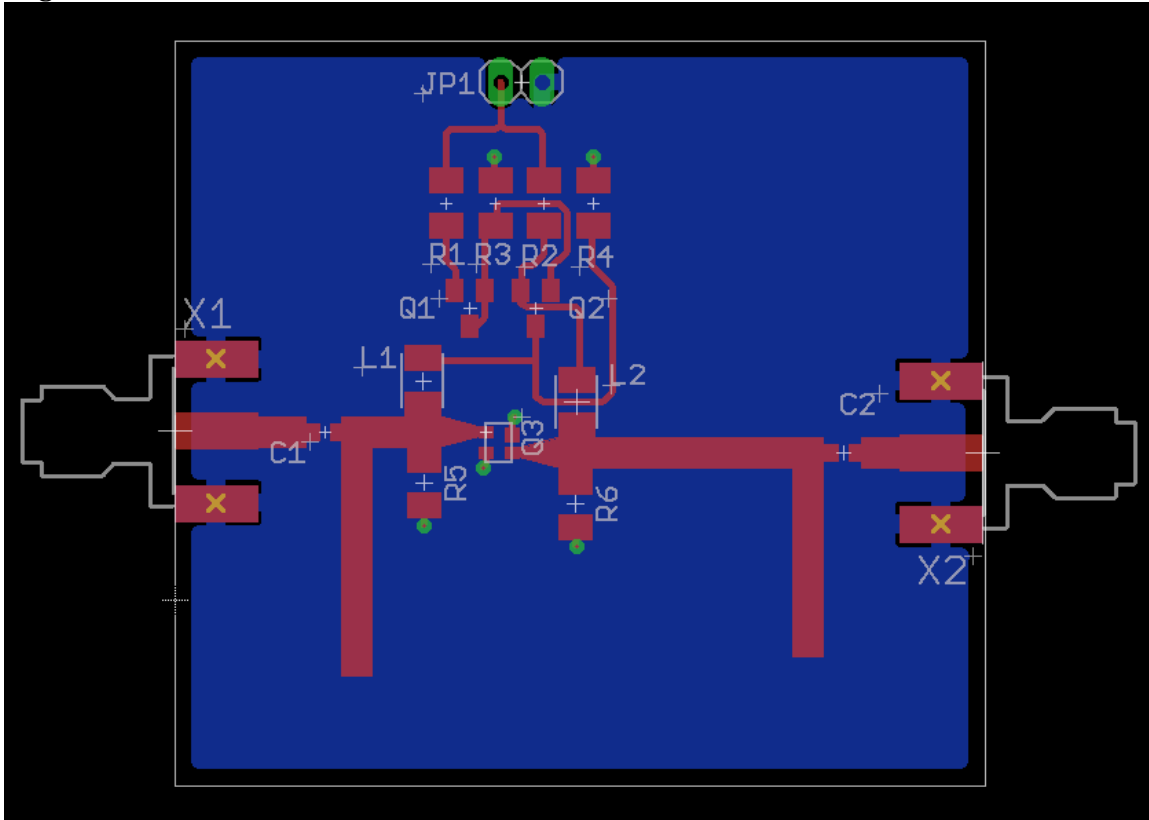

Figure 6: Eagle CAD LNA Layout

Conclusion

This lab explored the importance of a conjugate match and how it affects the gain of the amplifier, and also the affects of using stabilizing resistors. Some things that we found interesting in this lab were how big the affects of inductance due to a via had on the performance of the amplifier, its huge! Another thing that we learned from this lab was the usefulness of the amplifier design guide that is provided in ADS.

References:
Files from manufacturer:
SAV_541_S2_2V_60mA.s2p

Microwave transistor amplifiers (2nd ed.): analysis and design by Guillermo
Gonzales Prentice-Hall, Inc. Upper Saddle River, NJ, USA ©1996

K. Payne, "Practical RF Amplifier Design Using the Available Gain Procedure
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Agilent Technologies (5990-3356EN), 2008.