Efficiency improvement in Doherty Power Amplifier by using Class F approach

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Abstract— **In this contribution, the design of an uneven AB-C Doherty power amplifier (DPA) in GaN technology, implementing a Class F configuration for the Main device, is presented. Theoretical support will be given to understand why and how some relevant DPA's design parameters have to be carefully selected when a Class F strategy is adopted. Moreover, a comparison between the output performance obtained from a simple Tuned Load DPA and the here presented Class F DPA will be given.**

From the experimental results, the realised Class F DPA achieved, in an Output Back-off of 6dB, an average drain efficiency of 50% with a saturated output power of 3.2W at 2.14GHz.

I. Introduction

The DPA seems to be one of the most suitable PA architecture for wireless transmitters that have to deal with signals characterised by a high Peak-to-Average Power Ratio (PAPR), larger than 6-9dB and higher. Thanks to its feature to supply almost constant efficiency in a wide range of output power, the DPA allows to overcome the low average efficiency trouble that rises when traditional PAs (e.g. Class AB, F, or switched E) are used in such systems. The latter, in fact, shown a relevant high efficiency only for a fixed input power level, i.e. when operated close to their saturation region, thus they are not suitable to work with a large time-varying envelope signals.

Besides, the DPA is usually preferred to the other PA architectures such as Envelope Elimination & Restoration (EER), Envelope Tracking (ET), polar transmitter etc. due to its very simple scheme and, above all, due to the needless of any adaptive bias control circuitry which could further complicate the overall amplifying structure.

The typical DPA is implemented by a proper combination of two active devices (see Fig. 1) designed to operate as a Class AB (*Main*) and as a Class C (*Auxiliary*) power stage, respectively. These two PAs are connected at the output through a quarter-wave transmission line (*λ/4 TLine*), with the aim to properly perform an active load modulation concept [1].

In order to further improve the DPA performance, many efforts are currently focused to exploit the harmonic tuning techniques in such architecture. In this contest, some approaches have been proposed in [2] and [3] about the combination of the DPA with Class F configuration (namely F-DPA). However, these realisations are not supported by a rigorous theoretical treatment but usually they are obtained by a CAD optimization.

In [1] we have presented the complete theoretical and nonlinear analysis of a DPA employing a generic Class AB (*Main*) - Class C (*Auxiliary*) bias condition for the two active devices considering a Tuned Load configuration (TL-DPA). As a result, closed form design relationships to directly design an AB-C TL-DPA have been there tailored and validated through experimental results [4], showing the right way to design a DPA with TL harmonic termination.

In this paper, the fundamental design equation derived in [1] for a TL-DPA will be rearranged considering a Class F configuration for the *Main* PA and a TL for the *Auxiliary* PA. In fact, as will be later discussed, any beneficial harmonic tuning approach becomes unfeasible for the Auxiliary device, due to its Class C biasing condition, thus limiting the optimum solution for such amplifier to the classical TL configuration.

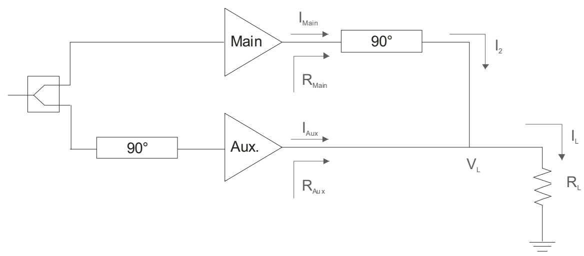

Fig. 1: Typical DPA configuration.

II. Theory Highlights

When a Tuned Load solution is considered, all the harmonic components of the output current are short-circuited with the aim to shape a purely sinusoidal waveform for the resulting output voltage. Conversely, in high frequency Class F approach (i.e. considering only the first three harmonics), the harmonic components of the device output current are properly terminated in order to square the resulting output voltage, i.e. in order to generate the voltage harmonic components with suitable phase relationships and amplitude ratios [5,6]. Moreover in [5] is also highlighted the role of the bias point and in particular the unfeasibility of realising a true Class F PA using a Class C bias condition, if not bringing the active device in deep saturated condition. For this reason, the Class F configuration has been considered applicable only for the *Main* device, being the *Auxiliary* one biased in Class C, to properly turn on only in the Doherty region [1].

Referring to the scheme depicted in Fig. 1, and accounting for the relationships inferred for the Tuned Load approach reported in [1], to adopt a Class F strategy for the Main device, some relevant DPA's design parameters have to be changed. To this purpose, in the following will be detailed how to establish the following parameter:

- the optimum external load value R_L.
- the output $\lambda/4$ *TL* characteristic impedance Z_0.
- the auxiliary device Class C bias condition.
- the input power splitting ratio.

It is well known that using a Class F strategy it is possible to increase the amplitude of the first output voltage harmonic component by a factor $\delta = 2/\sqrt{3}$ with respect to the same device working in TL configuration, while assuming the same bias point and output drain current waveform [5].

Therefore, considering the low power region where only the *Main* device is active, and its current waveform is imposed by the input signal, the DPA external load R_L and the $\lambda/4$ characteristic impedance Z_0 become respectively (refer to Fig. 1 for the quantities):

$$R_{L,F} = \frac{V_L}{I_2} = \frac{R_{L,TL}}{\delta} \tag{1}$$

$$Z_{0,F} = Z_{0,TL} \tag{2}$$

where the subscript TL or F identifies the *Main* amplifier in Tuned Load or Class F configuration, respectively.

In this way, the resistance "seen" by the Main device at fundamental frequency $R_{1,Main,F}$ results δ times higher with respect to the TL case $R_{1,Main,TL}$, as required for a Class F PA. Moreover, since the same bias point for the Main Amplifier is considered, the fundamental current component of the Auxiliary device ($I_{1,Aux}$) has to be δ times higher in order to properly modulate the Main resistance [1,5].

However, assuming that the output current of the Main device remains the same in TL-DPA and F-DPA, it follows that the turning-on condition and the final current conduction angle (CCA) of the Auxiliary device should remain unchanged also.

Thus, in the F-DPA, the Auxiliary device has to reach a fundamental current component δ times higher, while maintaining the same final CCA. Therefore, its maximum ($I_{Max,Aux,F}$) and "virtual" bias current ($I_{DC,Aux,F}$) respectively become:

$$I_{Max,Aux,F} = \delta \cdot I_{Max,Aux,TL} \tag{3}$$

$$I_{DC,Aux,F} = -\frac{x_{break}}{1-x_{break}} \cdot \delta \cdot I_{Max,Aux,TL} \tag{4}$$

Where x_{break} is the value of the normalised input signal when the current has to start to flow through the Auxiliary device and $I_{Max,Aux,TL}$ is the Auxiliary device maximum current in the TL-DPA case.

The different bias point and maximum current for the Auxiliary device imply a different voltage splitting ratio with respect to the TL case, defined as the ratio between the RF input voltages supplied to the Auxiliary and to the Main devices, resulting in a input voltage ratio $K_{V,F}$ given by:

$$K_{V,F} = \frac{g_{m1}}{g_{m2}} \cdot \frac{I_{Max,Aux,F}}{I_{Max,Main,F}} \cdot \frac{1-\cos\left(\frac{\theta_{AB}}{2}\right)}{1-\cos\left(\frac{\theta_C}{2}\right)} = \delta \cdot K_{V,TL} \tag{5}$$

being θ_{AB} and θ_C the final CCA, g_{m1} and g_{m2} the transconductances (assumed constant) of the Main and Auxiliary devices, respectively.

The previous equation (1)-(5) stresses the differences that have to be accounted for when a Class F harmonic termination for the *Main* device is adopted.

III. Class F DPA Design

In order to validate the proposed approach, an F-DPA has been designed and realized. The active device used to build the *2.14 GHz* F-DPA was a GaN HEMT with 1mm gate periphery. It has been fully characterized and modelled through a nonlinear equivalent circuit approach, resulting in the output IV characteristics depicted in Fig. 2. The selected *Main* bias point was V_{DD}=*15V* & $I_{DC,Main}$=52mA, corresponding to the 8% of its maximum current. Moreover the output back-off (OBO) of the DPA has been fixed in the typical value of 6dB. The *Auxiliary* bias point was chosen accounting for the relationships derived in [4] and according to equations (3) and (4).

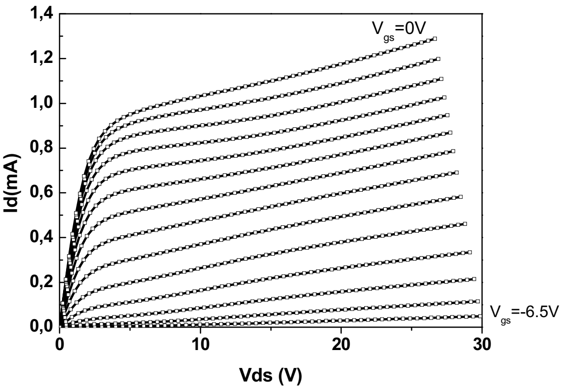

Fig. 2: Output DC I-V characteristics of the used active device.

In order to design the DPA, the following steps have been followed. First of all, the output matching network (OMN) for the *Main* device was designed to fulfil the load conditions at

$x=x_{break}$ and at the saturation, resulting in $R_{Main}=88.7\Omega$ and $R_{Main}=44.5\Omega$, respectively. Moreover, the OMN has to guarantee the compensation of the device output reactance and, in order to fulfil the Class F condition, the short circuit and open circuit condition at the second and third harmonic components of the drain current, respectively.

On the other hand, particular attention has to be paid designing this network, to assure the proper load curve behaviour when the R_{Main} at fundamental is modulated by the *Auxiliary*.

In Fig. 3 are reported the load curves obtained by the nonlinear simulation of the designed amplifier for the R_{Main} value 88.7Ω (curve A) and 44.5Ω (curve B).

Then, the input matching network has been designed for sake of simplicity to match the amplifier to 50Ω, at the section where the input power splitting will be placed.

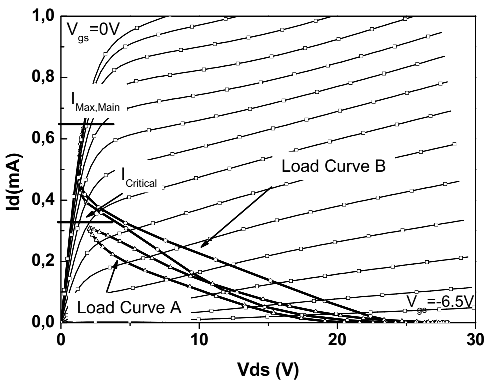

Fig. 3: Load curves of the *Main* device at break (curve A) and saturation (curve B) conditions.

Similarly, the OMN for the *Auxiliary* device was designed to fulfil again the Tuned Load conditions assuring the R_{Aux} optimum load condition (33.5Ω) across the intrinsic current source, compensating the device parasitic elements. In Fig. 4 is depicted the resulting load curve simulated at the saturation of the *Auxiliary* amplifier.

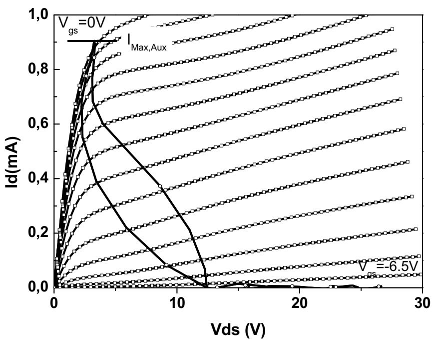

Fig. 4: Load curve of the *Auxiliary* device in saturation.

As it was made for the *Main* amplifier, also in this case the relevant input network was designed in order to match the *Auxiliary* device to 50Ω.

Afterwards, the uneven input power splitting was designed to fulfil the calculated power ratios (starting from (5)) resulting in $|S_{21}|=0.333$ and $|S_{31}|=0.943$, by using an uneven Branch Line power splitting.

Finally, the *Main* and *Auxiliary* amplifiers have been connected through the output λ/4 transformer with characteristic impedance $Z_0=38.5\Omega$ and closed to the output impedance $R_L=16.7\Omega$, as inferred from (1) and (2). The latter requirement was realized through a further λ/4 transformer starting from the external 50Ω standard load condition.

Finally, the networks have been smoothly tuned to optimize the Class F DPA operating conditions, and implemented in a distributed approach, resulting in the layout reported in Fig. 5.

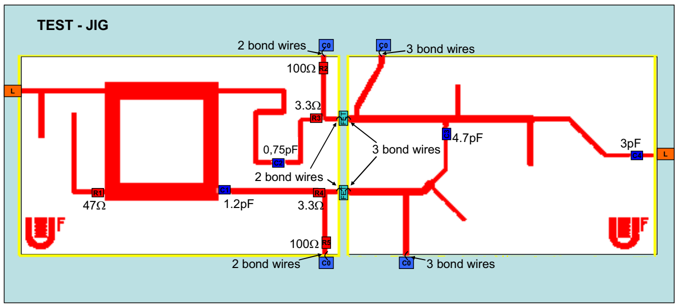

Fig. 5: Layout of the designed DPA.

The impedances seen across the intrinsic current sources of the *Main* and *Auxiliary* devices, as obtained through a full nonlinear simulation are depicted in Fig. 6.

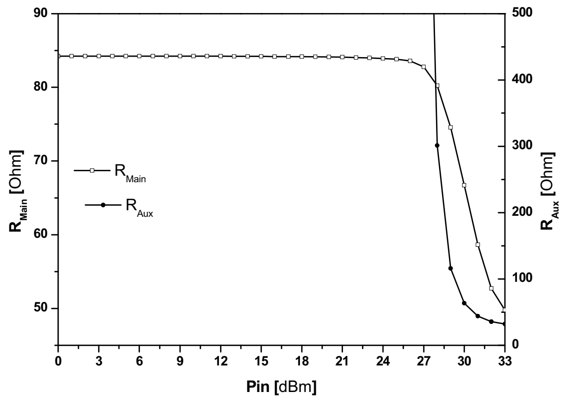

Fig. 6: Intrinsic load impedances of *Main* and *Auxiliary* devices, as obtained by a full nonlinear simulations.

Finally, in Fig. 7 are reported the comparison of the output performance obtained from the full nonlinear simulations of the TL-DPA presented in [4] and the F-DPA here reported, as a function of the output power. As can be noted, the efficiency of the Class F is about 15% higher respect to the TL one at the break point, while at the saturation point the difference becomes slight lower due to the same contribution coming from the *Auxiliary* device. Also the final output power of the Class F is roughly 15% higher than the TL counterpart. Moreover, the resulting gain is lower for the Class F one, as expected by the increase of the input splitting ratio defined in (5).

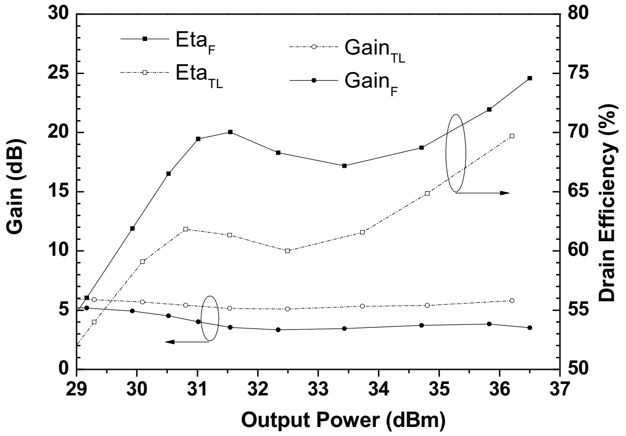

Fig. 7: Comparison between TL and F DPA efficiency and gain simulated behaviour.

IV. Experimental results

The uneven DPA was realized on a PTFE (ε_r=10, h=0.635 mm) substrate. After a small signal characterization, performed to verify the stability of the amplifier, it was measured under Continuous Wave (CW) signals, fixing the drain voltage to $V_{DD}=15V$ and varying the operating frequency in the neighbourhood of the nominal value. The best performances were obtained at 2.14GHz with a gate voltage $V_{GG,Main}=-5.9V$ ($I_{DC,Main}=0.57mA$) and $V_{GG,Aux}=-11V$ for the *Main* and *Auxiliary* devices, respectively.

The measured performances are reported in Fig. 8 compared with the simulated ones. The latter are clearly referred to the external point, thus accounting for the devices' losses [4]. In fact the efficiency values reported in Fig. 8 are lower respect to the ones in Fig. 7. Moreover from Fig. 8 is evident how the measured gain is higher respect to the simulated one, maybe because the g_m value of the actual devices is higher with respect to the one used in simulation.

From the experimental results, the actual Doherty region results in an *OBO* range of 6dB and in a corresponding input back-off (*IBO*) of 7dB. In this region, an average drain efficiency of 50% has been registered achieving a saturated output power of 3.2W.

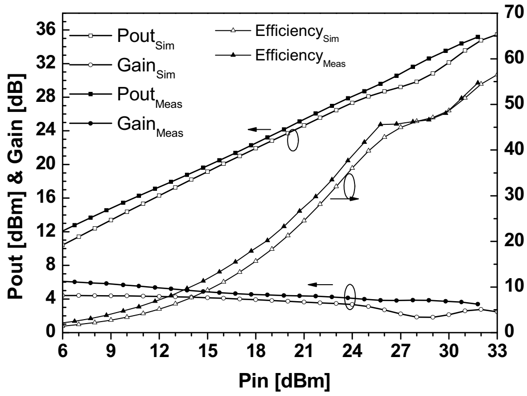

Fig. 8: Comparison between the simulated and measured performances of the realised Class F DPA.

V. Conclusions

In this paper, the integration of the Class F strategy in the Doherty amplifier architecture has been proposed. In particular, the design relationships developed for a TL DPA have been tailored accounting for a Class F harmonic termination for the *Main* device. The relevant differences between the two approaches have been focused and discussed, showing an improvement of roughly 15% in output power and efficiency behaviour of F-DPA towards TL-DPA.

The realised F-DPA achieved, in an Output Back-off of 6dB, an average drain efficiency of 50% with a saturated output power of 3.2W.

References

[1] P. Colantonio, F. Giannini, R. Giofre`, and L. Piazzon, "The AB-C Doherty power amplifier. I. Theory" International Journal on RF and Microwave Computer-Aided Engineering (2008), DOI 10.1002/mmce20350.

[2] J. Kim; J. Moon; Y. Y. Woo; S. Hong; I. Kim; J. Kim; B. Kim, "Analysis of a Fully Matched Saturated Doherty Amplifier With Excellent Efficiency," IEEE Trans. on MTT, Vol. 56, pp. 328 – 338, Feb., 2008.

[3] Y. Suzuki, T. Hirota, and T. Nojima, "Highly efficient feed-forward amplifier using a class-F Doherty amplifier," in IEEE MTT-S Int. Microw. Symp. Dig., Jun. 2003, pp. 77–80.

[4] P. Colantonio, F. Giannini, R. Giofrè, L. Piazzon, "The AB-C Doherty power amplifier. II: Validation," International Journal on RF and Microwave Computer-Aided Engineering(2008), DOI 10.1002/mmce20351.

[5] P. Colantonio, F. Giannini, G. Leuzzi, E. Limiti, "On the Class-F Power Amplifier Design," International Journal on RF and Microwave Computer-Aided Engineering, Vol.9, N°2, March 1999, pp.129-149.

[6] F.H. Raab, "Maximum efficiency and output of class-F power amplifiers" IEEE Transactions on Microwave Theory and Techniques, Vol. 49, Is. 6, Part 2, June 2001 Page(s):1162 - 1166.