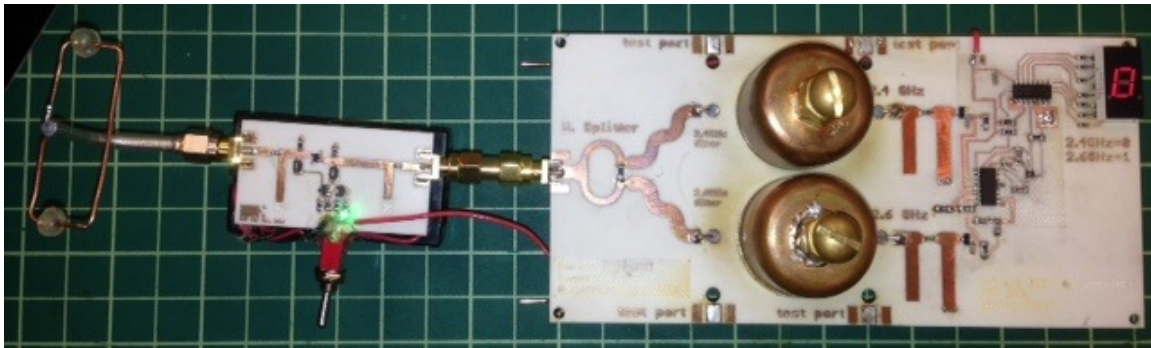


2.4-2.6GHz FSK Receiver



Abstract

Frequency Shift Keying is currently used in many applications for example wirelessly transmitting binary data. Using high frequency sinusoids, a transmitter shifts between two frequencies which are later interpreted a logic '1' or '0'. A 2.4 – 2.6GHz FSK receiver was designed, simulated in ADS and built using the rapid prototyping equipment in the Lab for Interconnected Devices at Portland State University. The receiver included an LNA on the front end, a Wilkinson power divider, resonant cavity filters and diode detectors. Later a 7-segment display with the appropriate logic was used to interpret the data and display the binary output.

Requirements

- Operate at 2.4 and 2.6 GHz
- Reliably distinguish between 2.4GHz and 2.6GHz signals
- Amplifier with at least 10dB gain and $S_{11} < -10\text{dB}$.
- 3dB power divider
- 2.4 and 2.6GHz Bandpass filters
- Diode detector to output DC when signal is received.

LNA

The LNA is the front end of the receiver. Its purpose is to amplify very weak signals without adding much noise to the system. This is done through various input and output matching networks. Initially, a packaged LNA (PSA-5043+) was going to be used, however after several iterations the measured performance did not meet specs, and instead an LNA (shown in Figure 1) designed for a previous project was used. The alternate LNA has a gain of 13dB at 2.4GHz, 11dB gain at 2.6GHz, and S_{11} approximately -10dB at 2.4GHz.

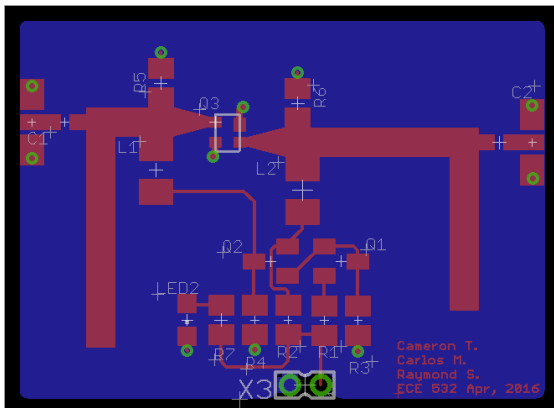


Figure 1: LNA Lavout

Wilkinson Splitter

A simple Wilkinson power divider, designed for 2.5GHz was implemented. The design was simulated in ADS, and the layout was done in Eagle CAD (shown in figure 2). The measurement of the splitter showed that the center frequency was indeed at 2.5GHz and the output on each channel had a loss of 3dB when properly terminated with 50 Ohms. S11 was measured to be approximately -15dB.

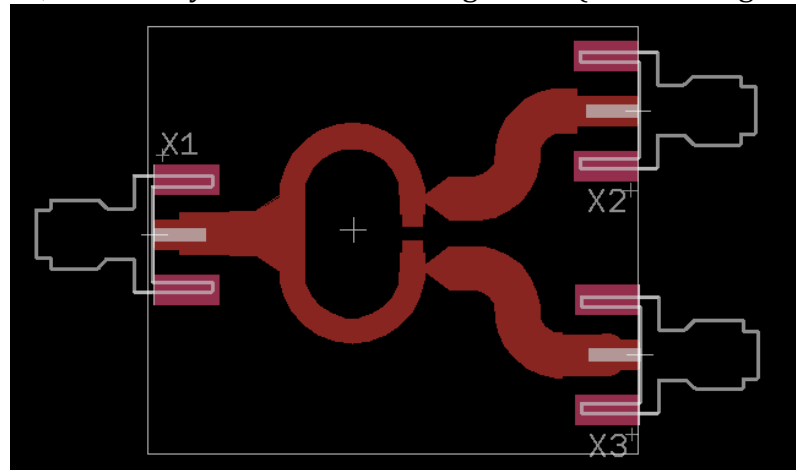


Figure 2: Wilkinson Splitter Layout

Filters

There were two different types of filters that were investigated in this project. First, a lumped element filter, using a combination of microstrip capacitors, and SMD components was designed in ADS and constructed. Second, a resonant cavity type filter was used.

Resonant Cavity Filters (Pipe Cap)

The resonant cavity filters were chosen because they offer a very high Q and low insertion loss, which will allow the receiver to easily distinguish between 2.4GHz and 2.6GHz. Shown below is an equivalent circuit for the resonant cavity. To construct the filter a one-inch copper pipe cap was used as a cavity. The volume of the pipe cap happens to be just right for the frequency range of interest. To tune the filter, a #4-40 brass screw was used to vary the inductance and capacitance of the cavity to just the desired frequency response. The insertion loss of the cavity filters is around 1dB, and a bandwidth of approximately 15MHz was achieved. S11 was also decent at approximately -15dB.

Construction of the filters also posed to be a challenge. Since the entire receiver was going to be on a single PCB, the filters needed to be mounted to the board. However

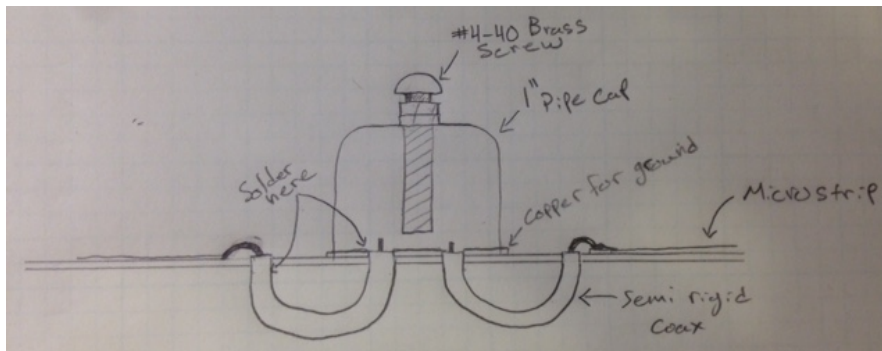


Figure 3: Pipe Cap Filter Sketch

getting the signal into the cavity while mounted to the board was not straightforward. To achieve this, two small sections of semi-rigid coax were used to loop

underneath the PCB and come back through a hole inside the cavity filter. This method was very successful and was also cost effective. Figure 3 is a sketch of how the filter is constructed.

Lumped Element Filter

A significant effort was made to create a 2.4GHz filter using SMD inductors, microstrip gap capacitances and component pad shunt capacitances. The simulation

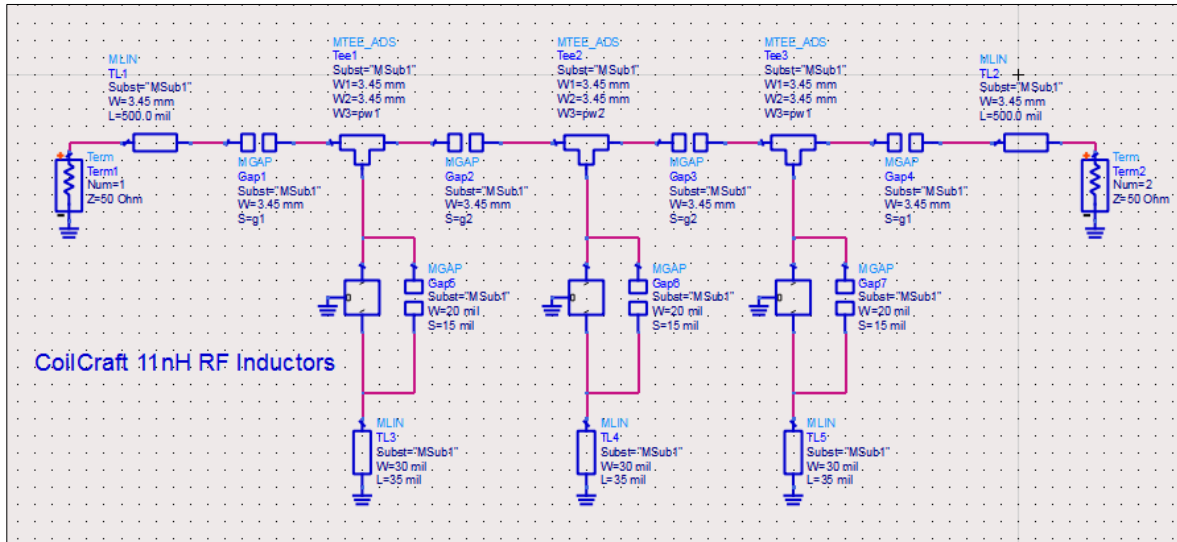


Figure 4, Compact 2.4GHz SMD BP filter

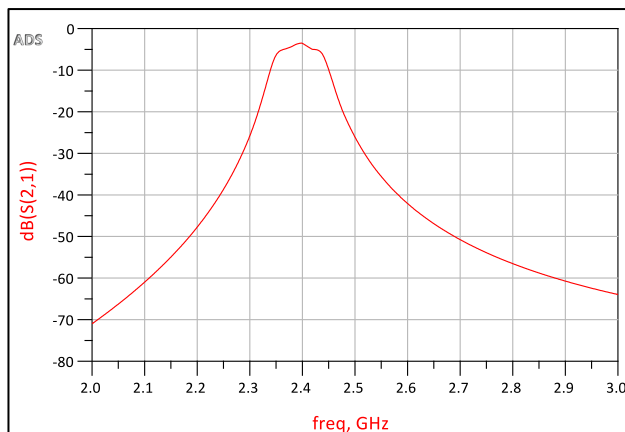


Figure 5, SMD filter S21 simulation



Figure 6, SMD filter

setup and results are shown in figure 5 and 6. The actual implementation shown in figure 6. This filter was very tricky to design and was never good enough to use for the project. It was determined that for this filter to work the tolerance of the gap capacitance cuts would have to be very tight thus more attention would need to be given to the calibration phase of the LPKF circuit board routing process.

Diode Detectors

To begin, an accurate model of the diode was created in ADS. Using the datasheet (see references) for the HSMS-2850 all of the small signal parameters are entered into ADS. Since the diode will be used without a DC bias, the focus was on the large signal characteristics. As in all RF circuits the behavior of the diode is strongly dependent on the DC bias point and input power. In this case there is no DC bias so input power was swept.

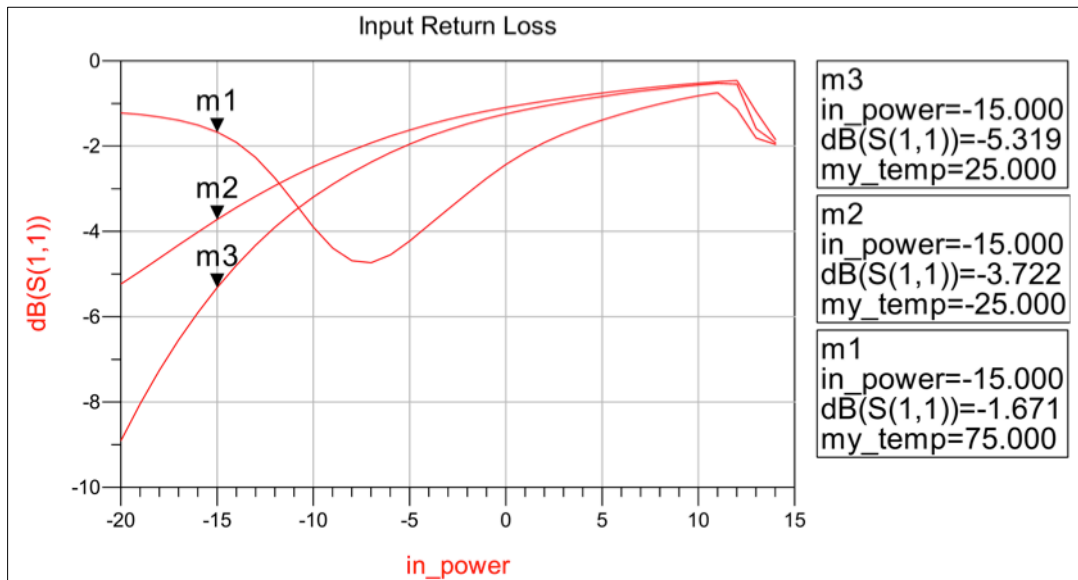


Figure 7, Detector power sweep.

The schematic below shows the matching network for the diode detector. Parasitics have been added due to the diode's packaging per app note Avago Technologies 1124. The short circuited stub serves two purposes, its is used as a matching network but more importantly it serves as a path to ground when the diode is not conducting.

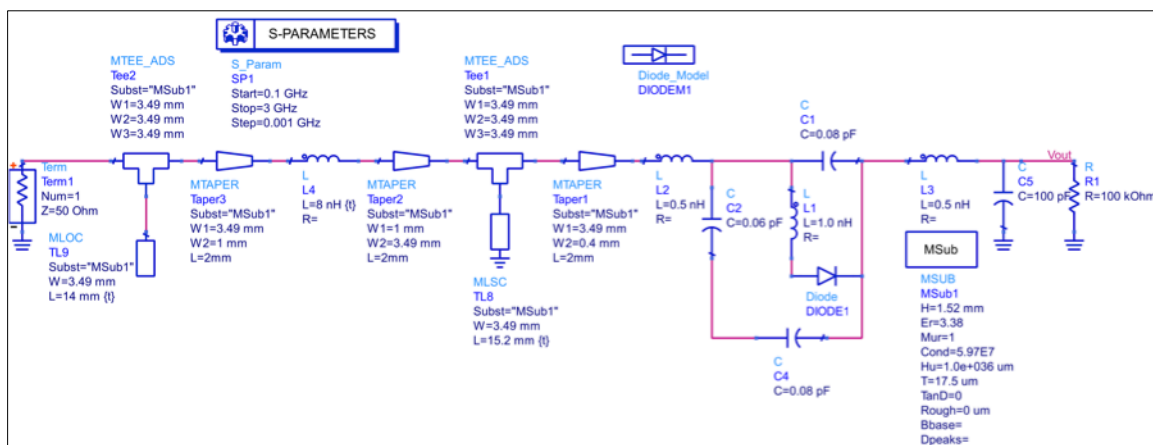


Figure 8, Detector simulation setup.

Display

A 7-segment display along with some digital logic was used to display when data has been received. The output of the diode detectors is sent to comparators, which sends signals to an OR gate and a 7-segment display driver to decide when to light up the display, and whether the signal is 2.4GHz or 2.6GHz. If the signal is 2.4GHz, the display will show a '0' and when the input signal is 2.6GHz, the display will show a '1'.

The comparators have a threshold of approximately 1 to 3mV, which is set by a resistive voltage divider. In total, there are three comparators that are being used; the first is used to detect the 2.4GHz signal, the second and third are used for the 2.6GHz signal. When the output of the 2.4GHz diode detector goes above the threshold, the output of comparator 1 goes high, this sends a signal to the OR gate, which allows the display to turn on. Comparator 2 is used in the same way for the 2.6 GHz signal, and comparator 3 is used in parallel with comparator 2 to send a signal to the 7-segment display driver to make the display show a 0 if it is low or a 1 if it is high. Shown below in figure 4 is the schematic of the logic circuit for the display.

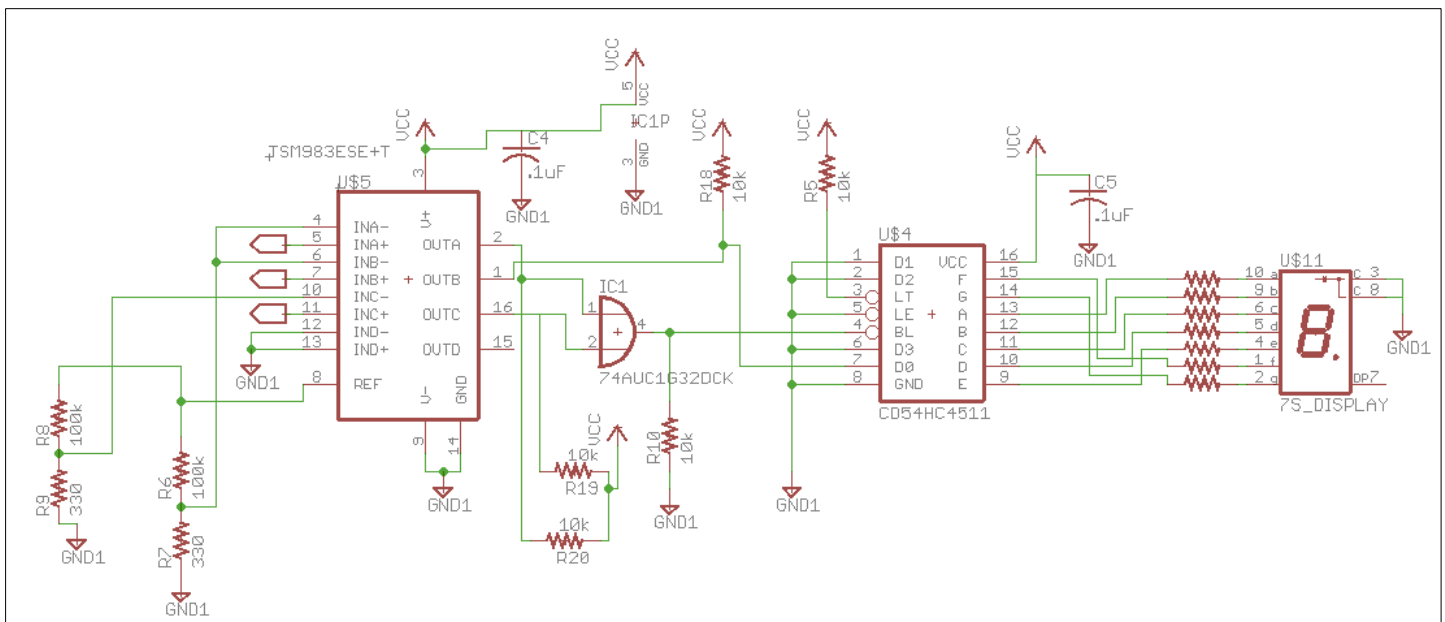


Figure 9: 7-Segment display Schematic

Antennas

To allow the receiver to pick up wireless signals, an antenna was added to the input to the LNA. There were two types of antennas that were explored, a folded dipole, and a Moxon antenna. A Folded dipole antenna is a $\lambda/2$ antenna that has input impedance around 300 Ohms. To transform this impedance to 50 Ohms, typically a balun with an appropriate turns ratio would be used, however the antenna seemed to still work fine without it.

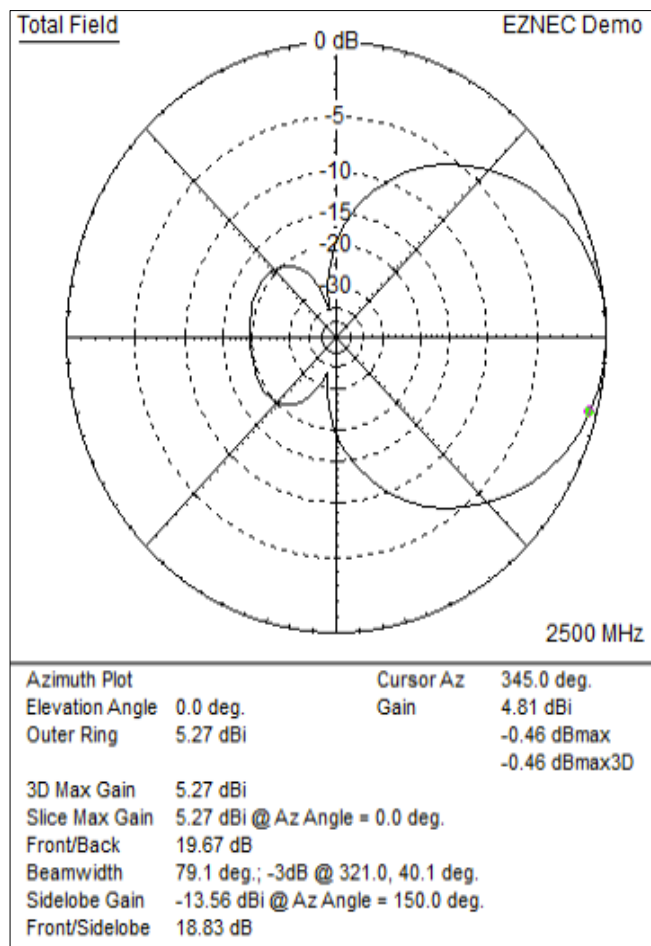


Figure 10: Radiation Pattern for Moxon Antenna



Figure 11: Moxon and Folded Dipole Antennas

The Moxon antenna is another form of a $\lambda/2$ antenna, however there is a reflector element in the near field that reflects the rear lobe of the radiation pattern to the front; this increases directivity and antenna gain. Below is a simulated Azimuth radiation pattern from EZNEC software.

Board Layout

Initially, there was an attempt to layout the entire PCB in ADS, however there were many issues encountered. Since time was also a constraint from this project, it was decided to generate the entire layout in Eagle. Certain circuit elements such as tuning stubs needed to be generated using ADS so that appropriate simulations could be made. Once trace lengths and widths were figured out, that design was exported from ADS and imported into Eagle. From here, other circuit elements such as resistors, capacitors and ICs could be inserted into the layout.

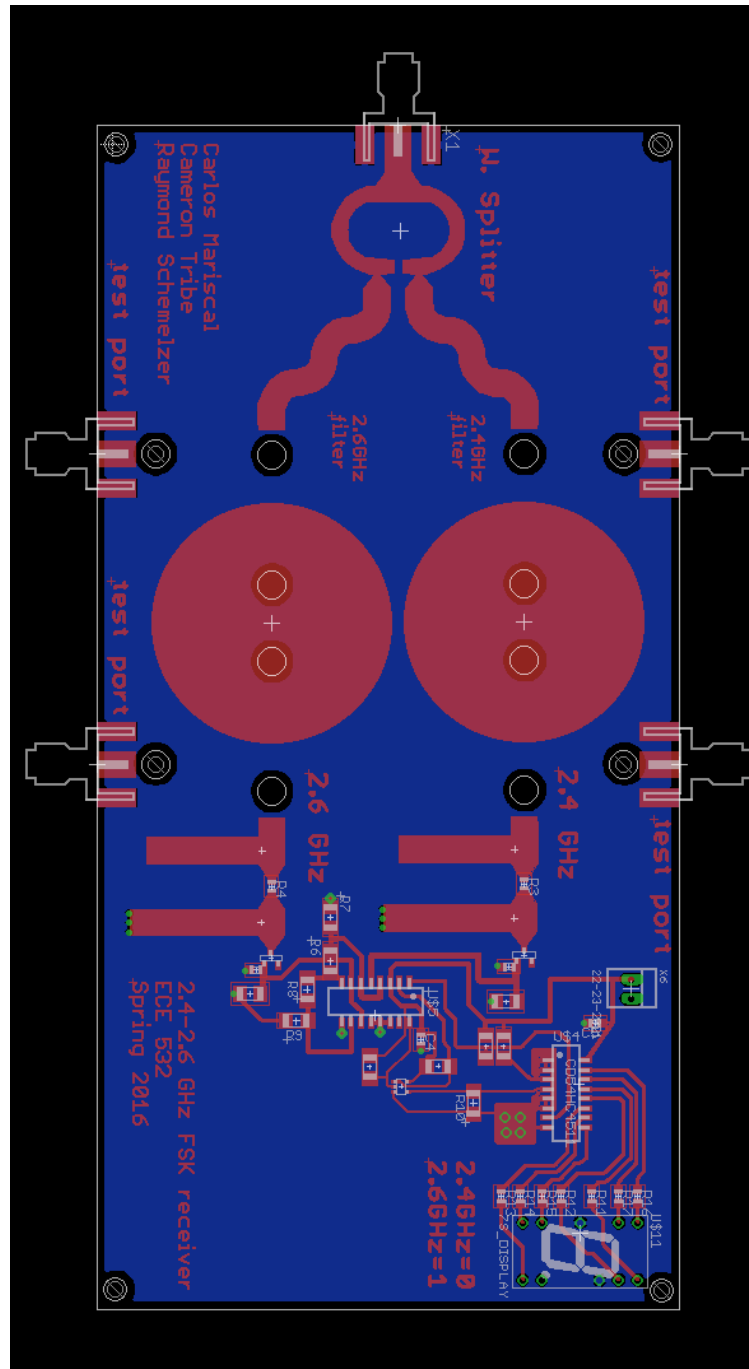


Figure 12: FSK Receiver Layout in Eagle CAD

Measurements

Performance based measurements were made to determine characteristics of the receiver. First, the antenna was removed and a signal generator was attached to the input of the LNA. The input power level was varied, and the frequency was held constant first at 2.4GHz then again at 2.6GHz. Input power was swept from -50dBm to -10dBm, below is the resulting curves from the output of the diode detectors.

From this plot it can be concluded that the minimum detectable level is approximately -45dBm.

Next, the input power level was held constant at -30dBm, the input frequency was varied and output voltage was measured for both the 2.4 and 2.6GHz outputs. Shown in figure 9 are the results of the tests. From these two sets of measurements, it was discovered that the 2.6GHz was much less sensitive than the 2.4GHz output.

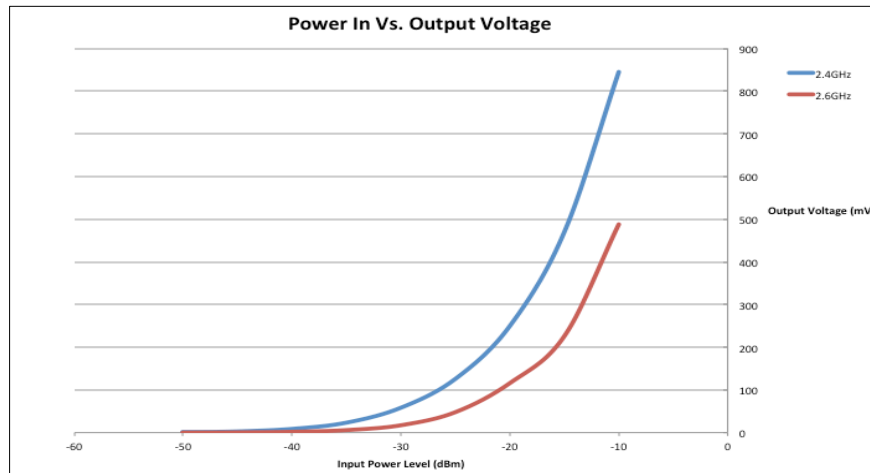


Figure 135: Power In Vs. Voltage Out

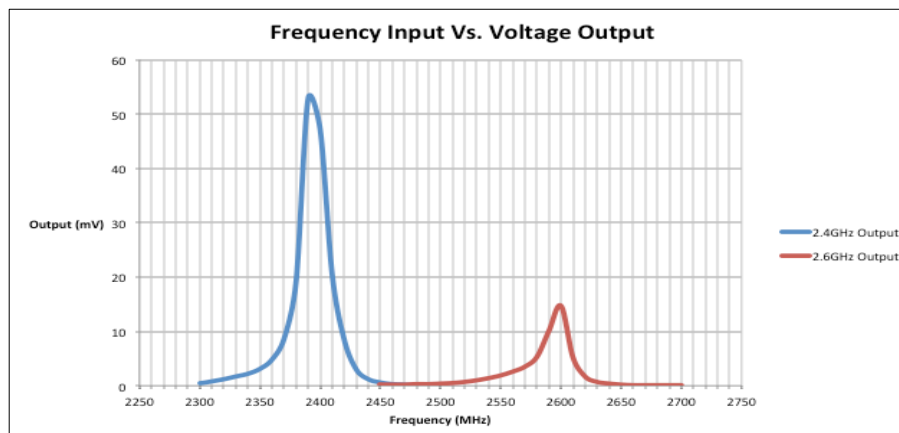


Figure 14: Frequency In Vs. Voltage Out

This is most likely caused by the lack of gain at 2.6GHz from the LNA. Other contributions to the lower output level could come from mismatches between stages, filter insertion loss, or diode detector insertion loss.

System Simulation and Data Analysis

The high frequency FSK receiver constructed for this project is a combination of microwave circuits designed to properly receive digital data transmitted from a link partner. A simulation setup was developed as shown in figure 15 to explore the

tradeoffs between microwave circuit/component margins, data rate and RX error ratio. Factors for this exploration included:

- Receiving Power Range = -100dBm to -10dBm
- Amplifier noise, linearity and sensitivity
- Bit rate of system
- Diode detector Inter Symbol Interference on output

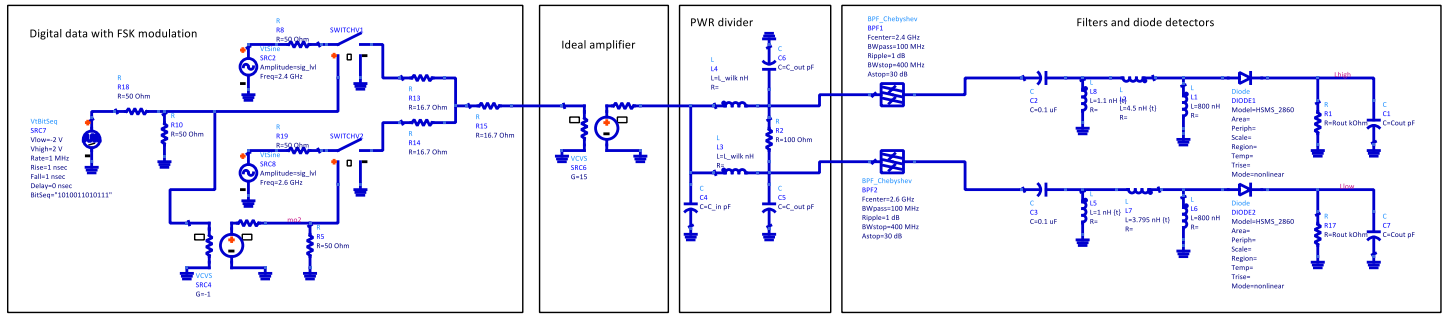


Figure 15, System simulation setup for debug and system sensitivity analysis

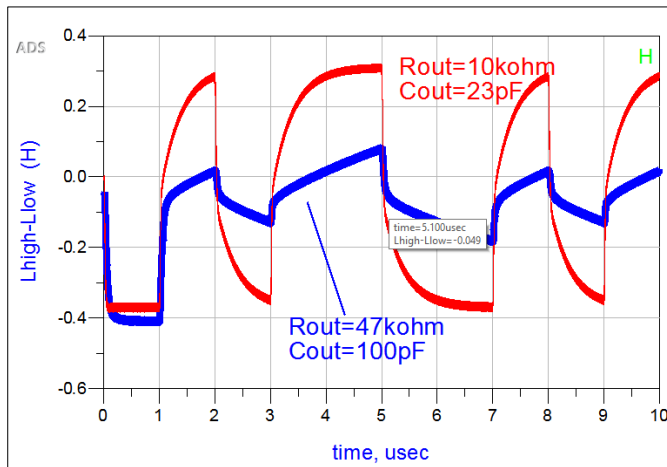


Figure 16, Data output for 2 output filters.

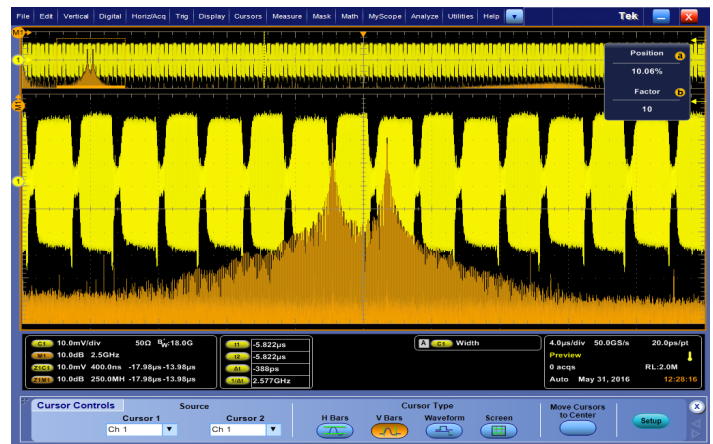


Figure 17, FSK signal output in time domain and frequency

For this project the detector output filter was analyzed for a system data rate of 1Mbps. In ADS a transient simulation was run with a typical TX bit sequence in order to highlight the effect long runs of ones or zeros followed by 1010 sequences effect the margin to making an incorrect bit decision. Figure 16 shows that at 1Mbps the RC charging and discharging with the 47Kohm and 100pF filter could have significant effect on the digital data detection. Also shown in figure 11 is the same bit sequence with a 10kohm and 23pF filter. The latter was not built, but may make a better filter for the 1Mbps data rate.

Next, a system was put together to make a simple FSK TX in order to test the validity of the simulation setup in this section. First a 6GHz SPDT switch was acquired and while the switch control bandwidth was not documented in the device datasheet it

was found the switch could effectively switch between A and B and the common at about 2MHz resulting in a 4Mbps transmitter. This switch was used to switch between two signal generators, one running at 2.4GHz and one running at 2.6GHz. The common output of the switch was taken to be the FSK signal. As a test the signal was measured on a real time oscilloscope and analyzed in both time and frequency domains. From figure 17 it is clear that both signals are present and that the switching works. Next this signal was used as the input to the receiver and the digital output was analyzed. The output of the constructed receiver trended similarly to the output of the simulation.

Conclusion

In about 5 weeks, a 2.4 – 2.6GHz FSK receiver was designed, built and tested. The receiver used an LNA made from a single transistor, matching networks, Wilkinson power divider, resonant cavity filters, diode detectors, and digital circuitry. Overall performance of the receiver proved to be exceptional, and if more time were to be put into this project, a microcontroller could be implemented to quickly interpret incoming data, and this device could be used to wirelessly receive data. Even walking through the halls of the engineering building at Portland State caused the display to frequently flicker, showing that it was receiving 2.4GHz from nearby routers.

This project has been a great learning experience about integrating a design in a modular approach. Each section was separately designed, simulated and tested to ensure that it was operating properly, then it was all brought together on a single PCB. Approaching a project in this way, there is less potential for error and more time can be spent on further project development.

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