Diode Detector Simulation using Avago Technologies EEsof ADS Software

Application Note 1156

Introduction

This application note has been written to demonstrate how the Avago Technologies EEsof ADS software package can be used to simulate a diode detector circuit reliably against temperature.

For this demonstration a simple two diode configuration has been proposed. This has the benefit of offering temperature compensation of the diode's bias-induced forward voltage. The circuit used in this demonstration is shown in Figure 1 below.

This circuit was designed around the Avago Technologies Schottky diode, HSMS-2865, which was developed for low cost, high volume, high frequency detector applications.

Detector Circuit

The input impedance in this example was chosen to be 33 Ohms. L1 and C2 are providing the reactive match, while R1 provides a good broadband resistive match.

The bias is applied to the first diode via R1, and R2 acts as the resistive load for the detector's output voltage. The second diode has an identical DC chain, and therefore the same forward current, assuming the diode's dc characteristics are identical. To achieve almost identical dc characteristics, the dice in a SOT-143 are selected from adjacent sites on a wafer, thus ensuring the best possible match between the two diodes. Vbias is selected in this example to give a bias current of
5 μA.

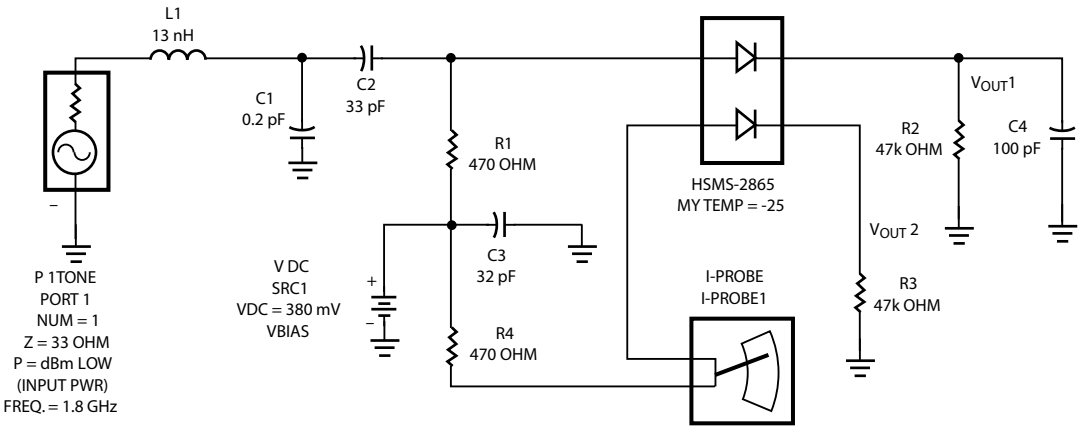


Figure 1. Diode Detector Circuit

At the node Vout1 there will be a DC voltage equal to the detected voltage Vo, plus the forward voltage, Vf, due to DC bias. At Vout2 there will only be Vf, the forward voltage generated by the dc bias. As we are measuring the voltage across Vout1 and Vout2, we should only be measuring Vo, the detected voltage. Any variation in Vf due to temperature should be cancelled.

As the input power and temperature are varied the S11 of the diode circuit will also vary. This variation is seen in Figure 8 (further detail on Large Signal S-Parameter simulation is given later). The reason for this S11 variation with input power can be easily seen in the junction resistance (Rj) and the saturation current (Is) calculations below.

$$Rj = \frac{nkT}{Is + Io}$$

$$Is = Iso\left(\frac{T}{298}\right)^{\frac{2}{n}} e^{-4060\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Where:

Rj = Junction Resistance
n = Diode Ideality Factor

k = Boltzmann's constant
T = Temperature in ° Kelvin
Is = Saturation Current
Io = Bias Current
Iso = Saturation current at 25°C

The denominator of the junction resistance equation is the diode's own saturation current and the externally applied bias current, Io. Within the circuit, there will also be a third current, the circulating current,
Ic = Vo/RL, produced by the rectification in the diode. Under small signal operation Ic is very much less than Is, and can therefore be ignored. However, as the input levels are increased, and the diode is moved into the non-linear region of operation, Ic will increase and cause a corresponding change in Rj and hence change the input impedance of the circuit.

The Output voltage is generated across R2 and R3, with the measurement being taken across nodes Vout1 and Vout2.

Diode Modeling

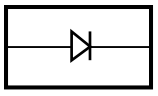
To simulate the diode performance in ADS, the non-linear PN junction diode model was used (The PN junction model can be used for a Schottky diode, assuming that Eg is set to 0.69). Avago Technologies publishes SPICE models for all of its Schottky diodes. These parameters can be entered into the model as seen in Figure 2. Before the diode model can be effectively used the package model[3] must also be included (contact Avago Technologies for further details on package models). This can be achieved by using lumped element components. The finished model for the HSMS-2865 diode can be seen in Figure 3.

The Diode model in Figure 2 specifies Tnom, the nominal temperature at which the SPICE parameters were extracted. By default this parameter is set to 27°C.

The PN junction diode symbol within ADS has the facility to set the physical temperature of operation. This temperature is different than the model Tnom. When a temperature is entered at the symbol level, ADS will scale Eg, Is, Isr, Cjo, and Vj[4].

Modifying the component variable my_temp to the desired value varies the diode temperature. The variable my_temp is seen in Figure 1 and Figure 3.

A confirmation of the temperature scaling can be seen from the simulated diode VI curves shown in Figure 4.



DIODE MODEL
b286DIE

Is = 5e - 8	Isr
Rs = 5	Nr
N = 1.08	Ikf
Ti =	Nbv
Cjo = 0.18e - 12	Ibvl
Vj = 0.65	Nbvl
M = 0.5	Tnom
Eg = 0.69	Ffe
Imax	
Xti = 2	
Kf	
Af	
Fc	
Bv = 7	
Ibv = 10 e - 5	

Figure 2. HSMS-286X Die Model

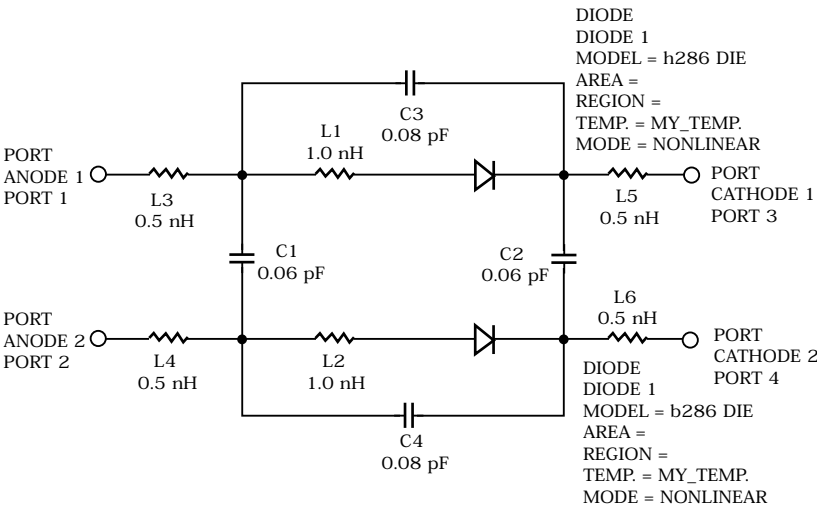


Figure 3. HSMS-2865 Packaged Diode Model

Non-Linear Circuit Simulation

A simulation of the DC (Video) output voltage of the circuit versus RF input power can be achieved by using the Harmonic Balance simulator. Figure 5 shows the simulator configuration, with associated variables.

The desired DC output voltage from the circuit is measured between node Vout1 and Vout2. To output this voltage from the simulator you can use the equation Vfc as shown in Figure 5. The Vfc function is used to measure a frequency selective voltage between two nodes.
[Our_vfc = vfc (vnode1, vnode2, Freq)]. In this example, our _vfc = vfc (Vout1, Vout2, 0 GHz).

This simulation was repeated three times, once at -25°C, 25°C, and 75°C. Each time the my_temp variable is set to the appropriate value, and the circuit is simulated using a different dataset (This enables all three temperatures to be displayed on the same graph). Figure 7 shows the results of the simulations. A close-up of the temperature variation can be seen in Figure 9.

By changing the circuit simulator from Harmonic Balance to Large Signal S-Parameters (LSSP) you can measure the S11 of the circuit against RF input power and temperature. Figure 6 shows the simulator configuration for LSSP analysis.

Figure 8 shows the results of this simulation, indicating that the match remains very good over a broad range of input power and temperature.

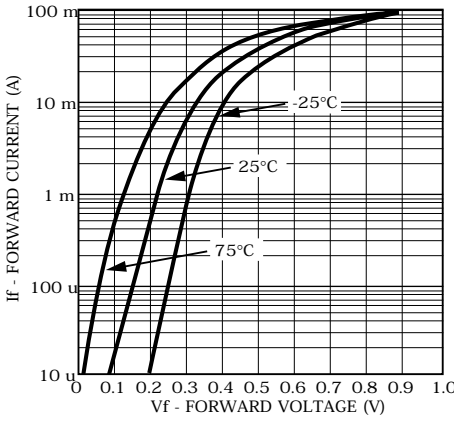


Figure 4. If vs. Vf over Temperature

MEAS EQN
Vfc
Vfc1
OUR_Vfc = Vfc(V_{OUT1}, V_{OUT2}, 0 M

VAR EQN
VAR
VAR1
INPUT _PWR = 0

HARMONIC BALANCE

HARMONIC BALANCE
HB1
FREQUENCY[1] = 1.8 GHz
ORDER[1] = 3
SWEEP VAR = "INPUT_PWR"
START = -25
STOP = 15
STEP = 1

Figure 5. Harmonic Balance Simulation Configuration

Summary

This application note has demonstrated a useful technique for accurately simulating diode detector circuit performance against RF power and temperature using Avago Technologies EEsof ADS software.

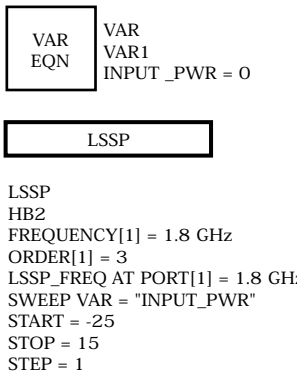


Figure 6. LSSP Simulator Configuration

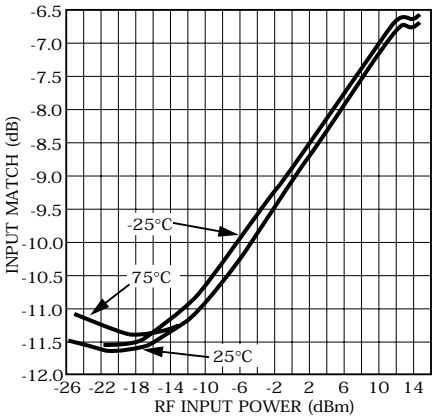


Figure 8. Input Match (S11) vs. RF Input Power

References

2. Avago Technologies Application Note 956-4, *Schottky Diode Voltage Doubler*
3. Avago Technologies Application Note 1124, *Linear Models for Diode Surface Mount Packages*
4. Avago Technologies EEsof *Circuit Components Manual for ADS*

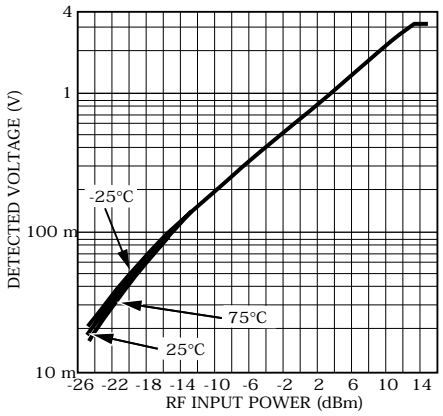


Figure 7. Detector Output Voltage vs. RF Input Power Over Temperature

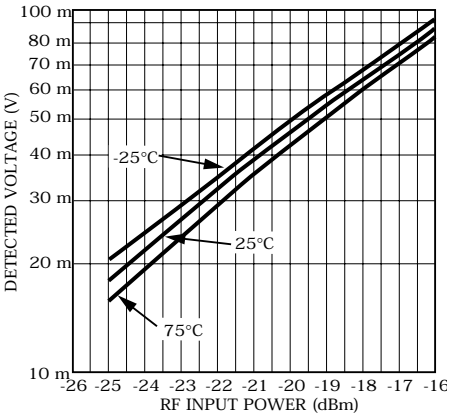


Figure 9. Close-up of Temperature Variation

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