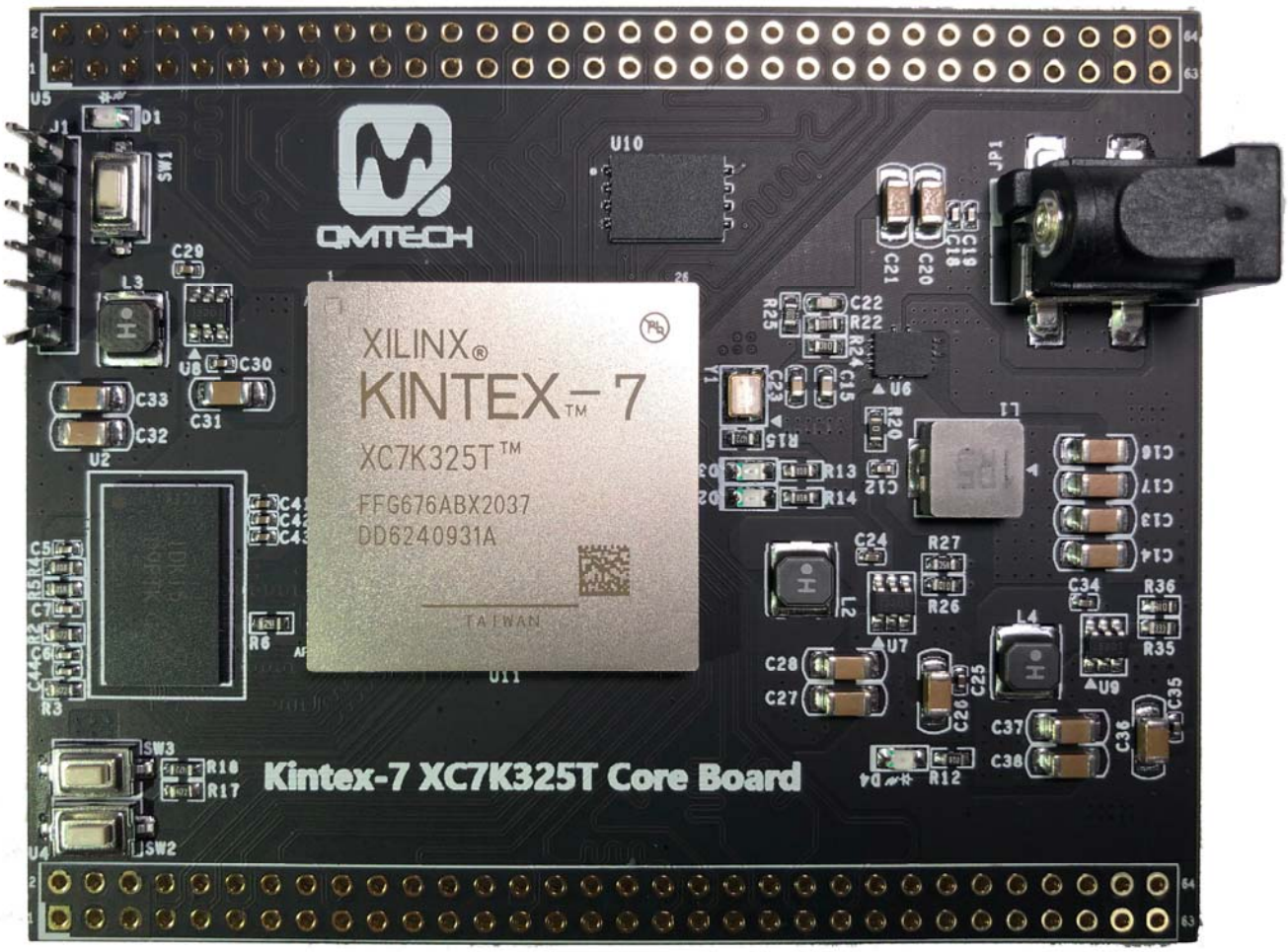
QMTECH XC7K325T CORE BOARD

USER MANUAL



Preface

The QMTECH® XC7K325T core board uses Xilinx Kintex®-7 devices to demonstrate best price/performance/watt at 28nm while giving you high DSP ratios, cost-effective packaging, and support for mainstream standards like PCIe® Gen3 and 10 Gigabit Ethernet. The Kintex-7 family is ideal for applications including 3G and 4G wireless, flat panel displays, and video over IP solutions.

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1. Introduction

1.1 Document Scope

This demo user manual introduces the QMTECH XC7K325T core board and describes how to setup the core board running with application software Xilinx Vivado 2018.3. Users may employee the on board rich logic resource FPGA XC7K325T-1FFG676C and large DDR3 memory MT41K128M16 to implement various applications. The core board also has 108 non-multiplexed FPGA IOs for extending customized modules, such as UART module, CMOS/CCD camera module, LCD/HDMI/VGA display module etc.

1.2 Kit Overview

Below section lists the parameters of the QMTECH XC7K325T core board:

- On-Board FPGA: XC7K325T-1FFG676C;
- On-Board FPGA external crystal frequency: 50MHz;
- XC7K325T-1FFG676C has rich block RAM resource up to 16,020Kb;
- XC7K325T-1FFG676C has 326,080 logic cells;
- On-Board S25FL256L SPI Flash, 32M bytes for user configuration code;
- On-Board 256MB Micron DDR3, MT41K128M16JT-125:K;
- On-Board core power supply for FPGA by using MP8712 wide input range DC/DC, it can provide 12A continuous/15A peak output current;
- XC7K325T core board has two 64p, 2.54mm pitch headers for extending user IOs. All IOs are precisely designed with length matching;
- XC7K325T core board has 3 user switches;
- XC7K325T core board has 4 user LEDs;
- XC7K325T core board has JTAG interface, by using 6p, 2.54mm pitch header;
- XC7K325T core board PCB size is: 6.7cm x 8.4cm;
- Default power source for board is: 2A@5V DC, the DC header type: DC-050, 5.5mmx2.1mm;

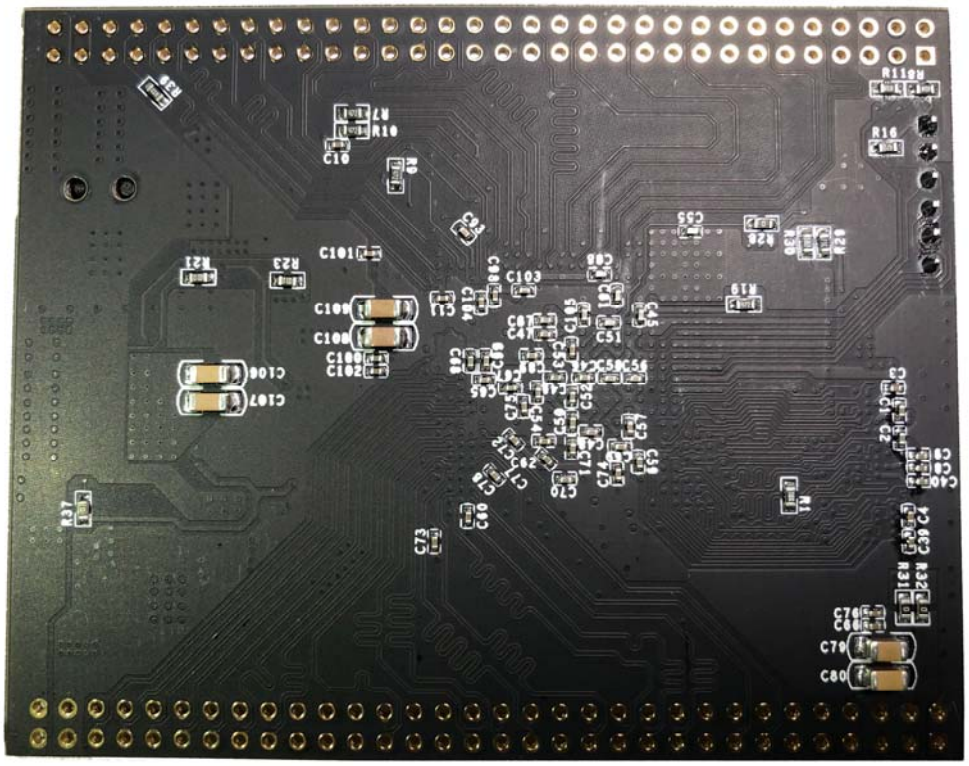


Figure 1-1. QMTECH XC7K325T Core Board Bottom View

2. Getting Started

Below image shows the dimension of the QMTECH XC7K325T core board: 6.71cm x 8.41cm. The unit in below image is millimeter(mm).

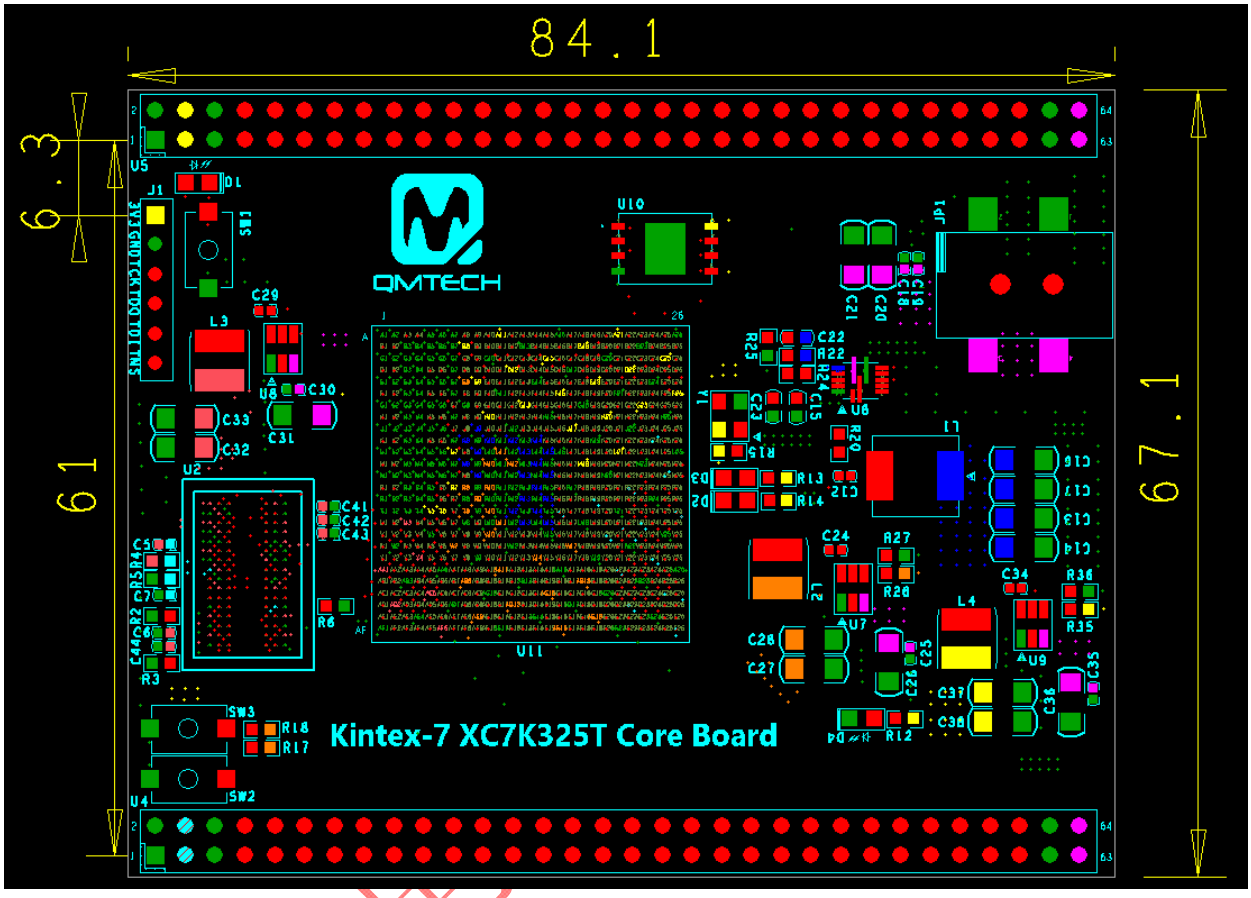


Figure 2-1. QMTECH XC7K325T Core Board Dimension

2.1 Install Development Tools

The QMTECH XC7K325T core board tool chain consists of Xilinx Vivado 2018.3(Preppared by Client), Xilinx USB platform cable(Preppared by Client), XC7K325T core board and 5V DC power supply. Below image shows the Xilinx Vivado 2018.3 development environment which could be downloaded from Xilinx office website:

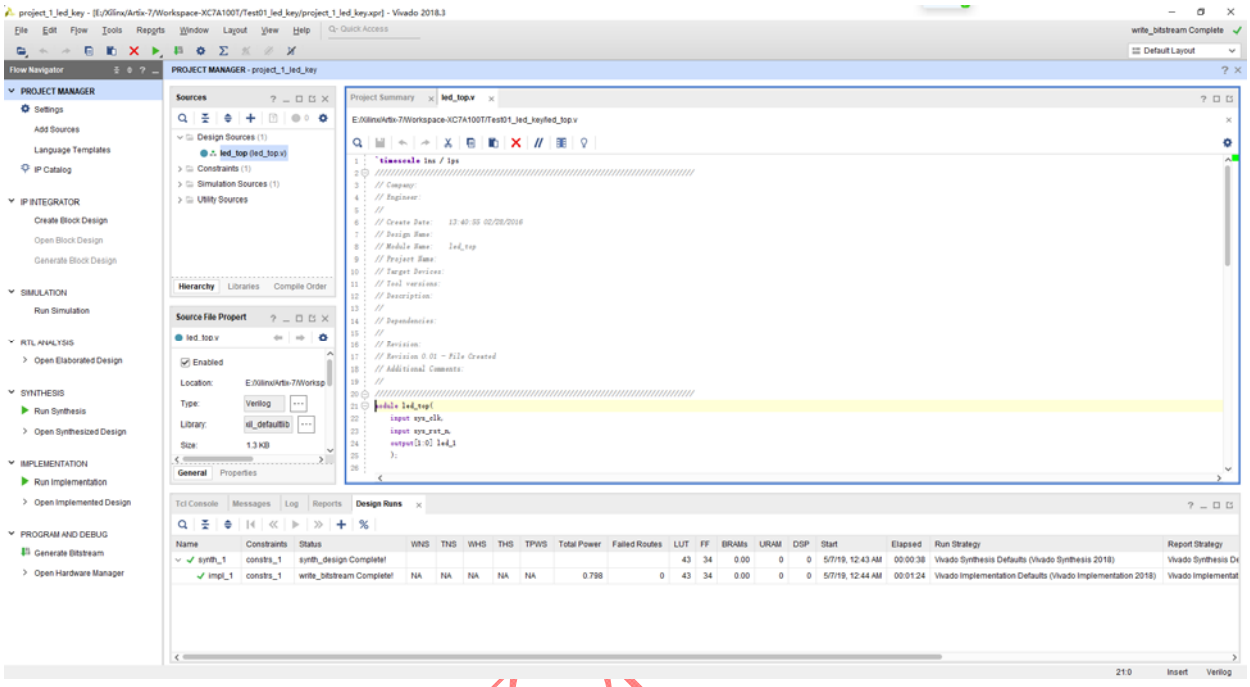


Figure 2-2. Vivado 2018.3

Below image shows the JTAG connection between Xilinx USB platform cable and XC7K325T core board:

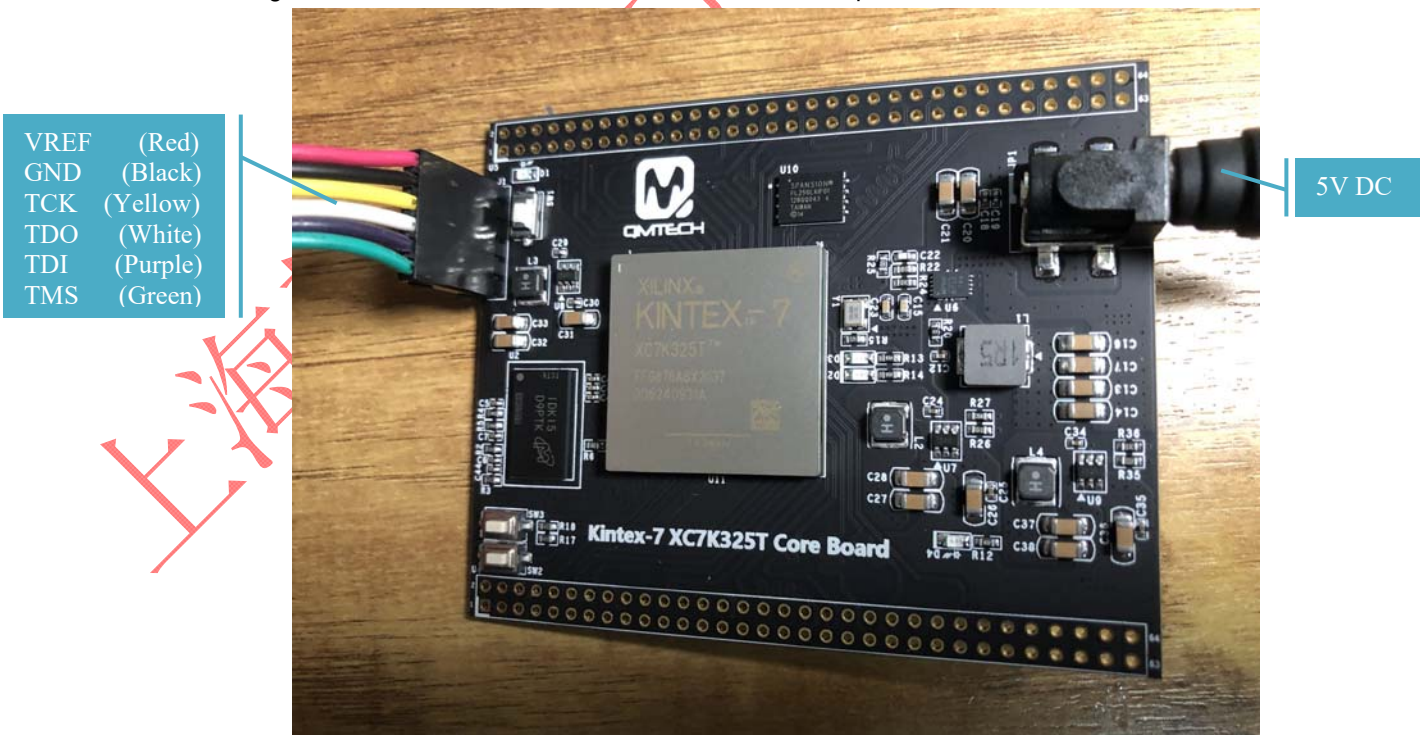
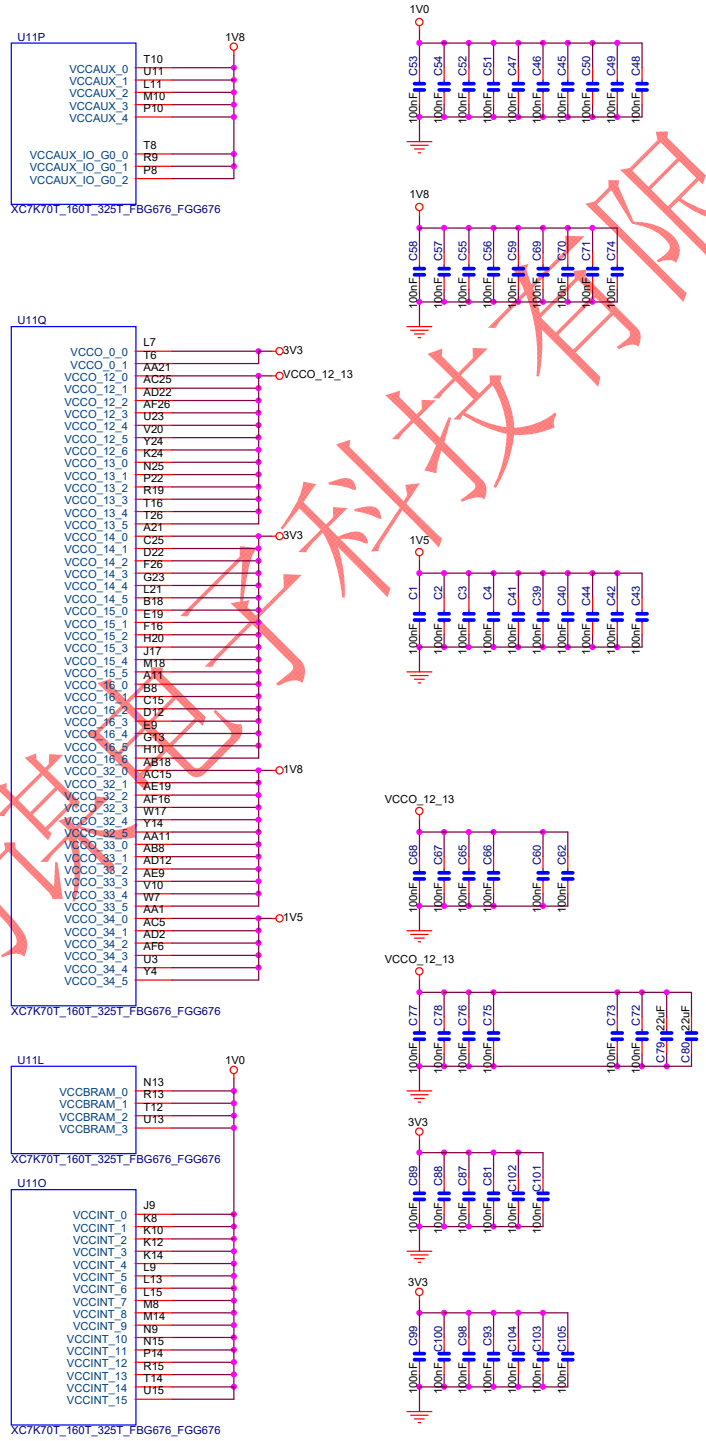


Figure 2-3. JTAG Connection and Power Supply

2.2 QMTECH XC7K325T Core Board Hardware Design

2.2.1 FPGA Power Supply

The core board needs 5V DC input as power supply which could be directly injected from power header **OR** the 64P female header U4/U5. The on board LED D4 indicates the 3.3V supply status, it will be turned on when the 5V power supply is active. In default status, all the FPGA banks IO power level is 3.3V because bank power supply is 3.3V. However, BANK12 and BANK13 IO's voltage level can be changed according to detailed custom requirement. There're two 0 ohm resisters can be removed: R31/R32, and instead the BANK12 and BANK13's power supply can be injected from 64P female header U4. Detailed design refers to HW schematic.



2.2.1 FPGA 1.0V Core Power Supply

The FPGA's power on sequence is as this: 1.0V -> 1.8V -> 1.5V & 3.3V. The FPGA core voltage 1.0V power supply is using high efficiency DC/DC chip MP8712 provided by MPS Inc. The MP8712 supports wide voltage input range from 3V to 18V. In normal use case, 5V DC power supply is suggested to be applied on the board. Below image shows the MP8712 hardware design:

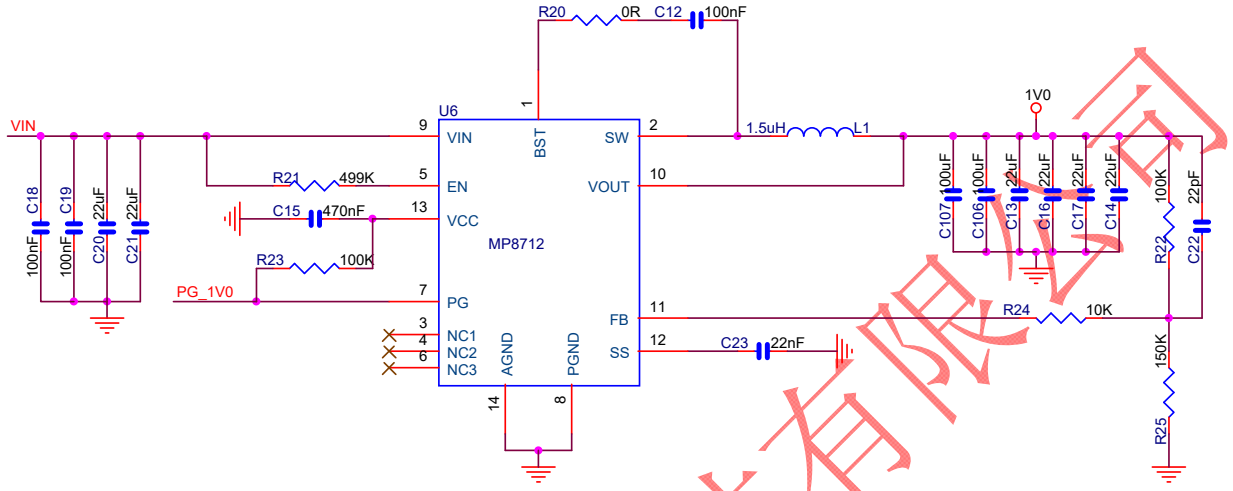


Figure 2-4. MP8712 Hardware Design

2.2.2 System Clock

FPGA chip XC7K325T-1FFG676C has system clock frequency 50MHz which is directly provided by external crystal. The crystal is designed with high accuracy and stability with low temperature drift 10ppm/° c. Below image shows the detailed hardware design:

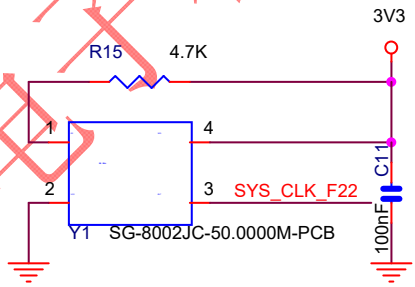


Figure 2-5. 50MHz System Clock

2.2.3 SPI Flash Boot

In default, the FPGA XC7K325T boots from external SPI Flash, detailed hardware design is shown in below figure. The SPI flash is using S25FL256L manufactured by Infineon(Spansion), with 256Mbit memory storage.

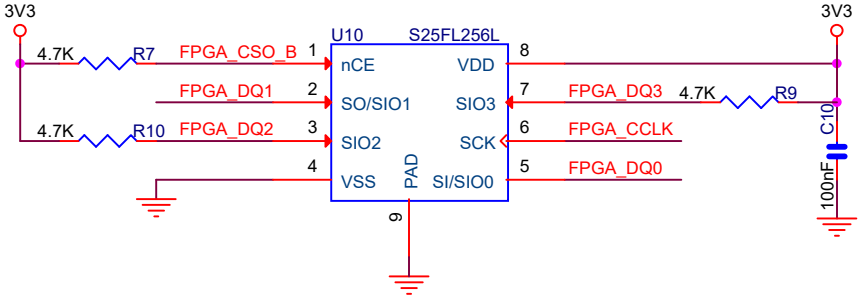


Figure 2-6. SPI Flash

The FPGA boot sequence setting M0:M1:M2 is configured as 1:0:0 which indicates FPGA will boot from SPI Flash after power on.

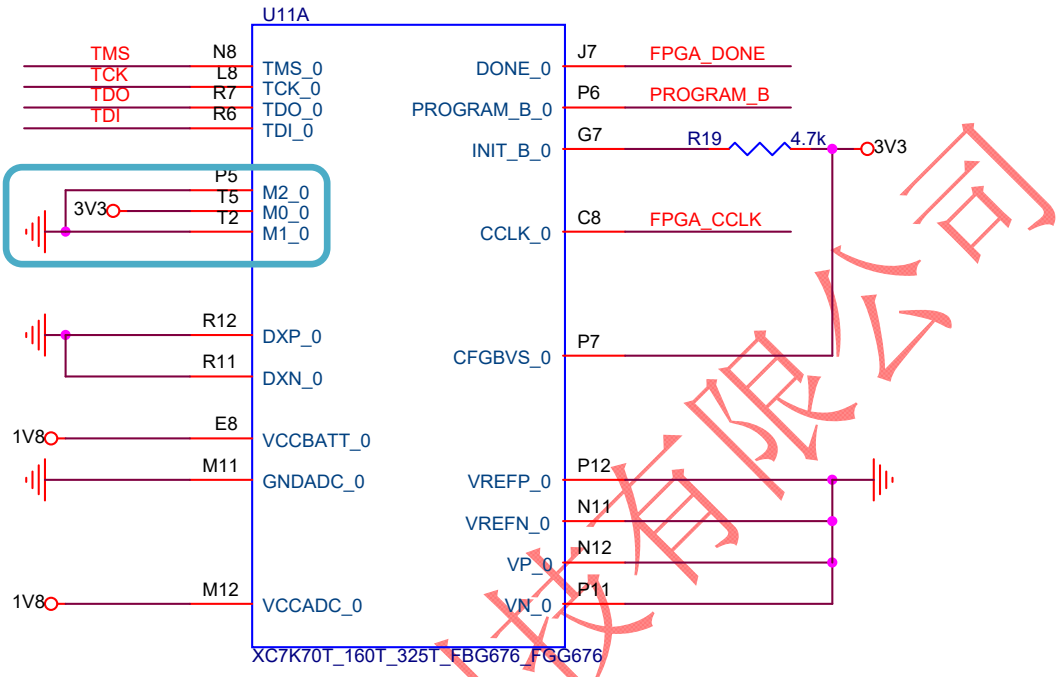


Figure 2-7. M0:M1:M2 Hardware Settings

The LED D1 will be turned on after the FPGA successfully loading configuration file from SPI Flash during power on stage. In this case, LED D1 could be used as FPGA loading status indicator.

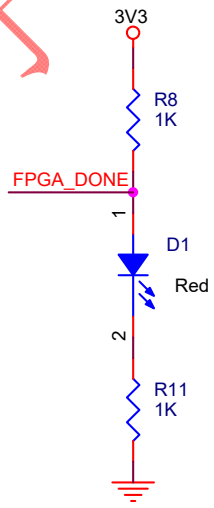


Figure 2-8. FPGA_DONE Status Indicator

2.2.4 User Extension IOs

The core board has two 64P 2.54mm pitch female headers which are used for extending user modules, such as ADC/DAC module, audio/video module, ethernet module, etc.

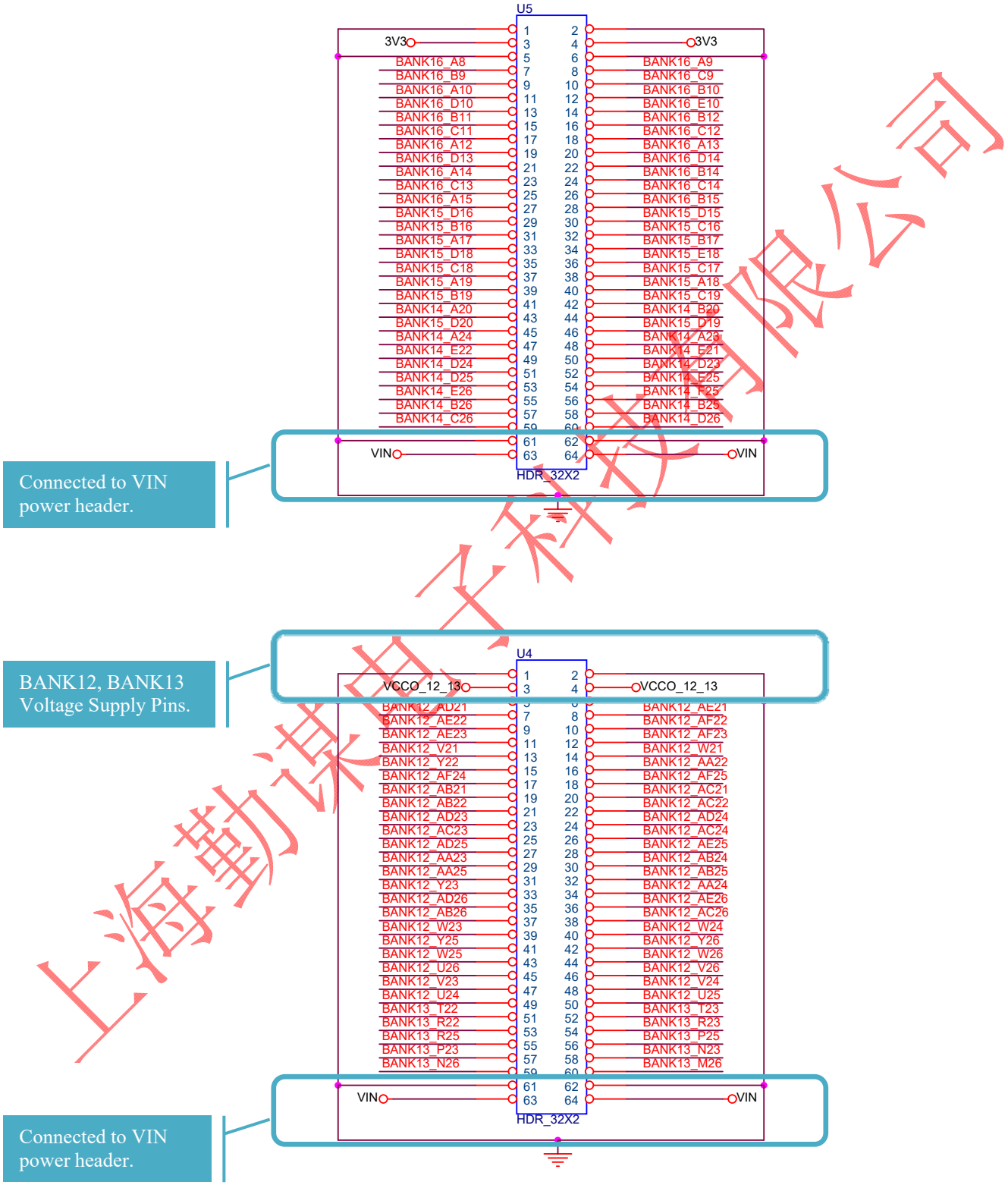


Figure 2-9. Extension IO

2.2.5 JTAG Port

The on board JTAG port uses 6P 2.54mm pitch header which could be easily connected to Xilinx USB platform cable. Below image shows the hardware design of the JTAG port:

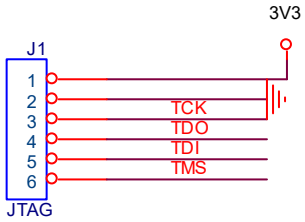


Figure 2-10. JTAG Port

2.2.6 User LEDs

Below image shows two user LEDs, one 3.3V power supply indicator and FPGA_DONE signal indicator:

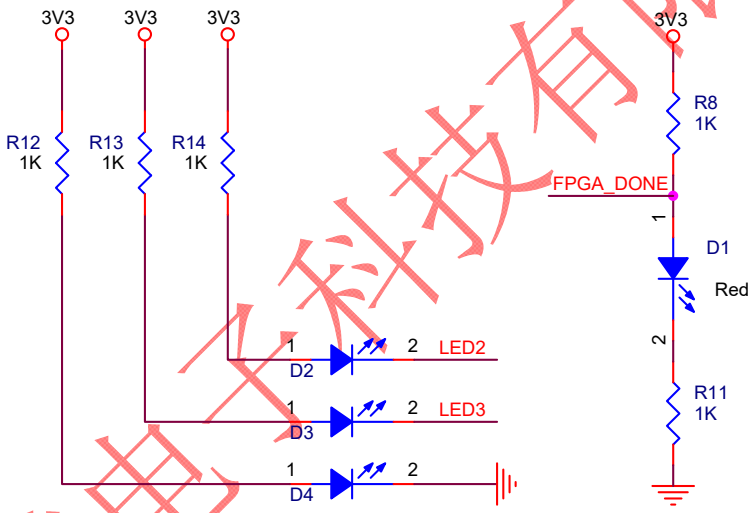


Figure 2-11. LEDs

2.2.7 User Keys

Below image shows the PROGRAM_B key and two user keys:

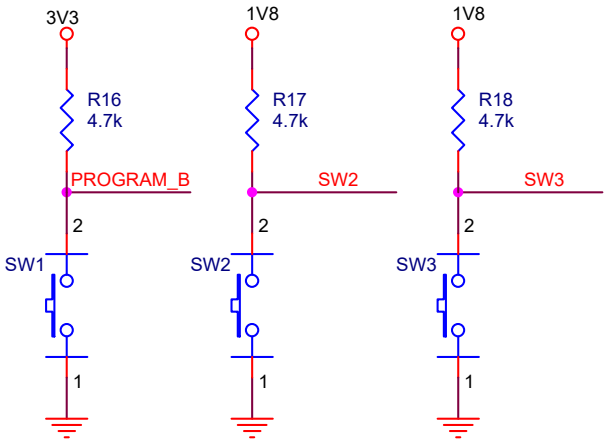


Figure 2-12. Keys

2.2.8 DDR3 Memory

The core board has on board 16bit width data bus, 256MB memory size DDR3 MT41K128M16JT-125:K provided by Micron. Below image shows the detailed hardware design:

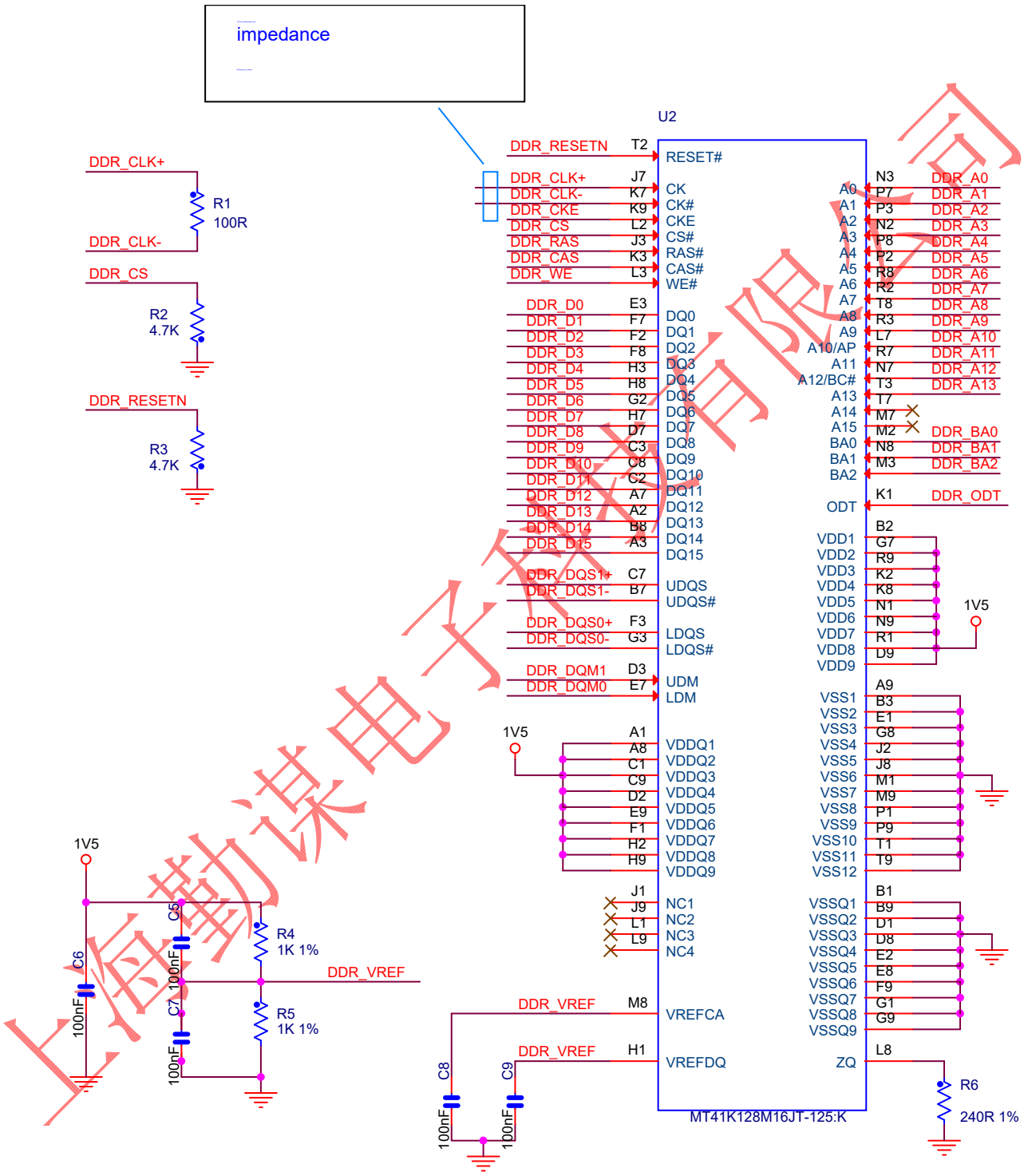


Figure 2-13. DDR3

3. Reference

[1] ug470_7Series_Config.pdf
[2] ds182_Kintex_7_Data_Sheet.pdf
[3] ug475_7Series_Pkg_Pinout.pdf
[4] S25FL256L_S25FL128L_256-MB_32-MB_128-MB_16-MB_3.0_V_FL-L_FLASH_MEMORY.pdf
[5] MT41K128M16.pdf
[6] TPS563201.pdf
[7] MP8712.PDF

4. Revision

Doc. Rev.	Date	Comments
0.1	01/12/2021	Initial Version.
1.0	10/12/2021	V1.0 Formal Release.