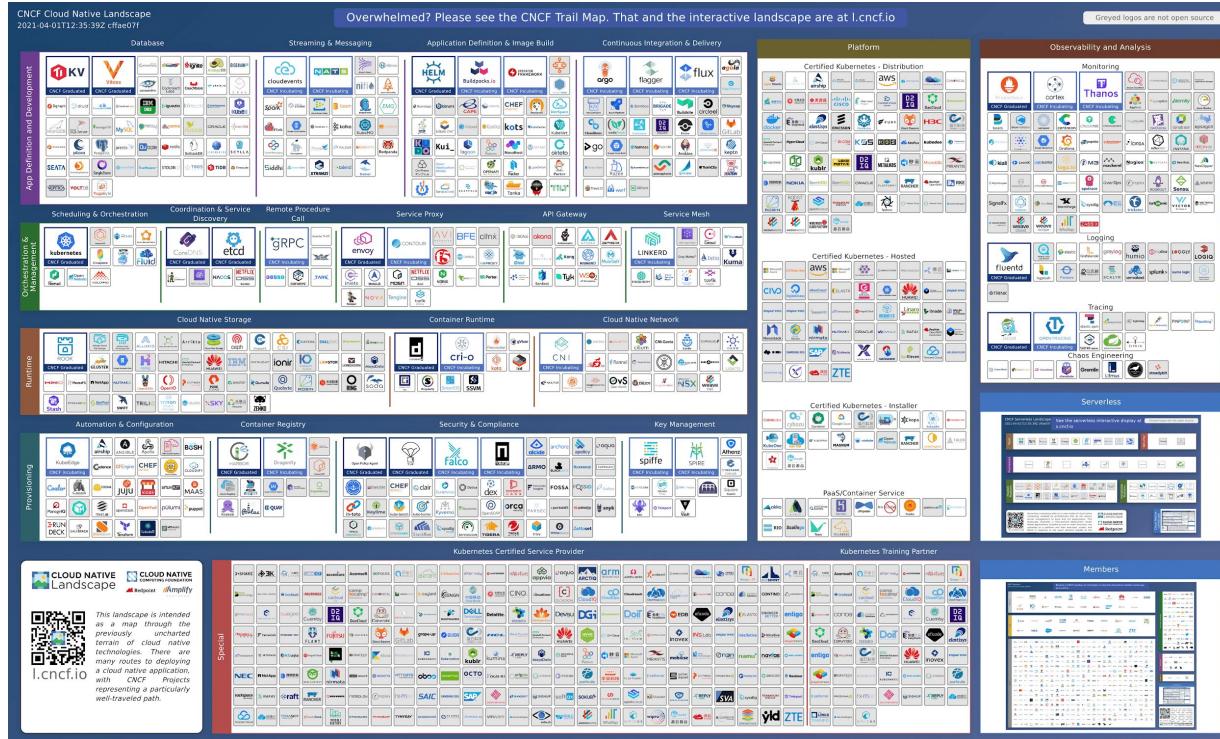




# RISC-V: The Lowest Layer of the Cloud-Native Landscape

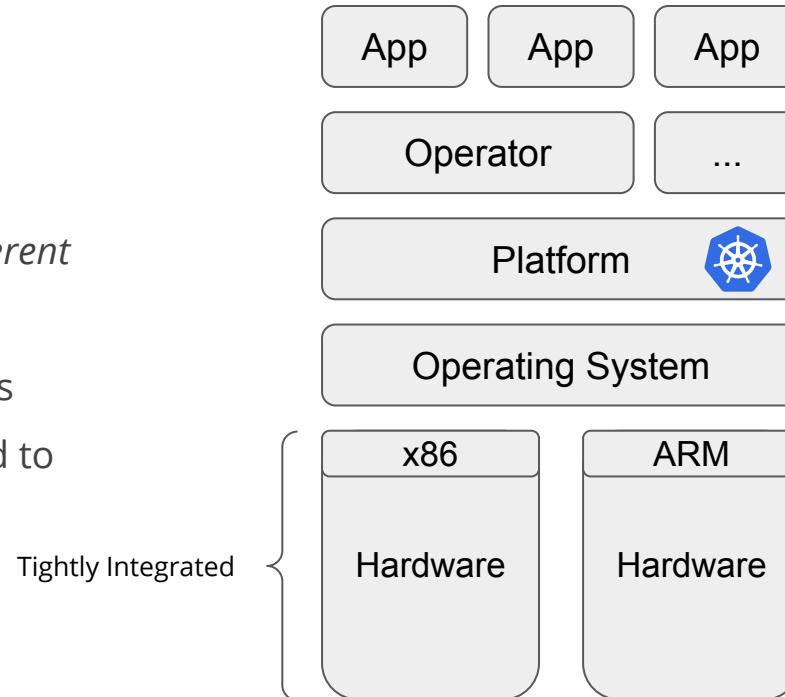
Carlos Eduardo - RISC-V Ambassador / Cloud Architect, Red Hat  
Daniel Mangum - Senior Software Engineer, Upbound

# State of the Cloud-Native Landscape



# What's Missing?

- Our stack of open source software is built on a foundation of proprietary hardware.
- Proprietary is *not bad*, it just has *different tradeoffs*.
- The proprietary hardware we use has served us quite well, why do we need to change?



# Why Should I Care?

- **Moore's Law (1965)**: number of transistors in ICs will double every year
- **Dennard Scaling (1974)**: as size of transistors shrinks, power density remains the same
- Physical limitations are causing the industry to rethink performance.
- Hardware will continue to accelerate software through the use of **Domain Specific Acceleration**.

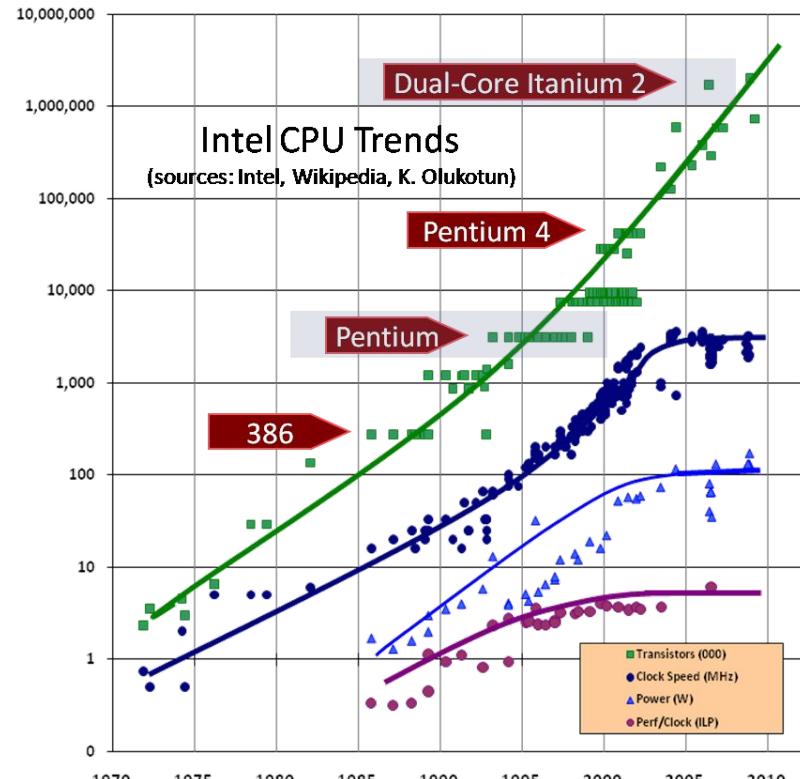
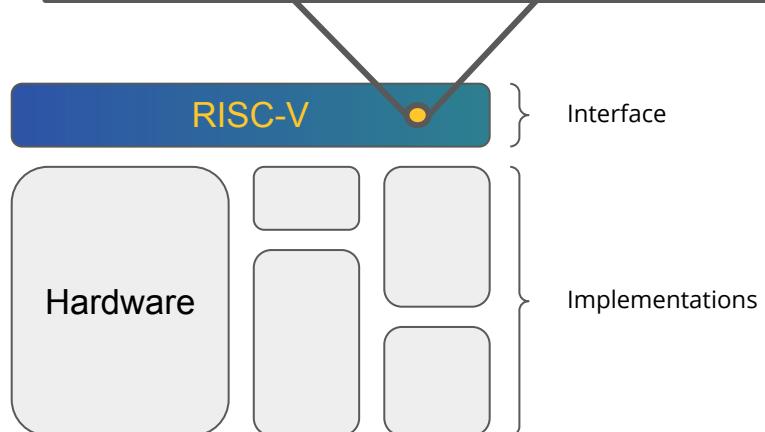


Image Credit: *The Free Lunch Is Over: A Fundamental Turn Toward Concurrency in Software*,  
Herb Sutter

# What is RISC-V?

- Open source Instruction Set Architecture (ISA)
- Modular: Built to be extended.
- Decouples the *interface* from the *implementation*.
- Heterogeneous hardware necessitates an open source ISA in order to maintain consistent software toolchains.

Name	Description	Version	Status
RV32I	Base Integer Instructions, 32 bit	2.0	Final
RV32E	Base Integer Instructions, 32 bit, embedded	1.9	Open
RV64I	Base Integer Instructions, 64 bit	2.0	Final
RV128I	Base Integer Instructions, 128 bit	1.7	Open
Q	Standard Extension Quad-precision Floating Point	2.0	Final
L	Standard Extension Decimal Floating Point	0.0	Open
C	Standard Extension Compressed Instructions	2.0	Final
B	Standard Extension Bit Manipulation	0.36	Open
M	Standard Extension Integer Multiply and Divide	2.0	Final
A	Standard Extension Atomic Instructions	2.0	Final
F	Standard Extension Single-precision Floating Point	2.0	Final
D	Standard Extension Double-precision Floating Point	2.0	Final
J	Standard Extension Dynamically Translated Languages	0.0	Open
T	Standard Extension Transactional Memory	0.0	Open
P	Standard Extension Packed SIMD Operations	0.1	Open
V	Standard Extension Vector Operations	0.2	Open
N	Standard Extension User Level Interrupts	1.1	Open



# Kubernetes on RISC-V



# Lots of Pull Requests later

Project	Description	Pull Request	Upstream
go/net	ipv4, ipv6, internal/socket: add riscv64 support	<a href="https://github.com/golang/net/pull/43">https://github.com/golang/net/pull/43</a>	✓
go/sys	unix: add riscv64 tag to endian_little.go	<a href="https://github.com/golang/sys/pull/10">https://github.com/golang/sys/pull/10</a>	✓
mattn/go-isatty	Update x/sys to support Risc-V	<a href="https://github.com/mattn/go-isatty/pull/1">https://github.com/mattn/go-isatty/pull/1</a>	✓
creack/pty	Add riscv64 support	<a href="https://github.com/creack/pty/pull/1">https://github.com/creack/pty/pull/1</a>	✓
docker/cli	Add riscv64 to manifest annotation and bash completion	<a href="https://github.com/docker/cli/pull/1">https://github.com/docker/cli/pull/1</a>	✓
opencontainers/runc	Bump x/sys and update syscall for initial Risc-V support	<a href="https://github.com/opencontainers/runc/pull/1">https://github.com/opencontainers/runc/pull/1</a>	✓
moby/moby	bump x/sys to fix riscv64 epoll	<a href="https://github.com/moby/moby/pull/1">https://github.com/moby/moby/pull/1</a>	
moby/moby	Update modules to support riscv64	<a href="https://github.com/moby/moby/pull/2">https://github.com/moby/moby/pull/2</a>	
moby/moby	allow dockerd builds without cgo - Tonis	<a href="https://github.com/moby/moby/pull/3">https://github.com/moby/moby/pull/3</a>	
containerd/containerd	bump x/sys to fix riscv64 epoll	<a href="https://github.com/containerd/containerd/pull/1">https://github.com/containerd/containerd/pull/1</a>	
containerd/containerd	Update x/sys, x/net and bbolt modules to support Risc-V architecture	<a href="https://github.com/containerd/containerd/pull/2">https://github.com/containerd/containerd/pull/2</a>	
docker/cli	bump x/sys to fix riscv64 epoll	<a href="https://github.com/docker/cli/pull/2">https://github.com/docker/cli/pull/2</a>	✓
docker/libnetwork	bridge: add riscv64 build tags - Tonis	<a href="https://github.com/docker/libnetwork/pull/2389">https://github.com/docker/libnetwork/pull/2389</a>	✓
LK4D4/vndr	add riscv64 support	<a href="https://github.com/LK4D4/vndr/pull/80">https://github.com/LK4D4/vndr/pull/80</a>	✓
vishvananda/netns	add riscv64 architecture	<a href="https://github.com/vishvananda/netns/pull/34">https://github.com/vishvananda/netns/pull/34</a>	✓
containers/libpod	build: allow to build without cgo on RISC-V	<a href="https://github.com/containers/libpod/pull/3437">https://github.com/containers/libpod/pull/3437</a>	✓

20+ Projects  
40+ PRs  
6 CNCF Projects  
95%+ Upstream

# Container images for RISC-V

## OpenFaaS:

- faas-gateway - [carlosedp/faas-gateway:riscv64](#)
- faas-basic-auth-plugin - [carlosedp/faas-basic-auth-plugin:riscv64](#)
- faas-swarm - [carlosedp/faas-swarm:riscv64](#)
- faas-netes - [carlosedp/faas-netes:riscv64](#)
- nats-streaming - [carlosedp/faas-nats-streaming:riscv64](#)
- queue-worker - [carlosedp/faas-queue-worker:riscv64](#)
- watchdog - [carlosedp/faas-watchdog:riscv64](#)
- Function base - [carlosedp/faas-debianfunction:riscv64](#)
- Figlet - [carlosedp/faas-figlet:riscv64](#)
- MarkdownRender - [carlosedp/faas-markdownrender:riscv64](#)
- QRCode - [carlosedp/faas-qrcode:riscv64](#)

## Prometheus:

- Prometheus - [carlosedp/prometheus:v2.11.1-riscv64](#)
- AlertManager - [carlosedp/alertmanager:v0.18.0-riscv64](#)

## Traefik:

- traefik v2 - [carlosedp/traefik:v2.1-riscv64](#)
- whoami - [carlosedp/whoami:riscv64](#)

## Kubernetes:

- kube-apiserver - [carlosedp/kube-apiserver:1.16.0](#)
- kube-scheduler - [carlosedp/kube-scheduler:1.16.0](#)
- kube-controller-manager - [carlosedp/kube-controller-manager:1.16.0](#)
- kube-proxy - [carlosedp/kube-proxy:1.16.0](#)
- pause - [carlosedp/pause:3.1](#)
- flannel - [carlosedp/flanneld:v0.11.0](#)
- etcd (v3.5.0) - [carlosedp/etcd:3.3.10](#)
- CoreDNS (v1.6.3) - [carlosedp/coredns:v1.6.2](#)

Kubernetes images are multi-arch with manifests to arm, arm64, amd64, riscv64 and ppc64le. Some version mismatches due to Kubernetes hard-coded version check for CoreDNS and etcd.

## Misc Images:

- Echo demo - [carlosedp/echo-riscv](#)
- Whoami (Traefik demo) - [carlosedp/whoami:riscv64](#)
- Kubernetes Pause - [carlosedp/k8s-pause:riscv64](#)
- CoreDNS v1.3.0 - [carlosedp/coredns:v1.3.0-riscv64](#)

# Huge leap but help still needed

Project	Description	Status
Golang	Go programming language	<input checked="" type="checkbox"/> Already upstream in 1.15. Pending binary distribution
SECCOMP	Risc-V Seccomp support to Linux Kernel	<input checked="" type="checkbox"/> Upstream from Kernel 5.5
Libseccomp	Upstream libseccomp patch	<input checked="" type="checkbox"/> Already upstream
Kubernetes	Have Kubernetes build on Risc-V	<input checked="" type="checkbox"/> Builds on RISC-V. Still not officially supported.
Golang CGO	Go extension for importing C code	<input checked="" type="checkbox"/> Already merged. Available on Go 1.16 (2021)
Runc	Container Runtime in C	<input checked="" type="checkbox"/> Already can be built with Go 1.16.
Golang SQLite	File database libraries	<input checked="" type="checkbox"/> Already can be built with Go 1.16.
Official Distros	Official Linux distributions	Still pending official support from most distros (Fedora, Ubuntu, Debian, Alpine)
Official Images	Build and publish official images	Depends on distro support (Debian, Alpine, Fedora)
Most projects	Build and distribute binaries and/or images	Changes on CI/CD and official images

# Demo





# Thank You!

Contact us:

<https://twitter.com/carlosedp>

<https://twitter.com/hasheddan>

Read us:

<https://carlosedp.com>

<https://danielmangum.com>

Follow up progress on:

<https://github.com/carlosedp/riscv-bringup>

<https://hub.docker.com/u/carlosedp>

END OF  
KUBECON  
PRESENTATION  
CONTENT



# Who is RISC-V?

**RISC-V is the free and open ISA**  
... Driven through Open collaboration  
... Enabling freedom of design across all domains and industries  
... Cementing the strategic foundation of semiconductors

**Welcome to the Open era of computing!**

# Disruptive Technology

## Barriers

Complexity

Design freedom

License and Royalty fees

Design ecosystem

Software ecosystem

## Legacy ISA

1500+ base instructions

Incremental ISA

\$\$\$ – Limited

\$\$\$

Moderate

Extensive

## RISC-V ISA

47 base instructions

Modular ISA

Free – Unlimited

Free

Growing rapidly. Numerous extensions, open and proprietary cores

Growing rapidly

# Unconstrained Opportunity

## RISC-V Business Model

### Barriers removed

- Design risk
- Cost of entry
- Partner limitations
- Supply chain

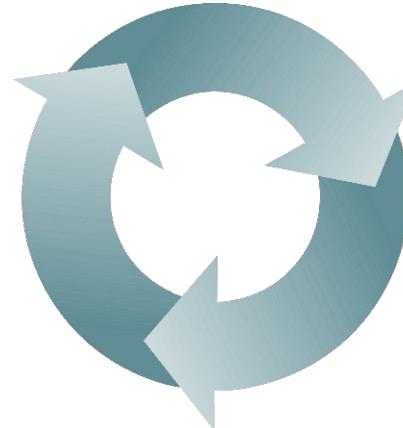
Development

Collaboration  
partners

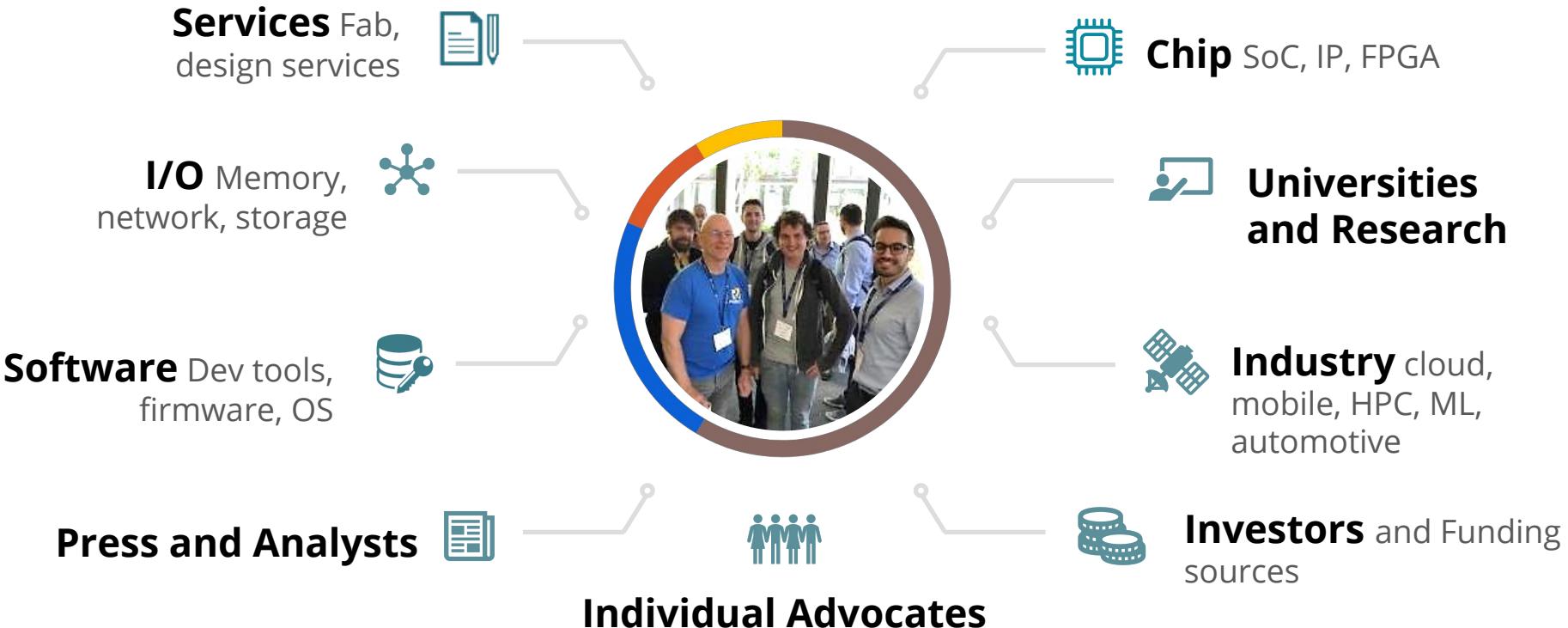
Supply chain

Expanded  
markets

Expanded  
geographies



# Dedicated Community



# RISC-V driving industry change

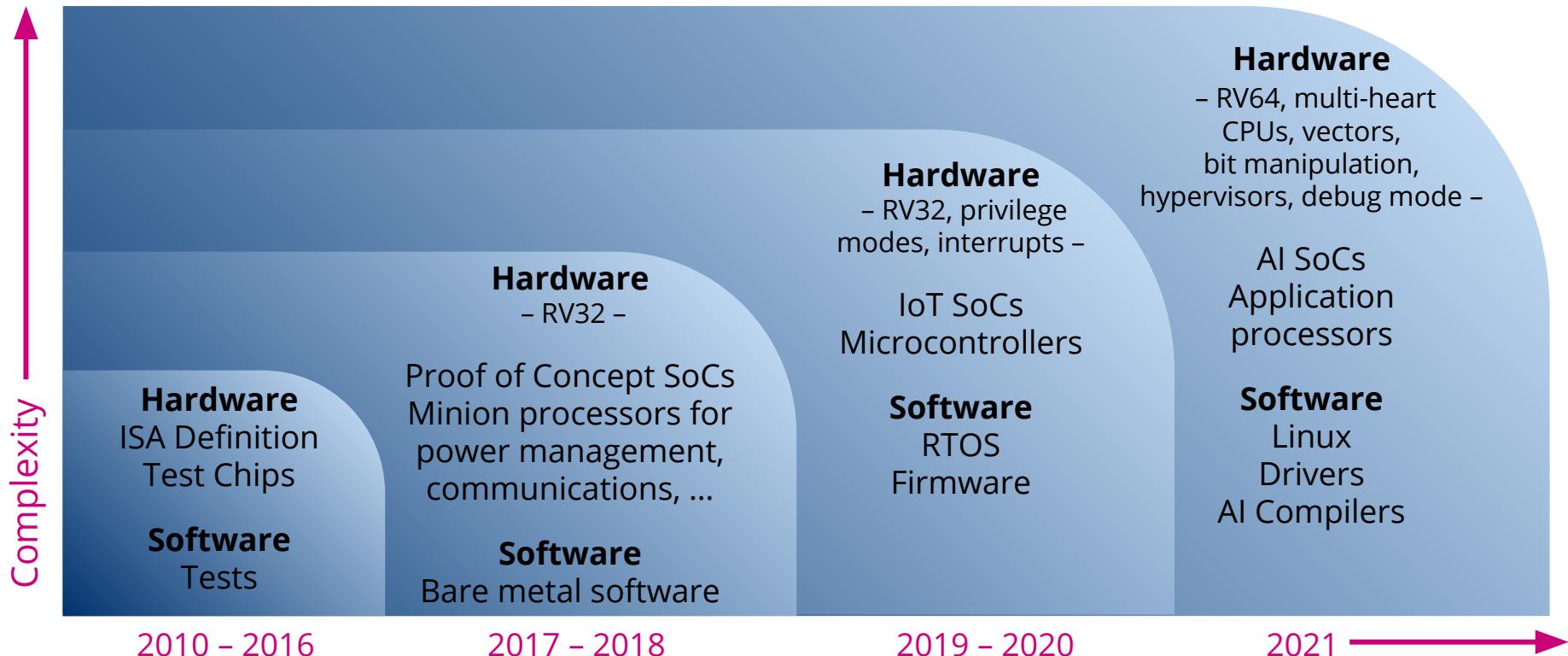
## In 2020 alone...

- ... **2,100+ individuals** in **47 RISC-V work groups** and committees, nearly triple the RISC-V groups and 54% increase in participation
- ... **259 RISC-V solutions** online including cores, SoCs, software, tools and developer boards.
- ... 70% growth in **28 local meetup** groups, with more than **4,000 engineers**
- ... We're in the news! We've **added 8,000+ followers on social media** and have participated in **100+ news articles** along with amplifying RISC-V community news 400+ times.

- ✓ **RISC-V Technical Steering Committee** to govern technical strategy, build technical leadership, and best practice decision-making
- ✓ **RISC-V Learn** encompassing university curricula, online learning, and Training Partners
- ✓ **RISC-V Ambassadors and Alliances** to reach beyond our community for industry collaboration, leadership, and technical engagement.
- ✓ **RISC-V Exchange** to showcase RISC-V cores, SoCs, developer boards, services, software, tools, and other resources.

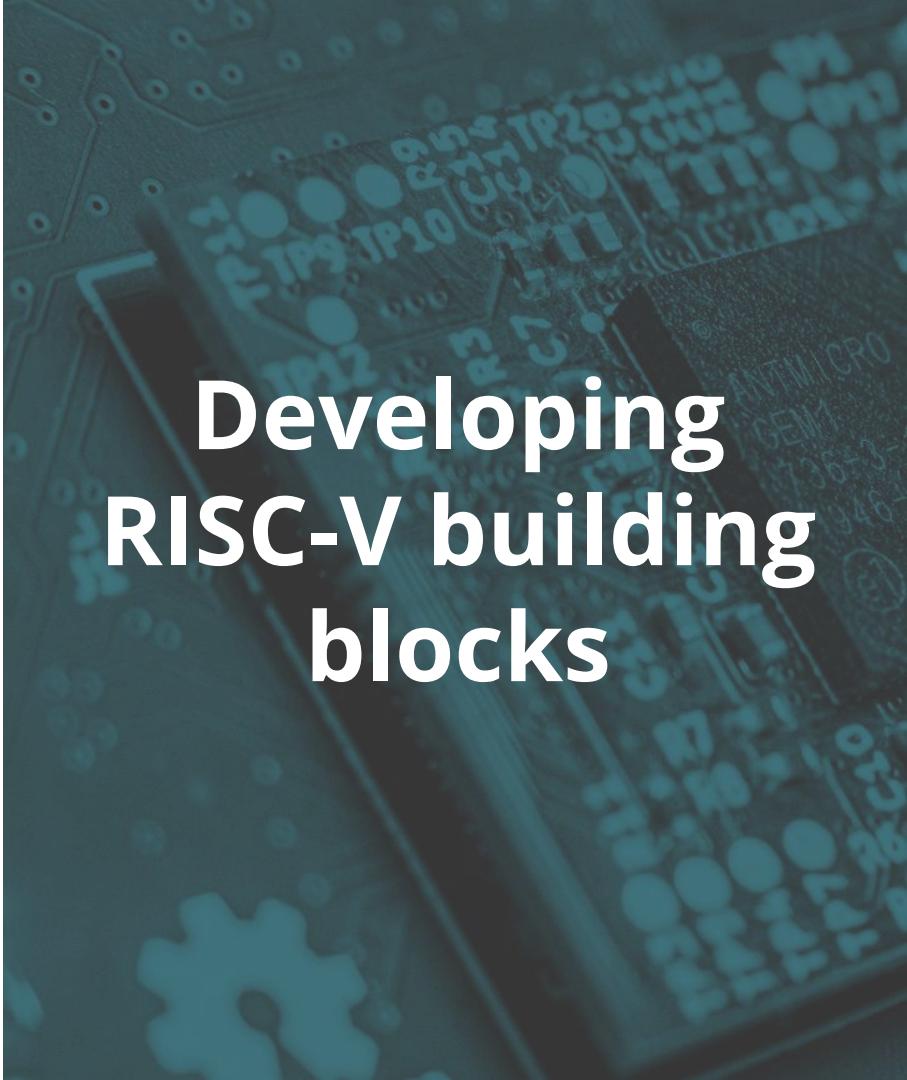


# Industry innovation on RISC-V



# Technical Progress

- Development process and deliverables are done with transparency.
- Technical Steering Committee brings industry best practice governance.
- 



Developing  
RISC-V building  
blocks

# RISC-V Visibility

- **Events** ranging from HPC, Embedded World, DAC, and Open Source Summit, to regional events in China, India, Japan, and Taiwan.
- **Blogs, announcements**, and **press briefings** generating thousands of mentions in the press.
- RISC-V solutions online via the **RISC-V Exchange** including cores, SoCs, services, software, tools and developer boards.
- **RISC-V Ambassadors** to support engineering leadership.



A photograph showing a man from the side, standing at a podium and speaking into a microphone. He is gesturing with his hands. In the foreground, the backs of several audience members' heads are visible. A large whiteboard or screen is behind him, displaying some text and diagrams.

# Building Careers

- Encouraging and Unleashing Curiousness & Innovation
- Inspiring
- Interactive experiences and projects for everyone
- Connecting People, Institutions
- Our Story is just beginning... through the power of people

## RISC-V Learn

- Connecting **universities** with 30 contributed labs, lectures, and materials to invigorate RISC-V in university curriculum.
- RISC-V **Training Partner program** together with our partners around the world to offer professional RISC-V training in a multitude of formats.
- RISC-V **online learning** to offer broad as well as deep technical knowledge to accelerate the developer experience
- RISC-V **careers and mentorship** to grow the pool of RISC-V resources.



## Cloud and data center applications

top cloud providers like Amazon and Alibaba are designing their own chips.



**Automotive** is transforming from autonomous vehicles to infotainment to safety, the whole vehicle relies on innovative electronics.



## Industrial IoT

incorporating artificial intelligence in manufacturing and industrial processes.



**Mobile and wireless** continue rapid evolution with each generation of hardware and increased capability.



**Consumer and IoT devices** bring incredible innovation and volume with billions of connected devices being in the next 5-10 years.



**Memory** was the largest semiconductor category by sales with \$158 billion in 2018, and the fastest-growing, with sales increasing

# RISC-V future is very bright



RISC-V is a community of passionate,  
dedicated, and invested stakeholders

As individuals  
As companies  
As universities  
As public institutions and non-profits  
As nations

**Build RISC-V into  
your company  
strategy, and your  
personal mission**

As one Global, connected movement

# Joining RISC-V International

---



# Meet the RISC-V Team



Calista Redmond  
CEO



Mark Himmelstein  
CTO



Kim McMahon  
Director of Visibility  
and Community  
Engagement



Stephano Cetola -  
Technical Program  
Manager



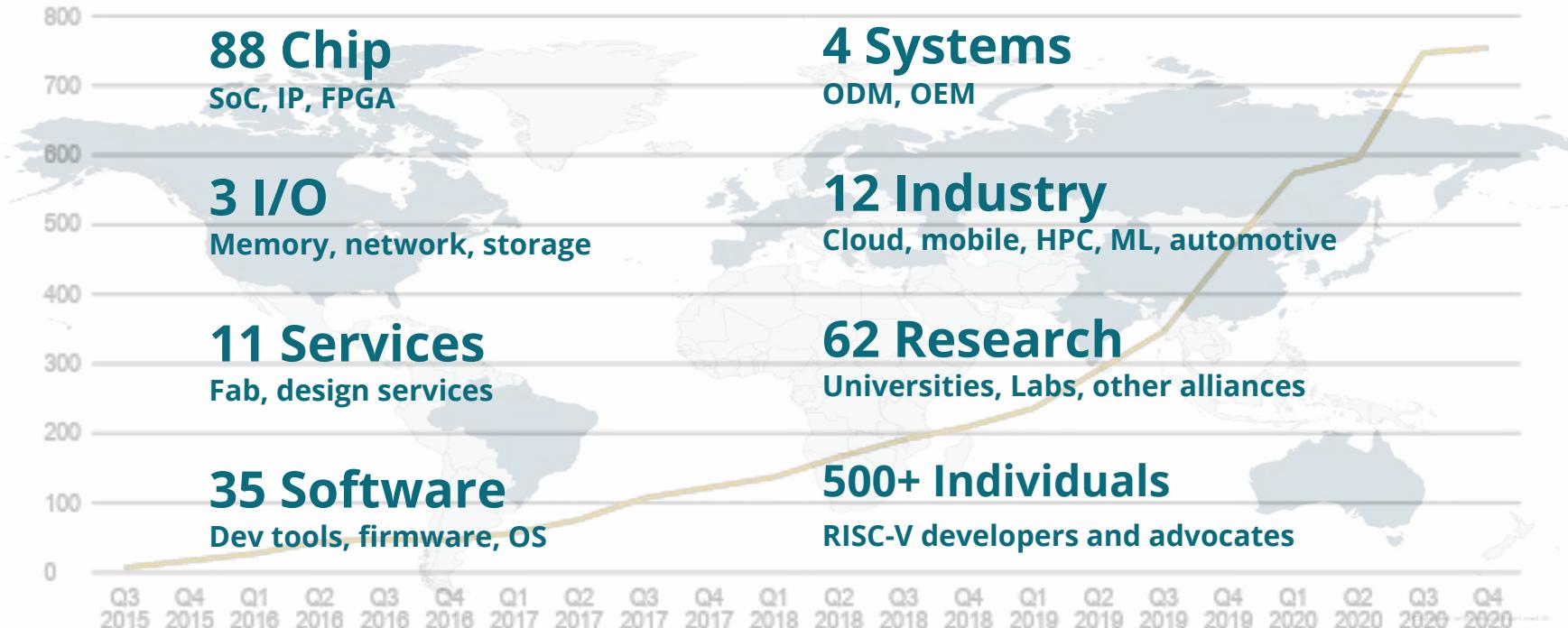
Megan Lehn  
Program Manager



Jenni McGinnis  
Program Manager

# More than 1,000 RISC-V Members!

across 50+ Countries



# Benefit of joining RISC-V

- ✓ Accelerate technical traction and insight
- ✓ Contribute technical priorities, approaches, and code
- ✓ Gain strategic and technical advantage
- ✓ Increase visibility, leadership, and market insight
- ✓ Fill and increase engineering skills, retain and attract talent
- ✓ Build innovation partner network and customer pipeline
- ✓ Deepen, engage, and lead in local and industry developer network
- ✓ Showcase RISC-V products, services, training, and resources



## Technical Deliverables

Guard against **fragmentation**

**Build** technical deliverables

**Collaborate** with technical working groups & SIGs,



## Architecture Compatibility

Testing and compatibility **suites**

Architecture **tests**



## Visibility

**Amplify** member news, content, and success with press and analysts

**Original** content programs  
RISC-V, industry, and regional **events**



## Learn

Multi-level **online learning**

Connecting **universities** with labs, tests, and curricula

RISC-V **Training Partners**



## Advocacy + Alliances

RISC-V **Ambassadors**

Geo and industry **alliances**

**Local** developer groups and events



## Marketplace Exchange

**Online marketplace** of providers, products, services, and learn

Technical developer **forums**

# RISC-V delivers incredible member support

# Membership Options



## Premier Member Benefits

- Community level benefits plus...
- Use of RISC-V Trademark for commercialization
- Board seat and Technical Steering Committee seat included for \$250k level
- Technical Steering Committee seat included for \$100k level
- Solution / Product listing highlighted on RISC-V Exchange
- 4 case studies a year
- 2 blogs per month
- 2 social media spotlights per month
- Spotlight member profile
- Inclusion in event promotions

## Premier Requirements

- Membership open to any type of legal entity
- \$250k Annual membership fee that includes Board seat and TSC seat
- \$100k Annual membership fee that includes TSC seat

## Strategic Member Benefits

- Community level benefits plus...
- Use of RISC-V Trademark for commercialization
- 3 Board reps elected for Strategic tier, includes Premier members that do not otherwise have a board seat.
- Eligible to lead workgroup and/or committee
- Solution / Product listing highlighted on the RISC-V Exchange
- 1 case study a year
- 1 blog per month
- 1 social media spotlight per month

## Strategic Member Requirements

- Membership open to any type of legal entity
- Annual membership fee based on employee size
  - 5,000+ employees: \$35k
  - 500-5,000 employees: \$15k
  - <500 employees: \$5k
  - <10 employees & company <2 yrs old: \$2k

## Community Member Benefits

- Accelerated development, reduced risk through open source, ratified ISA.
- Eligible to participate in workgroups, influence strategy and adoption
- 6 support programs in Technical Deliverables, Compliance, Visibility, Learning, Advocacy, and Marketplace
- 1 voting Academic Board rep, 1 non-voting Community Board rep
- Member logo / name listing on RISC-V website, by member level
- Event registration discount

## Community Requirements

- Membership open to
  - academic institutions,
  - non-profits,
  - individuals not representing a legal entity
- No annual membership fee

# Marketing and Visibility benefits

## Share your products and progress with RISC-V!



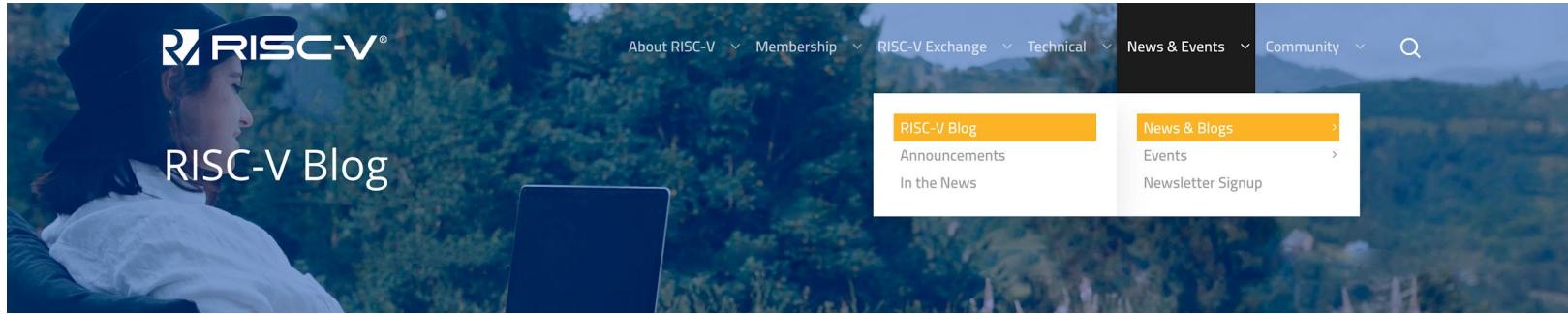
# RISC-V Events

## Participating with RISC-V in industry events

- Shows your support for open source and RISC-V
- Opportunity to demonstrate your knowledge and leadership to the community
- Demo your products and collect leads



# RISC-V Blog



The RISC-V blog and video program is a great way to showcase thought-leadership and industry commentary, as well as share technical information on your work with RISC-V.

Members can submit content to publish on RISC-V.org and we promote on social, as well as a link to the member website to drive traffic.

# Case Studies

Case studies help elevate the technical conversations to business objectives and challenges, showing the use and adoption of RISC-V across multiple industries and use cases.

**As a member, we will publish your case study!**

Case studies will be highlighted on our website and shared via our wide-reaching media channels and analyst relationships.

# Content - Social

RISC-V is happy to share community, member, and Ambassador content via our social channels!

- Members can submit original content for our posting on our social channels
- Members and the community can submit content for re-sharing.



# Press and Analysts



- Share member and community news "[In the News](#)"
- Highlight member announcements via social
- Provide RISC-V team member quotes for member press releases
- Options to submit member news and announcements and participate in media panels.

# Branding

As a member, use RISC-V branding in your marketing materials!

## Branding Guidelines and logos



# Working Groups

Join, participate, and engage with the RISC-V Community!



# Marketing Committee + Working Groups

Participate in the marketing committee to engage with your peers, learn about member marketing benefits, and contribute.

## Marketing Committee

Primary communication tool with members on RISC-V marketing initiatives.

**Meetings:** 2nd Tuesday of the month, 8am PT (5pm CEST)

## Marketing Content Committee

Discuss content topics such as website, exchange, and research.

**Meetings:** Last Tuesday of the month: 8am PT (5pm CEST)

## Marketing Events Committee

Discuss upcoming events and actions as well as event plans for future

**Meetings:** Every other Thursday: 9am PT (6pm CEST)

# Technical Working Groups

The technical groups are the heart of RISC-V. These groups create and maintain the hardware ISA and other items around it, including test and debug frameworks, software specs, and other technical artifacts. Visit our [Working Groups page](#) to find groups that fit your interests.

# Group/Meeting Types & Responsibilities

Group	Responsibilities
<b>Technical Steering Committee (TSC)</b>	Delegation of responsibilities to organizational components below it, strategy, escalations, group & chair & preliminary charter approvals, ratification, voting (most discussion and notification by email, <a href="#">web page listing and supporting docs</a> , automated voting system). The TSC has voting members and non-voting attendees. The voting members include premiers and HC and IC chairs. (non-voting attendees are advisors and RISC-V staff -- no organization can be represented more than once)
<b>Chief Technology Office (CTO)</b>	Runs TSC voting process, both Chairs meetings, Strategy, organization, IT, roadmap, resources, escalations,
<b>ISA Committees (IC)</b>	Approve and oversee package for TSC vote for the creation of ISA Extension TGs and filling the chair and vice-chair vacancies for its TGs. Develop strategy for the groups under it and complete coverage of areas of responsibility under it including gaps.
<b>Horizontal Committees (HC)</b>	Approve and oversee non-extension TGs, and has responsibilities to make sure that all Extension TGs cover the area overseen by the HC before ratification, Responsible for developing a holistic strategy and reaching out to the external ecosystem and community groups.
<b>Horizontal Subcommittees (HSC)</b>	It is a nested HC.
<b>Task Groups (TG)</b>	Must have charter that define deliverable work products: extension specifications, standards, requirements, best practices, etc.. TGs under the unpriv and priv SC can have ISA extension work products. TGs under HCs should not have ISA extension work products.
<b>Special Interest Groups (SIG)</b>	Topic discussion. No work product. Can be created by the TSC, ICs or HCs with TSC approval not required.
Meeting	Responsibilities
<b>Committee Chairs Meeting</b>	TSC strategy discussions. Invitees are IC chairs & HC chairs, RISC-V staff, TSC, and advisors and ad-hoc invitees.
<b>Chairs Meeting</b>	Invitees are RISC-V staff, Chairs & Vice Chairs of all ICs, HCs, HSCs, TGs, & SIGs. Policy approval, general governance, escalations, exceptions, final charter approval, voting as appropriate.

# Special Interest Groups (SIGs)

The SIGs have conversations and drive requirements in key industry and technology areas.

## SIG Academia and Training

Coordinate outreach to the open source community as well as researchers and educators in academia, and to curate and recommend training materials to both academics and professional training organizations.

**Meetings:** Every other Thursday: 8am PT (5pm CEST)

## SIG High Performance Computing (HPC)

**Meetings:** Monthly on 3rd Thurs: 4pm PT

## SIG Functional Safety

**Meetings:** Every other Thursday: 8am PT (5pm CEST)

## SIG Soft CPU

# The Community

Promote your products and people!



# RISC-V Alliances

RISC-V regional and industry alliances provide events, maintain relationships, and create multiple feedback channels in a way that no single organization could do on its own. See our [alliances page](#) for the full listing.

## Regional Alliances

Communicate locally, provide local events, and maintain relationships in a way that no single organization could do on its own.



## Industry Alliances

industry alliances create multiple feedback channels on both technical and non-technical topics that help both the RISC-V community and the industries using the RISC-V technology.



# RISC-V Training Partners

RISC-V Training Partners are focusing on RISC-V training in a professional setting. The Training Partner Program extends the breadth and reach of RISC-V knowledge, providing opportunities for a broader audience to learn. See our [Training Partner page](#) for more information on our training partners or how to become a RISC-V Training Partner.



# RISC-V Exchange

The RISC-V Exchange provides a window into work that people have accomplished around the world in the RISC-V community, including physical hardware, IP cores, and a great deal of software.

- [Available Boards](#)
- [Available Cores & SoCs](#)
- [Available Software](#)

[Contact us](#) if you have a product to add to the Exchange.

# RISC-V Ambassador Program

**RISC-V Ambassadors are individuals passionate about RISC-V and dedicated to growing and engaging the RISC-V community.**

Ambassadors are RISC-V experts and work together with RISC-V to ensure our global momentum and adoption. Successful ambassadors include engineers, developers, bloggers, influencers, evangelists who are already engaged with RISC-V in some way, including contributing to work groups, online groups, community events, training, workshops, and more.

**The RISC-V Ambassador Program empowers community members with tools and resources to:**

- Promote RISC-V projects and technology
- Educate a local community on the RISC-V mission and technical aspects
- Engage RISC-V member participation and community growth



Thank you  
Questions: [info@riscv.org](mailto:info@riscv.org)