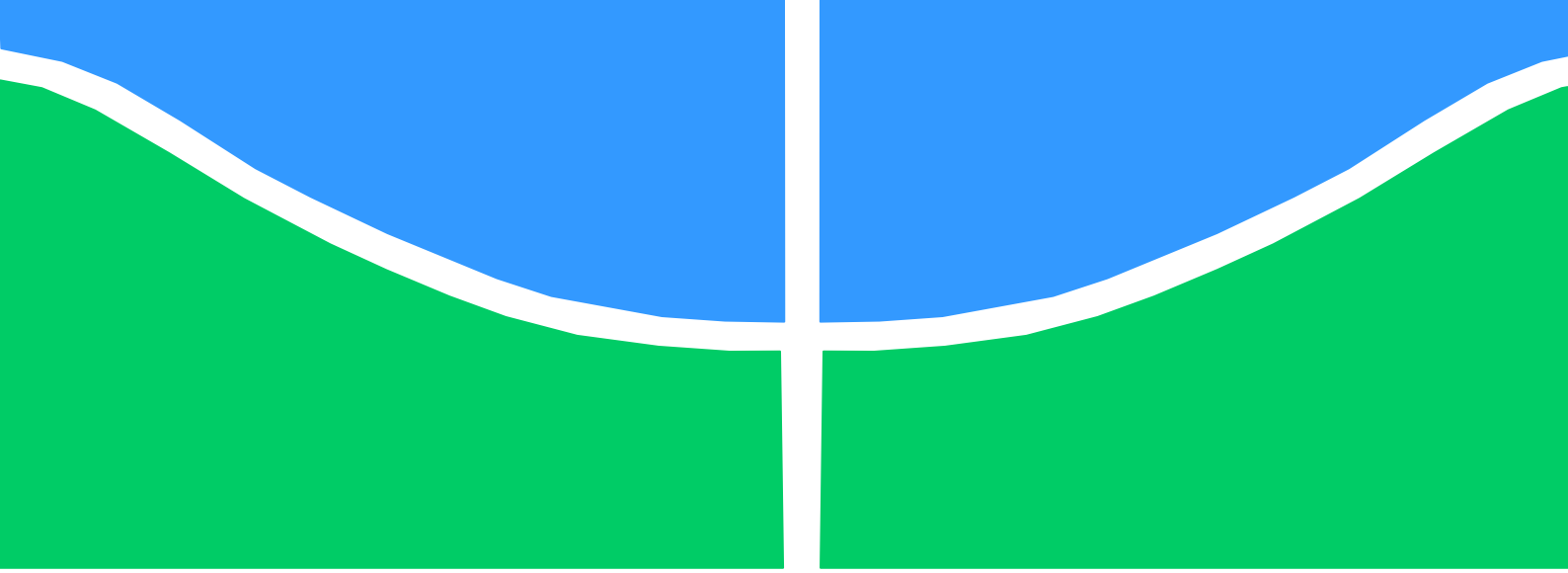

Universidade de Brasília - UnB
Departamento de Engenharia Eletrica - ENE

Pré-relatório Experimento 6
Circuitos sequenciais em VHDL

Carlos Eduardo Taborda Lottermann
180041509

Prof. Luís Fernando Ramos Molinaro

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Código em VHDL do 1º visto:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Visto_1 is
    Port ( PR : in  STD_LOGIC;
           CLR : in  STD_LOGIC;
           CLK : in  STD_LOGIC;
           J : in  STD_LOGIC;
                  K : in STD_LOGIC;
           Q : out  STD_LOGIC);
end Visto_1;

architecture F_F of Visto_1 is

signal JK : STD_LOGIC_VECTOR (1 downto 0);
signal Qbuf : STD_LOGIC;

begin
JK <= (J & K);
Q <= Qbuf;
process (PR, CLR, CLK)
begin
          if PR = '1' then Q <= '1';
          elsif CLR = '1' then Q <= '0';
          elsif rising_edge(CLK) then
                    case JK is
                              when "00" => Qbuf <= Qbuf;
                              when "01" => Qbuf <= '0';
                              when "10" => Qbuf <= '1';
                              when "11" => Qbuf <= not(Qbuf);
                              when others => Qbuf <= Qbuf;
                    end case;
          end if;
end process;

end F_F;
```

Arquivo UCF do 1º visto:

```
NET "PR" LOC = "N3";
NET "CLR" LOC = "E2";
NET "CLK" LOC = "F3";

NET "J" LOC = "L3";
NET "K" LOC = "P11";

NET "Q" LOC = "M5";
```

Código em VHDL do 2º visto:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity Visto_2 is
    Port ( CLK : in  STD_LOGIC;
           RST : in  STD_LOGIC;
           LOAD : in  STD_LOGIC;
           D : in  STD_LOGIC_VECTOR (3 downto 0);
           DIR : in  STD_LOGIC;
           L : in  STD_LOGIC;
           R : in  STD_LOGIC;
           Q : out  STD_LOGIC_VECTOR (3 downto 0));
end Visto_2;

architecture Visto_2_op of Visto_2 is

signal Qbuf : STD_LOGIC_VECTOR (3 downto 0);

begin
Q <= Qbuf;
process (CLK)
begin
          if rising_edge(CLK) then
                    if RST = '1' then Qbuf <= "0000";
                    elsif LOAD = '1' then Qbuf <= D;
                    elsif DIR = '0' then
                              if L = '0' then Qbuf <= (Qbuf(2) & Qbuf(1) & Qbuf(0) & '0'); end if;
                              if L = '1' then Qbuf <= (Qbuf(2) & Qbuf(1) & Qbuf(0) & '1'); end if;
                    elsif DIR = '1' then
                              if R = '0' then Qbuf <= ('0' & Qbuf(3) & Qbuf(2) & Qbuf(1)); end if;
                              if R = '1' then Qbuf <= ('1' & Qbuf(3) & Qbuf(2) & Qbuf(1)); end if;
                    end if;
          end if;
end process;

end Visto_2_op;
```

Arquivo UCF do 2º visto:

```
NET "RST" LOC = "A7";
NET "LOAD" LOC = "M4";

NET "CLK" LOC = "N3";
NET "DIR" LOC = "E2";
NET "L" LOC = "F3";
NET "R" LOC = "G3";

NET "D(0)" LOC = "P11";
NET "D(1)" LOC = "L3";
NET "D(2)" LOC = "K3";
NET "D(3)" LOC = "B4";
```