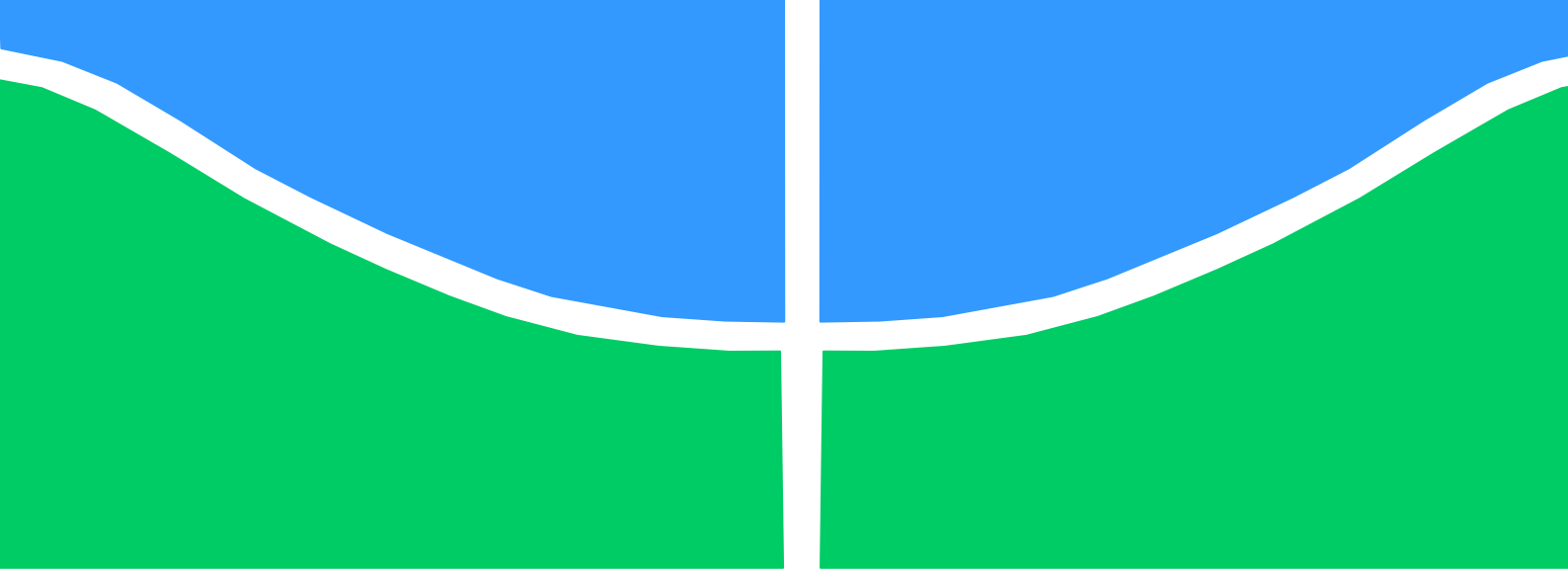


Universidade de Brasília - UnB
Departamento de Engenharia Eletrica - ENE

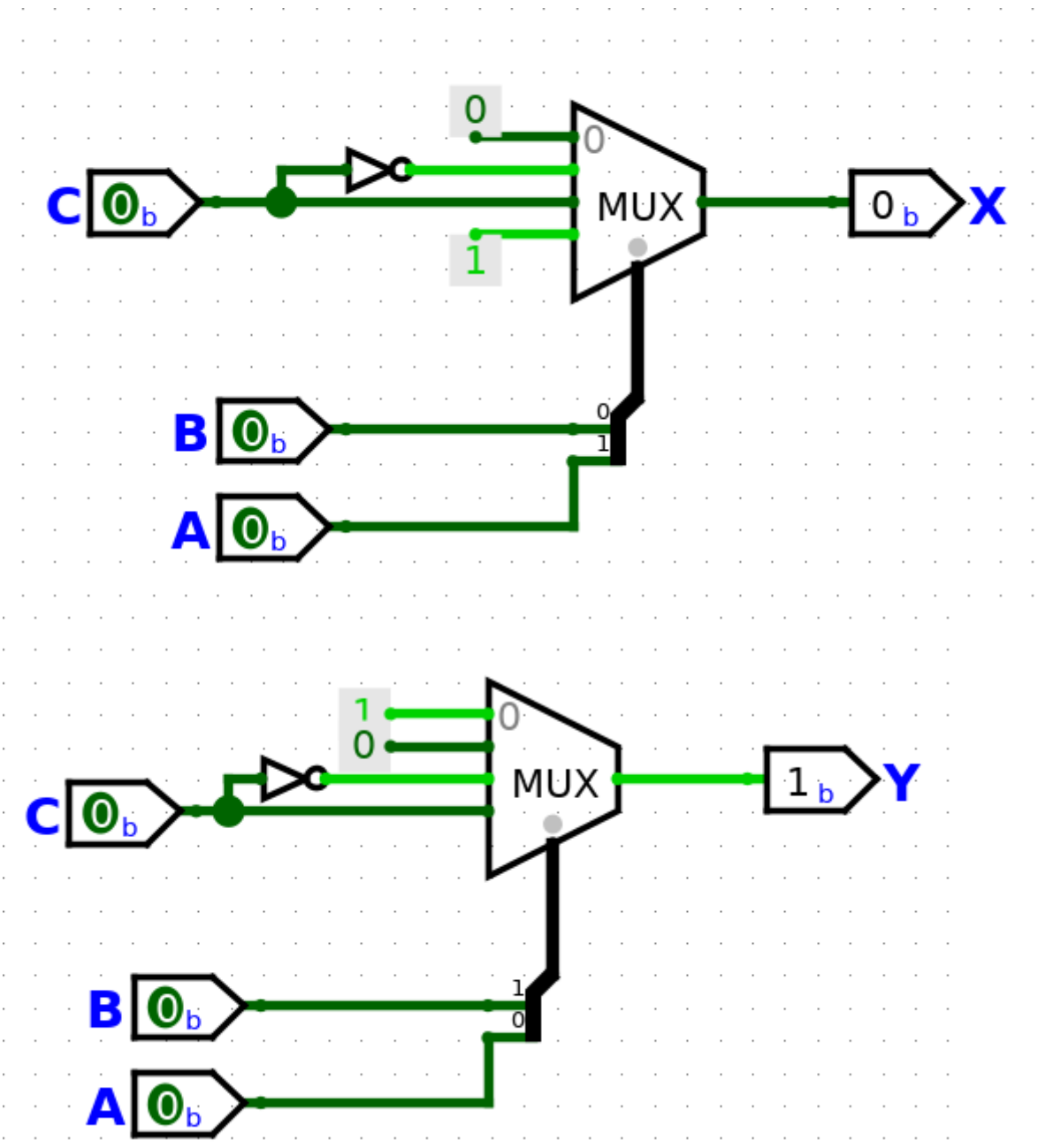
Pré-relatório Experimento 4
Implementação de circuitos combinacionais com multiplexadores

Carlos Eduardo Taborda Lottermann
180041509

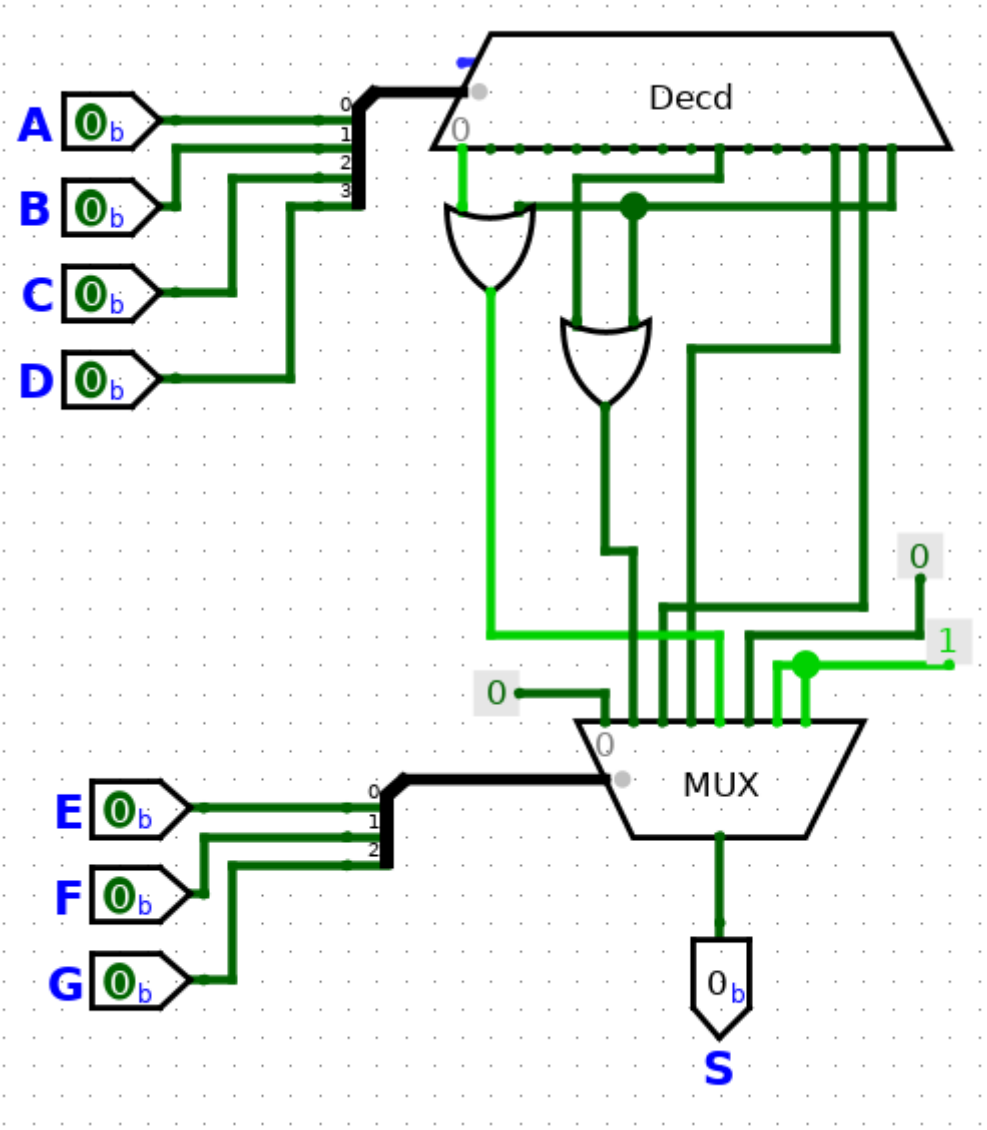
Prof. Luís Fernando Ramos Molinaro

Brasília, DF
2019

Desenhos esquemáticos:
Visto 1:



Visto 2:



Código em VHDL do 1º visto:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Visto_1 is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           C : in  STD_LOGIC;
           X : out  STD_LOGIC;
           Y : out  STD_LOGIC);
end Visto_1;

architecture Visto_1_op of Visto_1 is

component MUX is
Port ( S : in  STD_LOGIC_VECTOR (1 downto 0);
          D : in  STD_LOGIC_VECTOR (3 downto 0);
          Y : out  STD_LOGIC);
end component;

signal  X_sel : STD_LOGIC_VECTOR (1 downto 0);
signal  X_in    : STD_LOGIC_VECTOR (3 downto 0);
signal  Y_sel : STD_LOGIC_VECTOR (1 downto 0);
signal  Y_in    : STD_LOGIC_VECTOR (3 downto 0);

begin

X_sel(0) <= B;
X_sel(1) <= A;

X_in(0) <= '0';
X_in(1) <= not C;
X_in(2) <= C;
X_in(3) <= '1';
Xu: MUX port map(X_sel,X_in, X);
```

```
Y_sel(0) <= B;
Y_sel(1) <= A;

Y_in(0) <= '1';
Y_in(1) <= '0';
Y_in(2) <= not C;
Y_in(3) <= C;

Yu: MUX  port map(Y_sel,Y_in,Y);

end Visto_1_op;
```

Arquivo UCF do 1º visto:

```
NET "A" LOC = "K3";
NET "B" LOC = "L3";
NET "C" LOC = "P11";
NET "X" LOC = "M11";
NET "Y" LOC = "M5";
```

Código VHDL do 2º visto:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity Visto_2 is
    Port ( A : in  STD_LOGIC;
           B : in  STD_LOGIC;
           C : in  STD_LOGIC;
           D : in  STD_LOGIC;
           E : in  STD_LOGIC;
           F : in  STD_LOGIC;
           G : in  STD_LOGIC;
           S : out  STD_LOGIC);
end Visto_2;

architecture Visto_2_op of Visto_2 is

component MUX_8 is
    Port ( S : in  STD_LOGIC_VECTOR (2 downto 0);
           D : in  STD_LOGIC_VECTOR (7 downto 0);
           Y : out  STD_LOGIC);
end component;

component Decoder is
    Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);
           Y : out  STD_LOGIC_VECTOR (15 downto 0));
end component;

signal Decoder_sel : STD_LOGIC_VECTOR (3 downto 0);
signal Decoder_out : STD_LOGIC_VECTOR (15 downto 0);

signal MUX_sel : STD_LOGIC_VECTOR (2 downto 0);
signal MUX_in : STD_LOGIC_VECTOR (7 downto 0);
signal MUX_out : STD_LOGIC;
```

```
begin


Decoder_sel(0) <= A;
Decoder_sel(1) <= B;
Decoder_sel(2) <= C;
Decoder_sel(3) <= D;


Dec: Decoder port map(Decoder_sel,Decoder_out);


MUX_sel(0) <= E;
MUX_sel(1) <= F;
MUX_sel(2) <= G;


MUX_in(0) <= '0';
MUX_in(1) <= Decoder_out(9) or Decoder_out(15);
MUX_in(2) <= Decoder_out(14);
MUX_in(3) <= Decoder_out(13);
MUX_in(4) <= Decoder_out(1) or Decoder_out(15);
MUX_in(5) <= '0';
MUX_in(6) <= '1';
MUX_in(7) <= '1';


M: MUX_8 port map(MUX_sel,MUX_in,S);



end Visto_2_op;
```

Arquivo UCF do 2º visto:

```
NET "A" LOC = "F3";
NET "B" LOC = "G3";
NET "C" LOC = "B4";
NET "E" LOC = "K3";
NET "F" LOC = "L3";
NET "G" LOC = "P11";


NET "S" LOC = "M5";
```