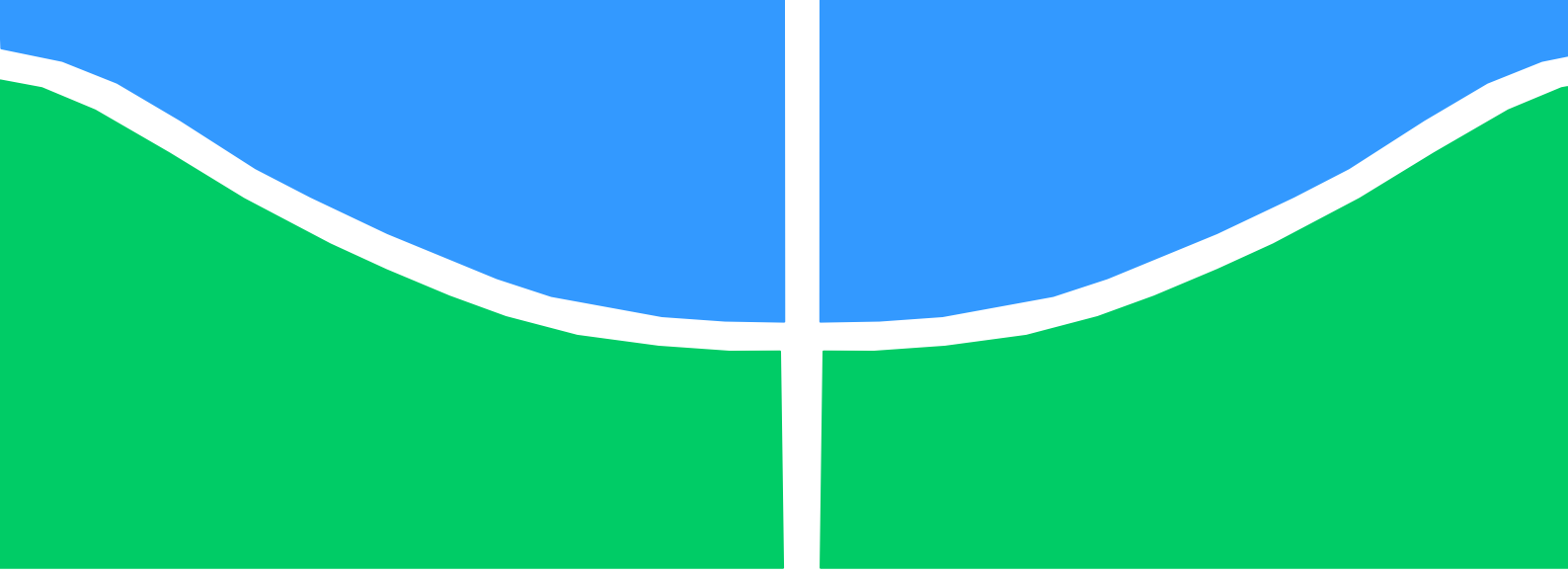

Universidade de Brasília - UnB
Departamento de Engenharia Eletrica - ENE

Pré-relatório Experimento 5
Somadores de palavras binárias e simulação de circuitos em VHDL

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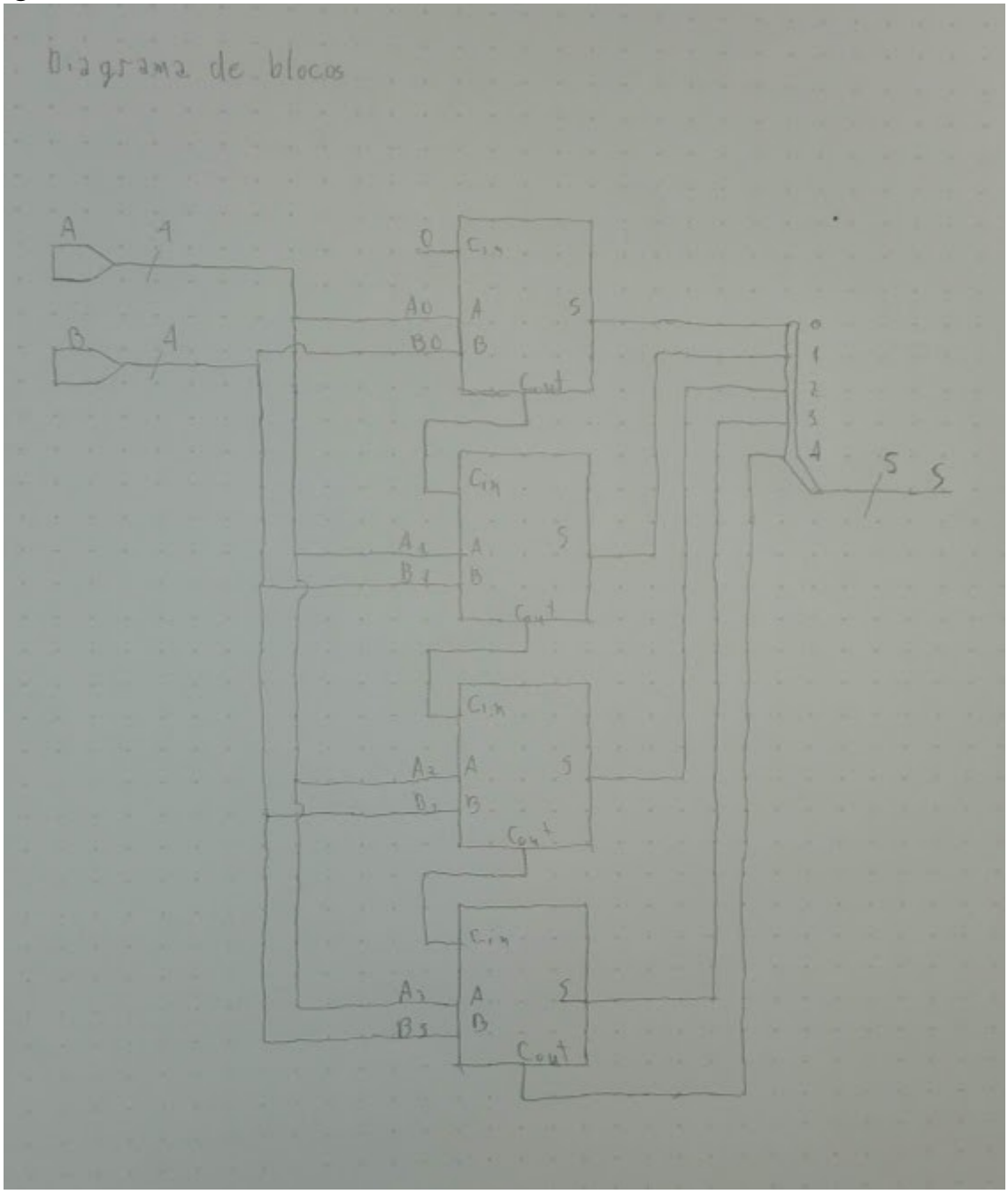
Diagrama de blocos visto 1:



VHDL visto 1

```
entity Visto_1 is
    Port ( A : in  STD_LOGIC_VECTOR (3 downto 0);
           B : in  STD_LOGIC_VECTOR (3 downto 0);
           S : out  STD_LOGIC_VECTOR (4 downto 0));
end Visto_1;

architecture Visto_1_op of Visto_1 is

component Sum is
Port (   A : in  STD_LOGIC;
                              B : in  STD_LOGIC;
                              Cin : in  STD_LOGIC;
                              S : out  STD_LOGIC;
                              Cout : out  STD_LOGIC);
end component;

signal carry : STD_LOGIC_VECTOR (3 downto 0);

begin

S0: Sum port map(A(0),B(0),'0',S(0),carry(0));
S1: Sum port map(A(1),B(1),carry(0),S(1),carry(1));
S2: Sum port map(A(2),B(2),carry(1),S(2),carry(2));
S3: Sum port map(A(3),B(3),carry(2),S(3),carry(3));
S(4) <= carry(3);



end Visto_1_op;
```

VHDL visto 2:

```
entity Visto_2 is
    Port ( A : in  UNSIGNED (3 downto 0);
           B : in  UNSIGNED (3 downto 0);
           S : out  STD_LOGIC_VECTOR (4 downto 0));
end Visto_2;

architecture Visto_2_op of Visto_2 is

begin

S <= ('0' & A) + ('0' & B);



end Visto_2_op;
```

VHDL visto 3:

```
entity testbench is
   Port ( F_dut : in  STD_LOGIC_VECTOR (4 downto 0);
          F_gm : in  STD_LOGIC_VECTOR (4 downto 0);
          A : out  STD_LOGIC_VECTOR (3 downto 0);
          B : out  STD_LOGIC_VECTOR (3 downto 0));
end testbench;
architecture test of testbench is
begin
process
          variable cont : STD_LOGIC_VECTOR (7 downto 0);
          begin

                    cont := "00000000";

                    for i in 1 to 256 loop

                              A(0) <= cont(0);
                              A(1) <= cont(1);
                              A(2) <= cont(2);
                              A(3) <= cont(3);
                              B(0) <= cont(4);
                              B(1) <= cont(5);
                              B(2) <= cont(6);
                              B(3) <= cont(7);
                              wait for 500 ns;

                              assert (F_dut = F_gm);

                              cont := cont + 1;

                    end loop;

                    wait;
          end process;
end test;
```

Testbench:

```
ENTITY test IS
END test;

ARCHITECTURE behavior OF test IS

   COMPONENT testbench
   PORT(
        F_dut : IN  std_logic_vector(4 downto 0);
        F_gm : IN  std_logic_vector(4 downto 0);
        A : OUT  std_logic_vector(3 downto 0);
        B : OUT  std_logic_vector(3 downto 0)
       );
   END COMPONENT;

 COMPONENT Visto_1
 PORT(
        A : in  STD_LOGIC_VECTOR (3 downto 0);
        B : in  STD_LOGIC_VECTOR (3 downto 0);
        S : out  STD_LOGIC_VECTOR (4 downto 0)
          ) ;
 END COMPONENT;

 COMPONENT Visto_2
 PORT(
        A : in  UNSIGNED (3 downto 0);
        B : in  UNSIGNED (3 downto 0);
        S : out  STD_LOGIC_VECTOR (4 downto 0)
          ) ;
 END COMPONENT;

  signal F_dut : std_logic_vector(4 downto 0);
  signal F_gm : std_logic_vector(4 downto 0);

  signal A : std_logic_vector(3 downto 0);
  signal B : std_logic_vector(3 downto 0);
```

```
BEGIN

U0: Visto_1 port map(A, B, F_dut);
U1: Visto_2 port map(A, B, F_gm);
U2: testbench port map(F_dut, F_gm, A, B);

END;
```

Arquivo UCF:

```
NET "A(0)" LOC = "P11";
NET "A(1)" LOC = "L3";
NET "A(2)" LOC = "K3";
NET "A(3)" LOC = "B4";
NET "B(0)" LOC = "G3";
NET "B(1)" LOC = "F3";
NET "B(2)" LOC = "E2";
NET "B(3)" LOC = "N3";

NET "S(0)" LOC = "M5";
NET "S(1)" LOC = "M11";
NET "S(2)" LOC = "P7";
NET "S(3)" LOC = "P6";
NET "S(4)" LOC = "N5";
```