The Coin Detector Circuit

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I. Introduction

This paper discusses the design of a Coin Detector Project that utilizes an inductor as an inductive proximity switch. The project covers basic analog/digital circuits that the students have learned during the first two years in the Electrical Engineering Technology Program at Purdue University. Figure 1 below shows the block diagram of the project.

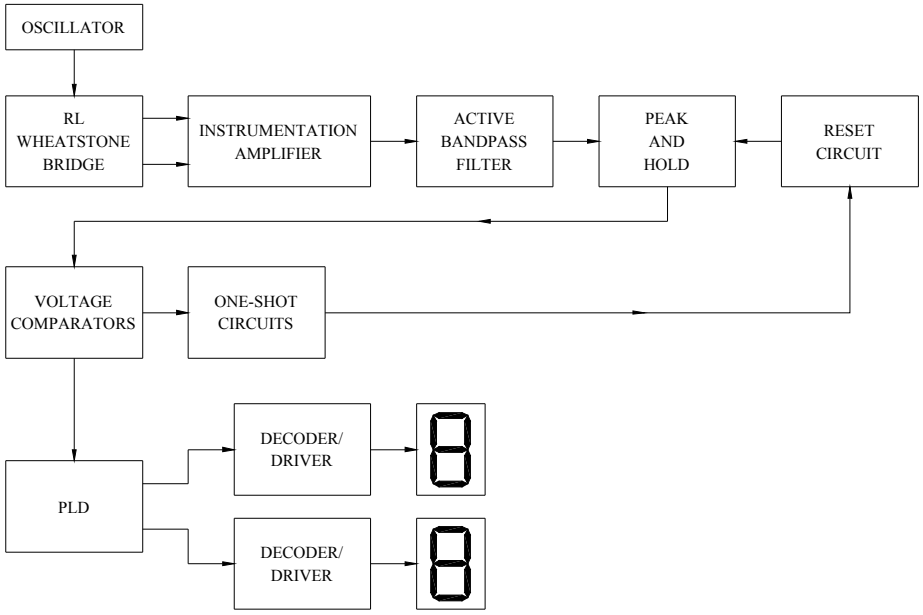

Figure 1 – The Block Diagram of the Circuit

In the ready mode, the circuit shows 00 at the seven-segment displays. When a quarter, a dime, or a nickel passes through the slot, the display becomes 25, 10, or 05 respectively in a two-second period and it then resets itself to 00.

The project consists of different stages that are manageable as weekly classroom activities. It helps the students to utilize their knowledge to design and build a working circuit.

II. Individual Stages of the Circuit

A. The Coin Slot

The design of the coin slot is in Figure 2 below. The material of this slot is non-metallic so that the value of the inductor on the slot is not affected. The U-shape slot provides a smooth passage for the coins to roll down the slope. A 33mH inductor is mounted on the side of the slot via a through hole. The top of the inductor is flush with the inner wall of the slot.

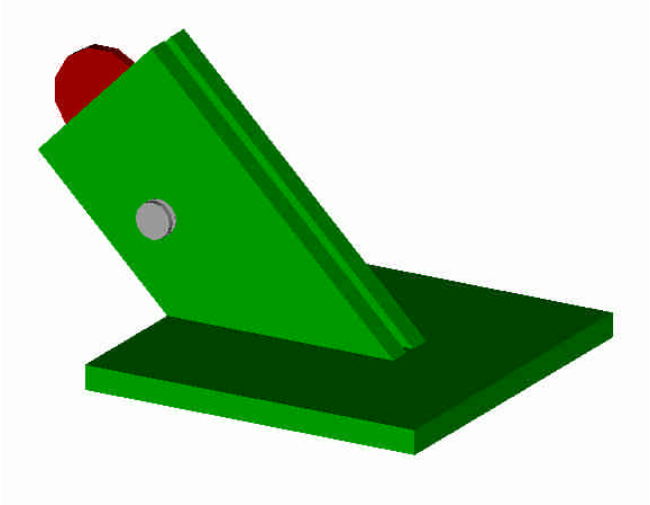

Figure 2 – The Coin Slot

The characteristics of the core of the inductor change when a coin passes in front of it. This change results in a decrease of the inductance value. The circuit will exploit this behavior of the inductor to detect the different coins passing through the slot.

B. The Sine Wave Oscillator

The schematic diagram of the oscillator is in Figure 3 on the next page.

If we let $C_1 = C_2 = C_3 = C$ and $R_3 = R_4 = R$, the oscillating frequency of the circuit is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi\left(0.01\mu F\right)\left(3.9k\Omega\right)} = 4.08kHz$$

In designing this oscillator, the students must match three capacitors and two resistors. After connecting the circuit, the students must carefully tune the rheostat R_1 so that oscillation occurs.

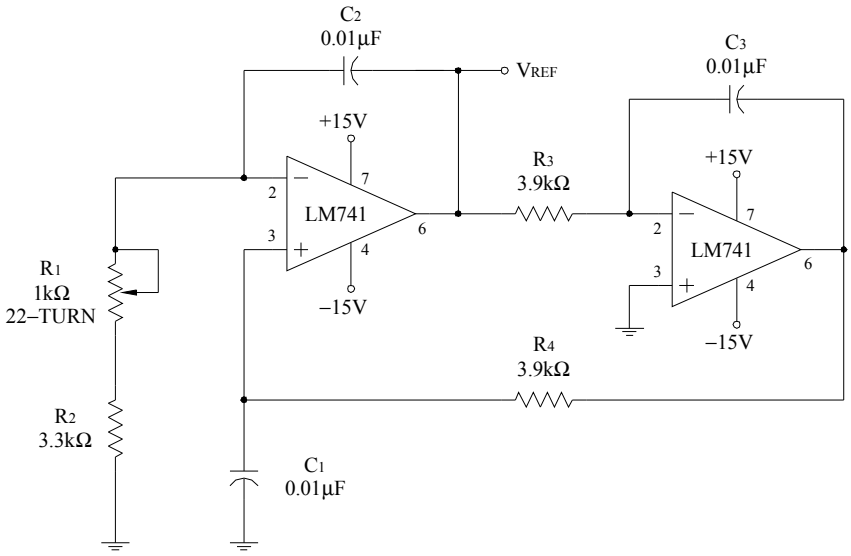

Figure 3 – The Sine Wave Oscillator

The output waveform of the voltage V_{REF} is in Figure 4 below. This output voltage has its peak value of $13.5V_{PEAK}$ and its frequency of 4kHz.

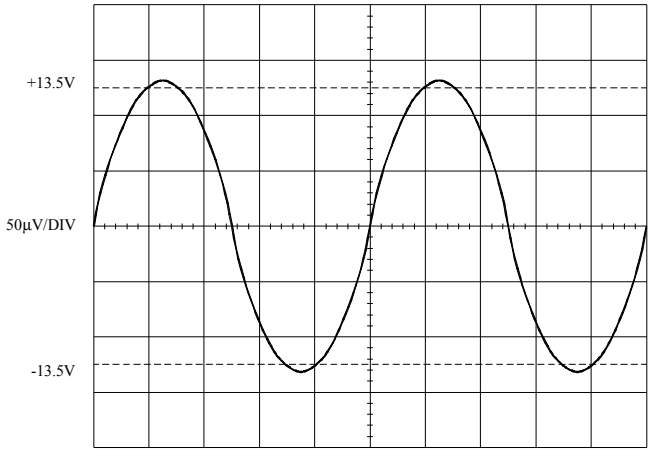

Figure 4 – The Output of the Oscillator

The output voltage of the oscillator is used as the reference voltage for a RL Wheatstone Bridge.

C. The RL Wheatstone Bridge

The schematic diagram of this circuit is in Figure 5 below. In the bridge, the inductor L_1 is mounted on the coin slot and connected to the circuit via a two-conductor shielded cable wire. The rheostat R_6 is for balancing the bridge. The reference voltage V_{REF} is the output voltage of the oscillator.

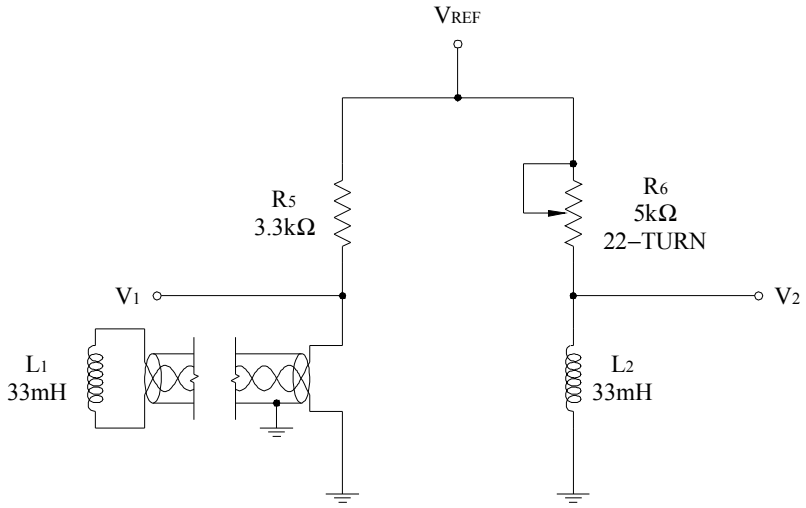

Figure 5 – The RL Wheatstone Bridge

When a coin passes in front of the inductor L_1, the inductance decreases resulting in an unbalanced bridge. The difference of the output voltages of the bridge is then amplified by an Instrumentation Amplifier.

D. The Instrumentation Amplifier

The schematic diagram of the Instrumentation Amplifier is in Figure 6 on the next page. The input voltages V_1 and V_2 of the circuit are the output voltages of the RL Wheatstone Bridge. In the amplifier, if we let $R_8 = R_9 = R_{10} = R_{11} = R_{12} = R_{13} = R$, the closed-loop gain of the circuit is:

$$A_{CL} = 1 + \frac{2R}{R_7} = 1 + \frac{2(15k\Omega)}{2.2k\Omega} = 14.6$$

The resistors R_8 through R_{13} in the circuit are precision resistors.

The output voltage V_3 of the amplifier has the following peak values:

- When there is no coin passing through, the peak value of the output voltage is 60mV.
- When 25¢ coin passes through, the peak value of the output voltage is 1V.
- When 10¢ coin passes through, the peak value of the output voltage is 0.7V.
- When 5¢ coin passes through, the peak value of the output voltage is 0.25V.

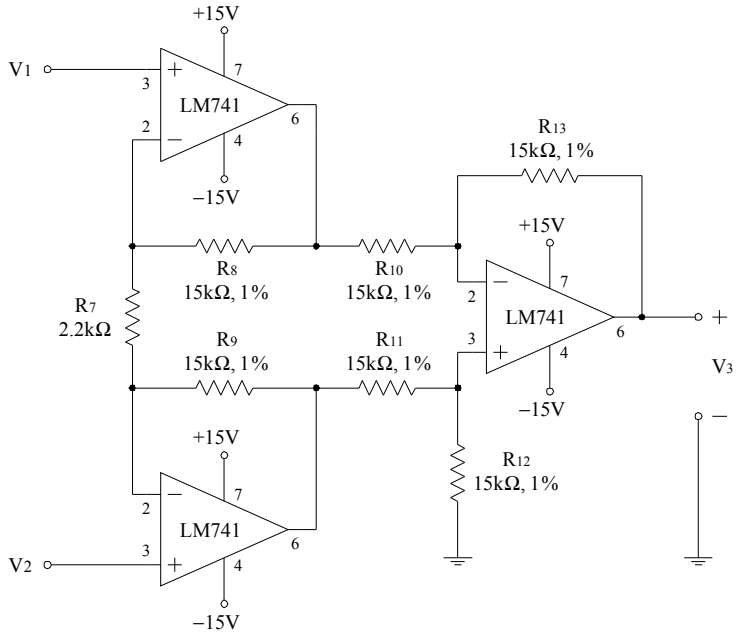

Figure 6 – The Instrumentation Amplifier

The voltage V_3 is not a perfect sine wave since we cannot perfectly balance the bridge and the stray capacitance in the cable also contributes to the presence of some minor interference. Figure 7 below shows one cycle of the waveform of the voltage V_3 when a 25¢ coin passes in front of the inductor L_1.

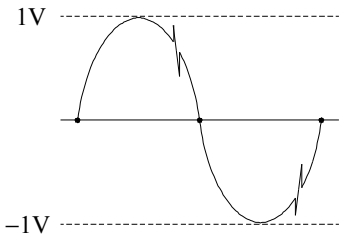

Figure 7 – The Voltage V_3 for 25¢ Coin

An Active Band Pass Filter is used in the next stage to eliminate the interference and amplify the signal further.

E. The Active Band Pass Filter

The schematic diagram of the filter is in Figure 8 below.

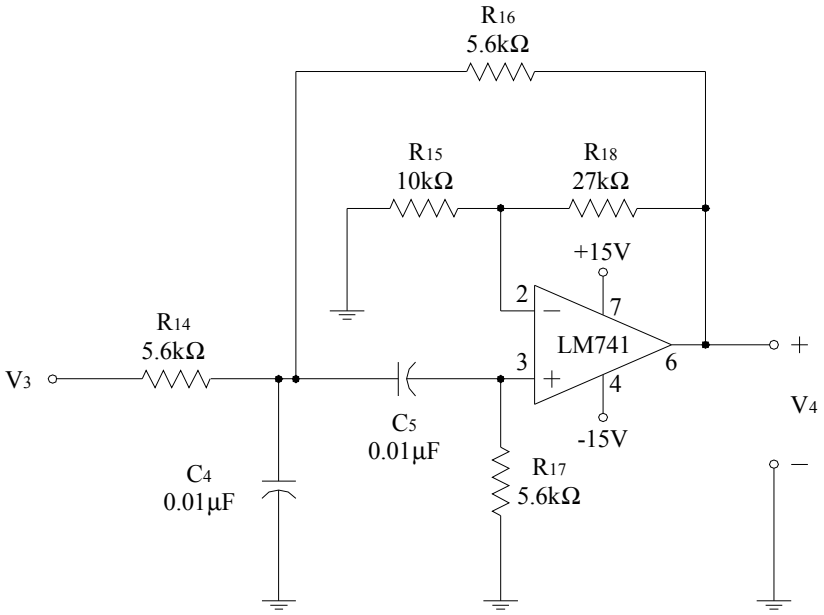

Figure 8 – The Active Band Pass Filter

If we let $R_{14} = R_{16} = R_{17} = R$ and $C_4 = C_5 = C$ in the filter, the center frequency is:

$$f_0 = \frac{\sqrt{2}}{2\pi RC} = \frac{\sqrt{2}}{2\pi (5.6k\Omega)(0.01mF)} = 4.02kHz$$

The Q sensitivity value of the filter is:

$$Q = \frac{\sqrt{2}}{4 - \left(1 + \frac{R_{18}}{R_{15}}\right)} = \frac{\sqrt{2}}{4 - \left(1 + \frac{27k\Omega}{10k\Omega}\right)} = 4.7$$

The output voltage V_4 of the filter is a sine wave whose peak values are:

- When there is no coin passing through, the peak value of the output voltage is 0.7V.
- When 25¢ coin passes through, the peak value of the output voltage is 12V.
- When 10¢ coin passes through, the peak value of the output voltage is 8V.
- When 5¢ coin passes through, the peak value of the output voltage is 3V.

Figure 8 below shows the different responses of the filter.

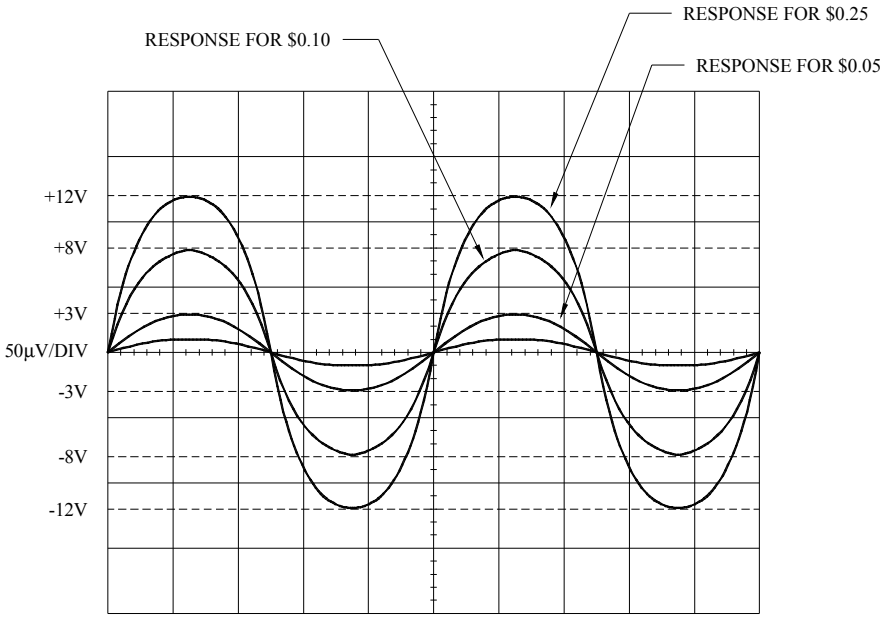

Figure 8 – The Output Waveforms of the Active Band Pass Filter

F. The Peak and Hold Circuit and the Reset Circuit

With the output of the active filter, we are able to distinguish the differences of the coins. The next stage of the circuit is to convert the peak values of the sine waves into DC voltages. This task can be accomplished by using the Peak and Hold circuit. The schematic diagram of this circuit is in Figure 9 on the next page.

When there is no reset signal presence at the input of the Reset circuit, the capacitor C_6 is fully charge and it holds the charge to produce a DC voltage equal to the peak value of the voltage V_4.

When the Reset circuit receives a signal, the transistor Q_1 acts as a closed switch. The collector-emitter junction of the transistor behaves as a short circuit providing a path for the capacitor C_6 to discharge through the resistor R_{21} and the collector-emitter junction. Under this condition, the Peak and Hold circuit is reset.

The discharging time constant is:

$$t = R_{21}C_6 = (560\Omega)(10mF) = 5.6ms$$

Therefore, if the reset signal lasts more than 5τ (28ms), the capacitor will be fully discharged and the Peak and Hold circuit is reset. The reset signal comes from the One-Shot circuit.

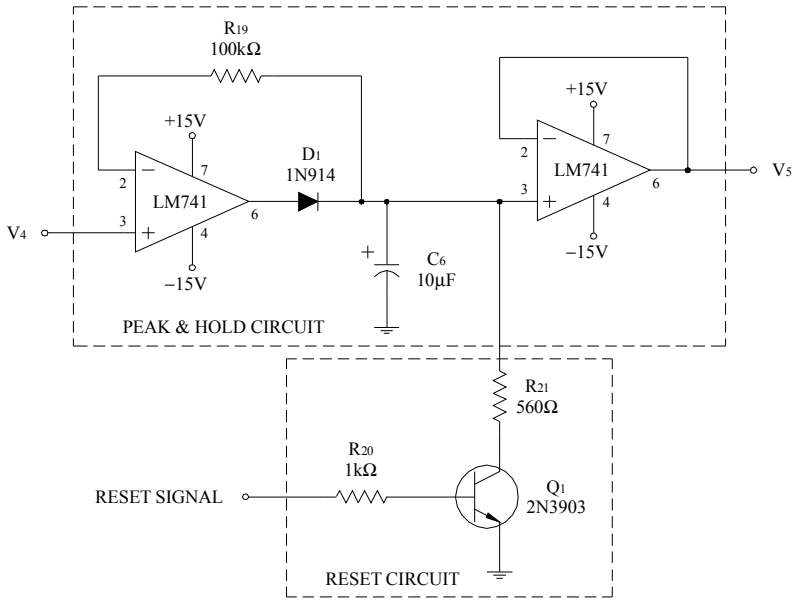

Figure 9 – The Peak and Hold Circuit and the Reset Circuit

At this part of the project, the output voltage V_5 can be:

- 0.7VDC when there is no coin passing through.
- 3VDC when 5¢ passes through.
- 8VDC when 10¢ passes through.
- 12VDC when 25¢ passes through.

G. The Voltage Comparators

The voltage V_5 goes into three Voltage Comparators to produce proper outputs for the Programmable Logic Device. The schematic diagram of this part of the circuit is in Figure 10 below. The potentiometer R_{22} is set so that the voltage at its wiper output to be 1.5V. The potentiometer R_{23} is set so that the voltage at its wiper output to be 6V. The potentiometer R_{24} is set so that the voltage at its wiper output to be 10V.

When there is no coin passing through the slot, the outputs of the Voltage Comparators are 0V.

When a 5¢ coin passes through, the output V_6 is approximately 4V and the remaining outputs V_7 and V_8 are 0V.

When a 10¢ coin passes through, the outputs V_6 and V_7 are approximately 4V and the output V_8 is 0V.

When a 25¢ coin passes through, all of the outputs are approximately 4V.

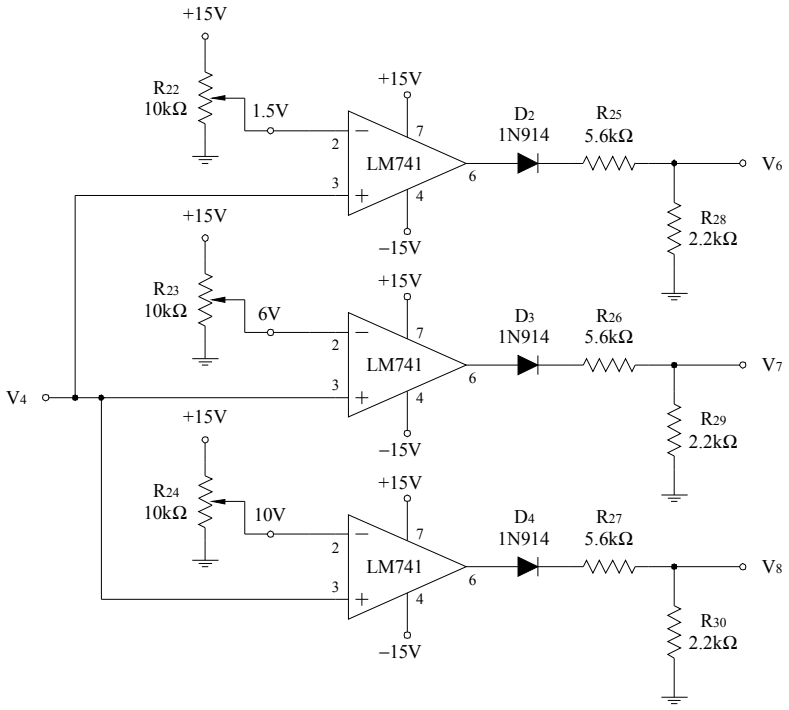

Figure 10 – The Voltage Comparators

In Figure 11 below shows the digital equivalent of the output voltages of the Voltage Comparators.

	V_8	V_7	V_6
NO COIN	0	0	0
NICKEL	0	0	1
DIME	0	1	1
QUARTER	1	1	1

Figure 11 – The Digital Equivalent of the Output Voltages

As in Figure 11, the output voltage V_6 changes its state when any coin passes through the slot. We can use this voltage as the trigger signal for the One-Shot circuit.

H. The One-Shot Circuits

The One-Shot circuits are used to maintain the seven-segment displays for duration of time as well as to reset the Peak and Hold circuit. The schematic diagram of the circuit is in Figure 12 below.

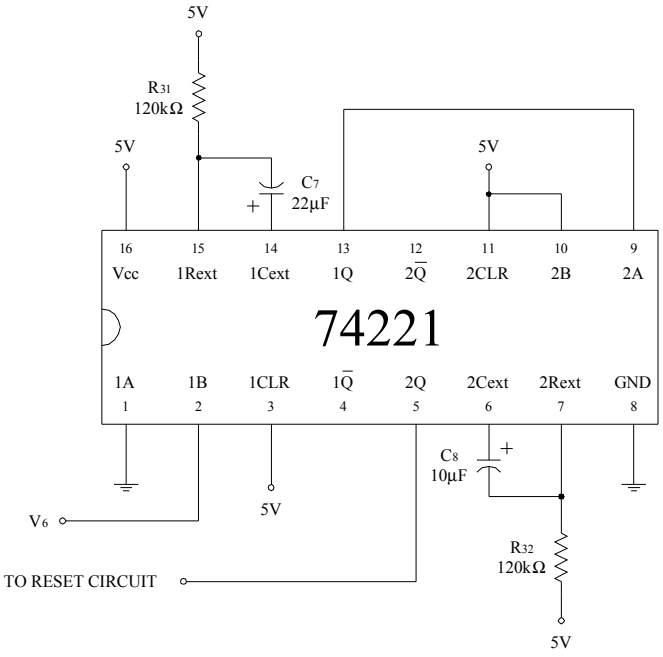

Figure 12 – The One-Shot Circuits

The 74221 Dual Monostable Multivibrator IC is used for the One-Shot circuits. When the input voltage V_6 goes from LOW to HIGH, the first one-shot circuit produces a pulse. The width of this pulse is:

$$PULSEWIDTH\#1 = 0.7C_7R_{31} = 0.7(22\mu F)(120k\Omega) = 1.85s$$

This is the time that the outputs V_6 through V_8 stay at their states when a coin is passing through the slot. At the end of this time period, the output 1Q of the first one-shot triggers the second one-shot. The pulse width of the second one-shot is:

$$PULSEWIDTH\#2 = 0.7C_8R_{32} = 0.7(10\mu F)(120k\Omega) = 840ms$$

This pulse is used as the reset signal to the Reset circuit. The duration of this pulse is much more than the 5τ required for the capacitor C_6 to be fully discharged.

I. The PLD, the Decoder/Drivers, and the Seven-Segment Display

The Programmable Logic Device in the circuit is the GAL16V8D EEPROM. This device has 8-bit input and 8-bit output. We use the outputs V_6 through V_8 of the Voltage Comparators as the input bits I/E, I/F, and I/G to the device. The outputs O/a through O/d are used for the Least Significant Digit and the outputs O/e through O/h are for the Most Significant Digit. The Truth Table of the inputs and outputs of the device is in Figure 13.

I/H	I/G	I/F	I/E	I/D	I/C	I/B	I/A	O/h	O/g	O/f	O/e	O/d	O/c	O/b	O/a
1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
1	0	0	1	1	1	1	1	0	0	0	0	0	1	0	1
1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
1	0	1	1	1	1	1	1	0	0	0	1	0	0	0	0
1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0
1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	0	0	1	0	0	1	0	1

Figure 13 – The Inputs and Outputs of the GAL16V8D

The program for the EEPROM is written using WinCupl as in Figure 14 below.

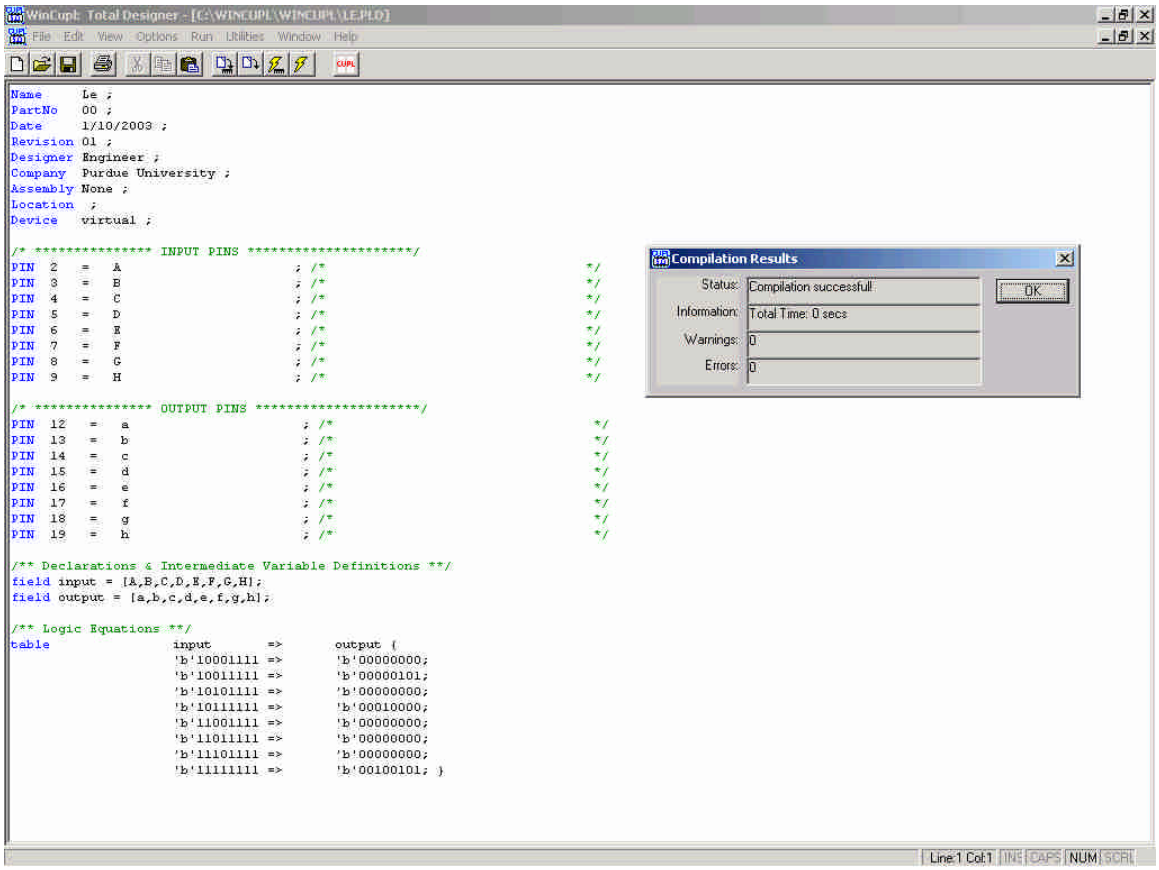

Figure 14 – The Program for the GAL16V8D

The outputs of the EEPROM are used to feed into two Decoder/Drivers to drive the Common Anode 7-segment displays. The schematic diagram of the circuit is in Figure 15 on the next page.

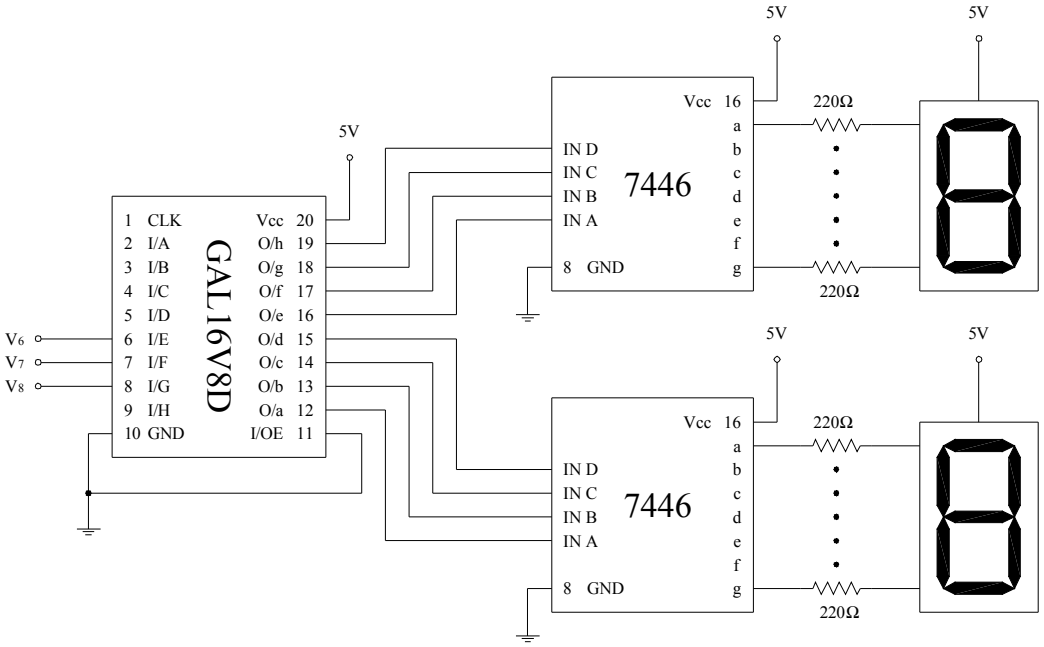

Figure 15 – The PLD, the Decoder/Drivers, and the 7-segment Displays

III. Conclusion

The project produces visual indicators for the value of the coin passing in front of the detection inductor. It consists of different analog/digital circuits that the students have learned during the first three semesters in the Electrical Engineering Technology Program of Purdue University. This design gives the students the opportunity to put into practice the theories and applications they possess. It also enhances their troubleshooting skills.

Bibliography

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3. Malvino, A. P. (1999). Electronic Principles (6th ed.). Ohio: Glencoe/McGraw-Hill.

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