

Lab 4 Report

Lab Members:

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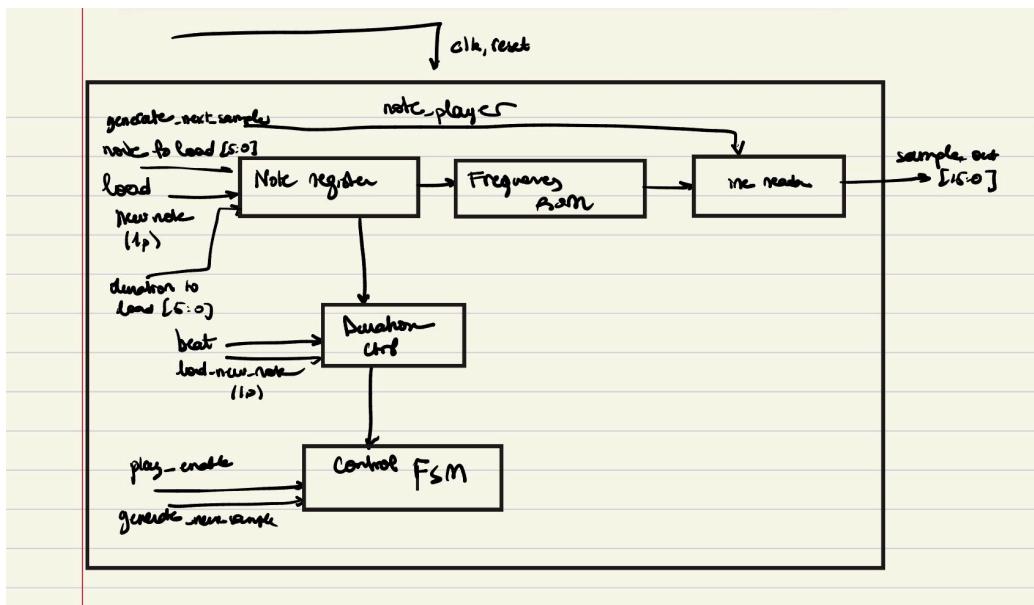
Carlos Henrique Aranguren

Sofia Baroudi

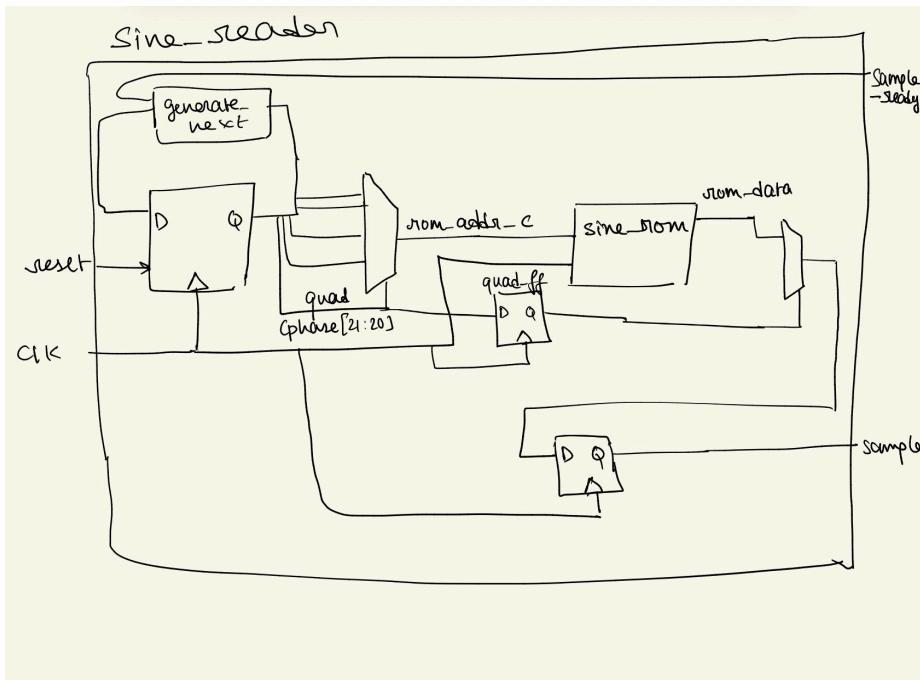
Zack Seifert

1. Block diagrams for note_player and sine_reader.

a. note_player



b. Sine_reader



2. Annotated Waveforms

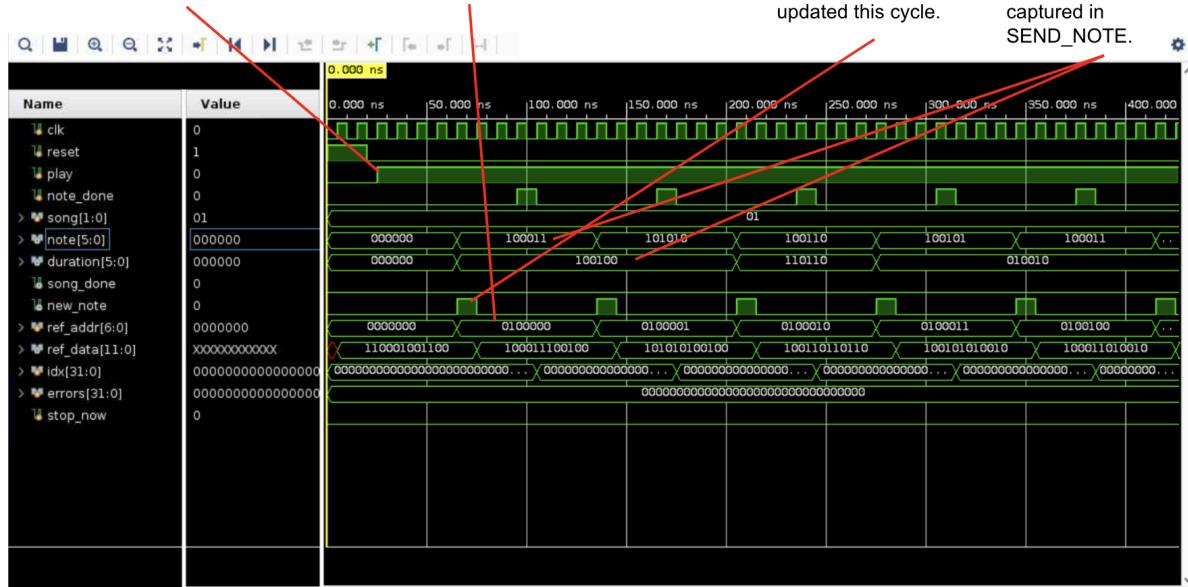
a. Song_reader.v

play goes high here to start playback;
FSM leaves IDLE.

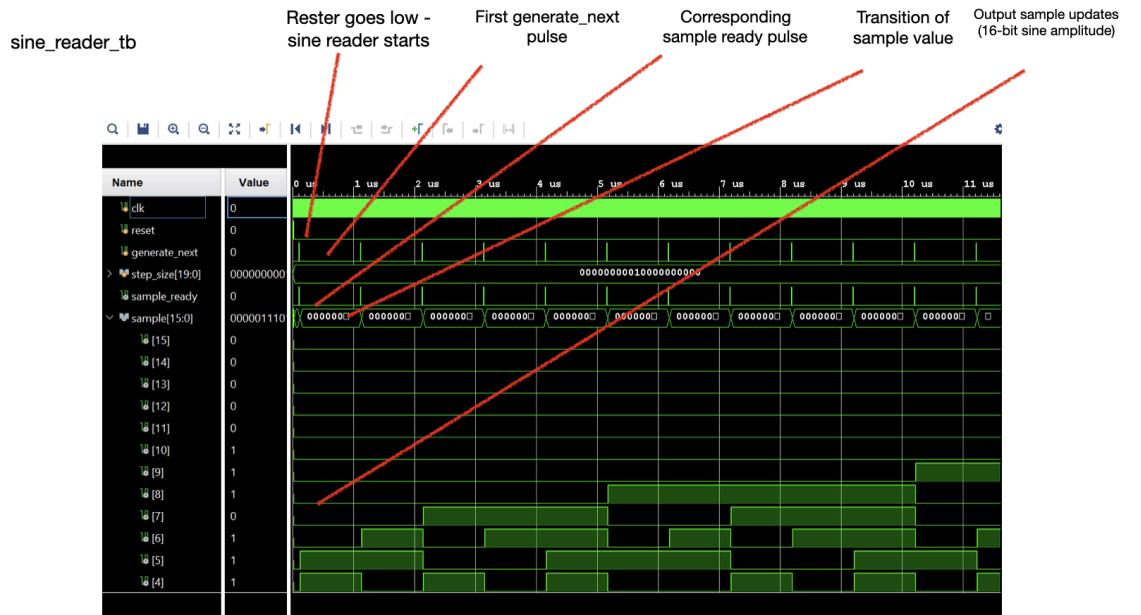
READ: ref_addr[6:0]=0100000 (song=01,
idx=00).

new_note 1-cycle
pulse → outputs
updated this cycle.

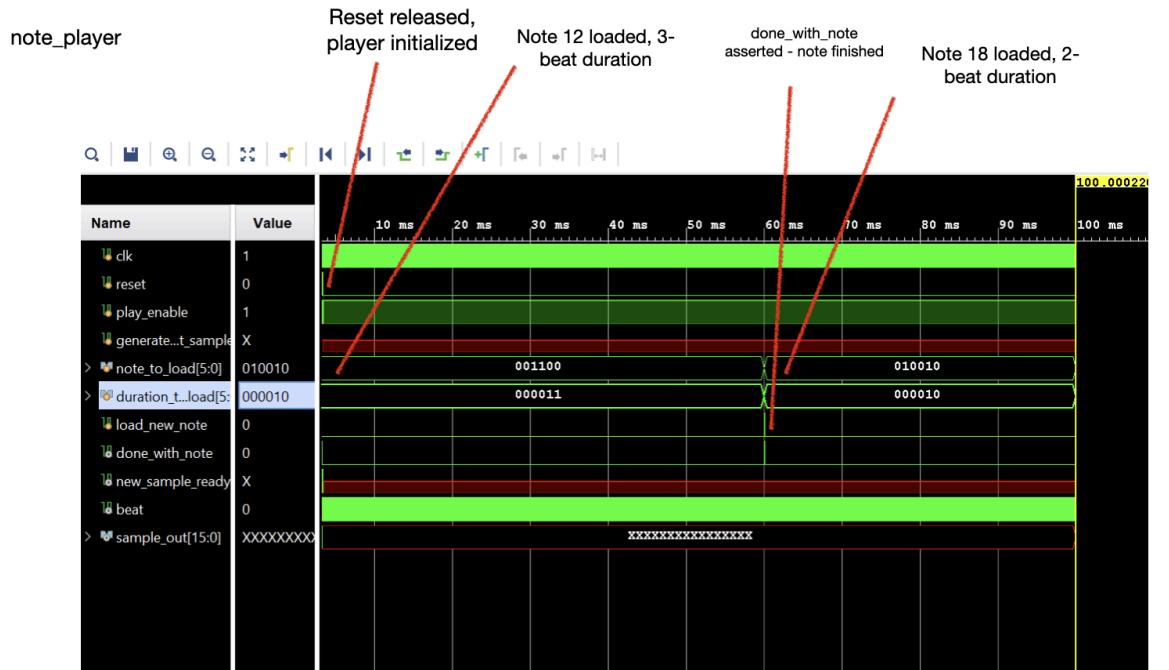
note=100011 (35),
duration=100100 (36)
captured in
SEND_NOTE.



b. Sine_reader.v



c. Note_player.v



d. MCU.v

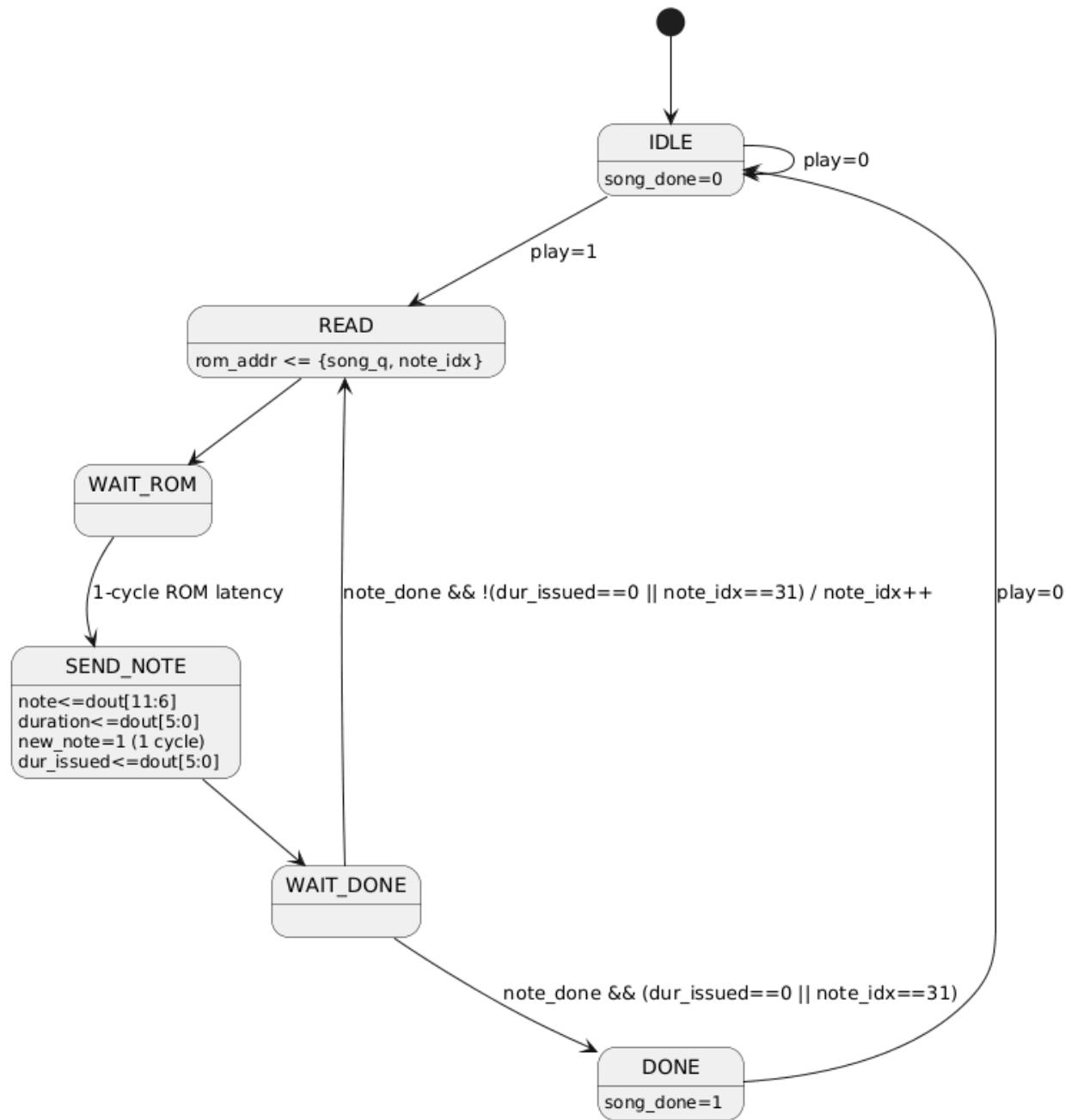
MCU_tb



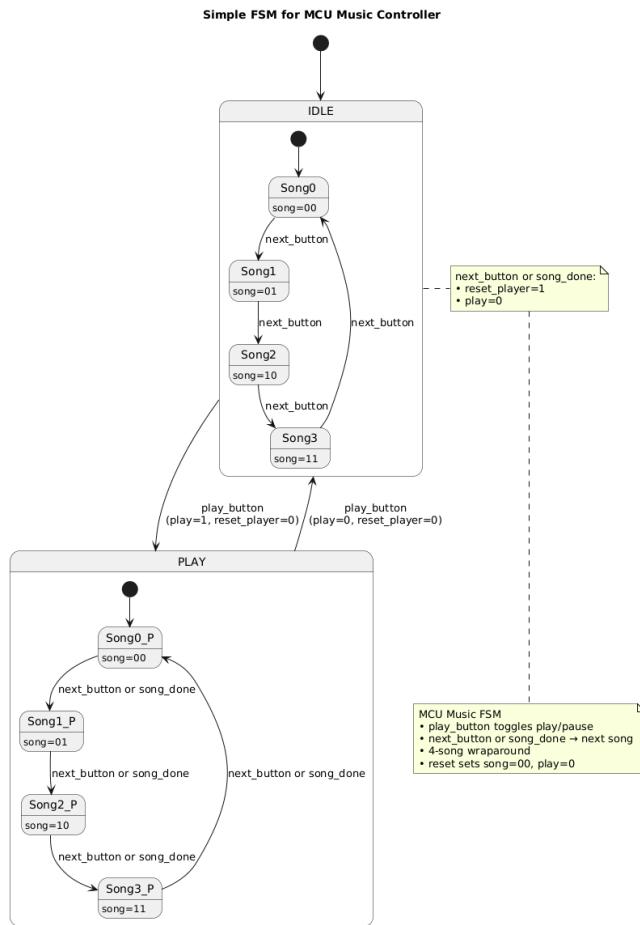
3.FSM state diagrams for song_reader and the MCU.

Song_reader.v:

song_reader FSM



MCU.v:



4. Timing diagrams for the song_reader, note_player, and sine_reader showing the delay in reading from the ROMs

- song_reader

Cycle	play	note_done	ref_addr[6:0]	rom_data_q {note,dur}	new_note	note	duration	state
0	1	0	01_00000	xxxxxxxxxxxx	0	000000	000000	IDLE
1	1	0	01_00000	xxxxxxxxxxxx	0	000000	000000	READ
2	1	0	01_00000	n0,d0	0	000000	000000	WAIT_ROM (ROM latency)
3	1	0	01_00000	n0,d0	1	n0	d0	SEND_NOTE (pulse)

4	1	0	01_00000	n0,d0	0	n0	d0	WAIT_DONE
5	1	1	01_00001	xxxxxxxxxxxx	0	n0	d0	READ (idx++)
6	1	0	01_00001	n1,d1	0	n0	d0	WAIT_ROM
7	1	0	01_00001	n1,d1	1	n1	d1	SEND_NOTE
8	1	0	01_00001	n1,d1	0	n1	d1	WAIT_DONE
9	1	1	01_00010	xxxxxxxxxxxx	0	n1	d1	READ (idx++)
...
k	1	1	01_11111	n31,d31	0	n31	d31	READ or DONE if d31=0
k+1	0	0	—	—	0	—	—	IDLE after song_done and play=0

- note_player

Cycle	reset	load_new_note	play_enable	beat	n o t e — t o — l o a d	dur_to_load	n o t e — q	d u r — q	f r e — q	step_size	gen_next	sine_sample	sine_ready	new_sample_ready	done_with_note
0	1	0	0	0	—	—	0 0	0 0	0 0	xxxx	0	0000	0	0	0

1	0	1	1	0	n 0	d0	n 0	d 0	n 0	xxxx	0	0000	0	0	0
2	0	0	1	0	—	—	n 0	d 0	n 0	S0	1	s0	1	1	0
3	0	0	1	0	—	—	n 0	d 0	n 0	S0	1	s1	1	1	0
...	0	0	1	1	—	—	n 0	d 0	n 0	S0	1	sk	1	1	0 (count down)
t	0	0	1	1	—	—	n 0	0 0	n 0	S0	1	s*	1	1	1 (done pulse)
t+1	0	1	1	0	n 1	d1	n 1	d 1	n 1	S1	1	s0	1	1	0 (next note)

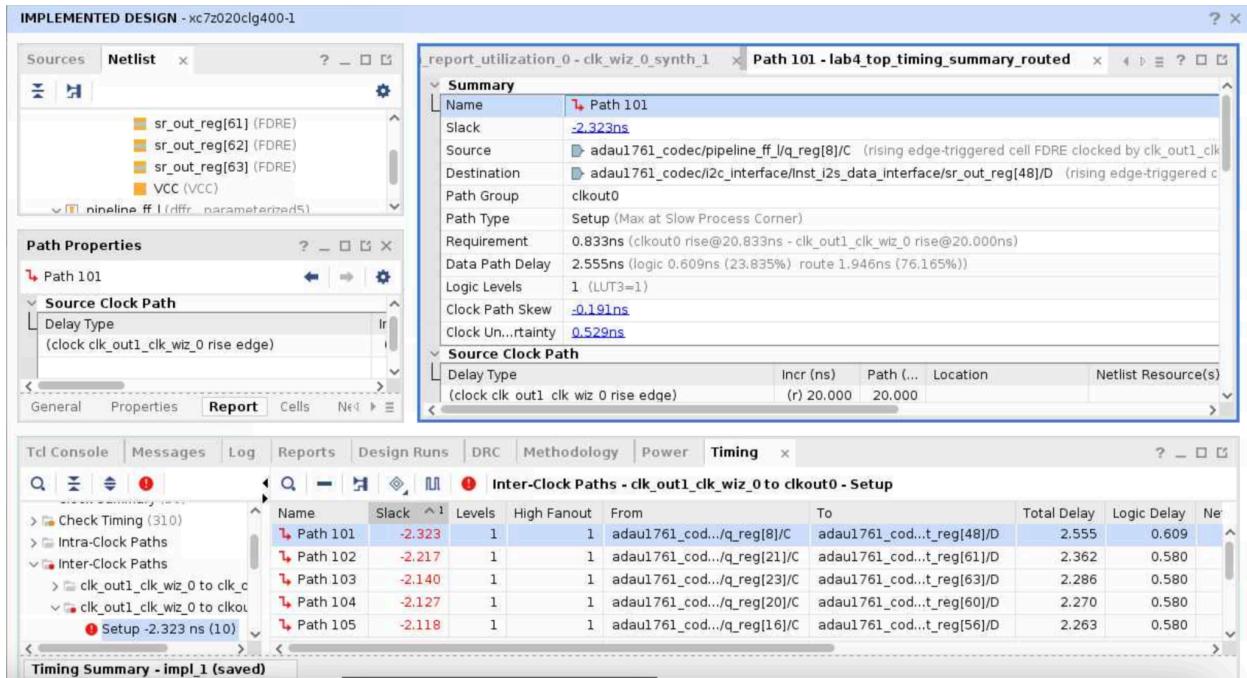
- sine_reader

Cycle	reset	generate_next	phase (Q.F)	rom_addr	rom_data	quad/quad_d	sample	sample_ready
0	1	0	0.0	0000000000	xxxx	00/xx	0000	0
1	0	1	P1	A0	xxxx	q0/xx	0000	1
2	0	1	P2	A1	D0	q1/q0	0000	1
3	0	1	P3	A2	D1	q1/q1	±D0	1
4	0	1	P4	A3	D2	q2/q2	±D1	1
5	0	0	hold	A3	D2	hold/hold	±D1	0

5.The critical path of your design. You can find it by going to “Design Runs” then double clicking on the Worst Negative Slack (WNS). Then, click on the Worst Negative Slack value under “Setup.” This report lists the longest paths in your design, with the one with the least positive/most negative being the critical path. Report the slack, source, and destination of the critical path. Look at the list of locations the signal visits under ‘Maximum Data Path’. Do you recognize where in your logic this path comes from?

Design Timing Summary		
Setup	Hold	Pulse Width
Worst Negative Slack (WNS): -2.323 ns	Worst Hold Slack (WHS): 0.022 ns	Worst Pulse Width Slack (WPWS): 2.00 ns
Total Negative Slack (TNS): -35.124 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.0 ns
Number of Failing Endpoints: 17	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 510	Total Number of Endpoints: 510	Total Number of Endpoints: 302

Worst Negative Slack: -2.323ns.



Path 101 is the longest path, and the source and destination are:

Source	adau1761_codec/pipeline_ff_l/q_reg[8]/C (rising edge-triggered cell FDRE clocked by clk_out1_clk_wiz_0)
Destination	adau1761_codec/i2c_interface/Inst_i2s_data_interface/sr_out_reg[48]/D (rising edge-triggered cell FDRE clocked by clk_out1_clk_wiz_0)

This path describes the entire logic chain between two flip flops in the note_player module.

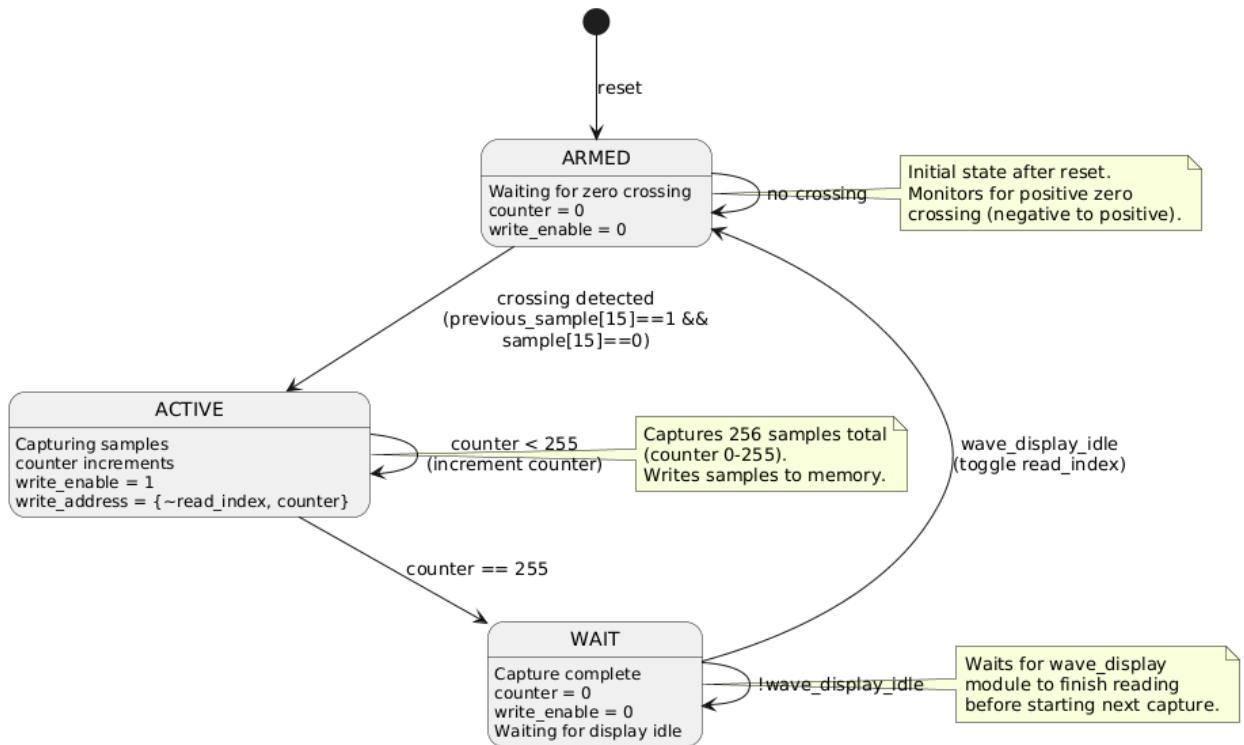
Lab 5 Report

Lab Members:

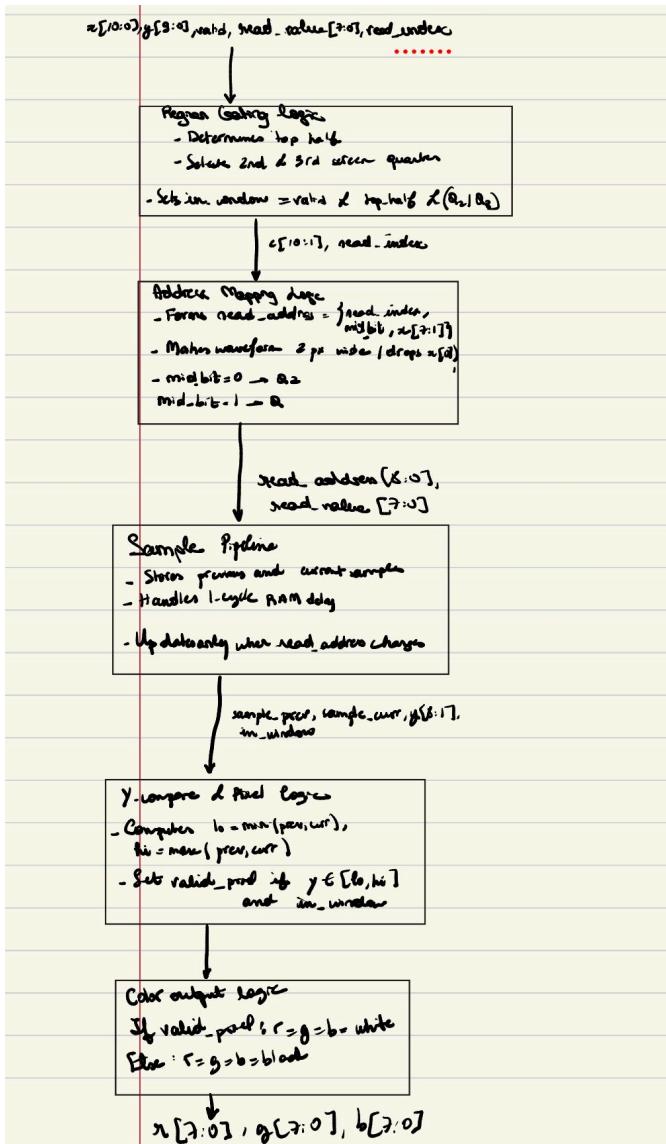
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1. Block/FSM diagrams

1. Wave_capture_tb



2. Wave_display



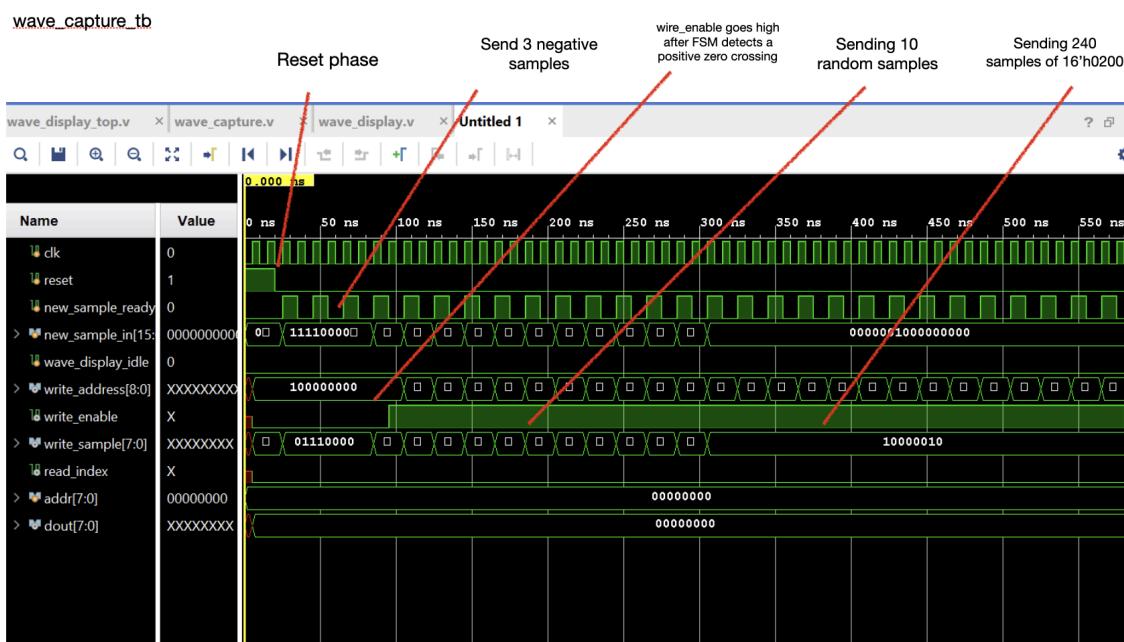
3. Timing diagram for wave_display

Cycle	read_address	read_value	read_value_adjusted	sample_prev	sample_curr	valid_pixel
0	0	10	37	0	0	0
1	1	20	42	0	37	depends on y

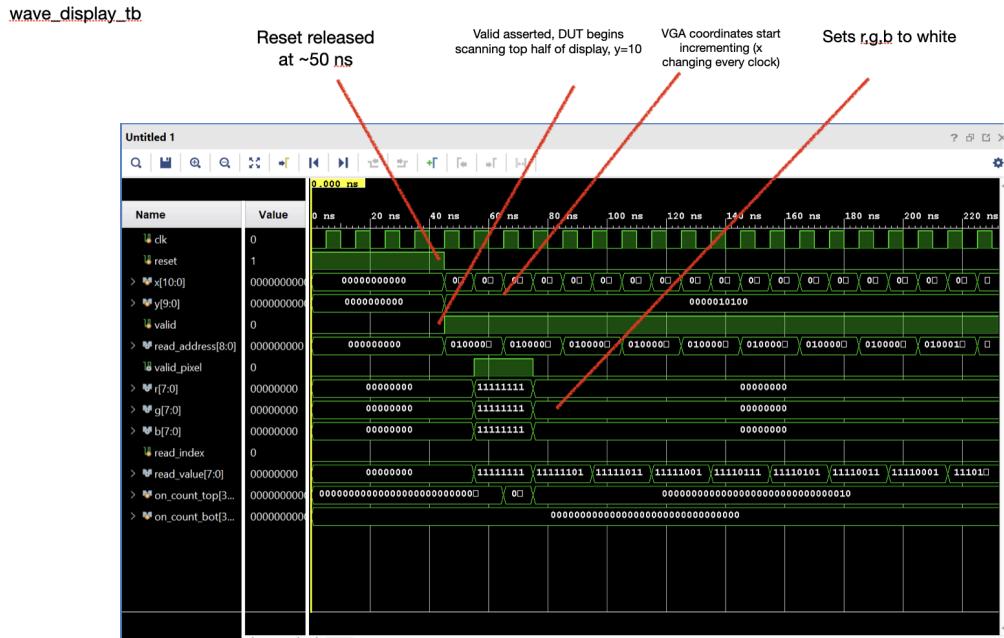
2	2	30	47	37	42	depends on y
3	3	40	52	42	47	depends on y

2. Annotated Wave forms

1. Wave_capture_tb



2. Wave_display_tb



3. Critical Path of design

Summary				
Name	Path 105			
Slack	1.289ns			
Source	wd_top/wd/sample_prev_ff/q_reg[1]/C (rising edge-triggered cell FDRE clocked by clk_out1_clk_wiz_0)			
Destination	U3/inst/srl16ly_0/srl[39].sr16_l/D (rising edge-triggered cell SRL16E clocked by clk_out2_clk_wiz_0)			
Path Group	clk_out2_clk_wiz_0			
Path Type	Setup (Max at Slow Process Corner)			
Requirement	10.000ns (clk_out2_clk_wiz_0 rise@40.000ns - clk_out1_clk_wiz_0 rise@30.000ns)			
Data Path Delay	8.169ns (logic 2.345ns (28.708%) route 5.824ns (71.292%))			
Logic Levels	7 (CARRY4=2 LUT3=1 LUT4=1 LUT5=1 LUT6=2)			
Clock Path Skew	-0.315ns			
Clock Uncertainty	0.210ns			
Source Clock Path				
Delay Type	Incr (ns)	Path (...)	Location	Netlist Resource(s)
(clock clk_out1_clk_wiz_0 rise edge)	(r) 30.000	30.000		

The Maximum Data Path goes through several flip flops as well as checking if the location of the current pixel is valid. This makes us assume that the maximum data path occurs in wave_display where it tries to check for the window in which to plot the signal.