PRÀCTICA 1:

ESTRUCTURA DE COMPUTADORS

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GEI
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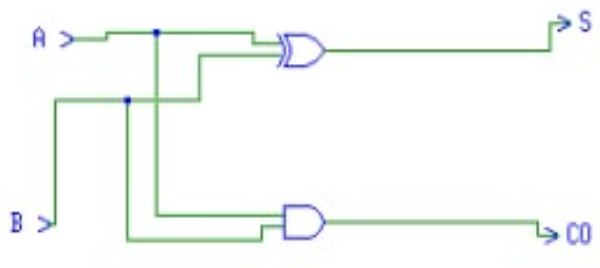
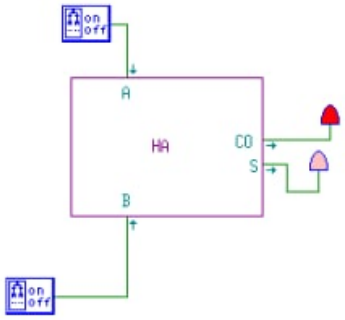
UNIVERSITAT ROVIRA I VIRGILI

ÍNDEX

1.- FASE 1

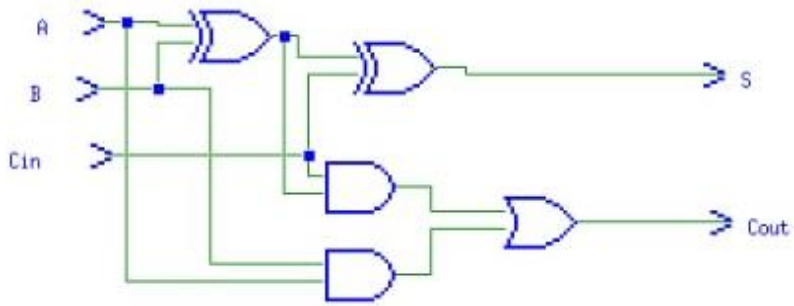
1.1.- Tarea 1:





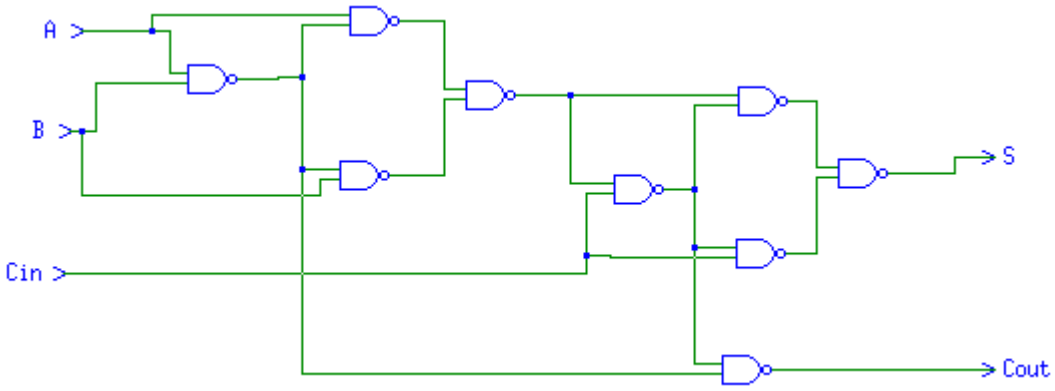
RetardoC = 3T
RetardoS = 4T

1.2.- Tarea 2:



RetardoC = 10T
RetardoS = 8T

1.3.- Tarea 3:

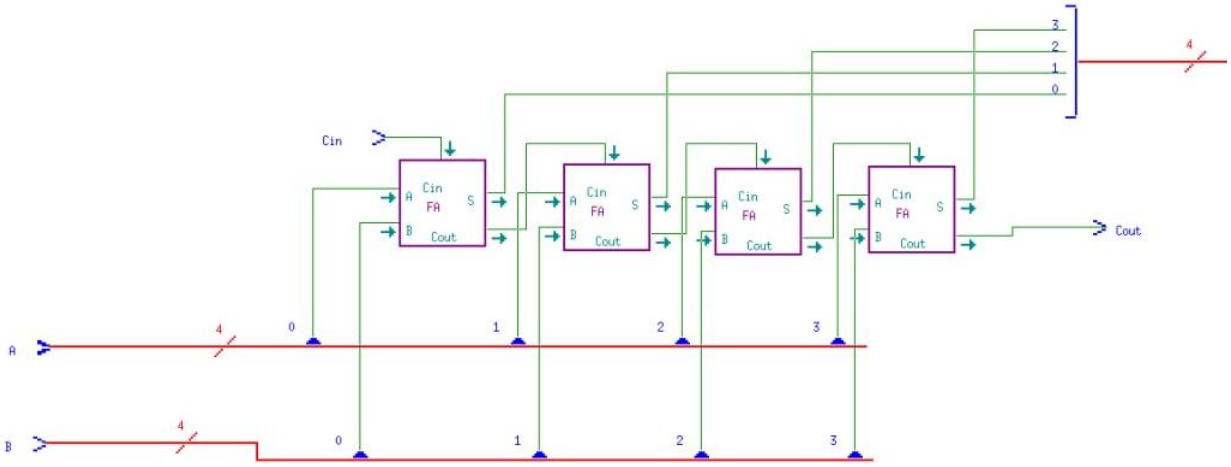


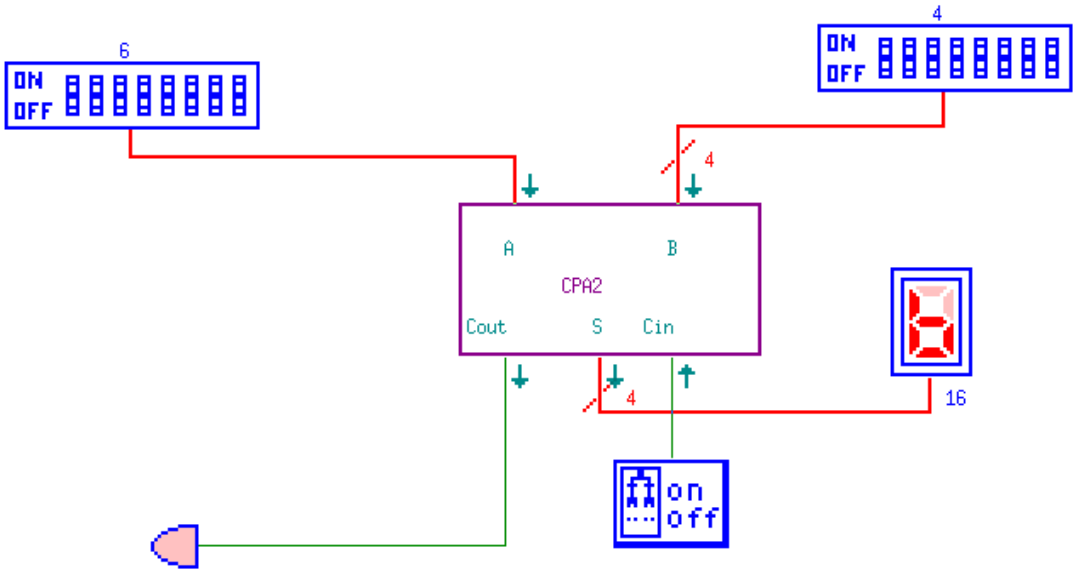
Suponemos un retardo de la NAND de 3T.

RetardoS = 18T
Retardo C = 15T

2.- FASE 2

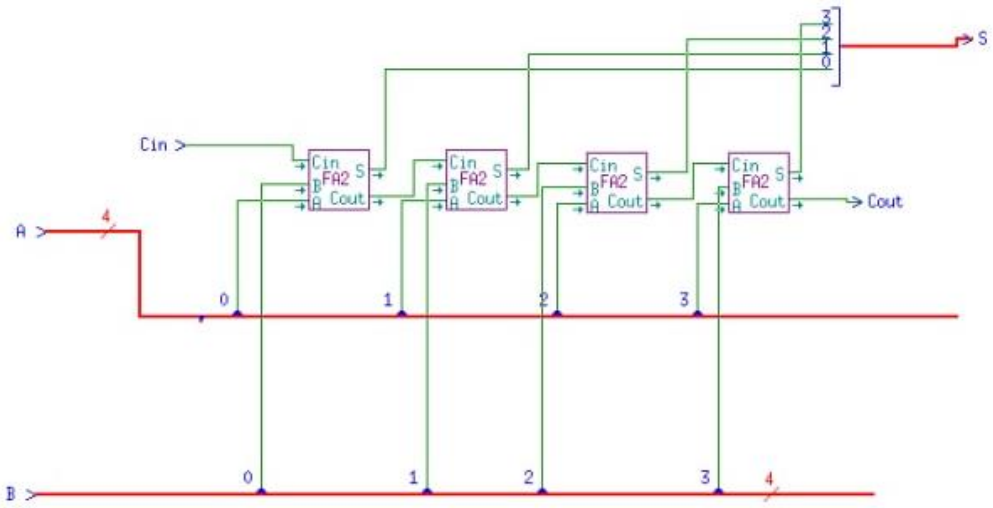
2.1.- Tarea 4:

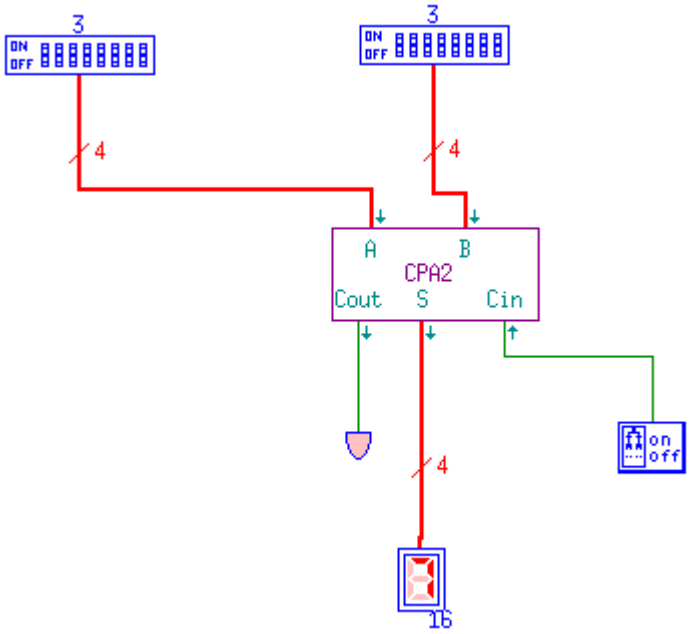




RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 10T + (4-1) * (10T - 4T) = 28T
RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela) =
= 10T + (4-2) * (10T - 4T) + (8T - 4T) = 30T

2.2.- Tarea 5:





TC=15 ; TS=18

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 15T + (4T-1bits) * (15T-9T) = 33T

RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 15T + (4T-2bits) * (15T-9T) + (18T-9T) = 36T

2.3.- Tarea 6:

IMPLEMENTACIÓ 1.

TS= 8 ; TC= 10

(4bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 10T + (4T-1bits) * (10T-4T) = 28T

RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 10T + (4T-2bits) * (10T-4T) + (8T-4) = 30T

(16 bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 10T + (16-1 bits) * (10T-4T) = 100T

RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 10T + (16-2bits)*(10T-4T) + (8T-4T) = 98T

(32bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 10T + (32-1bits)*(10T-4T) = 196T

RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 10T + (32T-2bits)*(10T-4T) + (8T-4T) = 194T

(128 bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 10T + (128T-1bits)*(10T-4T) = 772T

RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 10T + (128T-2bits)*(10T-4T) + (8T-4T) = 770T

IMPLEMENTACIÓ 2.
TS= 18 ; TC= 15
(4bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 15T + (4T-1bits) * (15T-9T) = 33T
RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 15T + (4T-2bits) * (15T-9T) + (18T-9T) = 36T
(16 bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 15T + (16-1 bits) * (15T-9T) = 105T

RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 15T + (16-2bits)*(15T-9T) + (18T-9T) = 108T

(32bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 15T + (32-1bits)*(15T-9T) = 201T

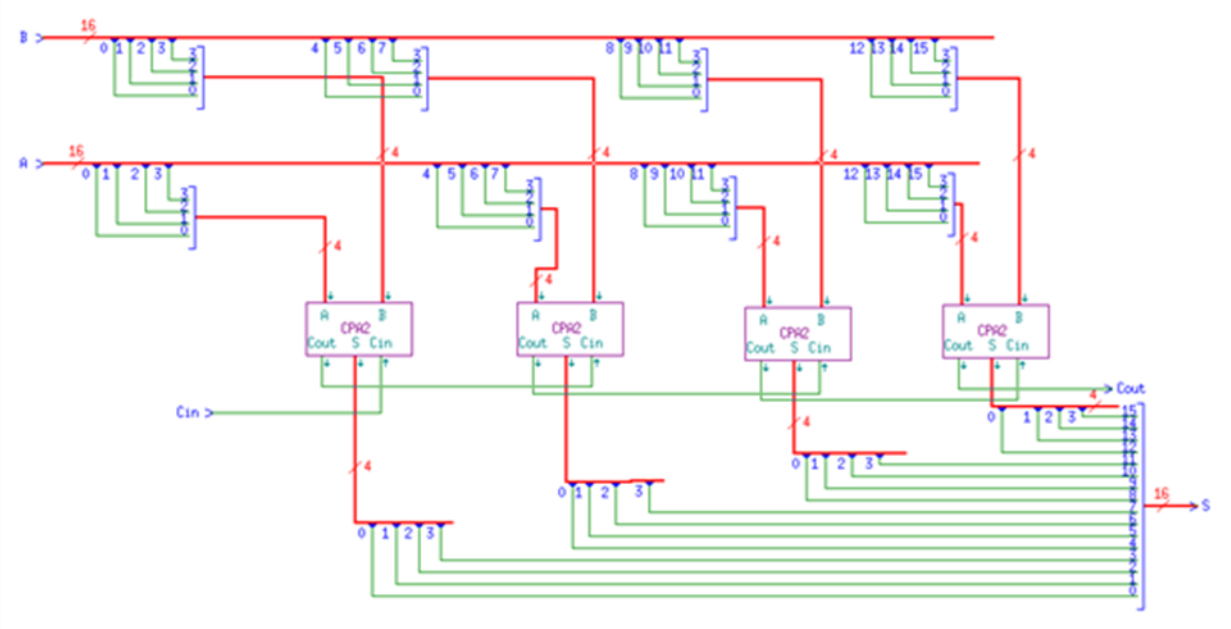
RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 15T + (32T-2bits)*(15T-9T) + (18T-9T) = 204T

(128 bits)

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 15T + (128T-1bits)*(15T-9T) = 777T

RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 15T + (128T-2bits)*(15T-9T) + (18T-9T) = 780T

2.4.- Tarea 7:



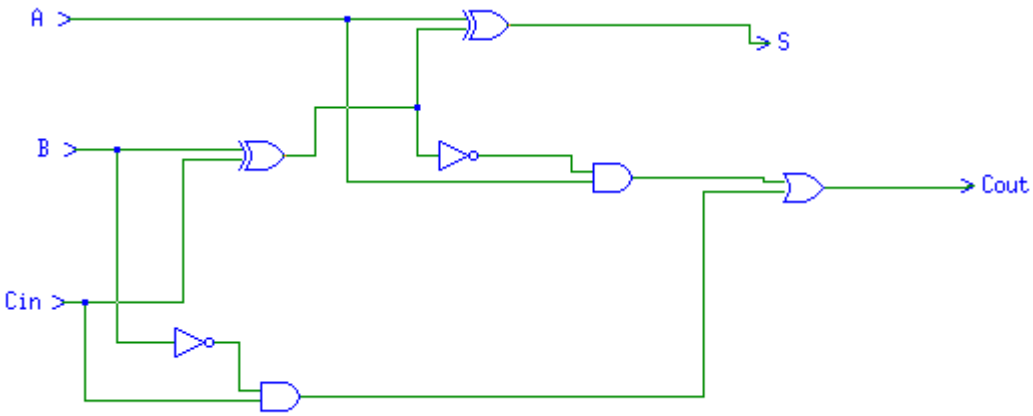
TC=10T ; TS=8T

RetardoC = TC(bit0) + (n-1 bits)*(TC-ParteParalela) =
= 10T + (16-1 bits) * (10T-4T) = 100T

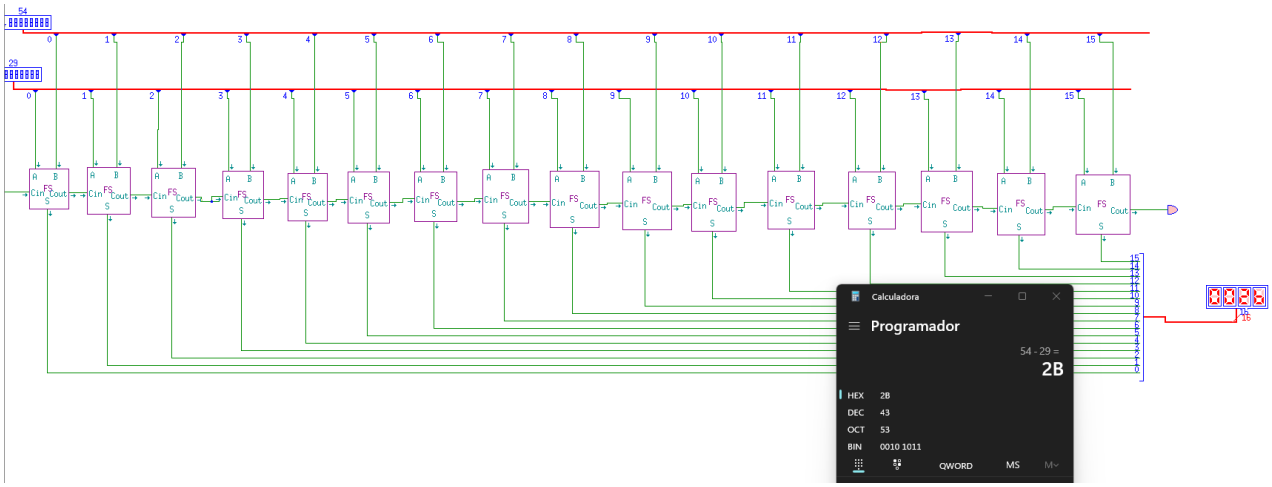
RetardoS = TC(bit0) + (n-2 bits)*(TC-ParteParalela) + (TS-ParteParalela)=
= 10T + (16-2bits)*(10T-4T) + (8T-4T) = 98T

2.5.- Tarea 8:

Full Substractor



Restador 16 Bits



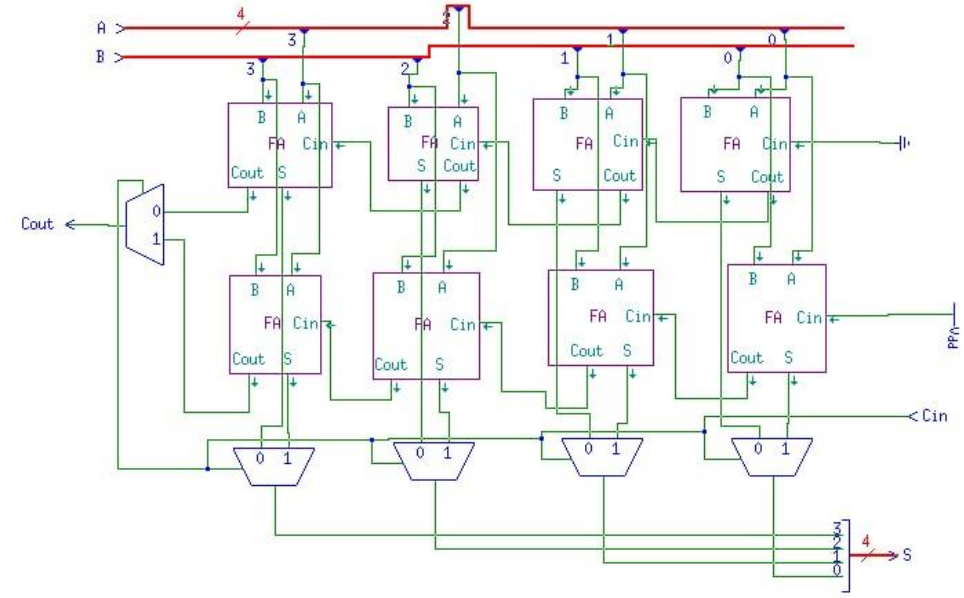
A=54

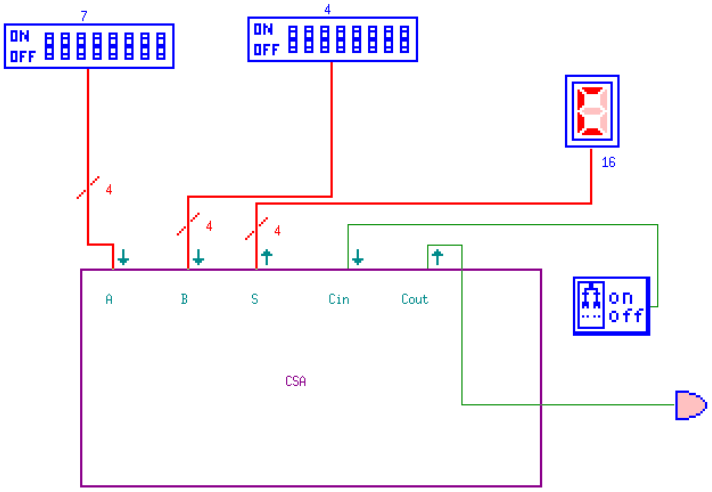
B=29

Cin activado

3.- FASE 3

3.1.- Tarea 9:





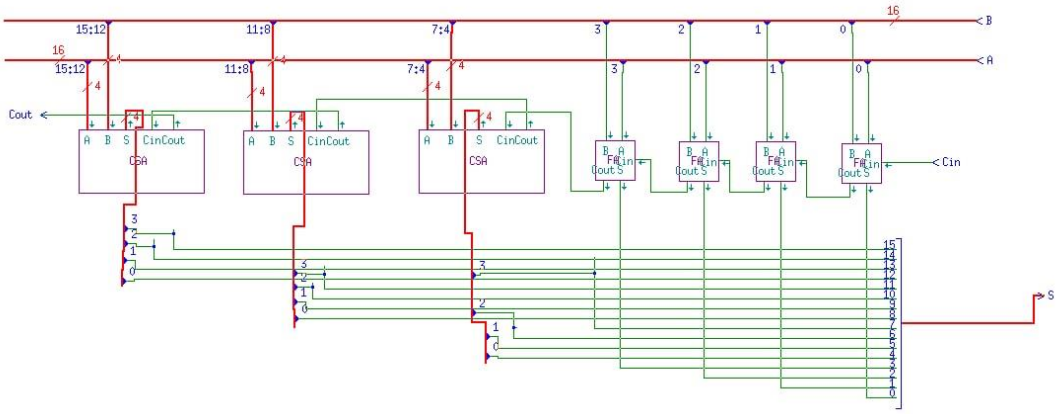
S(0)=8T
Cout(0)=10T
Stotal=10T+(4-2)*(10T-4T)+(8-4T)=26T
Ctotal=10+(3)*(10-4)=28T
RetardoCSA = RetardoCPA + RetardoMux = 28T + 2T = 30T

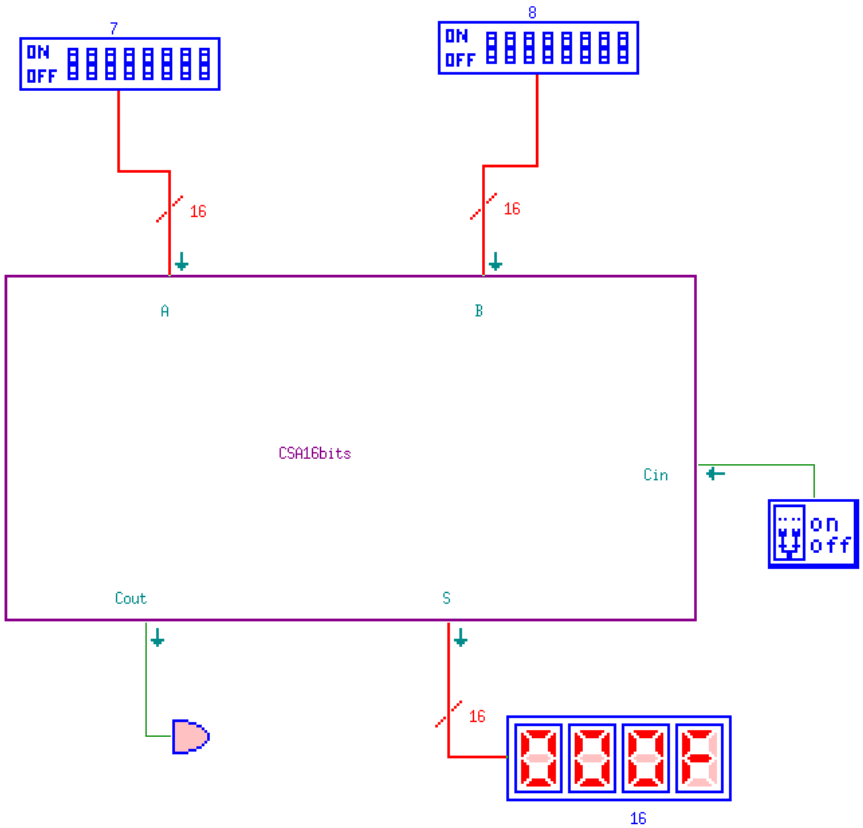
Area Xor=8, AND=6, OR=6
Area total=8*(2*8)+8*(2*6)+8*(6)+5*8=312

3.2.- Tarea 10:

RetardoCSA16bits = RetardoCPA0 +(M_módulos-1) * RetardoMux =

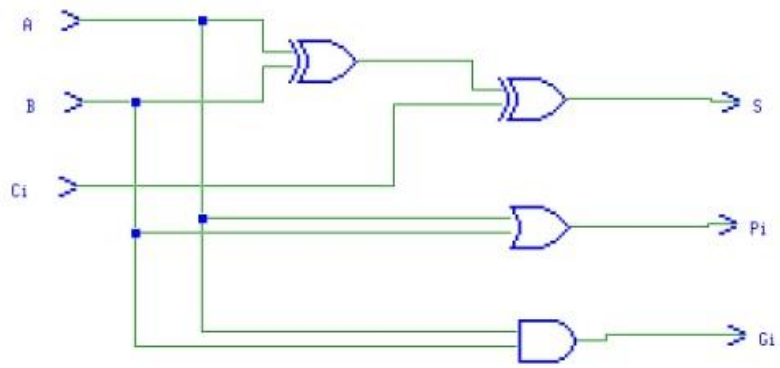
$$30T + (4-1)*2T = 36T$$





4.- FASE 4

4.1.- Tarea 11:



RetardoS = 8T
RetardoPi = 3T
RetardoGi = 3T

4.2.- Tarea 12:

Retardo CLA:

Generar y propagar	A, B	3 (AND)
C1 a Cn	P, G, C0	6 (Suma de productos)
Suma S	C, A, B	4 (XOR)
RETARDO TOTAL =		**13**

4.3.- Tarea 14:

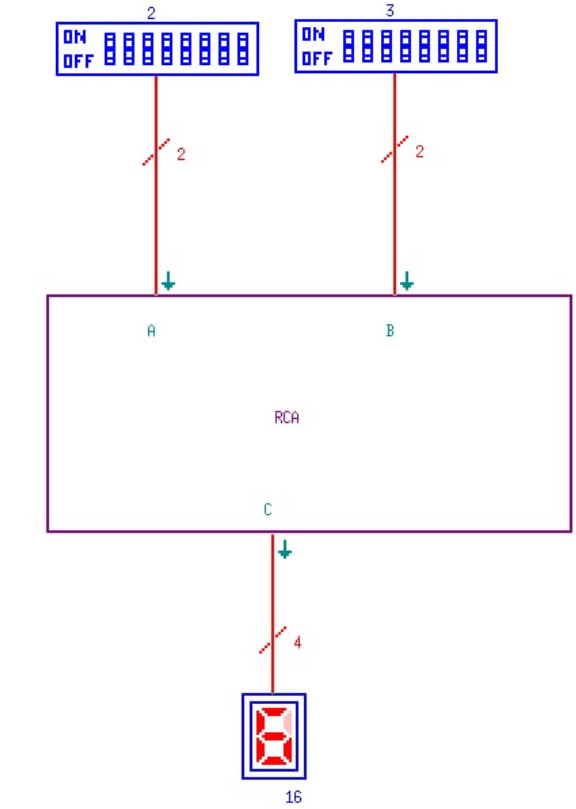
CLA1	**CLA2**	**CLA3**	**CLA4**
Retardo	Retardo	Retardo	Retardo
C0=0T	C0=15T	C0=27T	C0=39T
C1=6T	C1=18T	C1=30T	C1=42T
C2=9T	C2=21T	C2=33T	C2=45T
C3=12T	C3=24T	C3=36T	C3=48T
C4=15T	C4=27T	C4=39T	C4=51T
S0=8T	S0=19T	S0=31T	S0=43T
S1=10T	S1=22T	S1=34T	S1=46T
S2=13T	S2=25T	S2=37T	S2=49T
S3=16T	S3=28T	S3=40T	S3=55T

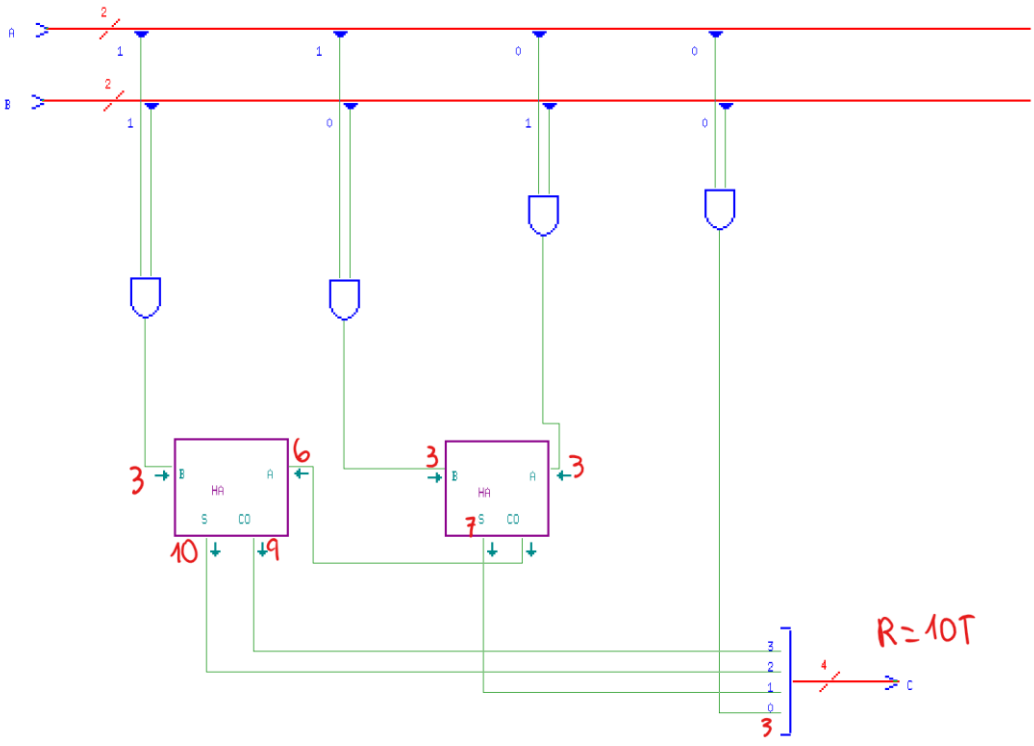
4.5.- Tarea 15:
Resum temps de retard i área:
CPA (16 bits)
Retardo=100T
CSA (16 bits)
Retardo=34T
CLA (16 bits)
Retardo=55T

Si analizamos los tiempos de retardo obtenidos en los diferentes circuitos podemos llegar a la conclusión de que el sumador más rápido entre los 3 es el CSA de 16 bits, siendo el CPA de 16 bits el más lento.

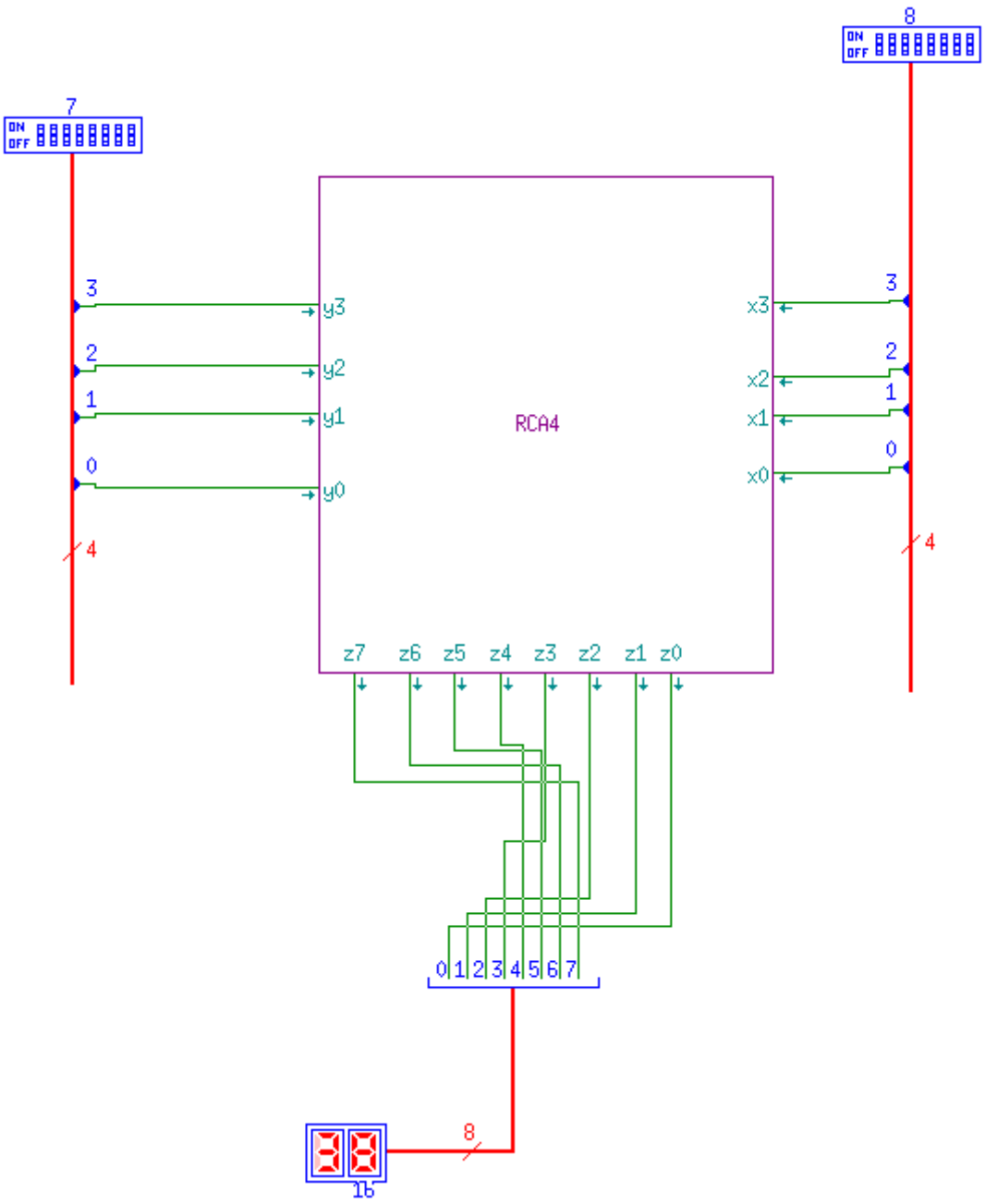
5.- FASE 5

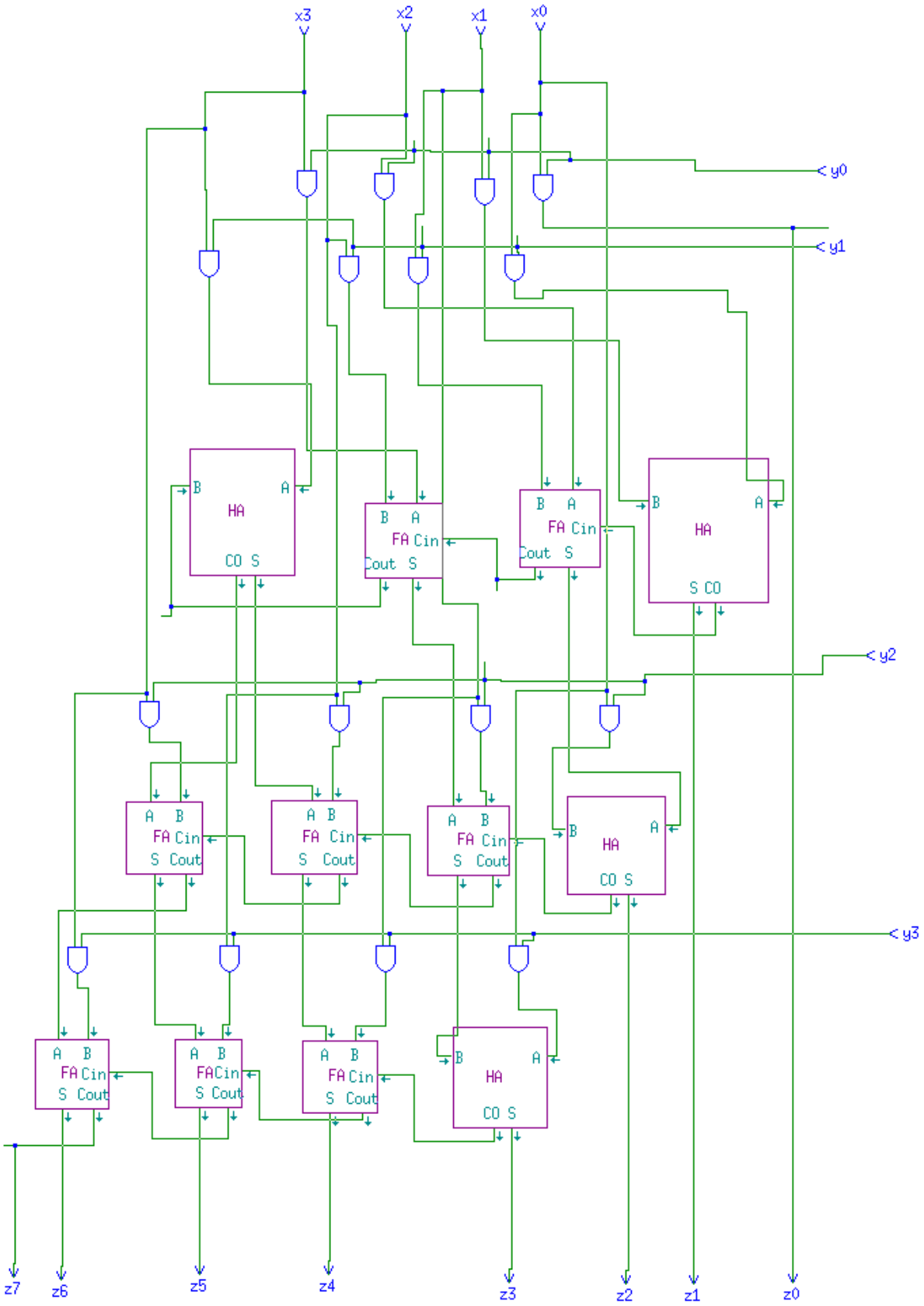
5.1.- Tarea 16:



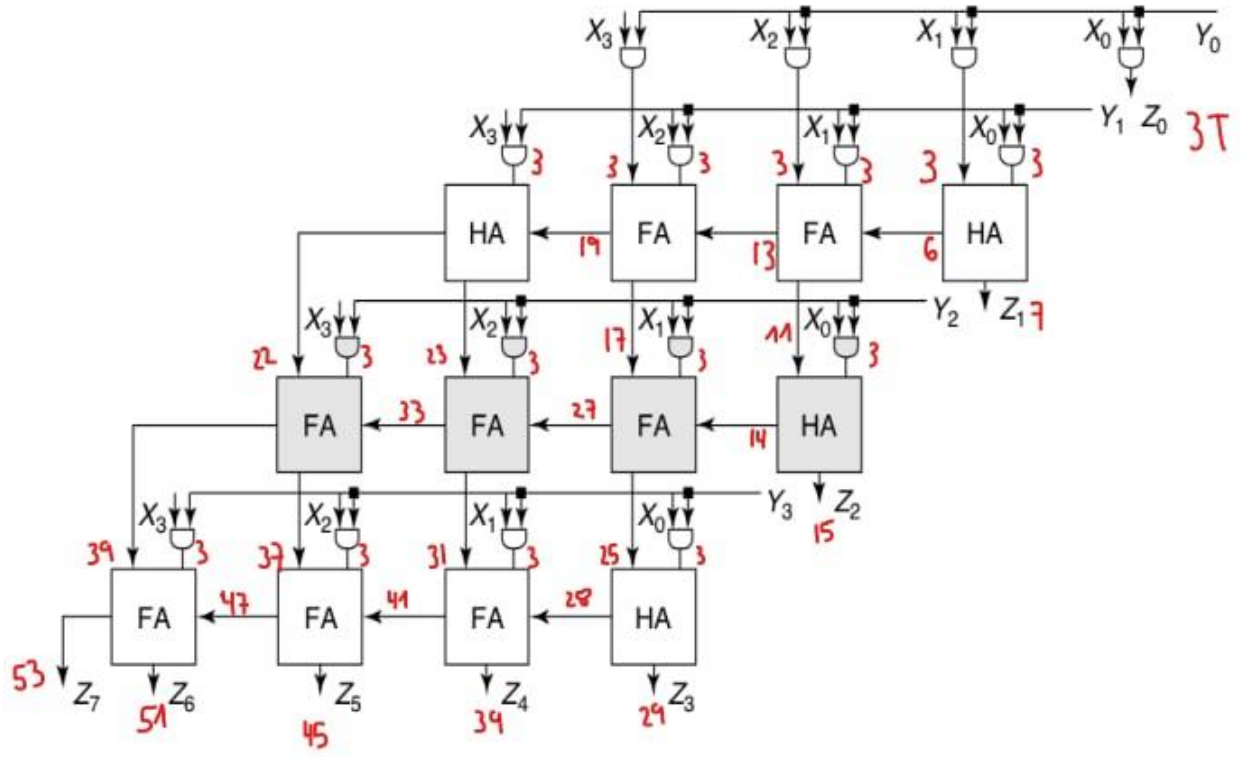


5.2.- Tarea 17:


8
7
3
2
1
0
y3
y2
y1
y0
RCA4
x3
x2
x1
x0
3
2
1
0
4
4
z7 z6 z5 z4 z3 z2 z1 z0
0 1 2 3 4 5 6 7
8
16


x3
x2
x1
x0
y0
y1
y2
y3
HA
FA Cin
S Cout
z7
z6
z5
z4
z3
z2
z1
z0

5.3.- Tarea 18:



T total = 53T

Área Total = (4*HA) + (8*FA) + (16*AND) =

= (4*14) + (8*34) + (16*6) = 424