LABORATORY 1 : Gate Design

VLSI .Curs 20-21. Cuatrimestre de tardor

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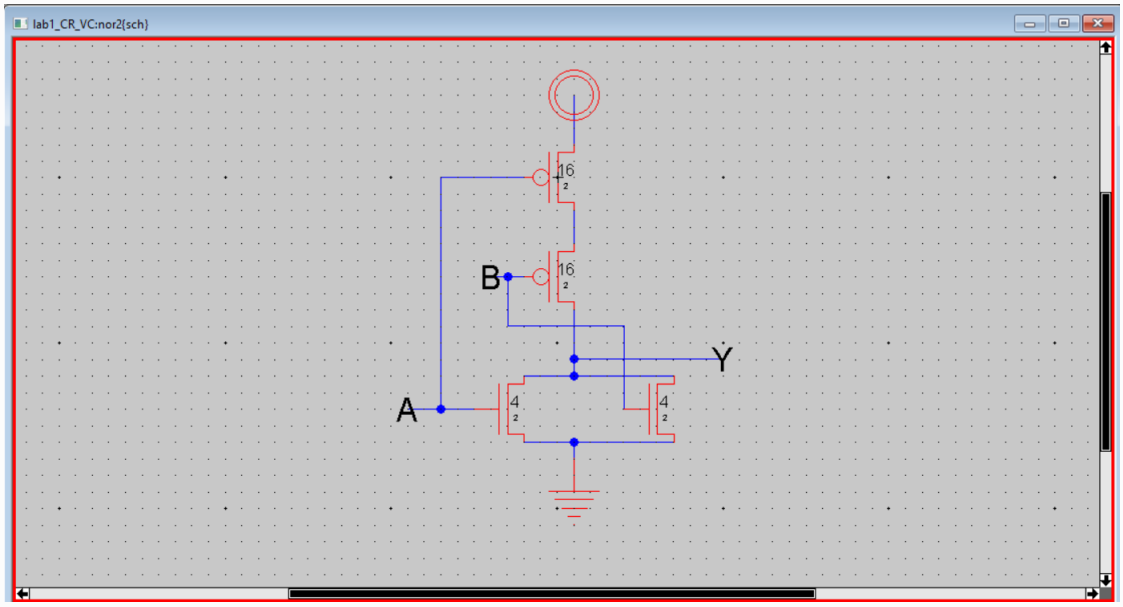
LAB 1: Gate Design

1. Work Time

8h between understanding the program and working in the laboratory

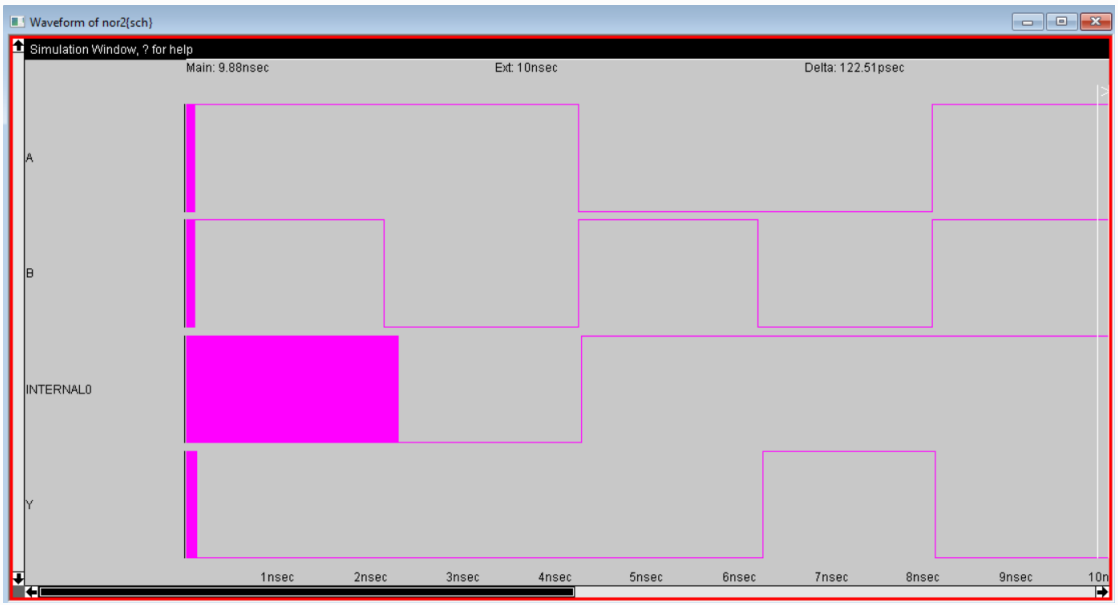
2. Schematic nor2

Schematic consisting of 2 transistors pMOS in series and 2 transistors nMOS in parallel. NOR with 2 inputs and 1 output

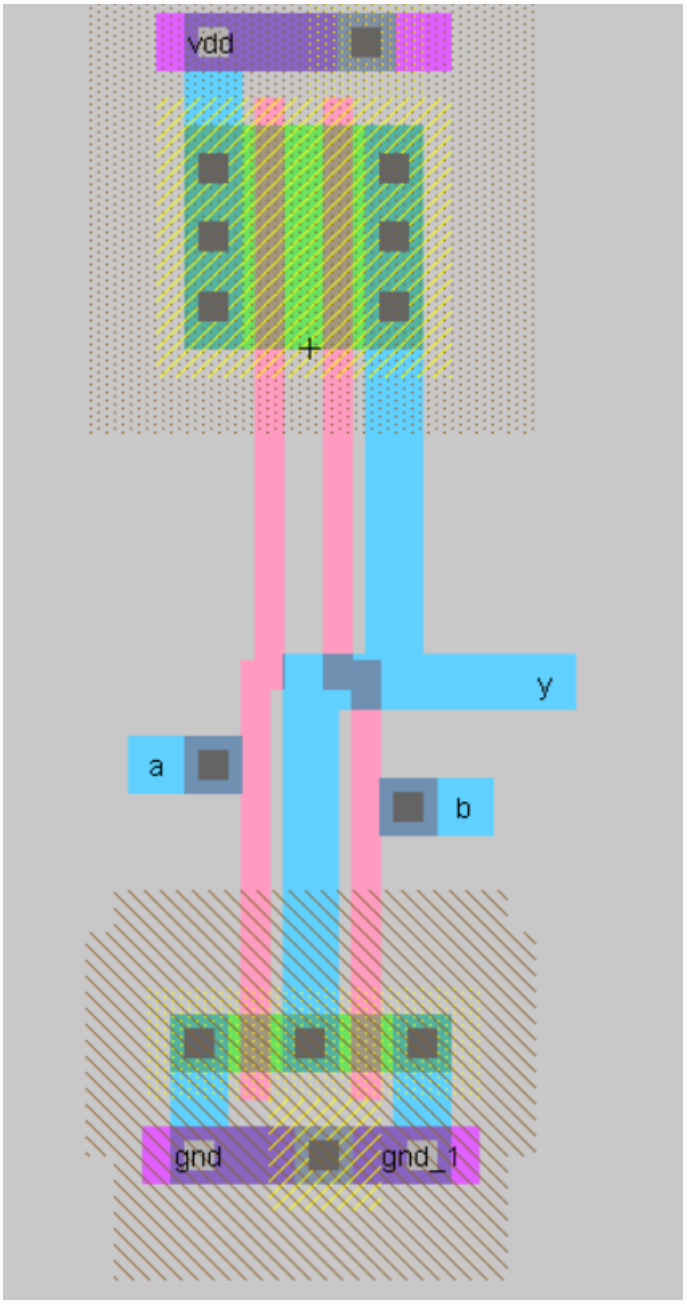


2.1 Waveform simulate nor2

We see that for the values A=0 and B=0, Y=1



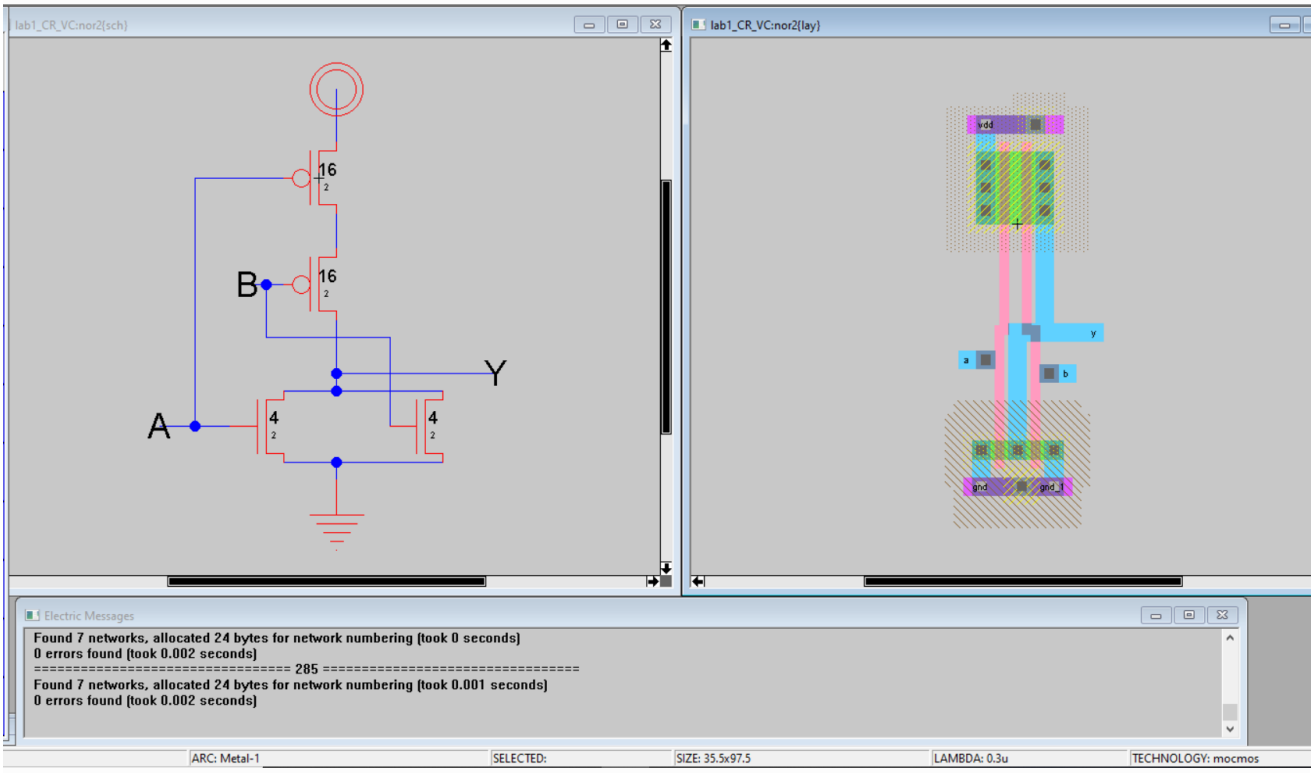
3. Layout nor2



2.1 Layout Verification Nor2

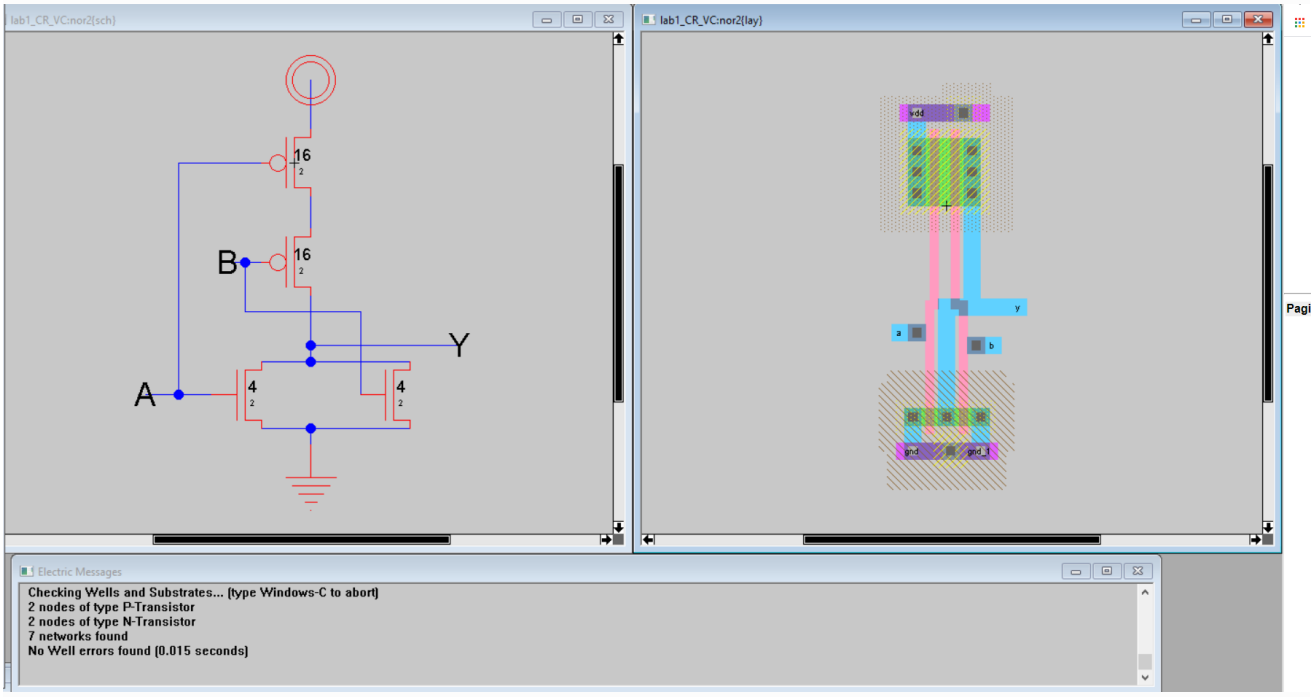
2.1.1 DRC

PASS!



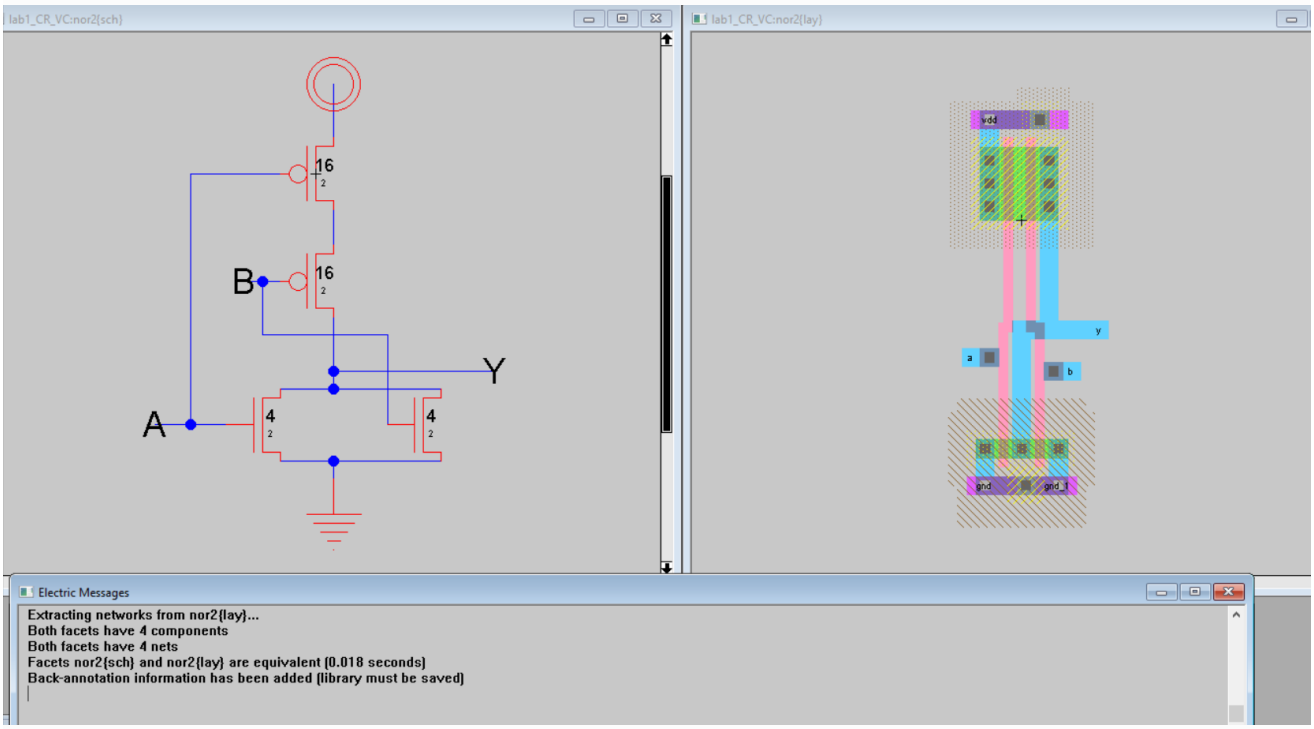
2.1.2 ERC

PASS!



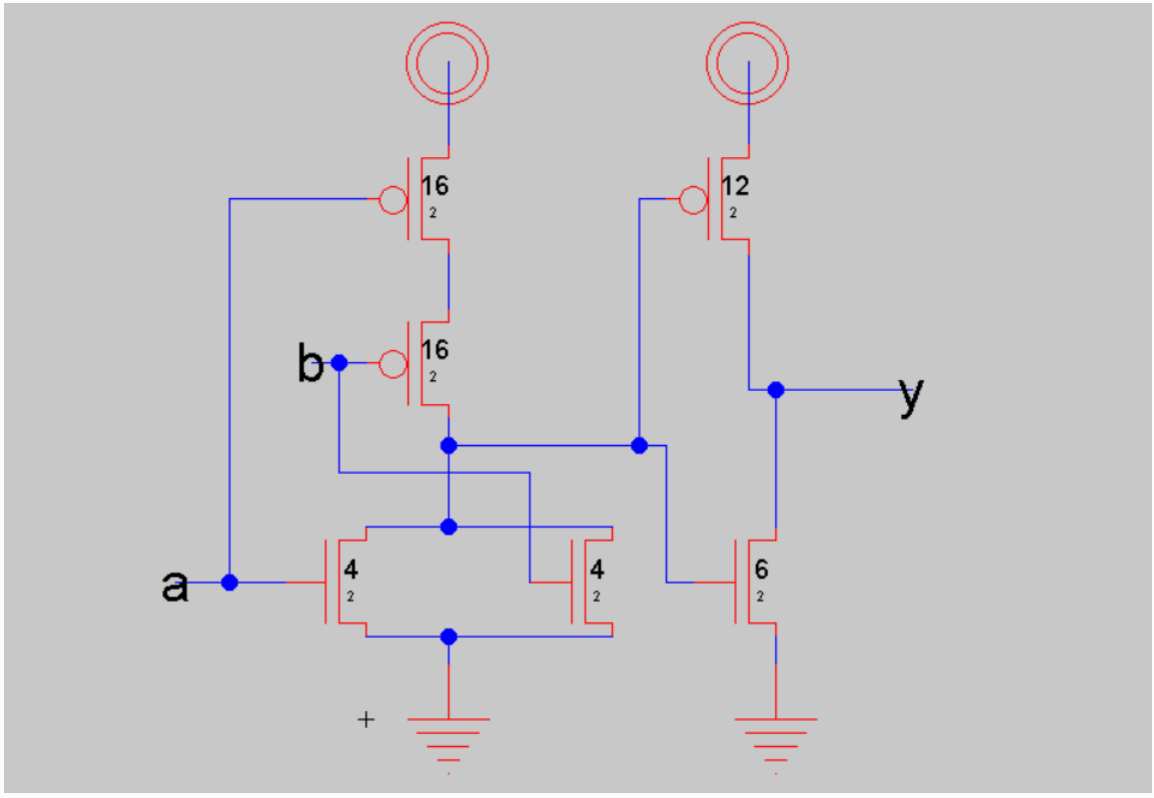
2.1.3 NCC

PASS!

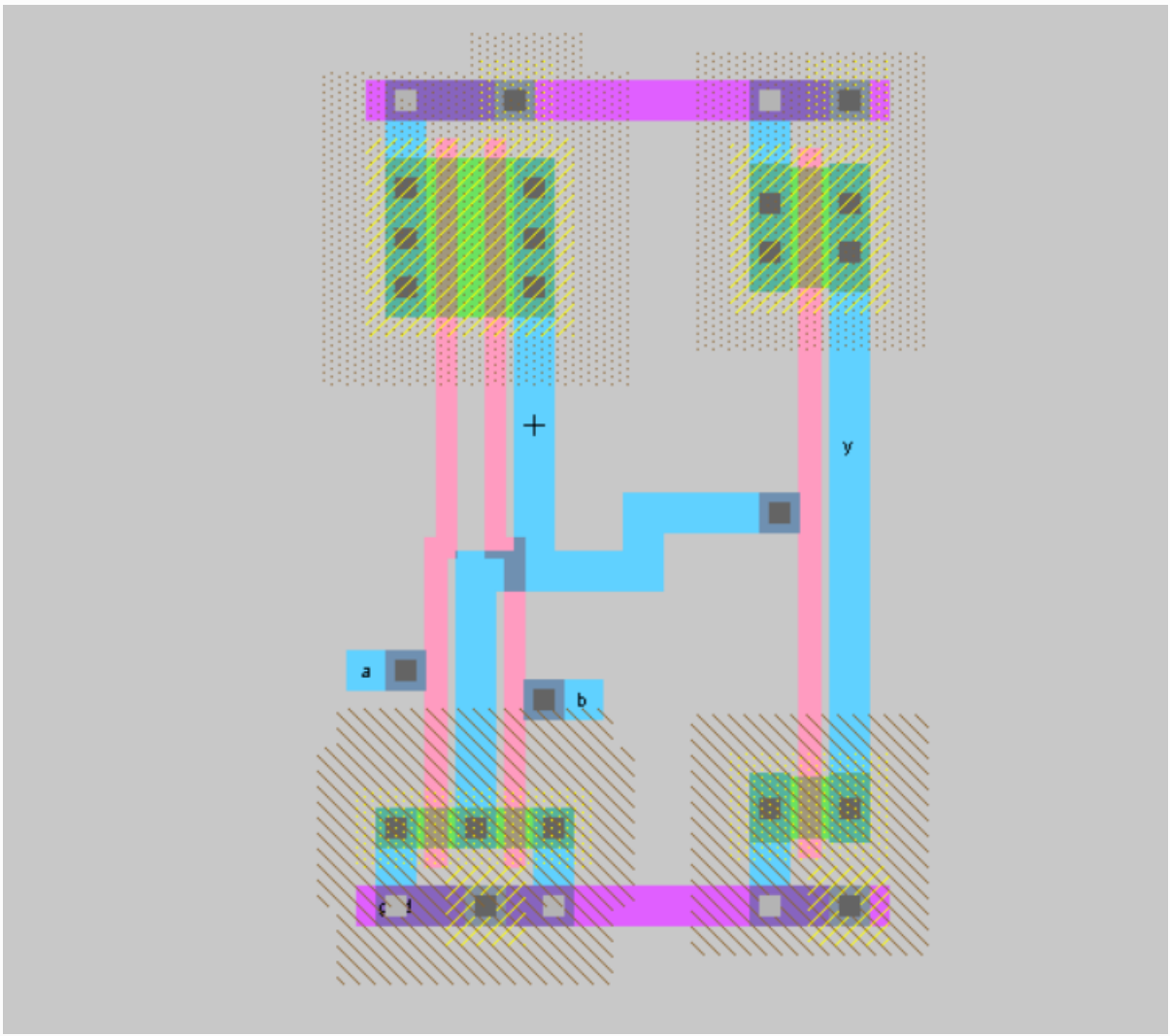


4. Schematic Or2

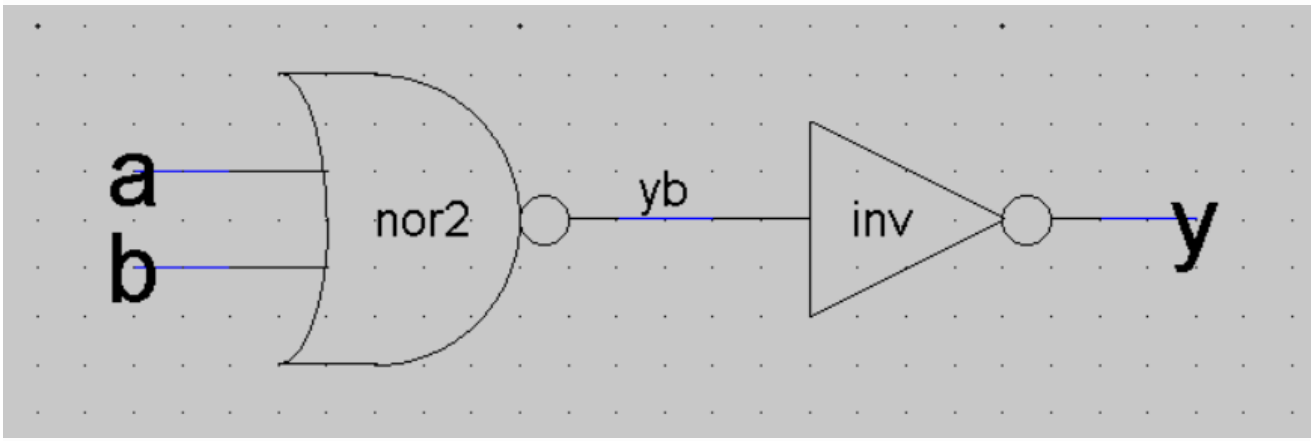
Schematic consisting in one 2-NOR and 1-INV. OR with 2 inputs and 1 output



5. Layout Or2

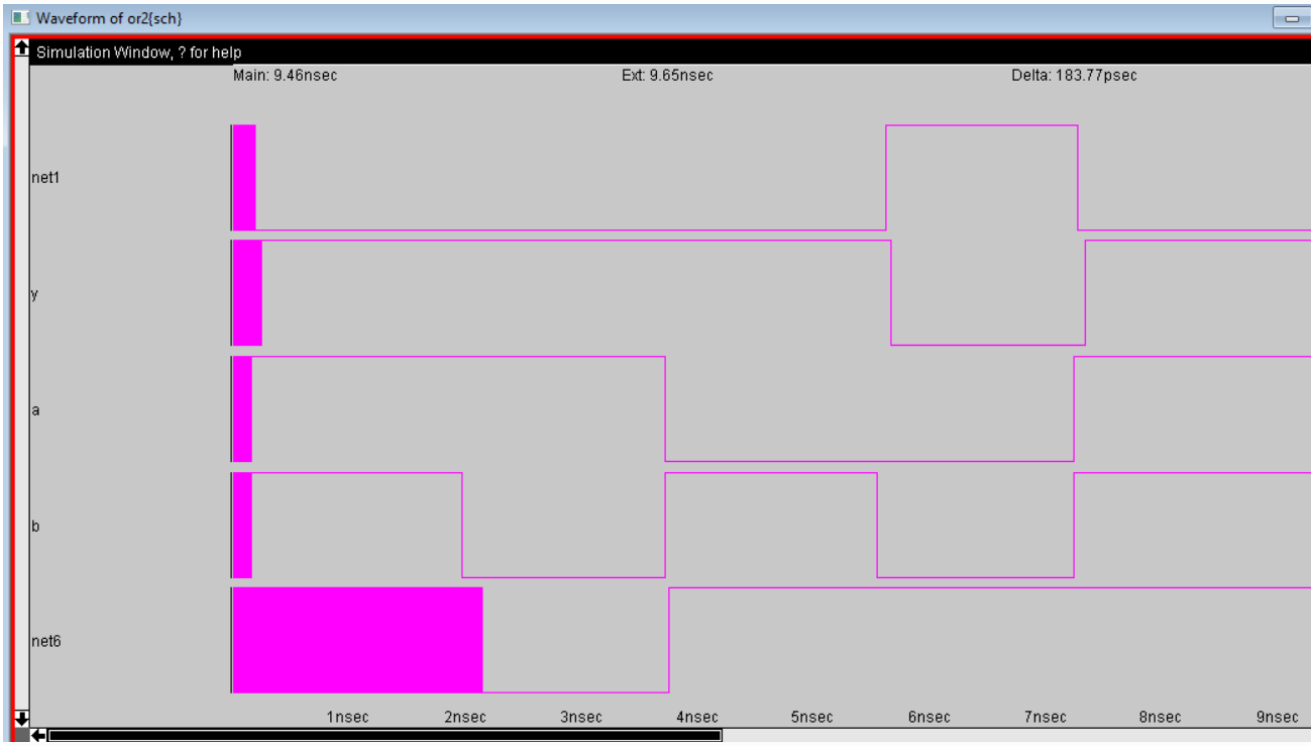


5.1 Icon Or2



6. Waveform simulate Or2

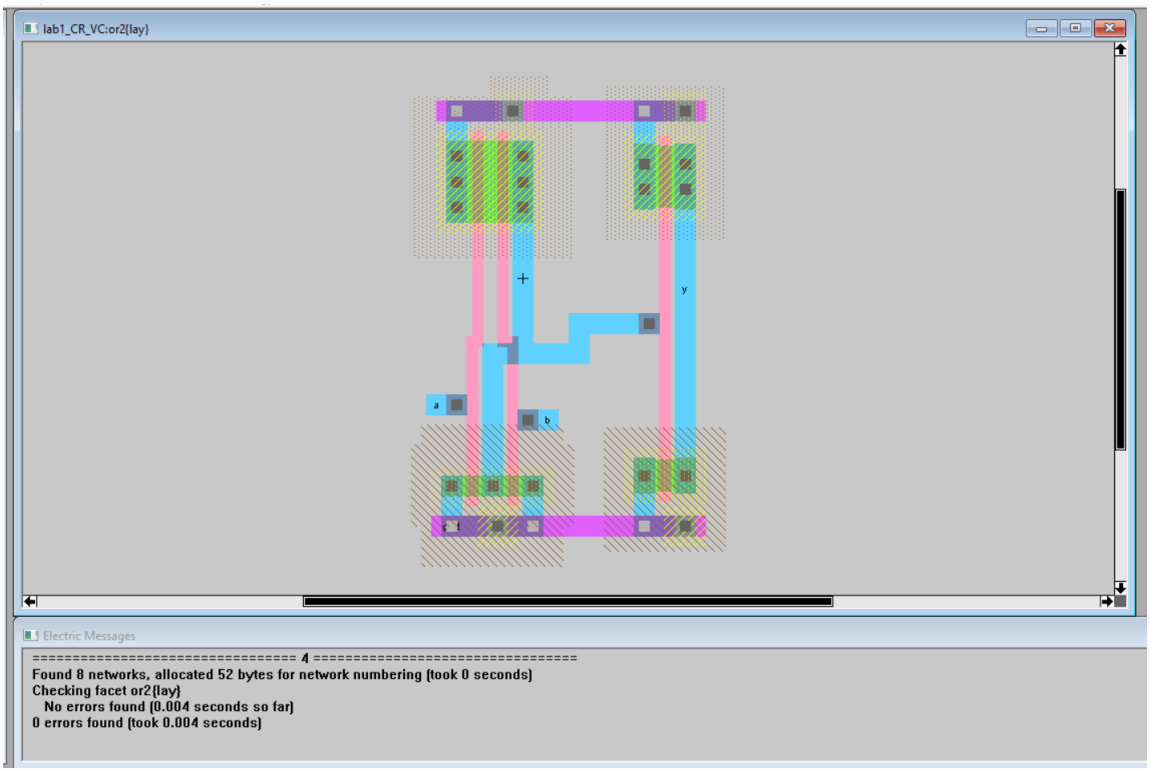
We see thar for the values A=1 or B=1, Y=1



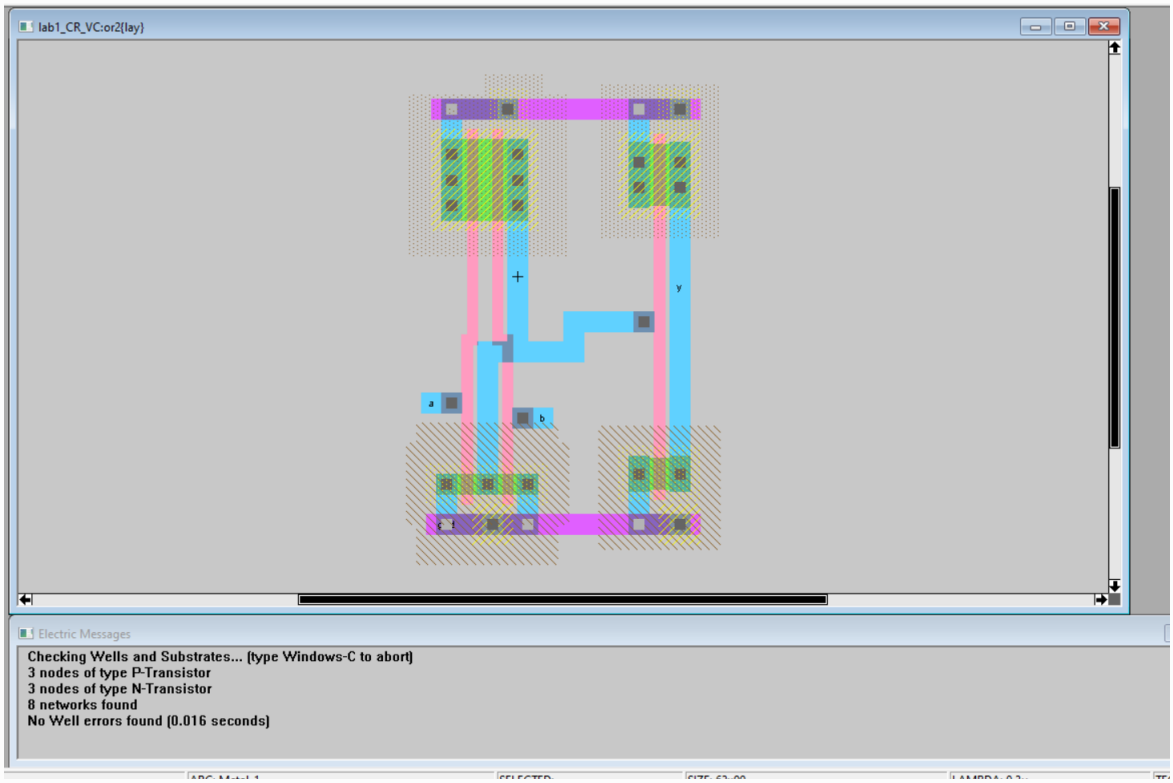
7.Layout Verification Or2

We see in the image the result of verification

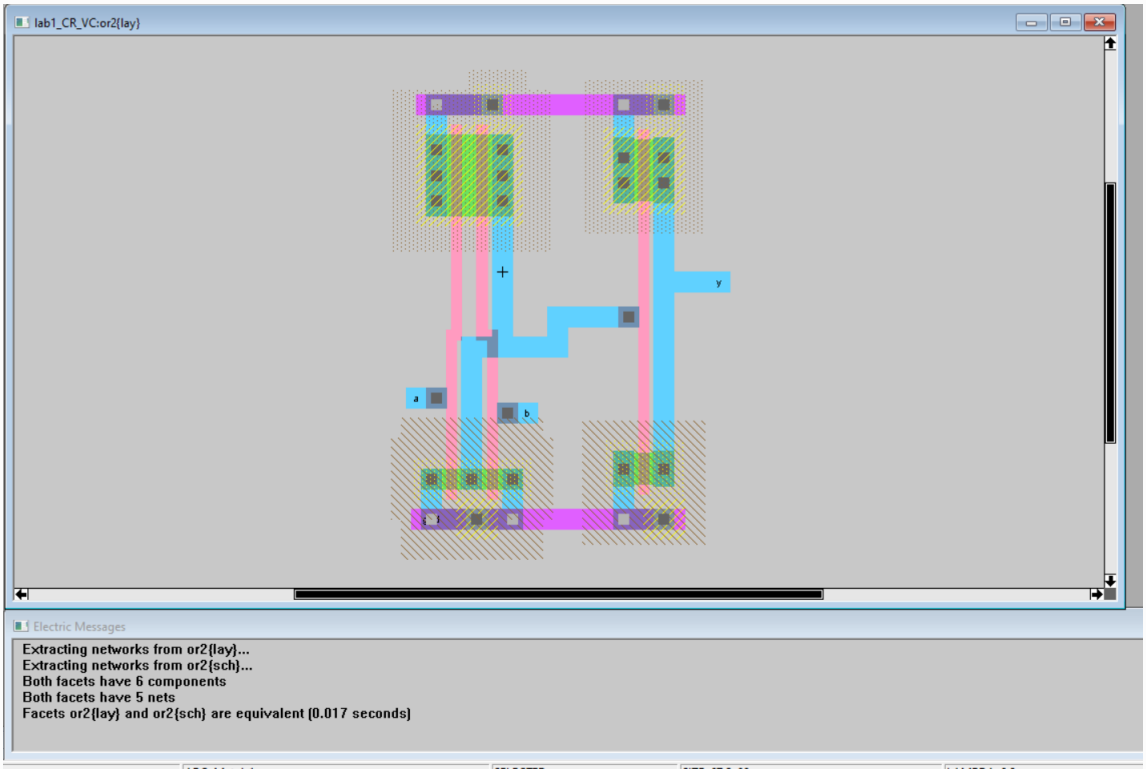
7.1 DRC



7.2 ERC


lab1_CR_VC:or2{lay}
y
a
b
Electric Messages
Checking Wells and Substrates... (type Windows-C to abort)
3 nodes of type P-Transistor
3 nodes of type N-Transistor
8 networks found
No Well errors found (0.016 seconds)

7.3 NCC


lab1_CR_VC:or2{lay}
y
a
b
Electric Messages
Extracting networks from or2{lay}...
Extracting networks from or2{sch}...
Both facets have 6 components
Both facets have 5 nets
Facets or2{lay} and or2{sch} are equivalent (0.017 seconds)