CS147 - Lab 16

Gate Level Modeling

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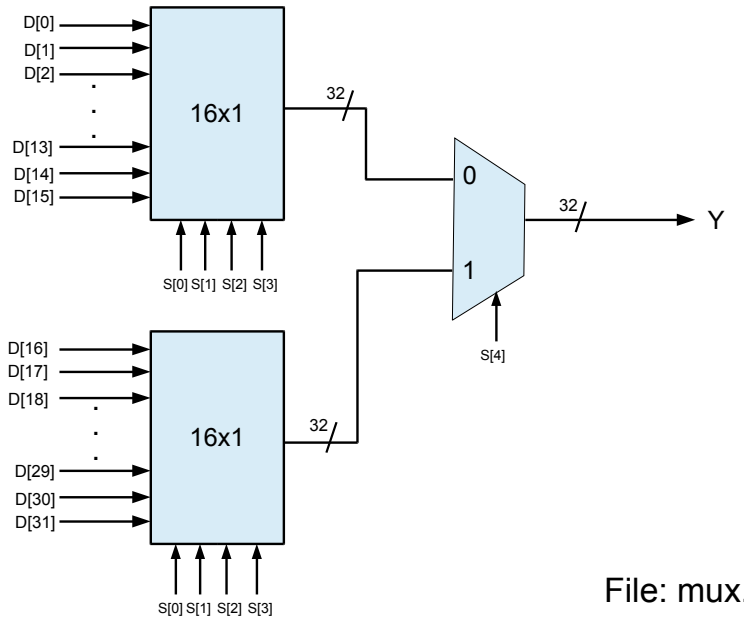
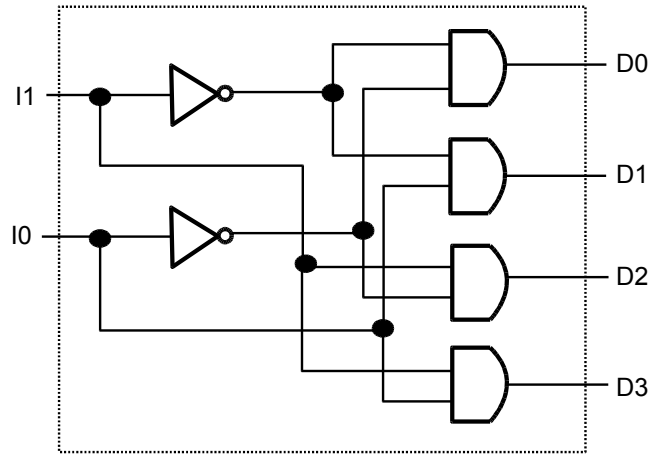
Implement 32-bit 32x1 MUX



File: mux.v

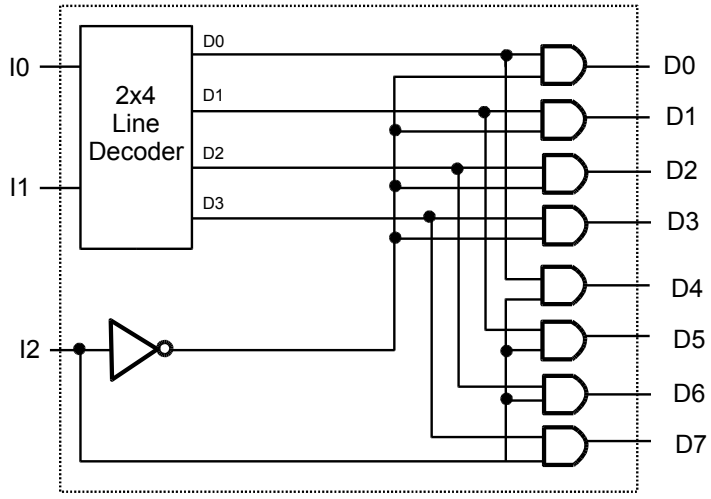
Implement 2-to-4 line decoder



File: logic.v

3

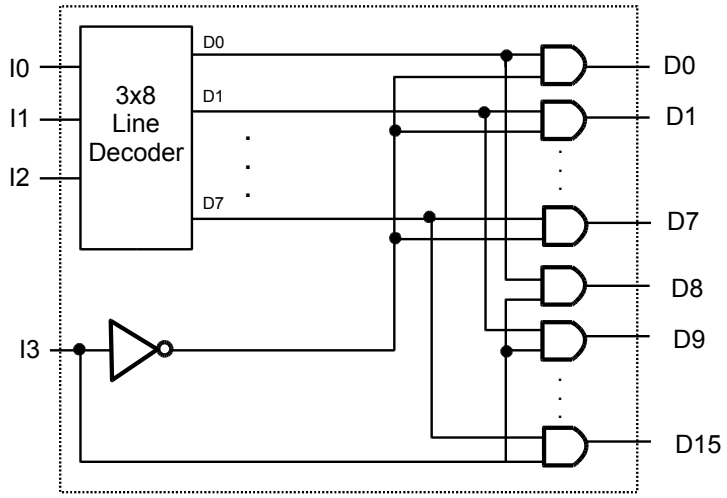
Implement 3-to-8 line decoder



File: logic.v

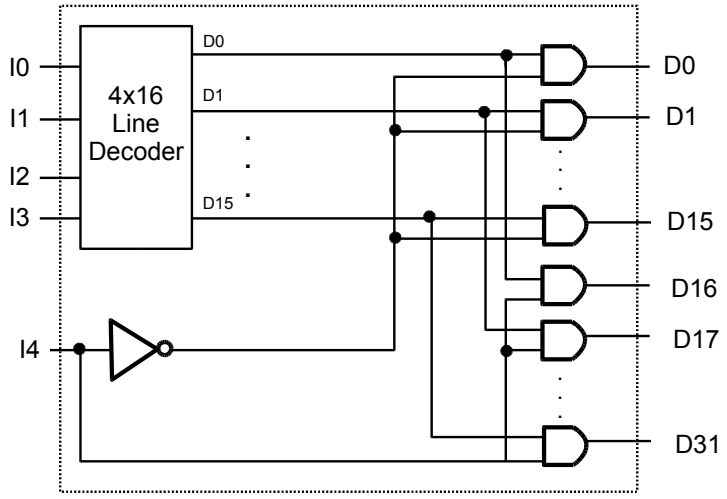
4

Implement 4-to-16 line decoder



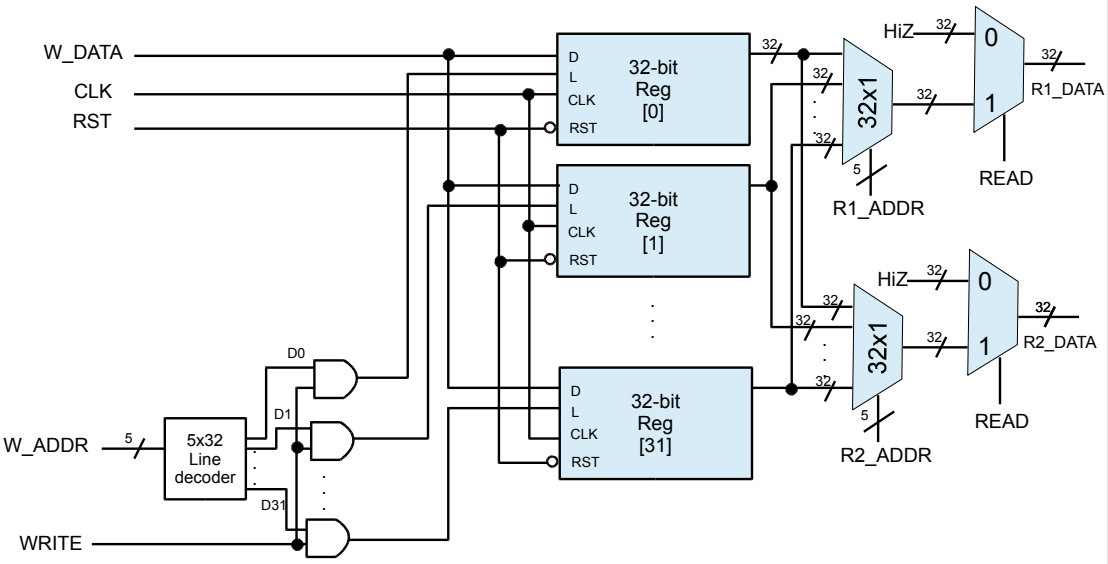
File: logic.v

Implement 5-to-32 line decoder



File: logic.v

Implement 32x32-bit Register File



File: register_file.v

CS147 - Lab 15

Gate Level Modeling

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