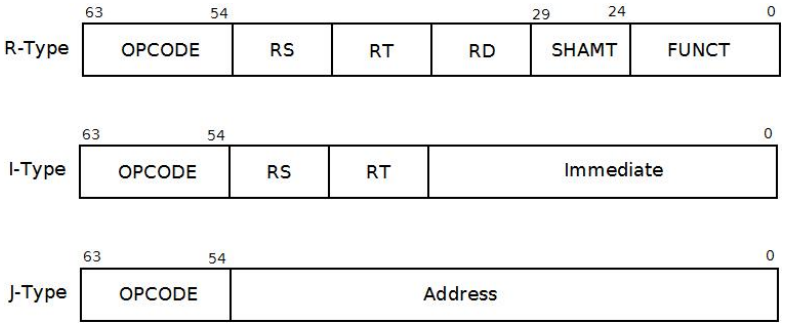
Class	CS147, Sec 01
Homework	I
Due Date	Sep 26, 2018 11:59 PM PST
Instructions	1. There are 5 questions with total 100 points. 2. Please create electronic document with your answer. 3. There is no need to include the question itself. However, you **MUST** include question number and sub-part index if any. Example: 5(b) 4. Please create a PDF document **hw1.pdf** and ***upload that in Canvas*** assignment page by the due date. 5. **Please re-check you submission for any logistic errors (empty file, corrupted PDF, and many more) and re-submit if needed. Once grading is started, any file with logistics errors will be given 0 point.** 6. **NO** handwritten (and scanned) document is accepted. You answer must be typed in (and computer drawn if diagram is asked) using word processing software. 7. **NO LATE SUBMISSION.** 8. **Please explain your answer clearly – just writing the final answer in a word or two is not sufficient in most of the cases.**

1. A computing system has a prøcessor which supports the following 3-types of instructions. The OpCøde field is encoded using 10 bit and shift amount in encoded with 6 bits. All R-type instructions have OpCode 0x0. This processor has a register file of total size 10KB. This computing system is connected to a word addressable memory of size of 32GB which has 32 bi-directional data pins (means read and write can be done one word at a time). This memory needs one clock cycle to complete any read/write request. A back to back read (or write) request can be done by the processor (i.e. issuing read operation to memory while it is processing data of previous read) but write after read must wait for a clock cycle. This memory is running with 1.2 GHz clock.
    a. How many registers are there in register file? [**2pts**]
    b. What is range of the immediate values that can be used with I-type arithmetic instructions assuming 2's complement form is used? [**3pts**]
    c. What is the maximum number of instructions supported by this processor? [**5pts**]
    d. How many address ports / pins are there in this memory device? [**3pts**]
    e. What is the clock period in 'ns' unit of the clock that drives this memory? [**2pts**]

f. If there are 4 million 64-bit data transaction in this system between processor and memory with 25% write operation mix with 0.1 probability of having a write operation immediately succeeding a read, what is the total time of this data transaction in 'ms' unit? [**15pts**]



2. A number system muNøte uses symbol Do, Re, Mi, Fa, So, La, Ti with equivalent decimal weight 0, 1, 2, 3, 4, 5, 6 respectively. In that case, answer the following.
    a. What is the decimal equivalent of TiLaSoDoReMiFa? [**5pts**]
    a. What is muNote equivalent of decimal number 1546781? [**5pts**]

3. Using Boolean algebra identity formulae prove LHS is equivalent to RHS.
    a. F(x,y,z) = x'z+xy = x'y'z+yz+xy [**5pts**]
    b. F(a,b,c,d) = a'b'c'd' + a'b'cd + a'b'cd' + ab'c'd' + ab'cd' + ab'cd = b'(c+d') [**5pts**]
    c. Prove (a) by constructing truth table of LHS and RHS. [**5pts**]
    d. Prove (b) by constructing truth table of LHS and RHS. [**5pts**]

4. Using K-Map technique simplify following functions and show all 'prime implicants' and 'Essential prime implicants' (use compact SOP form).
    a. f (A, B, C, D) = ∑ m (0, 5, 7, 8, 10, 12, 14, 15) [**5pts**]
    b. f(w, x, y, z) = ∑ m (1,3,4,7,11) + d(5, 12, 13, 14, 15) [**5pts**]

5. Design and implement a digital circuit which will detect a 4 bit number (input signals are w,x,y,z with 'w' representing MSB) which is less than 3 or greater than 12 or divisible by 3, i.e. if these conditions are met, the output (OUT) is 1, 0 otherwise. Implement the circuit with NAND only logic gate. You can assume multi-input NAND gate is available (i.e. 2 or more input pins as you need). You need to show the schematic diagram for the final logic circuit along with all the steps to derive the logic equation of the implemented circuit. [**30pts**]