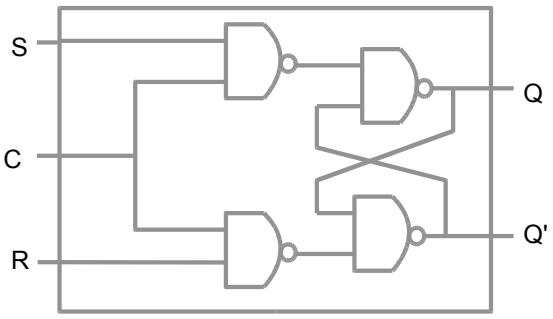
CS147 - Lab 15

Gate Level Modeling

Kaushik Patra
(kaushik.patra@sjsu.edu)

Implement 1-bit SR-Latch

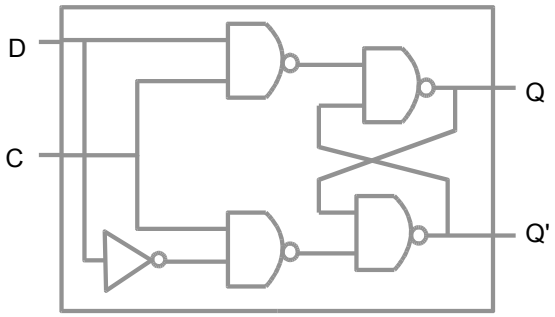


Truth Table

C	S	R	Q_T	Q_{T+1}	Q'_{T+1}
0	x	x	0	0	1
0	x	x	1	1	0
1	1	0	X	1	0
1	0	1	X	0	1
1	0	0	0	0	1
1	0	0	1	1	0
1	1	1	X	1	1

File: logic.v

Implement 1-bit D-latch

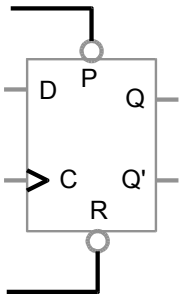


Truth Table

C	D	Q_T	Q_{T+1}	Q'_{T+1}
0	x	0	0	1
0	x	1	1	0
1	1	X	1	0
1	0	X	0	1

File: logic.v

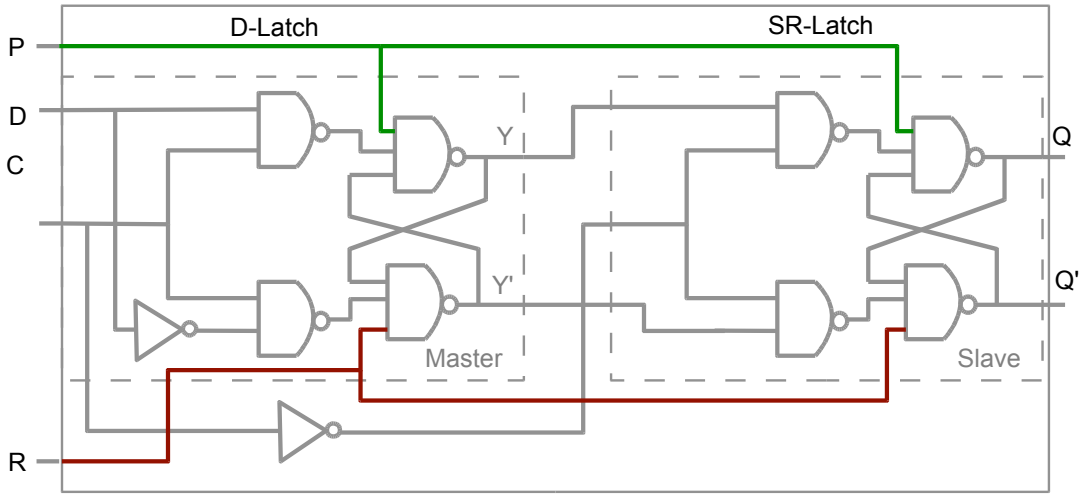
Implement 1-bit FlipFlop



C	D	P	R	Q_t	Q_{t+1}
x	x	0	0	x	?
x	x	0	1	x	1
x	x	1	0	x	0
0	x	1	1	0	0
0	x	1	1	1	1
1	0	1	1	x	0
1	1	1	1	x	1

File: logic.v

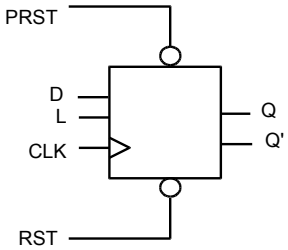
Implement 1-bit FlipFlop

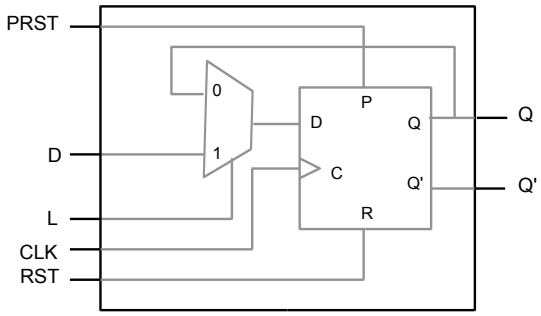


File: logic.v

5

Implement 1-bit Register

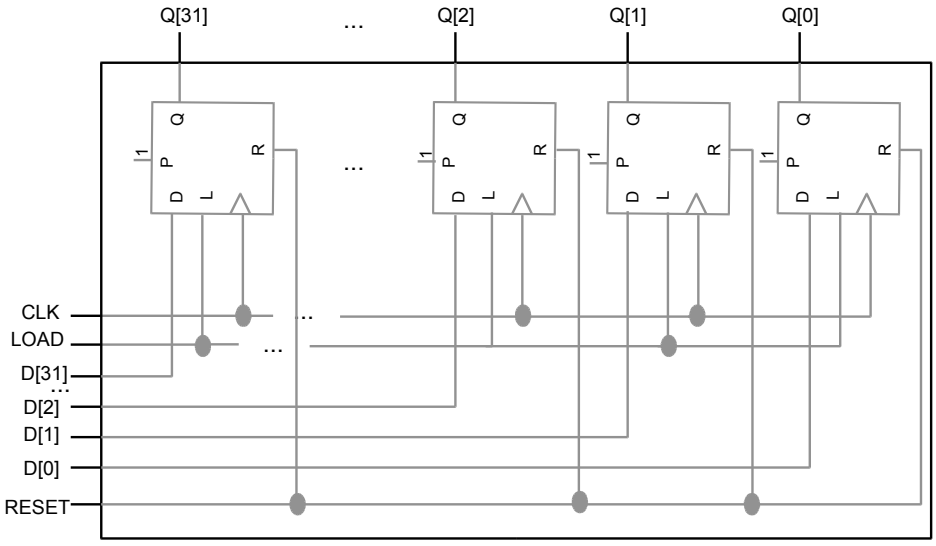




File: logic.v

6

Implement 32-bit Register



File: register_file.v

7

CS147 - Lab 15

Gate Level Modeling

Kaushik Patra
(kaushik.patra@sjsu.edu)

8