CS147 - Lab 12

Gate Level Modeling

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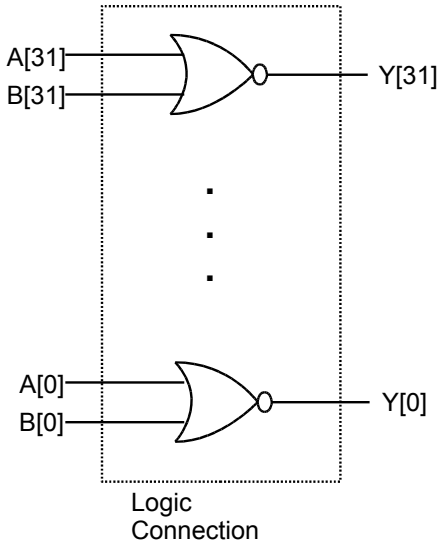
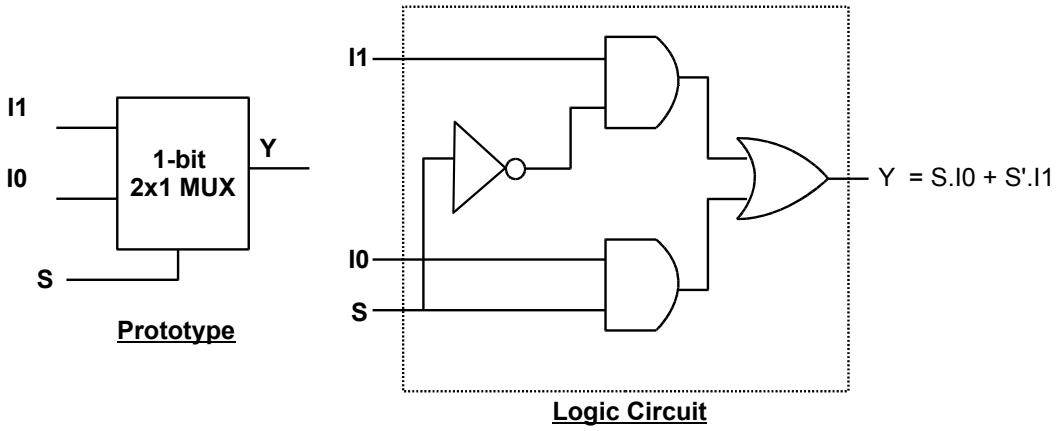
Repeating structure at gate level

```
module NOR32(Y,A,B);
//output
output [31:0] Y;
//input
input [31:0] A;
input [31:0] B;

genvar i;
generate
    for(i=0; i<32; i=i+1)
    begin : nor32_gen_loop
       nor nor_inst(Y[i], A[i], B[i]);
    end
endgenerate
endmodule
```



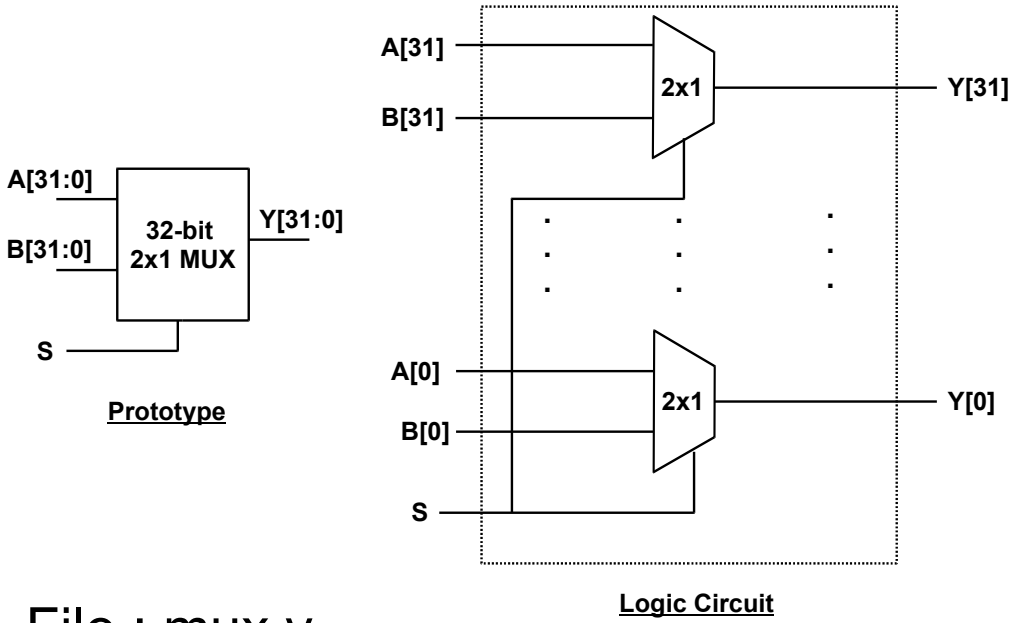
Implement a 1-bit 2x1 MUX



File : mux.v

3

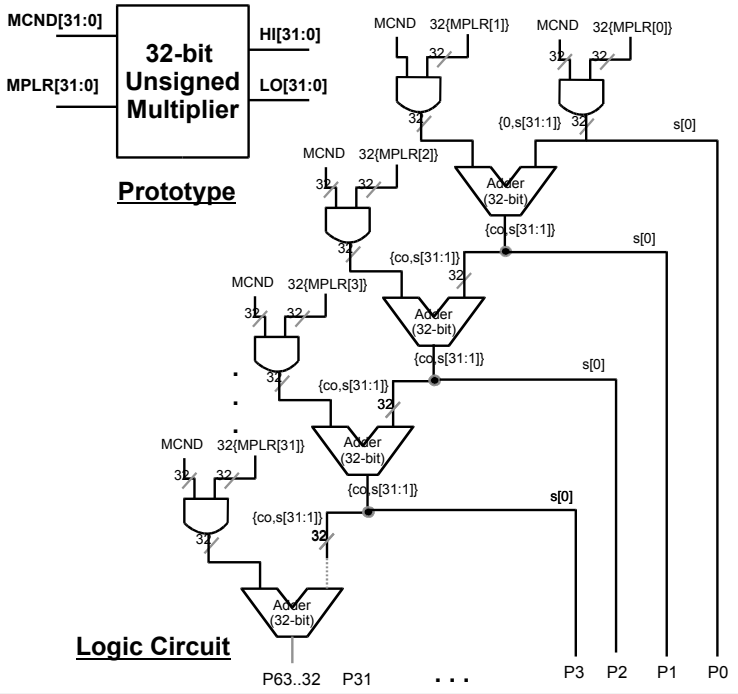
Implement a 32-bit 2x1 MUX



File : mux.v

4

Implement 32-bit Unsigned Multiplier



MCND – Multiplicand

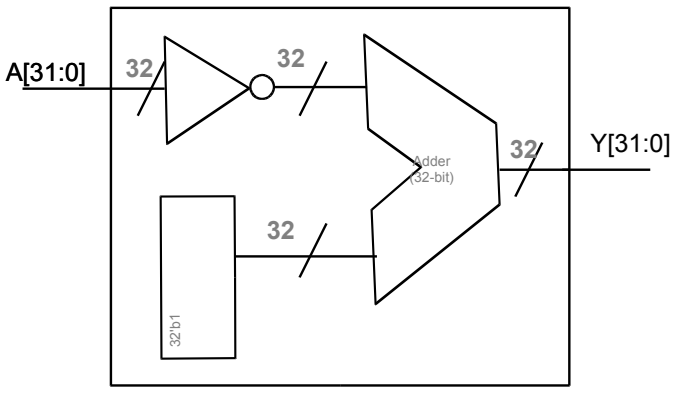
MPLR – Multiplier

PROD - Product

File : mult.v

5

Implement 2's complement

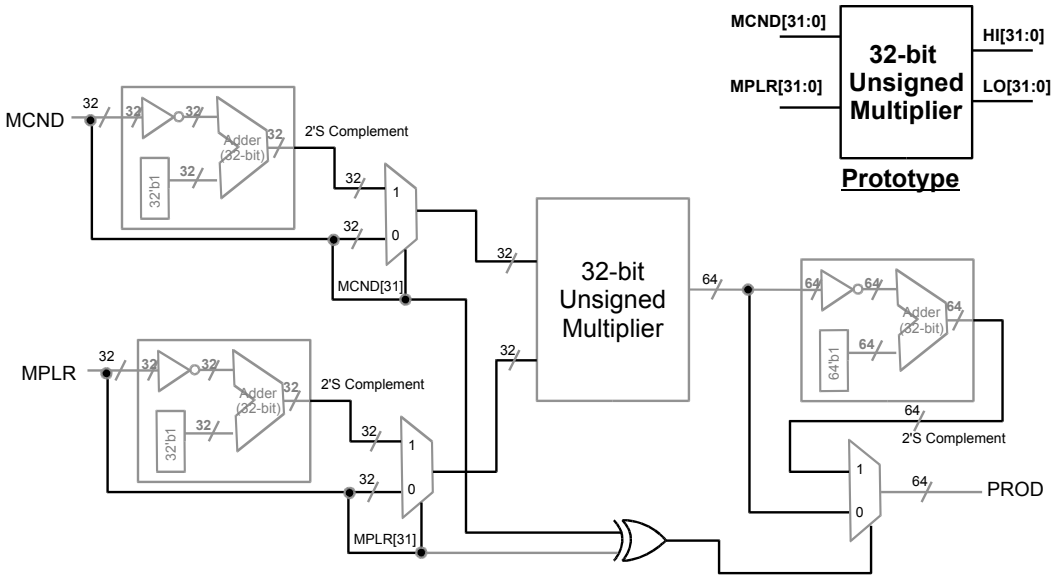


Logic Circuit

File : logic.v

6

Implement Signed Multiplication Circuit



File : mult.v

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