CS147 - Lab 14

Gate Level Modeling

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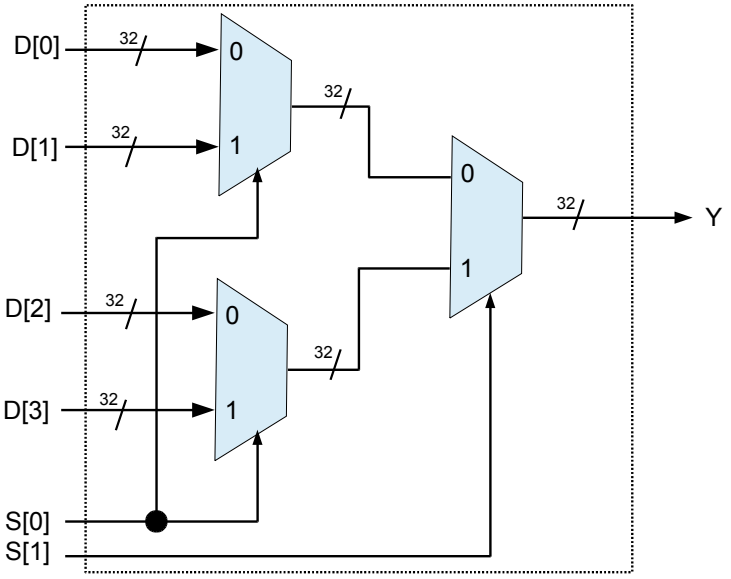
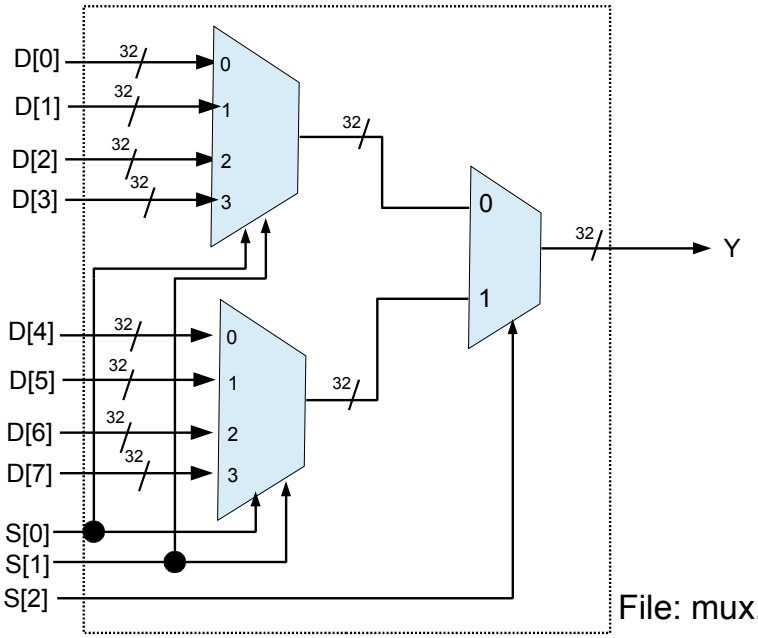
Implement 32-bit 4x1 MUX



File: mux.v

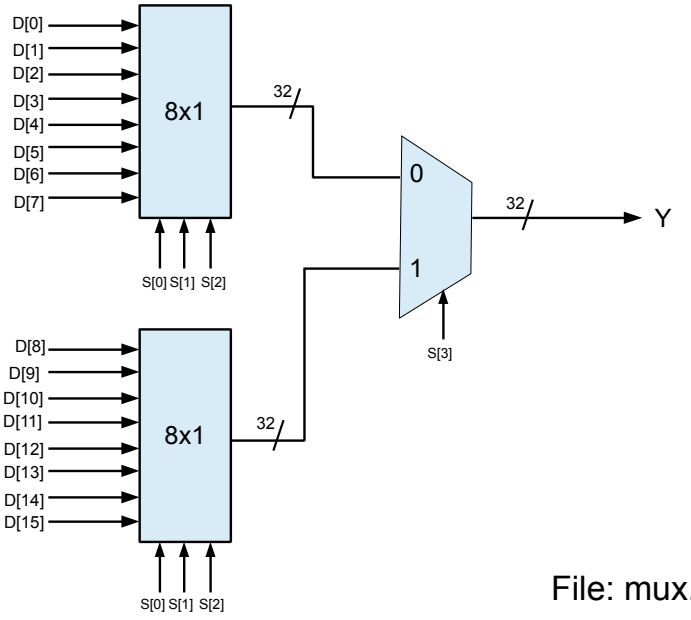
Implement 32-bit 8x1 MUX



File: mux.v

3

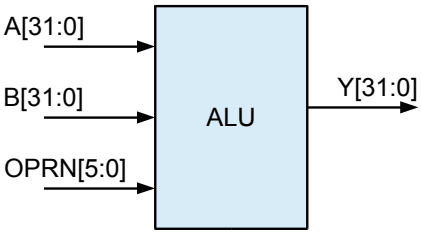
Implement 32-bit 16x1 MUX



File: mux.v

4

Implement 32-bit ALU



TYPE	OPRN CODE
add	xx0001
sub	xx0010
mul	xx0011
Shift R	xx0100
Shift L	xx0101
and	xx0110
or	xx0111
nor	xx1000
slt	xx1001

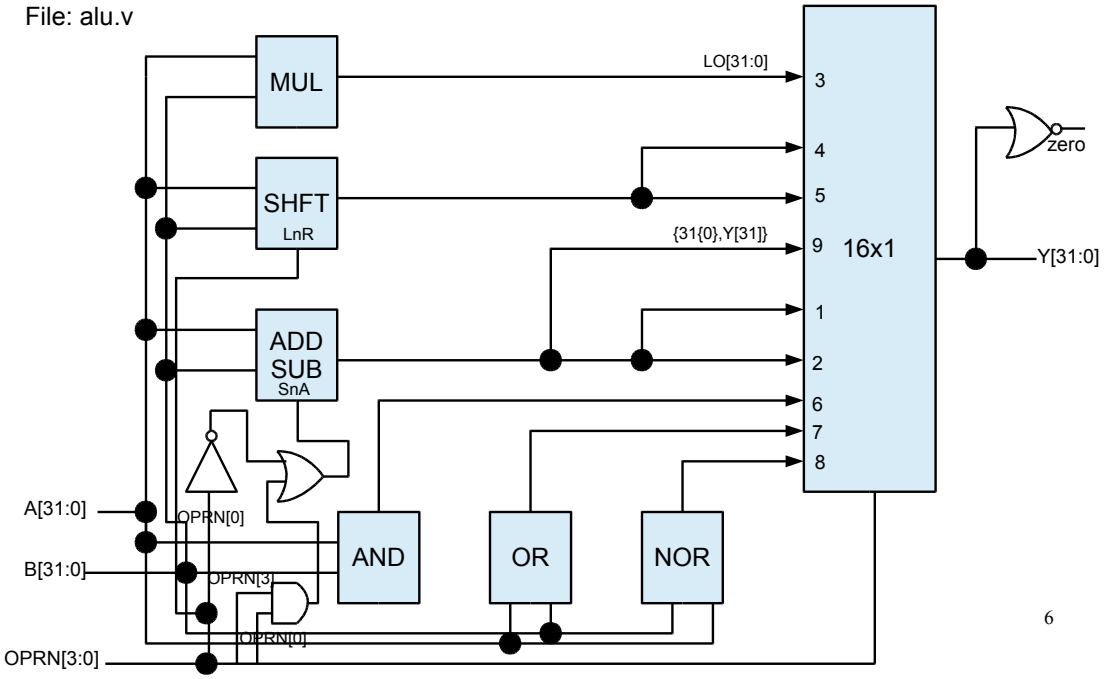
Control Signals:

- For Adder-Subtractor & SLT → SnA : OPRN[0]' + OPRN[3].OPRN[0]
- For shifter → LnR : OPRN[0]

5

Implement 32-bit ALU

File: alu.v



6

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