CS147 - Lab 11

Gate Level Modeling

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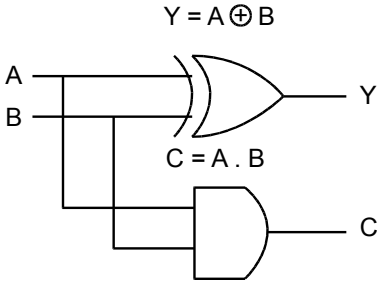
Components of Gate Level Model

- At gate level modeling, circuits are described in terms of logic gates.
- Verilog supports the following gates by default.
  - and / nand
  - or / nor
  - xor / xnor
  - buf / not
- Implicit connection list in instantiation, where OUT, IN1 and IN2 are wires.
  - and and_inst_1(OUT, IN1, IN2);
  - not not_inst_1(OUT,IN1);

Example – Half adder



half_adder.v

```
module half_adder(Y,C,A,B);
input A, B;
output Y,C;

xor inst1(Y, A, B);
and inst2(C, A, B);

endmodule
```

half_adder_tb.v

```
`timescale 1ns/1ps

module half_adder_tb;
reg A, B;
wire Y,C;

half_adder hs_inst_1(.Y(Y), .C(C),
                     .A(A), .B(B));

initial
begin
A=0; B=0;
#5 A=1; B=0;
#5 A=0; B=1;
#5 A=1; B=1;
End

endmodule
```

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Project III – Let's start it !!!

- Create a new project project_03 in ModelSim.
- Add all the existing code from project 2.
  - We'll replace part of the behavioral model with gate level model.
- Add new source files for half adder.
  - half_adder.v
  - half_adder_tb.v
- Compile the project and simulate half_adder_tb.
  - Observe the waveform and check if the behavior is correct.

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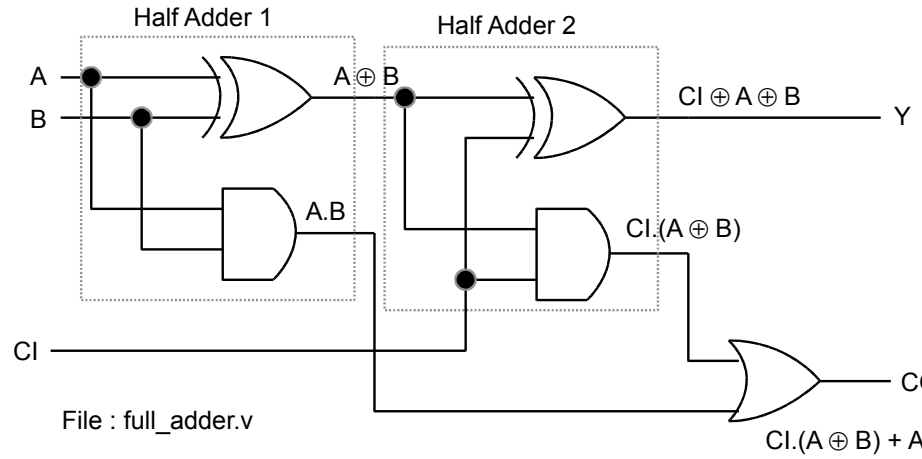
Implement a Full Adder

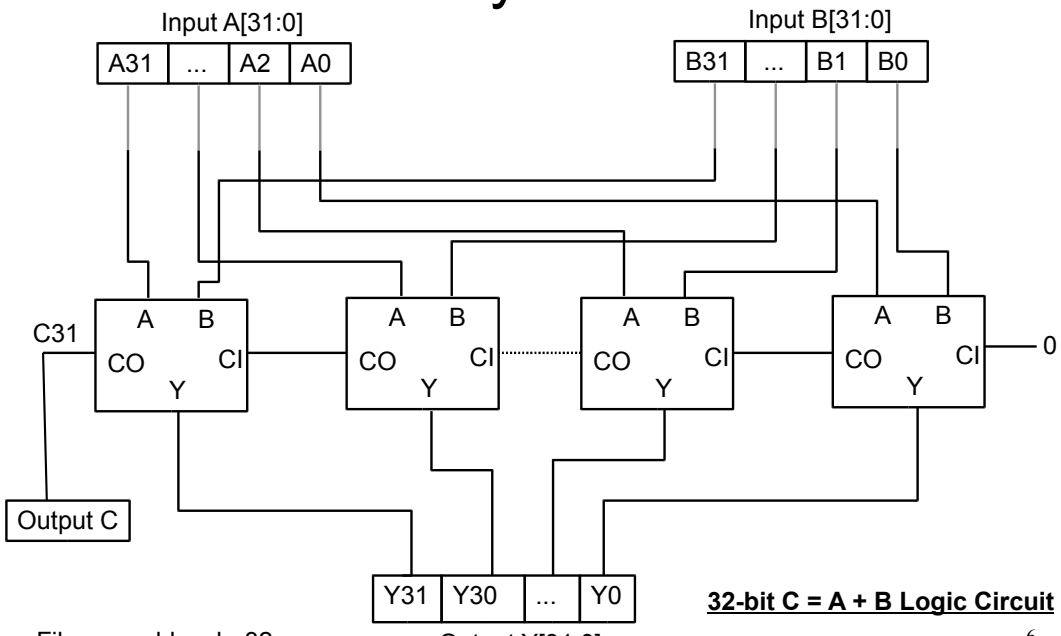
$Y = CI \oplus (A \oplus B)$

$CO = CI.(A \oplus B) + A.B$



File : full_adder.v

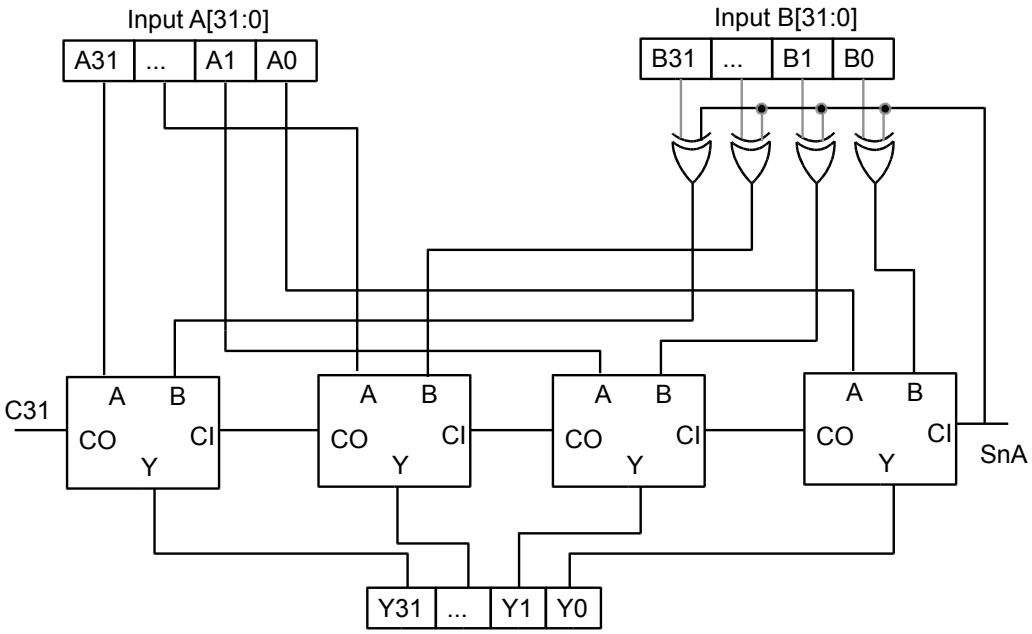
Implement a 32-bit Binary Ripple Carry Adder



32-bit C = A + B Logic Circuit

File : rc_add_sub_32.v

Extend the full adder to subtractor



File : rc_add_sub_32.v

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