CS147 - Lab 17

Gate Level Modeling

Kaushik Patra
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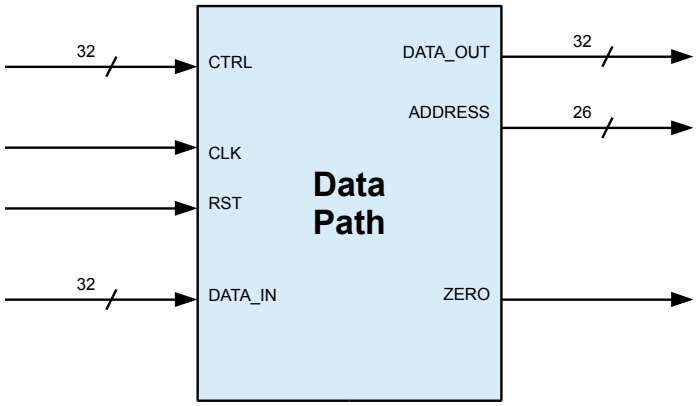
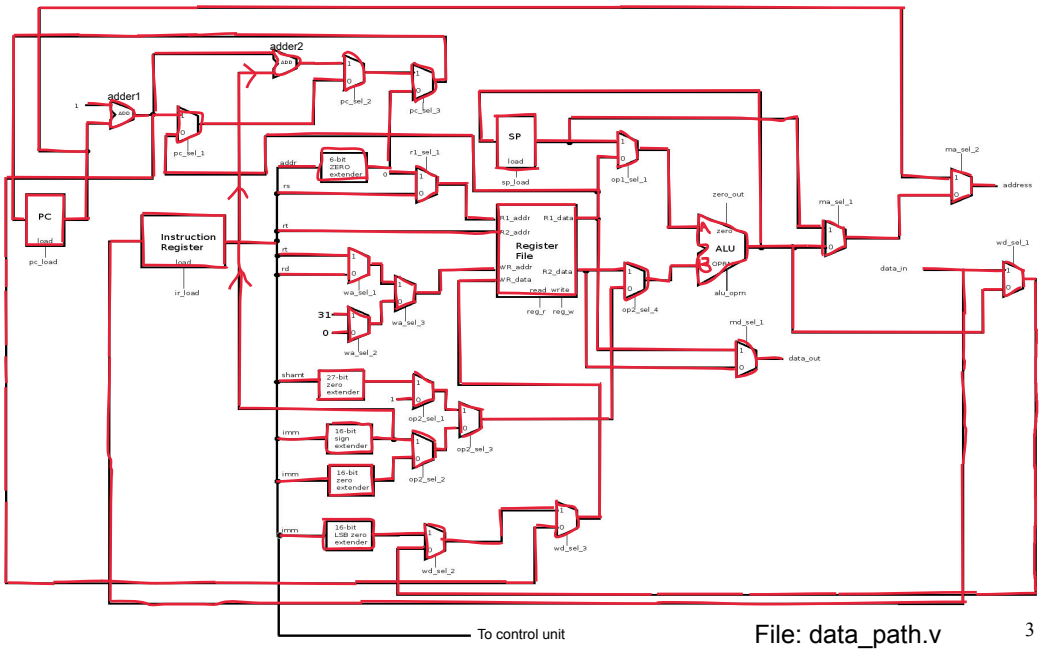
Implement Data Path



(*) Please download the latest source files

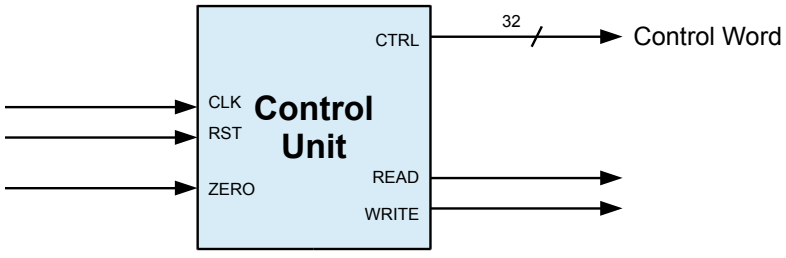
File: data_path.v

Implement Data Path



File: data_path.v

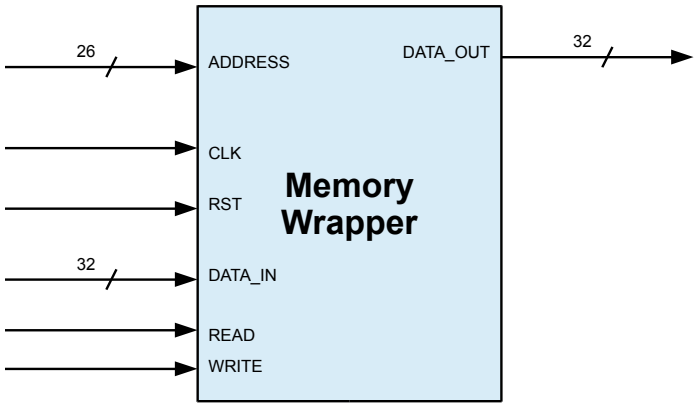
Implement Control Unit



(*) Behavioral Model

File: control_unit.v

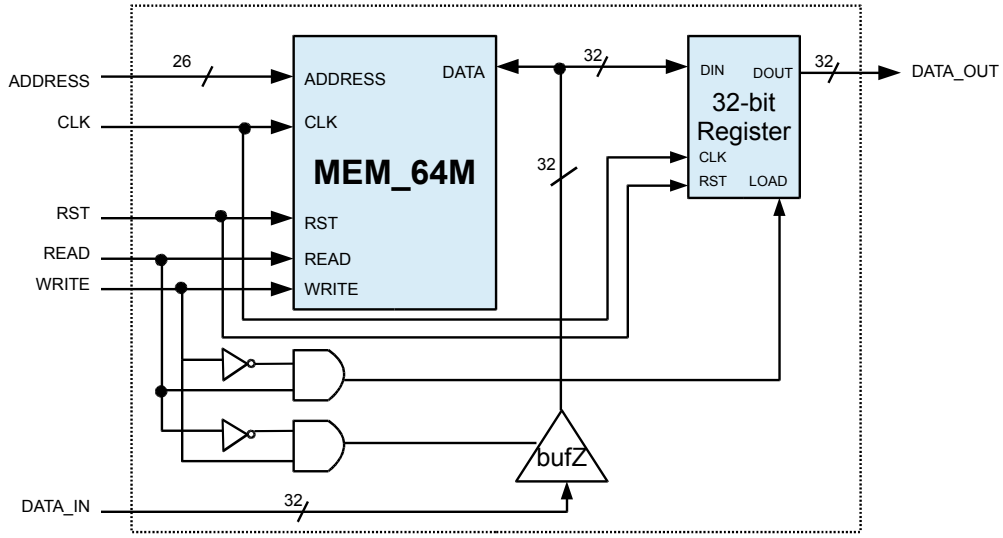
Memory Wrapper Implementation



(*) Please download the latest source files

File: memory.v

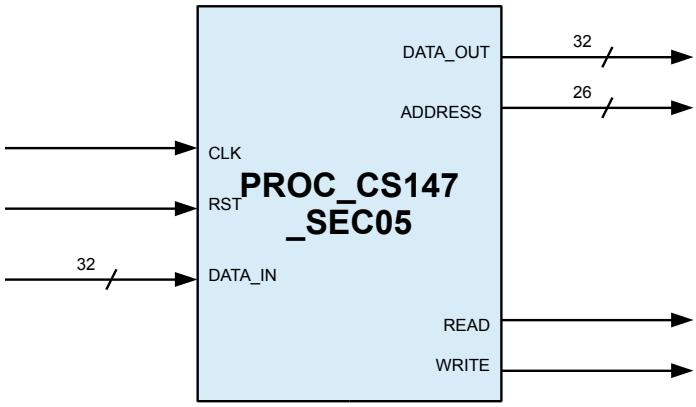
Memory Wrapper Implementation



(*) Please download the latest source files

File: memory.v

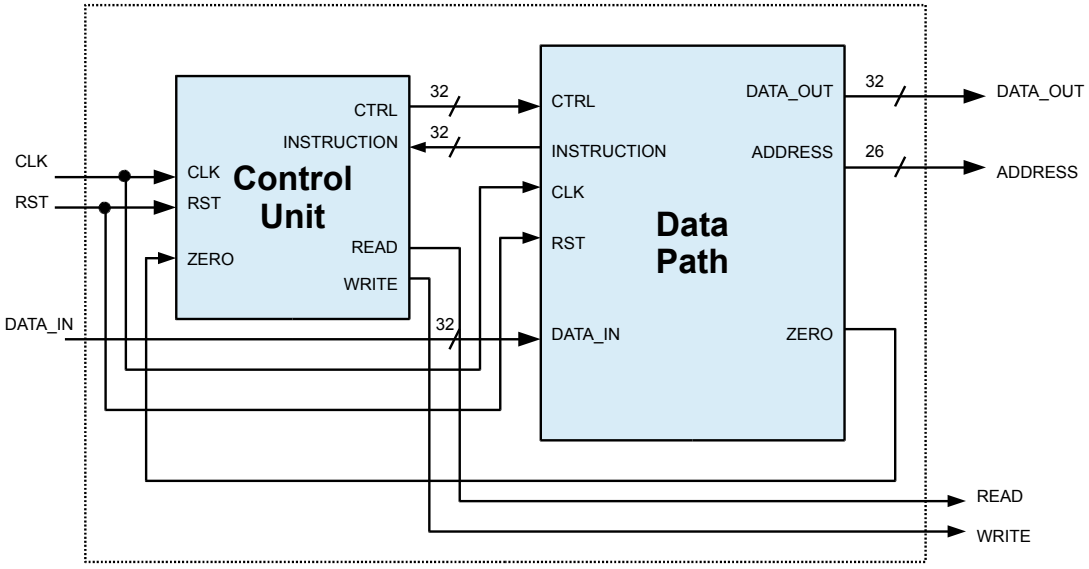
Processor Implementation



(*) Please download the latest source files

File: memory.v

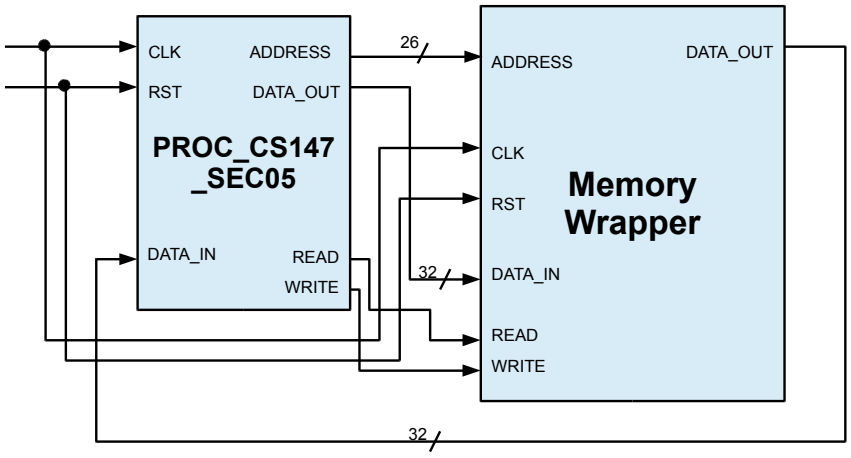
Processor Implementation



(*) Please download the latest source files

File: processor.v

System Implementation



(*) Please download the latest source files

File: memory.v

9

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10