CS147 - Lab 03

Data Flow Modeling I

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Operators

- Three types of operators
  - Unary : a = ~b; // a is not b
  - Binary : a = b && c; // logical and
  - Ternary : a = b ? c : d // if (b) a =c; else a=d;

Number Specification

- **Sized Number**
  - <size>'<base format><number>
    - 'h': Hexadecimal
    - 'b': Binary
    - 'o': Octal
    - 'd': Decimal
  - 6'h10 (10_{16}), 6'o10(10_{8}), 6'b10(10_{2}), 6'd10(10_{10})
- **Unsized numbers are all 32 bit**
  - 23456 // 32-bit decimal
  - 'hc3 // 32-bit hex
  - 'o21 // 32-bit octal

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Value Types

- Four type of values
  - 0 : Logic zero, false condition
  - 1 : Logic one, true condition
  - X : Unknown value
  - Z : High impedance, floating state

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Data Types

- **Nets**
  - Represents connection between hardware element just like in real circuit.
  - Declaration
    - wire a, d_out, b; // 1-bit
- **Registers**
  - Represents unsigned data storage elements in simulator
  - Not same as hardware registers.
  - Declaration
    - reg a, b, c; // 1-bit

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Data Types

- **Vectors**
  - Nets or registers can be declared as vectors or multi-bit sized net / register.
  - Declaration
    - wire [7:0] bus; // 8-bit bus
    - reg [31:0] dataA, dataB; // 2 32-bit buses.
- **Integer and real**
  - Used for manipulating signed quantities.
  - e.g. integer counter;
  - e.g. real delta = 4e10;

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Data Types

- **Arrays (single dimension only)**
  - Allowed for reg, integer and vector registers.
  - e.g.
    - integer counter [0:7] // array of 8 count var
    - reg [7:0] mem [0:2048]; // array of 2K 8-bit reg
  - To access
    - counter[5]; // 6th value in the array
    - reg[511]; // 512th 8-bit register

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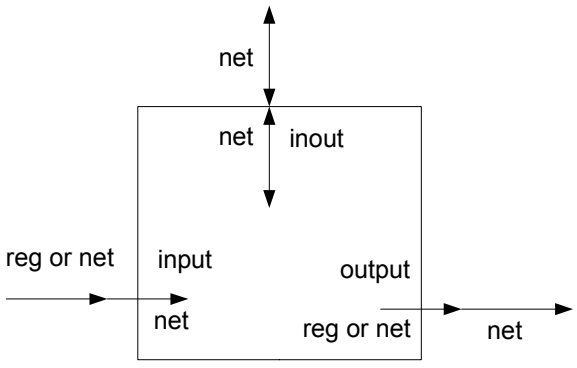
Port Connection Rule



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