Name: Student ID:

Class	CS147, Sec 01
Midterm	Fall 2018
Due Date	Oct 17, 2018 7:30 PM – 8:45 PM PST
Notes	1. Tear off Supplemental pages if any. 2. Closed book / note/ computer / internet exam 3. Hybrid exam (both paper/pencil + online) - you may use calculator 4. Write your name and student ID at header section on **EVERY PAGE** 5. **Explanation** of answer is **required if applied**. 6. Q1- 6 are main questions to answer. 7. Q7 is extra credit question 8. Use back of the pages if needed to answer questions.

Don't Open Until Instructed

1. A computing system is connected to a byte addressable memory of size of 32GB which has 32 bi-directional data pins (means read and write can be done one word at a time). This memory needs one clock cycle to complete any read/write request. A back to back read (or write) request can be done by the processor (i.e. issuing read operation to memory while it is processing data of previous read) but write after read must wait for a clock cycle. This memory is running with 2.5 GHz clock. If there are 16 million 32-bit data transaction in this system between processor and memory with 25% write operation mix with 0.1 probability of having a write operation immediately succeeding a read, what is the total time of this data transaction in 'ms' unit? [**3pts**]

Ans:

There is total 16 million operations with 32-bit data transactions.

- Number of read operations = 16*75% million = 12 million
- Number of write operations = 16*25% million = 4 million

Since each read operation takes 1 clock cycle, all read operations will take 12 million cycles.

Similarly, since each write operation takes 1 clock cycle, all write operations will take 4 million cycles.

However, out of 4 million 32-bit write operations there is 0.1 probability of having a write operation succeeding a read operation. There must be (0.1*4 million) = 0.4 million wait cycle for the preceding read data to be consumed by processor.

Therefore, this specific data transaction needs (4+12+0.4) million clock cycles = 16.4 million cycles.

This memory is running on 2.5GHz clock. Each clock cycle is 0.4ns. So, this operation will take ($16.4 * 10^6 * 0.4 * 10^{-9}$) sec = 6.56ms.

2. A number system muNote uses symbol Do, Re, Mi, Fa, So, La, Ti with equivalent decimal weight 0, 1, 2, 3, 4, 5, 6 respectively. What is the decimal equivalent of SoMiDoReTiLaFa? [**2pts**]

Ans:

Since 'muNote' number system has 7 symbols its base is 7. Each symbol has values Do=0, Re=1, Mi=2, Fa=3, So=4, La=5, Ti=6

Hence decimal representation of muNote value SoMiDoReTiLaFa is computed as following.

$(So * 7^6) + (Mi * 7^5) + (Do * 7^4) + (Re * 7^3) + (Ti * 7^2) + (La * 7^1) + (Fa * 7^0)$

$= (4 * 7^6) + (2 * 7^5) + (0 * 7^4) + (1 * 7^3) + (6 * 7^2) + (5 * 7^1) + (3 * 7^0)$

$= (4 * 117649) + (2 * 16807) + (0 * 2401) + (1 * 343) + (6 * 49) + (5 * 7) + (3 * 1)$

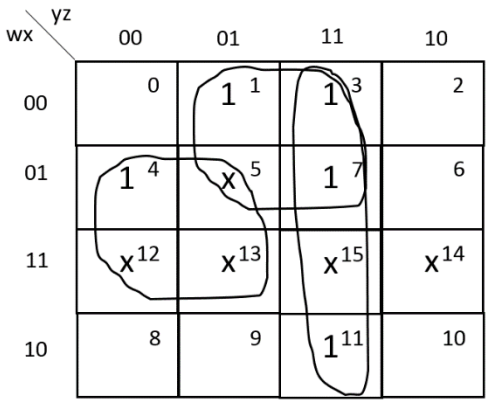
$= 470596 + 33614 + 0 + 343 + 294 + 35 + 3$

$= 504885$

Name: Student ID:

3. Using K-Map technique show all 'Essential prime implicants' (use compact SOP form) f(w, x, y, z) = ∑ m (1,3,4,7,11) + d(5, 12, 13, 14, 15). [**2pts**]

Ans:



Essential Prime Implicants are as following.

- ∑ m (1,3,5,7)
- ∑ m (4,5,12,13)
- ∑ m (3,7,11,15)

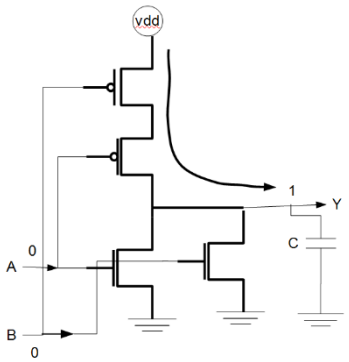
4. What value combination(s) of input operands can cause overflow in a ripple carry adder/subtraction logic circuit? Assume input operands are represented in 2's compliment format. Choose (mark 'x') from the list below. [**1pts**]

   - ☐ Any combination
   - ☐ Both positive
   - ☐ Both negative
   - ☐ One positive and another negative

5. What is the minimum size (in byte units) of total storage (register storage) needed in a 32-bit division logic circuit data path? [**1pts**]

   - ☐ 12
   - ☐ 20
   - ☐ 0
   - ☐ None of these

6. A CMOS transistor level logic schematic looks like following. What is this logic gate? [**1pts**]



   - ☐ AND
   - ☐ OR
   - ☐ NAND
   - ☐ NOR
   - ☐ INVERTER

Extra Credit Question

7. Design a one bit full adder using **one** 3x8 line decoder and **two** four input OR gates. Input of this full adders are A, B and Cin (carry in). There are two outputs S (sum) and Cout (carry out). Clearly explain your work and show schematic of your design. [**5pts**]

Ans:

Truth table for full adder is as following (fill out the table)

	Cin	A	B	S	Cout
m0	0	0	0	0	0
m1	0	0	1	1	0
m2	0	1	0	1	0
m3	0	1	1	0	1
m4	1	0	0	1	0
m5	1	0	1	0	1
m6	1	1	0	0	1
m7	1	1	1	1	1

- Compact SOP form of S = ∑ m (1,2,4,7)
- Compact SOP form of Cout = ∑ m (3,5,6,7)

A 3x8 line decoder can generate minterms for given Boolean variable as inputs. We have to use two 4 input OR gates connecting to right minterm output from decoder to implement this full adder circuit.