Class	CS147, Sec 01
Homework	III
Due Date	Dec 08, 2018 11:59 PM PST
Instructions	1. There are 7 questions with total 100 points. 2. Please create electronic document with your answer. 3. There is no need to include the question itself. However, you **MUST** include question number and sub-part index if any. Example: 5(b) 4. Please create a PDF document **hw3.pdf** and ***upload that in Canvas*** assignment page by the due date. 5. **Please re-check you submission for any logistic errors (empty file, corrupted PDF, and many more) and re-submit if needed. Once grading is started, any file with logistics errors will be given 0 point.** 6. **NO** handwritten (and scanned) document is accepted. You answer must be typed in (and computer drawn if diagram is asked) using word processing software. 7. **NO LATE SUBMISSION.** 8. **Please explain your answer clearly – just writing the final answer in a word or two is not sufficient in most of the cases.**

1. Assume a word addressable memory and a register file on a computing system contains the following data at an instance of time during running of a program. What is the operand value retrieved if : [**5*5pts = 25pts**]

   a. Next instruction is direct addressing with memory address 0x10003010?
   b. Next instruction is indirect addressing with memory address 0x10003010?
   c. Next instruction is register addressing with register address 7?
   d. Next instruction is register indirect addressing with register address 7?
   e. Next instruction is displacement addressing with register address 20 and offset address as 0xF6 (8-bit 2's complement format for offset)?

MEM ADDR	CONTENT		REG	CONTENT	REG	CONTENT
0x1000301B	0x00000005		R00	0x00000000	R16	0x90003024
0x1000301A	0x00000006		R01	0x00000001	R17	0x90003025
0x10003019	0x00000007		R02	0x00000002	R18	0x90003026
0x10003018	0x00000008		R03	0x00000003	R19	0x90003027
0x10003017	0x00000009		R04	0x00000004	R20	0x10003018
0x10003016	0x00000010		R05	0x00000005	R21	0x10003027
0x10003015	0x00000011		R06	0x00000006	R22	0x10003028
0x10003014	0x00000012		R07	0x10003013	R23	0x10003029
0x10003013	0x00000010		R08	0x90003024	R24	0x10003030
0x10003012	0x00000011		R09	0x00000006	R25	0x10003031

0x10003011	0x00000012	R10	0x00000007	R26	0x10003032
0x10003010	0x10003014	R11	0x00000008	R27	0x10003033
0x1000300F	0x10003015	R12	0x00000009	R28	0x10003034
0x1000300E	0x00000001	R13	0x00000010	R29	0x10003035
0x1000300D	0x00000002	R14	0x00000011	R30	0x10003036
0x1000300C	0x00000003	R15	0x00000012	R31	0x10003037

2. A NUMA computer cluster has 200 computing nodes with each node associated with 128GB RAM. Average local memory access time is 50ns and average remote memory access time is 180ns. Assume a program is running on one node in this cluster. It is consuming total of 230GB with local memory occupancy as 100GB. If there are 1 million (**1,000,000**) memory access in this program with probability of accessing a remote memory location as 0.25 what is the total time the program is busy accessing memory in millisecond (ms) unit ? [**10pts**]

3. A computing system with traditional disk (rotating hard disk) transfer data to main memory at minimum unit of 2KB of block of data (i.e. it has to adjust read/write head per 2KB block data access). Its average access time is 1ms. It has transfer rate of 100Mbps (mega-bits per second). Another computing system has solid state disk (with random access technique) transfer data to main memory at minimum unit of 1KB of block of data. It has access time of 50us per block of data transfer and refresh time of 250us. Both the system runs Linux operating system with initial size of 2MB to be loaded into main memory during boot time. Which system will boot faster and how much (ratio their performance)? [**10pts**]

4. Your Project II processor is modified to hook into a cache memory system (i.e. states are introduced to handle cache miss) and running on 1GHz clock. This system is connected to a memory system with separate instruction and data cache. Both these caches has access time 1ns and cache miss penalty of 150ns. However, miss rate for instruction cache is 5% and miss rate for data cache is 10%. If the following piece of code is executed in that processor and the 'loop' block (starting from 'loop' label to last 'jmp loop') has been executed 10,000 times what is the total execution time of this program so far in 'us' (microsecond) unit? [**10pts**]

```
       addi r2, r2, 0x0001;
       lui r0, 0x0100;
       sw r1, r0, 0x0000;
 loop: addi r0, r0, 0x0001;
       sw r2, r0, 0x0000;
       addi r3, r2, 0x0000;
       add r2, r2, r1;
       addi r1, r3, 0x0000;
       j loop;
```

5. A 32-bit computer system supports 4GB byte addressable memory. It's processor has cache with block size of 1KB. Both the control and tag bits per cache line is 8 bits each. Assume that cache line is fully mapped from bits of the address A excluding block bits and tag bits in the address.
   a. How much data is cached within this cache memory in MB unit? [**10pts**]
   b. Also determine actual size of the cache memory in KB unit. [**10pts**]
   c. Whole memory is divided into how many blocks? [**5pts**]

6. Now, assume that the system in the #5 uses 8-way associative cache but cache same amount of information.
   a. Determine TAG, CACHE LINE INDEX and BLOCK INDEX of the address 0x30AB23F2. [**5pts**]
   b. What is the actual size of the cache memory in this case in KB unit? [**5pts**]

7. A 32-bit computer system uses virtual memory with 4K page size. It also uses a cache same as #6. For any memory access, both TLB and cache access time is 1ns each. TLB miss rate is 25% with 20us penalty. Cache miss rate is 10% with 150us penalty. Page fault rate is 0.01% with page service (bring back page from disk to memory) 1s.
   a. How much time would be spent for one million (1,000,000) memory access in second unit? [**5pts**]
   b. Determine TAG, CACHE LINE INDEX and BLOCK INDEX for a virtual address 0x4CD67821 with TLB entry for 0x4CD67 is 0x28701, if this system uses same cache as in #6. [**5pts**]