

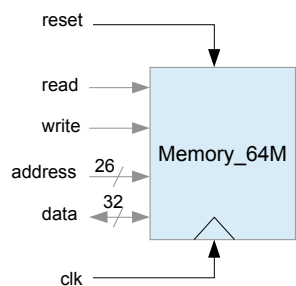
CS147 - Lab 05

Memory Modeling

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Memory Modeling



- 64MB memory
- Reset on -ve edge of reset signal.
- Synchronous with +ve edge of clock.
- InOut style data 32-bit port .
- Read operation at read=1 and write=0
- Write operation at read=0 and write=1
- Data port 'data' goes to hiZ state for any other combination of read/write signal.

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Memory Modeling

This defines a variable
Inside a module whose
Value can be modified
In a upper level module
(which is instantiating
This module).

```
module MEMORY_64MB(DATA, READ, WRITE, ADDR, CLK, RST);
// Parameter for the memory initialization file name
parameter mem_init_file = "mem_content_01.dat";
// input ports
input READ, WRITE, CLK, RST;
input [`ADDRESS_INDEX_LIMIT:0] ADDR;
// inout ports
inout [`DATA_INDEX_LIMIT:0] DATA;
. . .
endmodule
```

List of Ports

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Memory Modeling

Memory is modeled as
Array of vector of
Registers. This is an
Array of 26M 32-bit
Registers.

```
module MEMORY_64MB(DATA, READ, WRITE, ADDR, CLK, RST);
. . .
// meory bank
reg [`DATA_INDEX_LIMIT:0] sram_32x64m [0:`MEM_INDEX_LIMIT]; // memory storage
integer i; // index for reset operation
reg [`DATA_INDEX_LIMIT:0] data_ret; // return data register
assign DATA = ((READ==1'b1)&&(WRITE==1'b0)) ? data_ret : {`DATA_WIDTH{1'bz}};
. . .
endmodule
```

Return data
Register for
Read operation.

For a read operation, set
DATA to the value of
data_ret register.
Otherwise set it to HiZ. For
operations other than read,
the DATA Port needs to be
driven by register outside of
The module, hence it need to
Electrically detached from
Inside the memory for non-read
Operation.

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Memory Modeling

If the RST is 0, i.e. -ve Edge happened for this Signal, loop through all the index of the array of registers and set them to all 0. Once reset is Done load the content From mem_init_file into Memory portion as Requested in the memory Data file.

Always at -ve edge Of RST or +ve edge of CLK do the following section.

```
module MEMORY_64MB(DATA, READ, WRITE, ADDR, CLK, RST);
    . . .
    always @ (negedge RST or posedge CLK)
    begin
        if (RST == 1'b0)
        begin
            for(i=0; i<=MEM_INDEX_LIMIT; i = i + 1)
                sram_32x64m[i] = { `DATA_WIDTH(1'b0) };
            $readmemh(mem_init_file, sram_32x64m);
        end
        else
        begin
            if ((READ==1'b1)&&(WRITE==1'b0)) // read operation
                data_ret = sram_32x64m[ADDR];
            else if ((READ==1'b0)&&(WRITE==1'b1)) // write operation
                sram_32x64m[ADDR] = DATA;
        end
    end
endmodule
```

If it is a read operation assign data_ret value to the value of The memory content as address ADDR. If it write operation, then Set the memory content of the at address ADDR to the Value in DATA.

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Memory Data File

Address at which The successive data To be loaded.

Data can be loaded Into multiple address location

```
@0001000
00414020 00414021 00414022 00414023
00414024 00414025 00414026 00414027
00414028 00414029 0041402a 0041402b
0041402c 0041402d 0041402e 0041402f

@002f00a
00514020 00514021 00514022 00514023
00514024 00514025 00514026 00514027
00514028 00514029 0051402a 0051402b
0051402c 0051402d 0051402e 0051402f
```

Content of the memory starting at Data address 0x002f00a. Each data is separated by space / tab / newline.

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