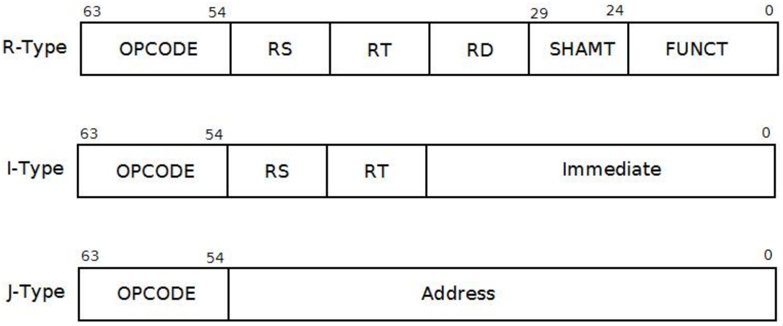
Class	CS147, Sec 01
Homework	I
Due Date	Sep 26, 2018 11:59 PM PST
Instructions	1. There are 5 questions with total 100 points. 2. Please create electronic document with your answer. 3. There is no need to include the question itself. However, you **MUST** include question number and sub-part index if any. Example: 5(b) 4. Please create a PDF document **hw1.pdf** and ***upload that in Canvas*** assignment page by the due date. 5. **Please re-check you submission for any logistic errors (empty file, corrupted PDF, and many more) and re-submit if needed. Once grading is started, any file with logistics errors will be given 0 point.** 6. **NO** handwritten (and scanned) document is accepted. You answer must be typed in (and computer drawn if diagram is asked) using word processing software. 7. **NO LATE SUBMISSION.** 8. **Please explain your answer clearly – just writing the final answer in a word or two is not sufficient in most of the cases.**

1. A computing system has a processor which supports the following 3-types of instructions. The OpCode field is encoded using 10 bit and shift amount in encoded with 6 bits. All R-type instructions have OpCode 0x0. This processor has a register file of total size 10KB. This computing system is connected to a word addressable memory of size of 32GB which has 32 bi-directional data pins (means read and write can be done one word at a time). This memory needs one clock cycle to complete any read/write request. A back to back read (or write) request can be done by the processor (i.e. issuing read operation to memory while it is processing data of previous read) but write after read must wait for a clock cycle. This memory is running with 1.2 GHz clock.
   a. How many registers are there in register file? [**2pts**]
   b. What is range of the immediate values that can be used with I-type arithmetic instructions assuming 2's complement form is used? [**3pts**]
   c. What is the maximum number of instructions supported by this processor? [**5pts**]
   d. How many address ports / pins are there in this memory device? [**3pts**]
   e. What is the clock period in 'ns' unit of the clock that drives this memory? [**2pts**]
   f. If there are 4 million 64-bit data transaction in this system between processor and memory with 25% write operation mix with 0.1 probability of having a write operation immediately succeeding a read, what is the total time of this data transaction in 'ms' unit? [**15pts**]



ANS:

a) Since shift amount is encoded with 6 bits, number of bits per register is 2^6 = 64. Therefore, each register stores 8 bytes. If total size of register file is 10KB then number of registers in the register file will be 10KB/8Bytes = 10K/8 = $2^{11}/2^3 = 2^8$ = 256.

b) Since there are 256 registers, each register fields in instruction format is encoded with 8 bits. The 'opcode' field is 10 bits long. Therefore, immediate field will be (64-8-8-10) = 38 bits long. With 38 bit we can encode values of range [-2^{37}, 2^{37}-1] = [-137438953472, 137438953471] using 2's complement format. This will the range of the numeric values that can be used with I-type arithmetic instructions.

c) There are 2^{10} = 1024 opcodes that can be encoded with this instruction format. One of them in R-type instructions' opcode 0x0. Therefore, there are (1024-1) = 1023 Non-R type instructions. Number of bits in 'FUNCT' field is (64 – 10 – 3*8 – 6) = 24. Therefore, there can be total 2^{24} = 16777216 functions encoded. Therefore, total number of instructions can be encoded with this format is (16777216 + 1023) = 16778239.

d) Since the memory is word addressable there will be 32GB/4B = 8G = 2^{33} addresses to be generated to uniquely address each word. This needs $\log_2(2^{33})$ = 33 bits for address field. Therefore, memory will have 33 address port / pin.

e) Clock period = 1/clock frequency. For this memory clock, clock period is (1/1.2GHz) = 0.833ns

f) With 25% write operation mix there are 3 million 64-bit read and 1 million 64-bit write. Since memory is 32-bit (since it has 32 bidirectional data pins) any 64-bit read/write operation will take 2 read/write. Hence there are 6 million read and 2 million write operations done by the memory. Each of this read and write operation will take 1 clock cycle. Hence total number of clock cycle needed is 8 million.

However, out of 1 million 64-bit write operations there is 0.1 probability of having a write operation succeeding a read operation. There must be (0.1*1 million) = 0.1 million wait cycle for the preceding read data to be consumed by processor.

Therefore, this specific data transaction needs 8.1 million clock cycle. Each clock cycle is 0.8333ns. So, this operation will take (8.1 million * 0.8333ns) = 6.75ms.

2. A number system muNote uses symbol Do, Re, Mi, Fa, So, La, Ti with equivalent decimal weight 0, 1, 2, 3, 4, 5, 6 respectively. In that case, answer the following.

   a. What is the decimal equivalent of TiLaSoDoReMiFa? [**5pts**]

   a. What is muNote equivalent of decimal number 1546781? [**5pts**]

Ans:

a) Since 'muNote' number system has 7 symbols its base is 7. Hence decimal representation of muNote value TiLaSoDoReMiFa is computed as following.

(Ti * 7^6) + (La * 7^5) + (So * 7^4) + (Do * 7^3) + (Re * 7^2) + (Mi * 7^1) + (Fa * 7^0)

= (6 * 7^6) + (5 * 7^5) + (4 * 7^4) + (0 * 7^3) + (1 * 7^2) + (2 * 7^1) + (3 * 7^0)

= 705894 + 84035 + 9604 + 0 + 49 + 14 + 3

= **799599**

b) Value represented in decimal as 1546781 will be represented in rainbow as **ReTiReDoReFaTiLa**. Computation is as following.

Steps				Quotient	Remainder	Symbol
1546781	/	7	=	220968	5	La
220968	/	7	=	31566	6	Ti
31566	/	7	=	4509	3	Fa
4509	/	7	=	644	1	Re
644	/	7	=	92	0	Do
92	/	7	=	13	1	Re
13	/	7	=	1	6	Ti
1	/	7	=	0	1	Re

3. Using Boolean algebra identity formulae prove LHS is equivalent to RHS.
    a. F(x,y,z) = x'z+xy = x'y'z+yz+xy [**5pts**]
    b. F(a,b,c,d) = a’b’c’d’ + a’b’cd + a’b’cd’ + ab’c’d’ + ab’cd’ + ab’cd = b’(c+d’) [**5pts**]
    c. Prove (a) by constructing truth table of LHS and RHS. [**5pts**]
    d. Prove (b) by constructing truth table of LHS and RHS. [**5pts**]

ANS:

a) x'z+xy = x'z+xy+xy

= x'z(y+y')+xy(z+z')+xy

= x'yz+x'y'z+xyz+xyz'+xy

= x'y'z+(x'yz+xyz)+(xyz'+xy)

= x'y'z+(x+x')yz+(1+z')xy

= x'y'z+yz+xy

b) a’b’c’d’ + a’b’cd + a’b’cd’ + ab’c’d’ + ab’cd’ + ab’cd

= a’b’c’d’ + ab’c’d’)+ (a’b’cd + a'b'cd’) + (ab’cd’ + ab’cd)

= b'c'd'(a+a') + a'b'c(d+d') + ab'c(d'+d)

= b'c'd'.1 + a'b'c.1 + ab'c.1

= b'c'd' + a'b'c + ab'c

= b'c'd' + b'c(a'+a)

= b'c'd' + b'c.1

= b'c'd' + b'c

= b'(c'd' + c)

= b'((c+c')(c+d'))

= b'(1.(c+d'))

= b'(c+d')

c) Both LHS and RHS Boolean expression truth table are equal. Thus LHS = RHS.

LHS (x'z+xy)			
x	**y**	**z**	**F(x,y,z)**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

RHS (x'y'z+yz+xy)			
x	**y**	**z**	**F(x,y,z)**
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

d) Both LHS and RHS Boolean expression truth table are equal. Thus LHS = RHS.

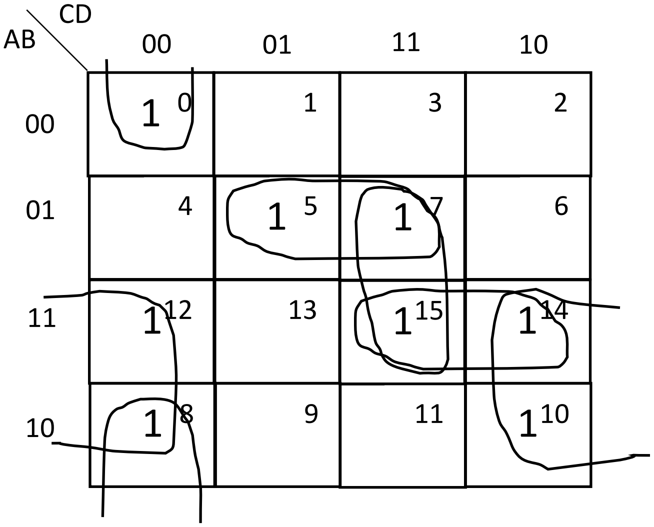
LHS (a’b’c’d’ + a’b’cd + a’b’cd’ + ab’c’d’ + ab’cd’ + ab’cd)				
a	**b**	**c**	**d**	**F(a,b,c,d)**
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

RHS (b’(c+d’))				
a	**b**	**c**	**d**	**F(a,b,c,d)**
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

4. Using K-Map technique simplify following functions and show all 'prime implicants' and 'Essential prime implicants' (use compact SOP form).
   a. f (A, B, C, D) = ∑ m (0, 5, 7, 8, 10, 12, 14, 15)
   b. f(w, x, y, z) = ∑ m (1,3,4,7,11) + d(5, 12, 13, 14, 15)

ANS:

a) f (A, B, C, D) = ∑ m (0, 5, 7, 8, 10, 12, 14, 15)



AB \ CD	00	01	11	10
00	1^{0}	1	3	2
01	4	1^{5}	1^{7}	6
11	1^{12}	13	1^{15}	1^{14}
10	1^{8}	9	11	1^{10}

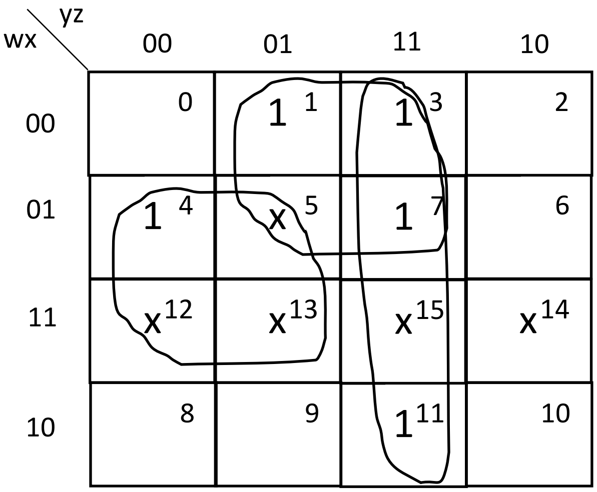
Prime Implicants:

- ∑ m (0, 8)
- ∑ m (8, 10, 12, 14)
- ∑ m (5,7)
- ∑ m (7,15)
- ∑ m (14, 15)

Essential Prime Implicants:

- ∑ m (0, 8)
- ∑ m (8, 10, 12, 14)
- ∑ m (5,7)
- ∑ m (7,15) or ∑ m (14, 15)

b) f(w, x, y, z) = ∑ m (1,3,4,7,11) + d(5, 12, 13, 14, 15)



wx \ yz	00	01	11	10
00	0	1^{1}	1^{3}	2
01	1^{4}	x^{5}	1^{7}	6
11	x^{12}	x^{13}	x^{15}	x^{14}
10	8	9	1^{11}	10

Prime Implicants:

- $\sum m\ (1,3,5,7)$
- $\sum m\ (4,5,12,13)$
- $\sum m\ (3,7,11,15)$

Essential Prime Implicants:

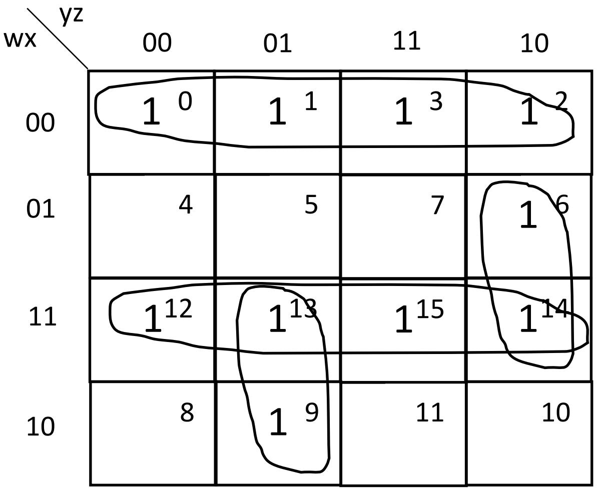
- $\sum m\ (1,3,5,7)$
- $\sum m\ (4,5,12,13)$
- $\sum m\ (3,7,11,15)$

5. Design and implement a digital circuit which will detect a 4 bit number (input signals are w,x,y,z with 'w' representing MSB) which is less than 3 or greater than 12 or divisible by 3, i.e. if these conditions are met, the output (OUT) is 1, 0 otherwise. Implement the circuit with NAND only logic gate. You can assume multi-input NAND gate is available (i.e. 2 or more input pins as you need). You need to show the schematic diagram for the final logic circuit along with all the steps to derive the logic equation of the implemented circuit. [**30pts**]

ANS:

The truth table for the function will be as following.

m#	W	X	Y	Z	OUT
0	0	0	0	0	**1**
1	0	0	0	1	**1**
2	0	0	1	0	**1**
3	0	0	1	1	**1**
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	**1**
7	0	1	1	1	0
8	1	0	0	0	0
9	1	0	0	1	**1**
10	1	0	1	0	0
11	1	0	1	1	0
12	1	1	0	0	**1**
13	1	1	0	1	**1**
14	1	1	1	0	**1**
15	1	1	1	1	**1**



wx \ yz	00	01	11	10
00	1 0	1 1	1 3	1 2
01	4	5	7	1 6
11	1 12	1 13	1 15	1 14
10	8	1 9	11	10

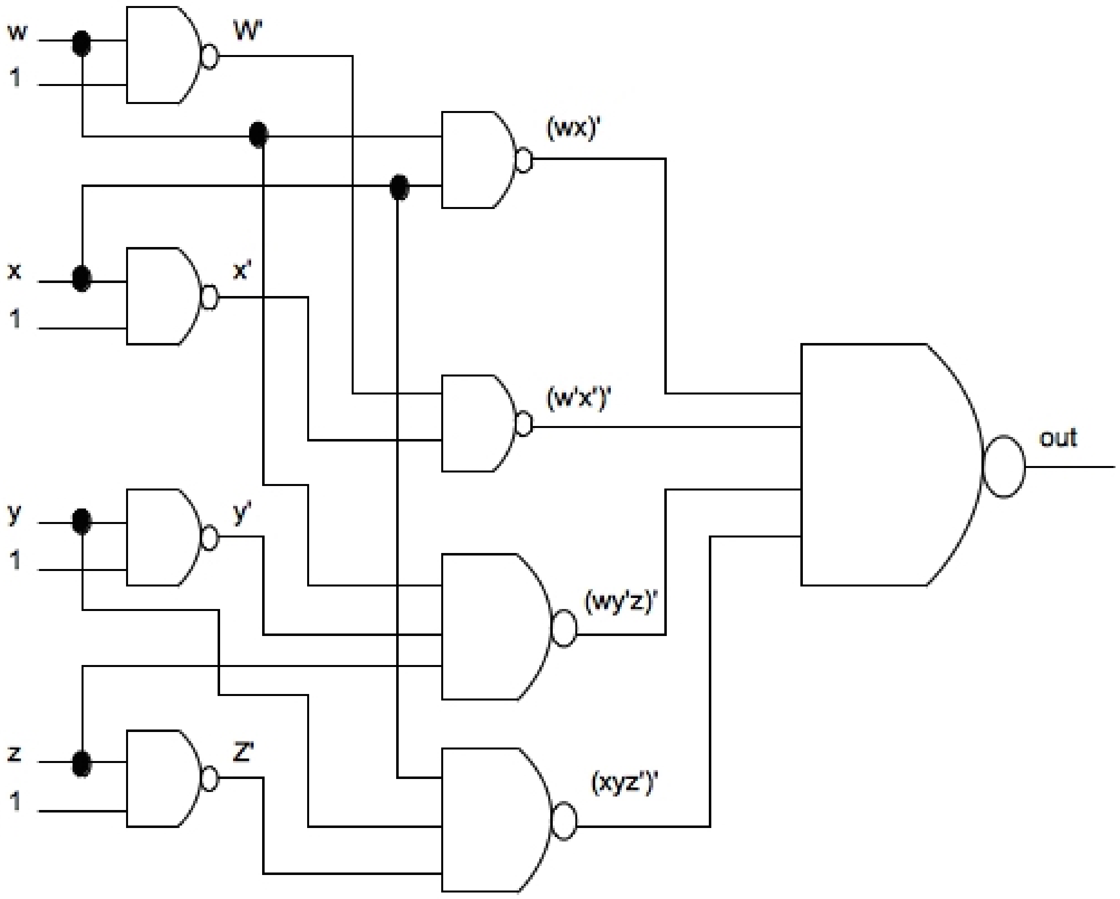
The NAND only equation should be as following form the above K-Map.

$$\begin{aligned} out &= wx + w'x' + wy'z + xyz' \\ &= ((wx)'.(w'x')'.(wy'z)'.(xyz')')' \end{aligned}$$

If m2, m6 were grouped instead of m6, m14 then the equation would be as below.

$$\begin{aligned} out &= wx + w'x' + wy'z + w'yz' \\ &= ((wx)'.(w'x')'.(wy'z)'.(w'yz')')' \end{aligned}$$

The logic circuit schematic should be of the following figure (assuming there are more than two input NAND gate is available).


w
1
W'
x
1
x'
y
1
y'
z
1
Z'
(wx)'
(w'x')'
(wy'z)'
(xyz')'
out