Solar_Connector

- SOLAR+
- ADC
- SOLAR−

File: Solar_Connector.kicad_sch

Solar_Connector1

- SOLAR+
- ADC
- SOLAR−

File: Solar_Connector.kicad_sch

Solar_Connector2

- SOLAR+
- ADC
- SOLAR−

File: Solar_Connector.kicad_sch

Solar_Connector3

- SOLAR+
- ADC
- SOLAR−

File: Solar_Connector.kicad_sch

GND

STM32 MCU

- NRST
- ADC1
- ADC2
- ADC3
- ADC4
- UART_RX
- SDA1
- SCL1
- UART_TX

File: STM32_MCU.kicad_sch

MPPT DC−DC

- VIN_MPPT1
- VOUT_MPPT1
- SMBALERT_MPPT1
- SDA_MPPT1
- SCL_MPPT1
- BATSENS+_MPPT1

File: MPPT.kicad_sch

Battery_Connector

- VBAT

File: Battery_Connector.kicad_sch

Power

- VBUS_IN
- 3.3V_OUT
- EN_3V3
- EN_5V0

File: Power.kicad_sch

Board Connector

- 3.3V_PIN
- PIN_0
- PIN_1
- PIN_2
- PIN_3
- PIN_4
- PIN_5
- PIN_6
- PIN_7
- PIN_8
- PIN_9
- PIN_10
- PIN_11
- PIN_12
- PIN_13
- PIN_14

File: Board_Connector.kicad_sch

USB Power

- USB_VBUS

File: USB_Power.kicad_sch

?
LSM115JE3_TR13
D
LSM115JE3_TR13
D1
+5V

Mounting Holes

File: Mounting_Holes.kicad_sch

6.1.6   Power supply scheme

Figure 18. Power supply scheme

VBAT

1.55 – 3.6 V

Backup circuitry
(LSE, RTC,
Backup registers)

V_{DD}

Power switch

n x VDD

Regulator

V_{CORE}

V_{DDIO1}
OUT

GPIOs

Level shifter

IO
logic

Kernel logic
(CPU, Digital
& Memories)

n x 100 nF
+1 x 4.7 µF

IN

n x VSS

V_{DDA}

VDDA

10 nF
+1 µF

V_{REF}

VREF+

ADCs/
DACs/
OPAMPs/
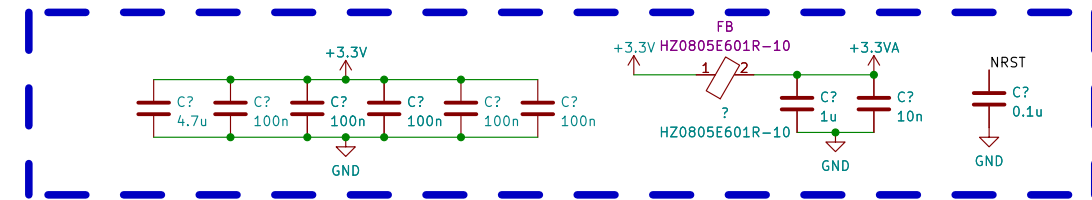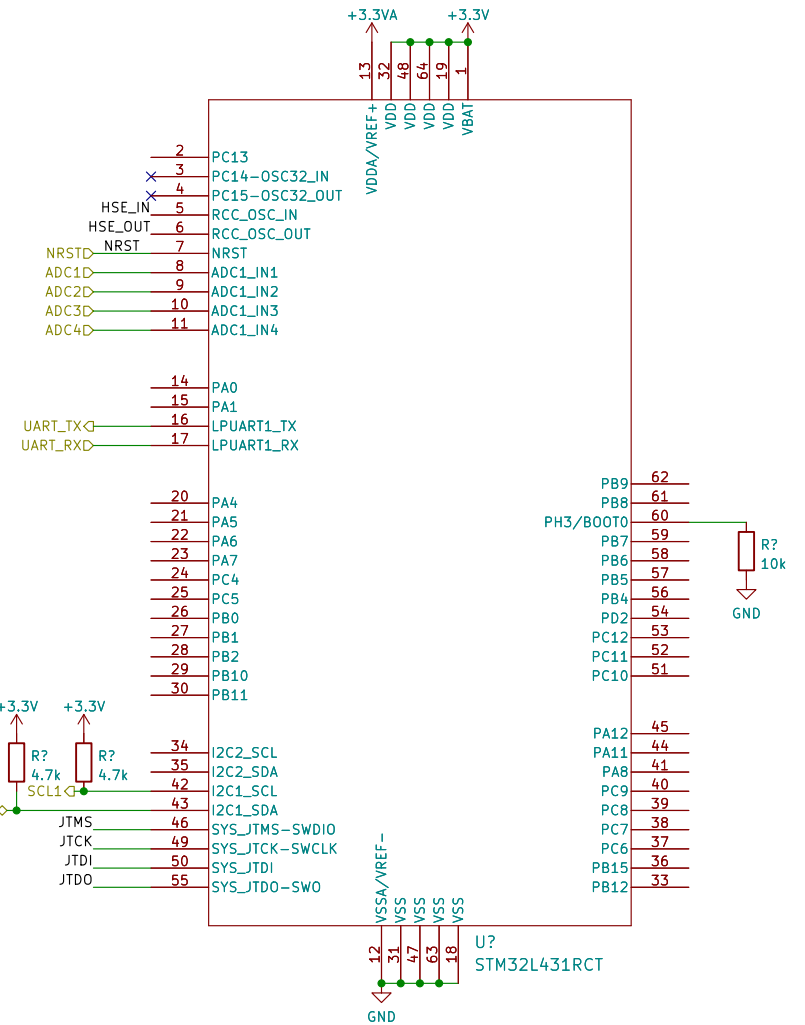COMPs/
VREFBUF

100nF +1µF

VREF−

VSSA

MSv41628V1
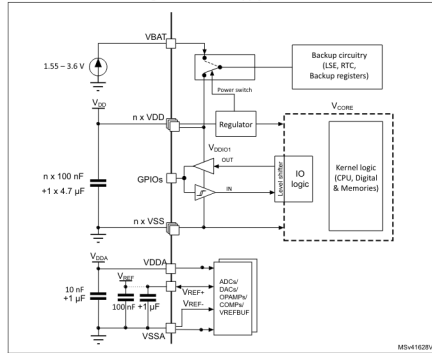
Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} etc.) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

Figure 30. Recommended NRST pin protection

External
reset circuit[1]

V_{DD}

R_{PU}

NRST[2]

0.1 µF

Filter

Internal reset

MS19878V3
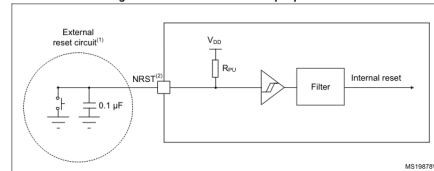
1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 63: NRST pin characteristics*. Otherwise the reset will not be taken into account by the device.
3. The external capacitor on NRST must be placed as close as possible to the device.

+3.3VA   +3.3V

13 VDDA/VREF+
32 VDD
48 VDD
64 VDD
19 VDD
1   VBAT

2   PC13
3   PC14-OSC32_IN
4   PC15-OSC32_OUT
HSE_IN 5 RCC_OSC_IN
HSE_OUT 6 RCC_OSC_OUT
NRST   7 NRST
ADC1   8 ADC1_IN1
ADC2   9 ADC1_IN2
ADC3   10 ADC1_IN3
ADC4   11 ADC1_IN4

14 PA0
15 PA1
UART_TX 16 LPUART1_TX
UART_RX 17 LPUART1_RX

20 PA4
21 PA5
22 PA6
23 PA7
24 PC4
25 PC5
26 PB0
27 PB1
28 PB2
29 PB10
30 PB11

+3.3V +3.3V
R?   R?
4.7k   4.7k
34 I2C2_SCL
35 I2C2_SDA
SCL1 42 I2C1_SCL
SDA1 43 I2C1_SDA
JTMS 46 SYS_JTMS-SWDIO
JTCK 49 SYS_JTCK-SWCLK
JTDI 50 SYS_JTDI
JTDO 55 SYS_JTDO-SWO

62 PB9
61 PB8
60 PH3/BOOT0
59 PB7
58 PB6
57 PB5
56 PB4
54 PD2
53 PC12
52 PC11
51 PC10

+3.3V
R?
10k
GND

45 PA12
44 PA11
41 PA8
40 PC9
39 PC8
38 PC7
37 PC6
36 PB15
33 PB12

12 VSSA/VREF−
31 VSS
47 VSS
63 VSS
18 VSS

GND

U?
STM32L431RCT

NRST

+3.3V   FB   +3.3VA
HZ0805E601R-10
1   2
?
HZ0805E601R-10

C?   C?   C?   C?   C?   C?
4.7u   100n   100n   100n   100n   100n

GND

C?   C?
1u   10n

GND

NRST
C?
0.1u
GND

+3.3V

VTref 1

J?
Conn_ARM_JTAG_SWD_10

RESET 10 R? 22 NRST

SWDCLK/TCK 4 R? 22 JTCK R?
SWDIO/TMS   2 R? 22 JTMS R?
SWO/TDO   6 R? 22 JTDO R?
NC/TDI   8 R? 22 JTDI R?

GNDDetect 9
GND   3

GND

HSE_IN
HSE_OUT

XTAL?
NX5032GA-8.000M-STD-CSU-1

R?
3.3k

C?   C?
6p   6p

GND

Rext must be 3316 Ohms aprox. so resistor measurement is advised to get as close as possible.

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Sheet: /STM32 MCU/
File: STM32_MCU.kicad_sch

Title: EPS Schematics

Size: A4   Date: 2023-04-08   **Rev: v0.0.2**
KiCad E.D.A. kicad 6.0.11-2627ca5db0~126~ubuntu20.04.1   Id: 2/12

The compensation capacitor should be a solid
or "polymer" electrolytic type such as the
Panasonic ZA hybrid series to preserve stable
ESR overtemperature. Conventional, or "wet",
electrolytic capacitors should be avoided as
their ESR increases dramatically at low temperature.

Figure 5 shows an example of a proper Kelvin connection
to the current sense resistors.

4162L_F05

Figure 5. Kelvin Current Sensing with an 0805 Resistor.

VIN_MPPT1

R?
2.5

C?
0.1uF

C?
150uF   GND

GND

?
RQ3G100GNTB
Q
RQ3G100GNTB

5	DRAIN_1	SOURCE_1	1	7
6	DRAIN_2	SOURCE_2	2	
7	DRAIN_3	SOURCE_3	3	
8	DRAIN_4	GATE	4	
9	DRAIN_5			

VOUT

R? 10m

SMBALERT_MPPT1
SCL_MPPT1
SDA_MPPT1

GND

R?
100k

R?
100k

VCC2P5   INTVCC

J?
Conn_02x02_Odd_Even

U?
LTC4162EUFD-L41#PBF

+3.3V

15 DVCC
8   VCC2P5   VCC2P5
2   INTVCC   INTVCC

7   VIN   VOUT   28
                VOUTA   3
6   INFET   BATFET 22
5   CLP   BOOST   1
4   CLN   SW   26
12 SMBALERT   CSP   21
13 SCL   CSN   20
14 SDA   BATSENS+ 19
16 SYNC   NTCBIAS 9
17 CELLS0   NTC   10
18 CELLS1
11 RT   AGND   29
                PGND   24
                PGND   23

R?
63.4k

GND

A 22nF multi-layer ceramic capacitor
is required from SW to BOOST.

1uF C?

4,7uF C?

GND

VOUT   GND

Q?
2N7002

C? 22nF

4,7uH
L?

R?
10m

C?
10uF

GND

VOUT_MPPT1

C?
10uF

GND

MN1: FDMC8327L
MN2: 2N7002
R1: NTCS0402E3103FLT
L1: XAL5030-472MEC

BATSENS+_MPPT1

C?
10uF

C?
150uF

R?
10k

GND

Power Path Controller
The LTC4162 features input and output N-channel MOS-
FET charge pump gate drivers. These drivers make up a
dual unidirectional power path system that allows power
to be delivered to the system load by either the input
supply or the battery, whichever is greater.
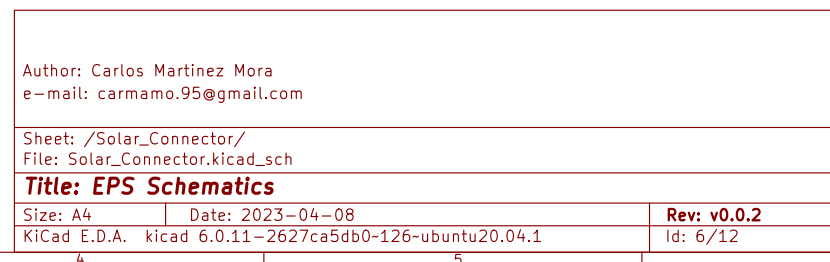
JP?
Jumper_3_Open

R?
10k

TH?
10k

GND

Author: Carlos Martinez Mora
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Sheet: /MPPT DC-DC/
File: MPPT.kicad_sch

Title: EPS Schematics

Size: A4   Date: 2023-04-08   Rev: v0.0.2
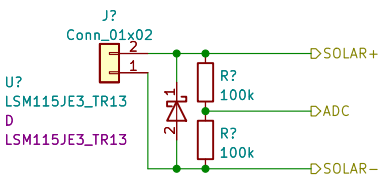KiCad E.D.A.   kicad 6.0.11-2627ca5db0~126~ubuntu20.04.1   Id: 3/12

USB CONNECTOR

P?
USB_C_Plug

Pin	Signal
A4	VBUS
A5	CC
B5	VCONN
A7	D−
A6	D+
B10	RX1−
B11	RX1+
A3	TX1−
A2	TX1+
A10	RX2−
A11	RX2+
B3	TX2−
B2	TX2+
A8	SBU1
B8	SBU2

USB_VBUS

▷USB_VBUS

R?
5.1k

R?
5.1k

U?
PESD5V0H1BSFYL
D
PESD5V0H1BSFYL

GND

SHIELD
GND
S1
A1
GND

3.3V LDO

?
NCP176AMX330TCG
IC
NCP176AMX330TCG

USB_VBUS

C?
C

Pin	Signal		Pin	Signal
5	N/C		1	OUT
6	IN		2	FB
7	GND_2		3	GND_1
			4	EN

GND

+3.3V

C?
C

GND

Layout Consideration

Follow the PCB layout guidelines for optimal performance of RT8258.

▸ Keep the traces of the main current paths as short and wide as possible.

▸ Put the input capacitor as close as possible to the device pins (VIN and GND).

▸ PHASE node is with high frequency voltage swing and should be kept at small area. Keep sensitive components away from the PHASE node to prevent stray capacitive noise pick-up.

▸ Place the feedback components to the FB pin as close as possible.

▸ Connect the GND to a ground plane for noise reduction and thermal dissipation.

10.2 Layout Example

Figure 23. Layout Example

Figure 4. PCB Layout Guide
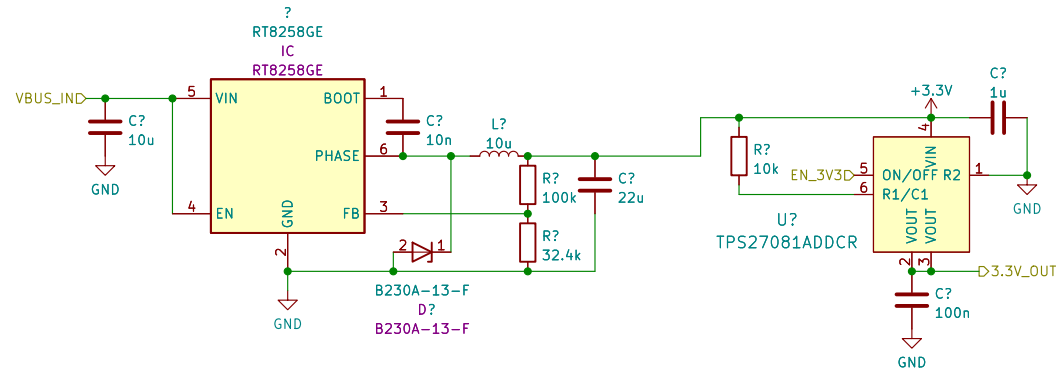
Ground Pin. This pin should be connected to the (−) terminal of the output capacitor and it should be kept away from the D1 and input capacitor for noise prevention.
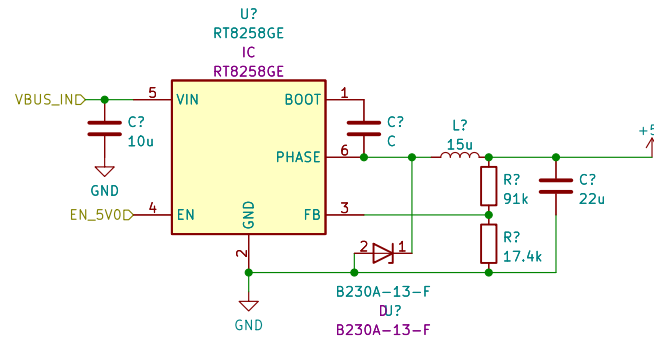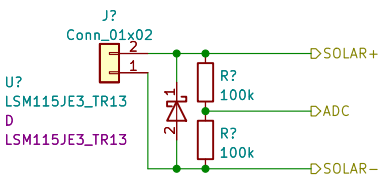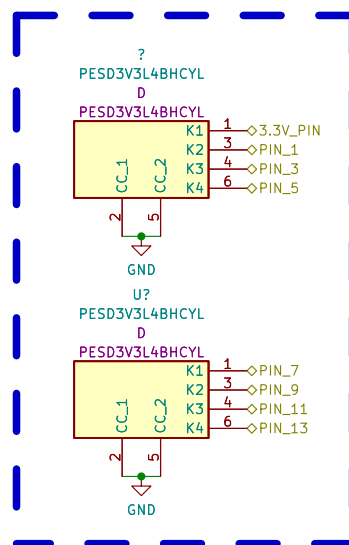
Author: Carlos Martinez Mora
e-mail: carmamo.95@gmail.com

Sheet: /Power/
File: Power.kicad_sch

Title: EPS Schematics

| Size: A4 | Date: 2023−04−08 | Rev: v0.0.2 |
| KiCad E.D.A. kicad 6.0.11−2627ca5db0~126~ubuntu20.04.1 | | Id: 5/12 |

J?
Conn_01x02

2
1

?
LSM115JE3_TR13
D
LSM115JE3_TR13
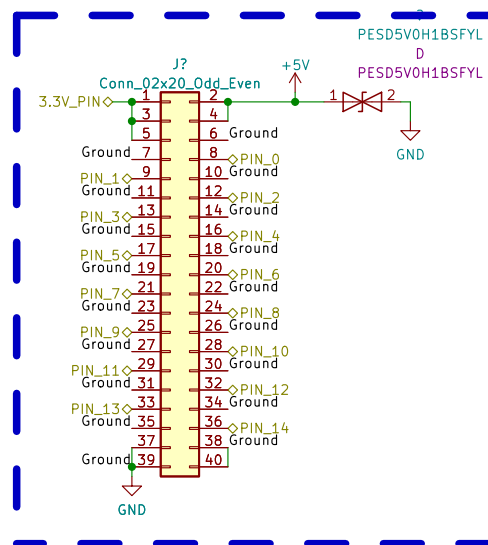
2 1

R?
100k

R?
100k

SOLAR+

ADC

SOLAR−

Title: EPS Schematics

Size: A4   Date: 2023—04—08   Rev: v0.0.2

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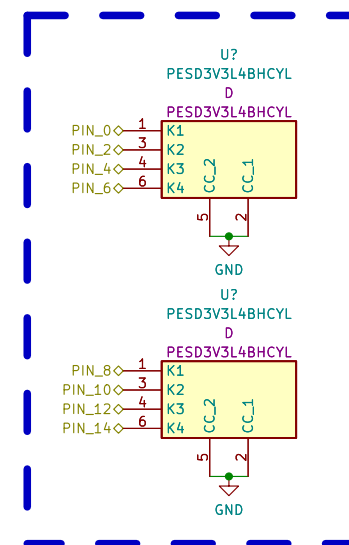
J?
Conn_01x02

U?
LSM115JE3_TR13
D
LSM115JE3_TR13

R?
100k

R?
100k

SOLAR+

ADC

SOLAR-

J?
Conn_01x02

U?
LSM115JE3_TR13
D
LSM115JE3_TR13

R?
100k

R?
100k

SOLAR+

ADC

SOLAR−

J?
Conn_01x02

U?
LSM115JE3_TR13
D
LSM115JE3_TR13

R?
100k

R?
100k

SOLAR+

ADC

SOLAR−

ESD 3.3V

?
PESD3V3L4BHCYL
D
PESD3V3L4BHCYL

K1 1	3.3V_PIN
K2 3	PIN_1
K3 4	PIN_3
K4 6	PIN_5

CC_1 2 CC_2 5

GND

U?
PESD3V3L4BHCYL
D
PESD3V3L4BHCYL

K1 1	PIN_7
K2 3	PIN_9
K3 4	PIN_11
K4 6	PIN_13

CC_1 2 CC_2 5

GND

BOARD CONNECTOR

J?
Conn_02x20_Odd_Even

+5V

3.3V_PIN	1	2	
	3	4	
	5	6	Ground
Ground	7	8	PIN_0
PIN_1	9	10	Ground
Ground	11	12	PIN_2
PIN_3	13	14	Ground
Ground	15	16	PIN_4
PIN_5	17	18	Ground
Ground	19	20	PIN_6
PIN_7	21	22	Ground
Ground	23	24	PIN_8
PIN_9	25	26	Ground
Ground	27	28	PIN_10
PIN_11	29	30	Ground
Ground	31	32	PIN_12
PIN_13	33	34	Ground
Ground	35	36	PIN_14
	37	38	Ground
Ground	39	40	

GND

PESD5V0H1BSFYL
D
PESD5V0H1BSFYL

1   2

GND

ESD 3.3V

U?
PESD3V3L4BHCYL
D
PESD3V3L4BHCYL

PIN_0 1	K1
PIN_2 3	K2
PIN_4 4	K3
PIN_6 6	K4

CC_2 5 CC_1 2

GND

U?
PESD3V3L4BHCYL
D
PESD3V3L4BHCYL

PIN_8 1	K1
PIN_10 3	K2
PIN_12 4	K3
PIN_14 6	K4

CC_2 5 CC_1 2

GND

Title: EPS Schematics

Size: A4	Date: 2023-04-08	Rev: v0.0.2
KiCad E.D.A. kicad 6.0.11-2627ca5db0~126~ubuntu20.04.1		Id: 10/12

VBAT
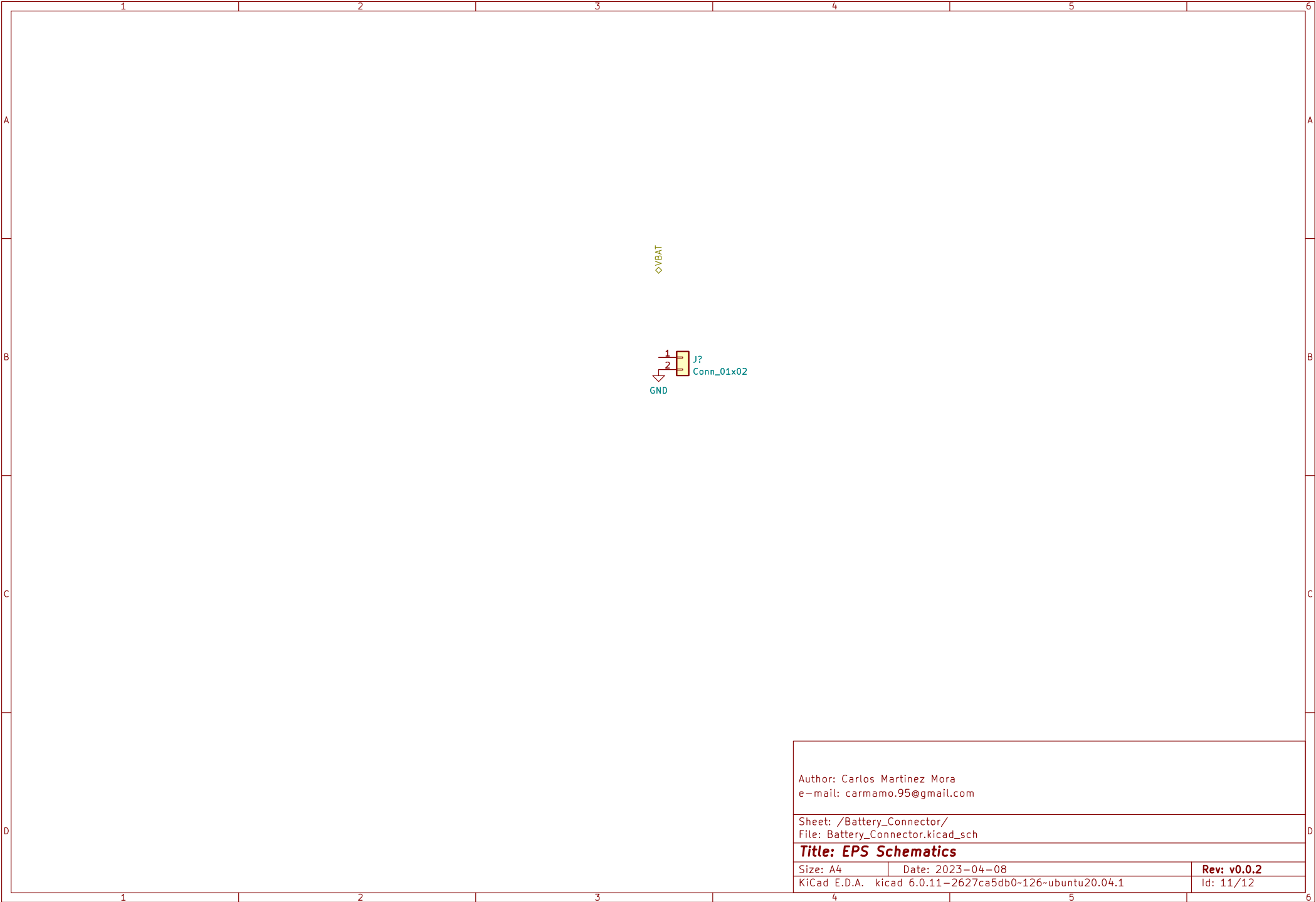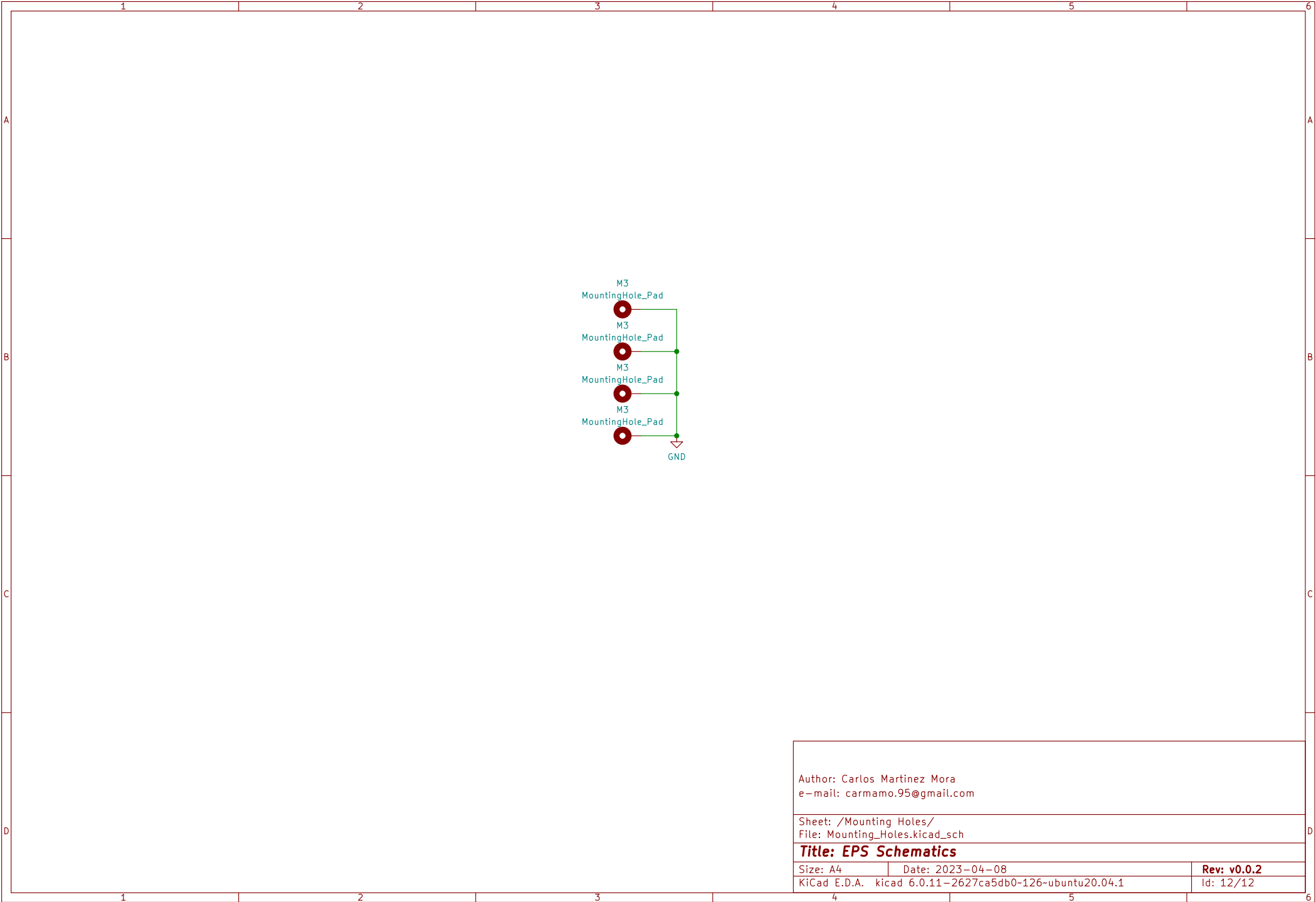
1
2
J?
Conn_01x02

GND

Author: Carlos Martinez Mora
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Sheet: /Battery_Connector/
File: Battery_Connector.kicad_sch

Title: EPS Schematics

| Size: A4 | Date: 2023−04−08 | Rev: v0.0.2 |
| KiCad E.D.A. kicad 6.0.11−2627ca5db0~126~ubuntu20.04.1 | | Id: 11/12 |

M3
MountingHole_Pad

M3
MountingHole_Pad

M3
MountingHole_Pad

M3
MountingHole_Pad

GND

Title: EPS Schematics