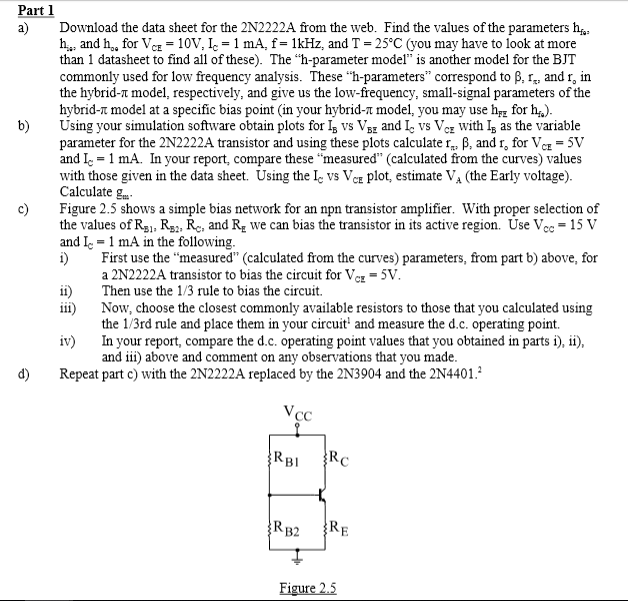
ELEC 301 – Mini Project 2

# Part I



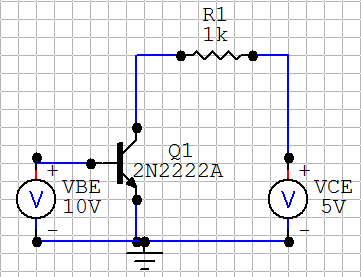
**a)** Below are the 2N2222A parameters as found on the datasheet located at http://www.ret.hu/DataSheets/21\_2N/STM\_009/CD00003223.pdf:

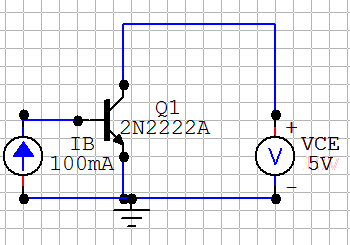
For T = 25 C, Ic = 1mA, f = 1kHz, VCE = 10V

hfe: Min = 50, Max = 300

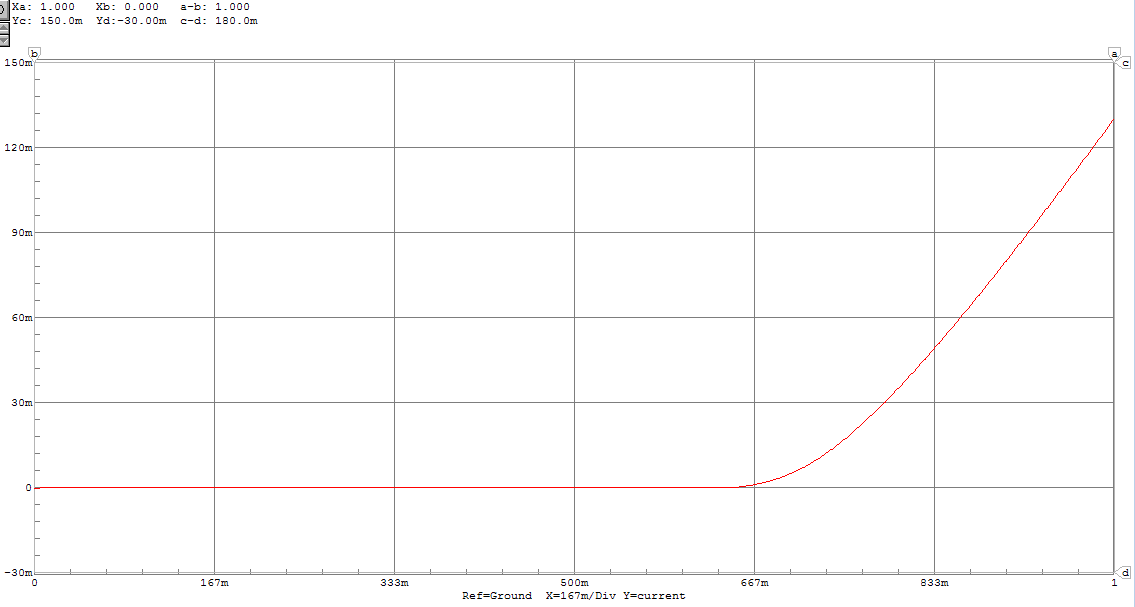
hie: Min = 2kΩ, Max = 8kΩ

hoe: Min = 5μS, Max = 35μS 🡪ro = (hoe)-1 : Min = 28.5kΩ Max = 200kΩ

**b)** The following circuits were modeled using CircuitMaker Student Version to obtain a variety of plots for interpretation.

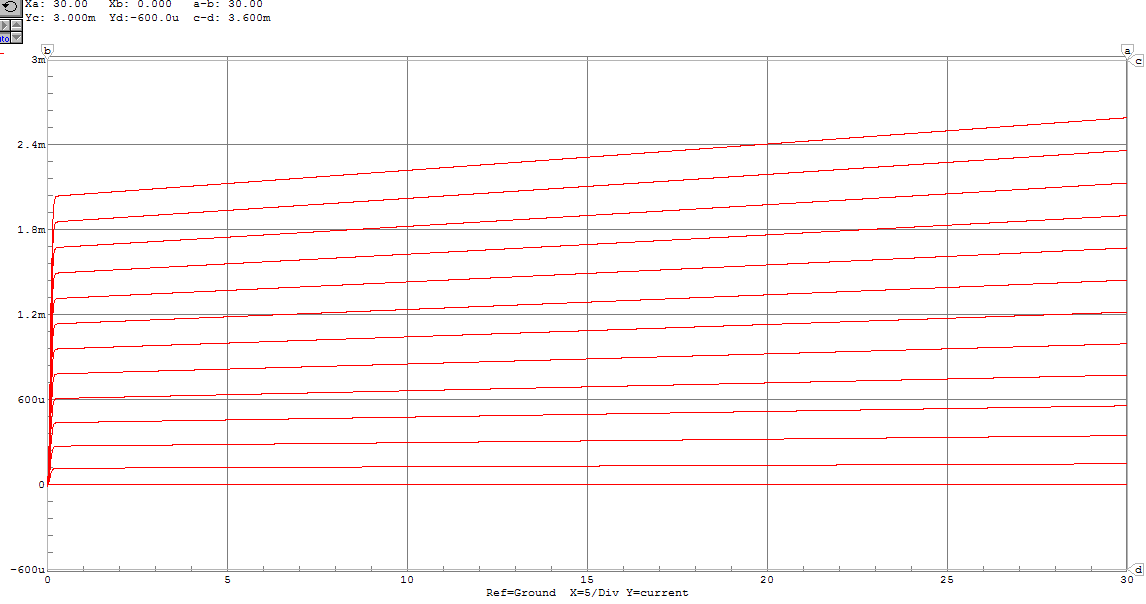


First, we have IB vs VBE with VBE as the variable parameter.



IB of the 2N2222A transistor as a function of changing VBE with VCE = 5V

We also obtain characteristic plots of the transistor by plotting IC as a function of VCE with IB as a variable parameter.



IC of the 2N2222A transistor as a function of changing VCE with IB varying from 0A to 12μA in 1μA intervals. The point at which VCE = 5V and IC = 1mA is marked.

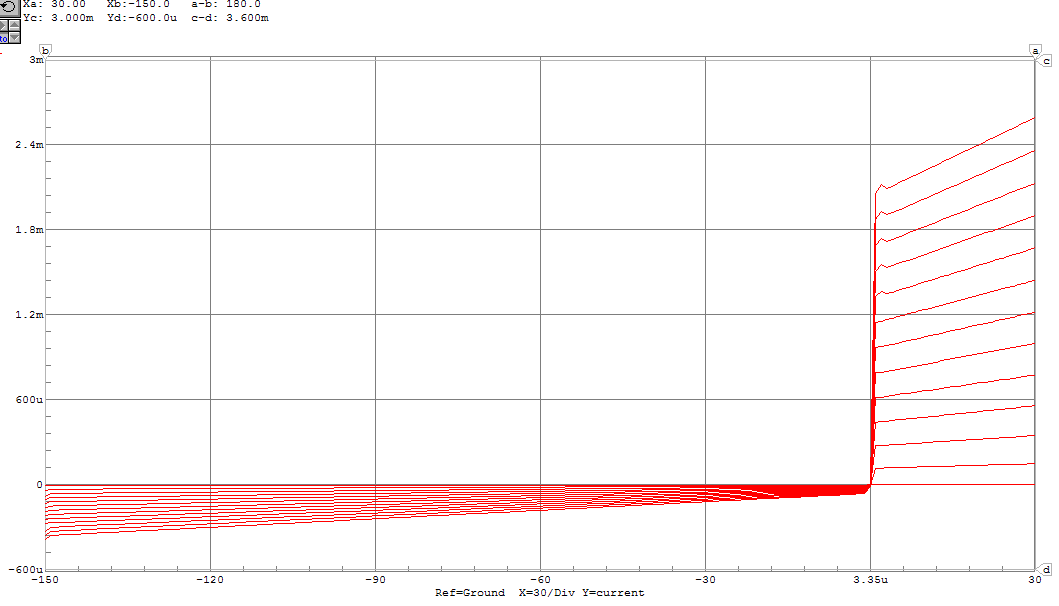
Now we would like to calculate the small signal transistor parameters at VCE = 5V and IC = 1mA. First rπ is determined.

IB is selected based on the characteristic curve that contains VCE = 5V and IC = 1mA. This point is marked on the above figure. It corresponds to IB = 6 μA.

We determine rπ from VT/IB. At room temperature, VT is approximately 25 mV, therefore:

ϐ is determined next. In this case, it is equal to IC/IB. Therefore:

Finally rO is determined. First, we find the early voltage by extrapolating the characteristic curves backwards.



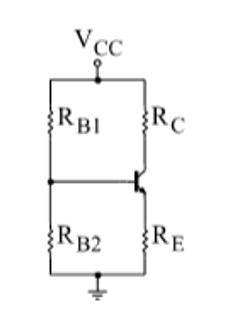
From this plot, we see that Since we can determine that:

Finally, we can determine gm.

These measured values are compared to those given in the datasheet.

|  |  |  |  |
| --- | --- | --- | --- |
|  | **ϐ / hfe** | **rπ / hie** | **ro / (hoe)-1** |
| **Measured** | 166.7 | 4167 | 110,000 |
| **Datasheet** | 50-300 | 2000-8000 | 28,500-200,000 |

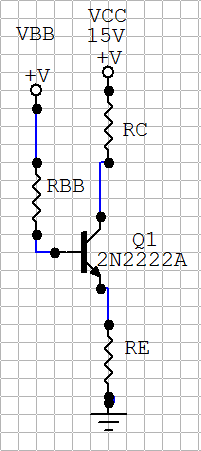
As we can see, all of our measured values fall within the ranges specified on the datasheet.

**c)** i) From this circuit we are looking to find values for RC, RE, RB1 and RB2such that the transistor is biased for VCE = 5V when VCC = 15 V and IC = 1mA.

First, focus on RC and RE. From Kirchoff’s Voltage Law, we establish the following relationship:

RE is set to 5000Ω, and by the above relationship RC must also be equal to 5000Ω. This sets

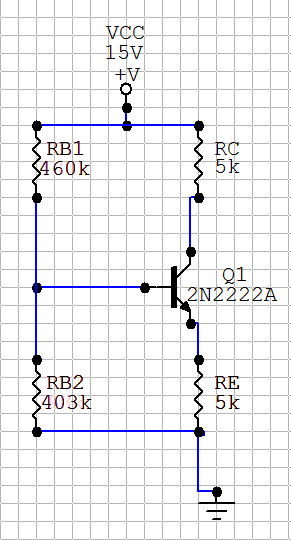
The attention is now drawn towards RB1 and RB2­­. We find the following Thevenin equivalent in order to simplify our analysis.



We now select a value for VBB that will determine RBB. We know that VBB must be less than VCC in order for the CB junction to be forward biased and that VBB must be greater than VB, which will equal 0.7 + VE. This approximately equals 5.7 V. It is also known that which is a small current, so we choose a value on the low end of our range, 7 V.

Finally, we work backwards from the following relationships:

So, in summary:

This bias circuit is simulated in order to obtain the DC operating point.

From the multimeter feature:

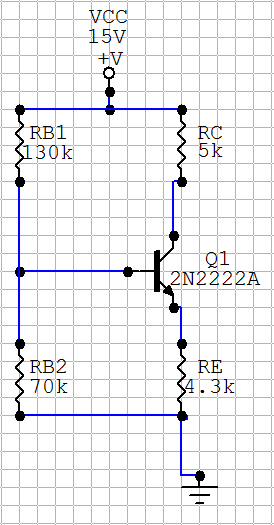
IC = 1.014 mA

V­CE = 9.932 – 5.099 = 4.83 V

ii) The one-third rule is now used to bias the circuit. The first version is chosen.

These conditions are sufficient to govern all resistor values in the bias circuit.

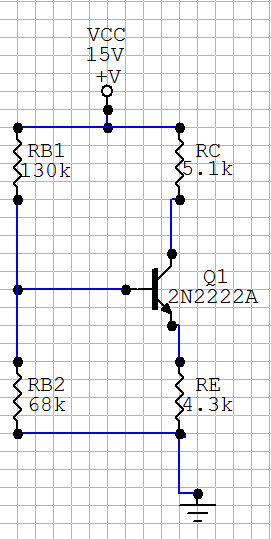
This circuit is simulated in order to obtain the DC operating point:

From the multimeter feature:

IC = 1.011 mA

VCE = 9.943 – 4.375 = 5.57 V

iii) With consultation from, <http://ecee.colorado.edu/~mcclurel/resistorsandcaps.pdf>, an approximation of the bias circuit described in ii) using commonly available resistors was simulated.



Using the multimeter feature to obtain the DC operating point:

IC = 0.991 mA

VCE = 9.946 – 4.287 = 5.66 V

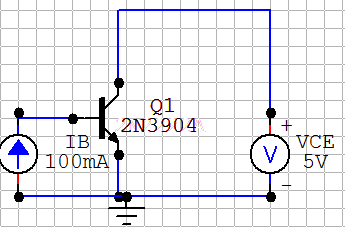
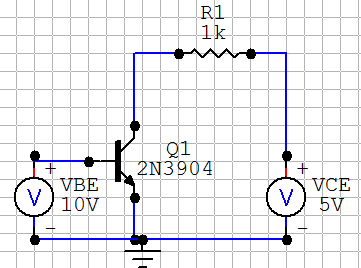
iv) Below is a table containing the DC operating points from the previous sections.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Desired Values** | **Manual Bias** | **1/3 Rule** | **1/3 Rule w/ Commonly Available Resistors** |
| **IC** | 1 mA | 1.014 mA | 1.011 mA | 0.991 mA |
| **VCE** | 5 V | 4.83 V | 5.57 V | 5.66 V |

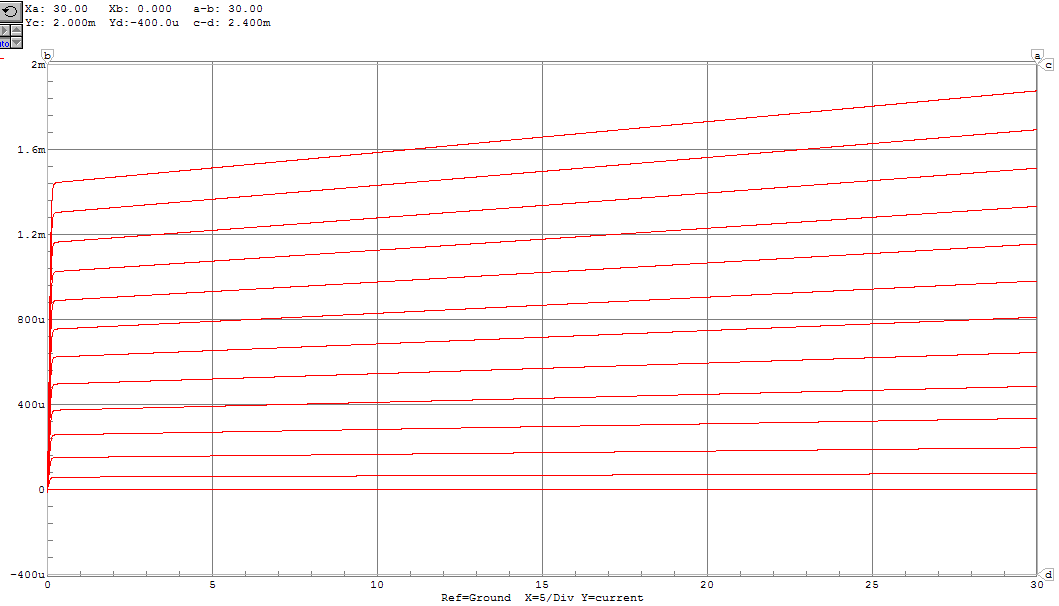
From here we observe that all of these methods result in constant IC values that are very close to our desired values. Though the manual method is more effective at establishing VCE close to our desired value, we can nonetheless conclude that any of these circuits can be used to establish our desired amplifier in the development stage.

**d)**

Now, we would like to see how these bias circuits work with transistors with different parameters. First, we use the **2N3904** transistor. Β, ro, and rπ are found below, in the same method as was used for the 2N2222A transistor.



We obtain characteristic plots of the transistor by plotting IC as a function of VCE with IB as a variable parameter.



IC of the 2N3904 transistor as a function of changing VCE with IB varying from 0A to 12μA in 1μA intervals. The point at which VCE = 5V and IC = 1mA is marked.

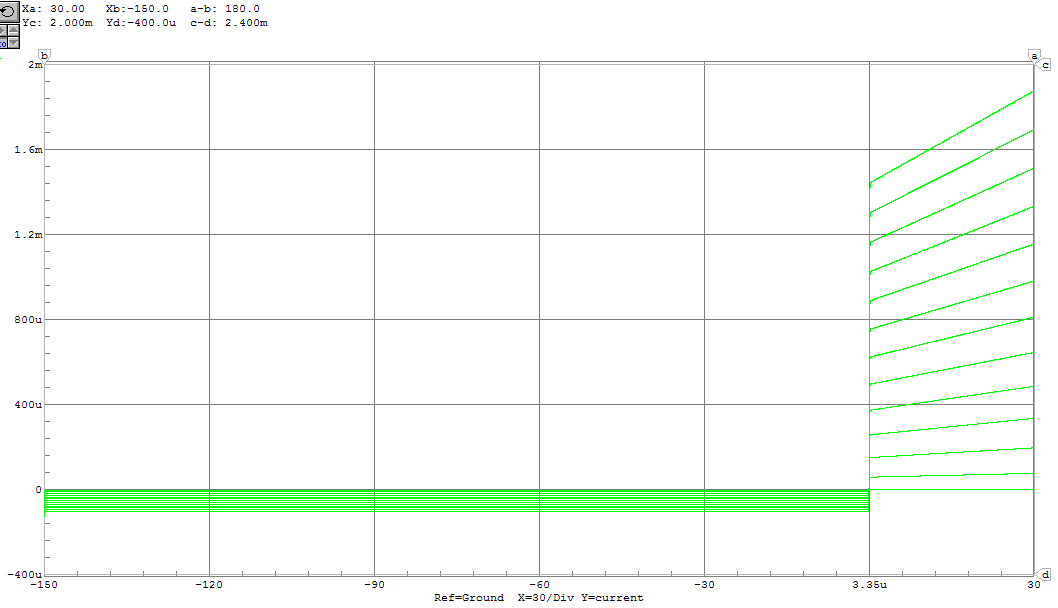
Now we would like to calculate the small signal transistor parameters at VCE = 5V and IC = 1mA. First rπ is determined.

IB is selected based on the characteristic curve that contains VCE = 5V and IC = 1mA. This point is marked on the above figure. It corresponds to IB = 8.5 μA.

We determine rπ from VT/IB. At room temperature, VT is approximately 25 mV, therefore:

ϐ is determined next. In this case, it is equal to IC/IB. Therefore:

Finally rO is determined. First, we find the early voltage by extrapolating the characteristic curves backwards.



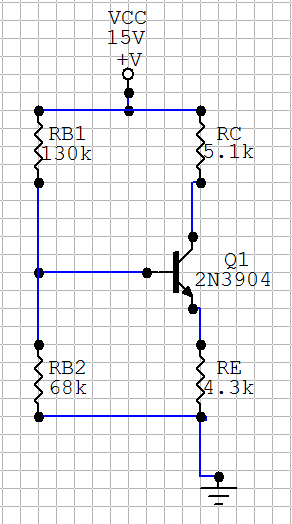
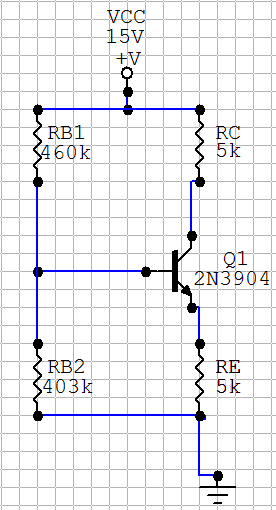
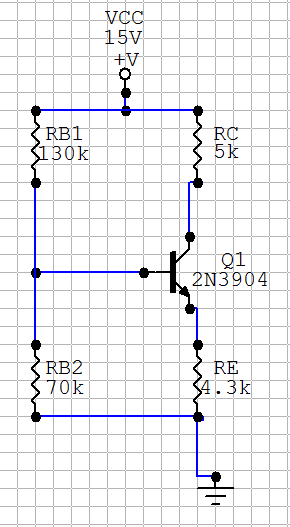
From this plot, we see that Since we can determine that:

Finally, we can determine gm.

In summary,

|  |  |  |  |
| --- | --- | --- | --- |
|  | **ϐ** | **rπ** | **ro** |
| **2N2222A** | 166.7 | 4167 | 110,000 |
| **2N3904** | 117.6 | 2941 | 100,000 |

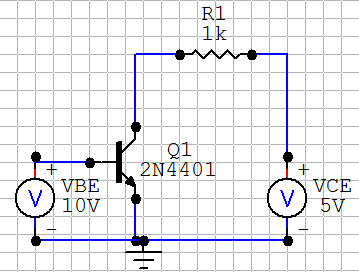
This transistor is inserted into the bias circuits developed for the 2N2222A transistor in order to test tolerance of the biasing solution to varying transistor parameters. (In this case, smaller ϐ and rπ)

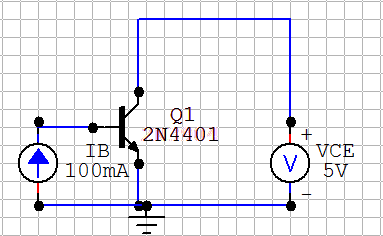


By using the multimeter feature in each of these circuits, the resulting DC operating points are returned.

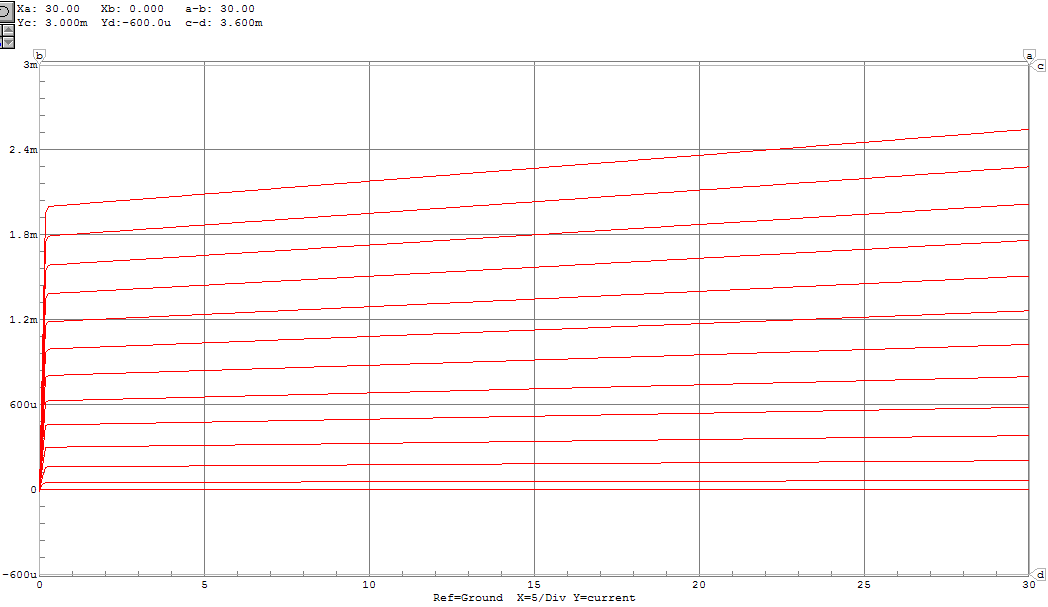
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Desired Values** | **Manual Bias** | **1/3 Rule** | **1/3 Rule w/ Commonly Available Resistors** |
| **IC** | 1 mA | 0.925 mA | 0.975 mA | 0.956 mA |
| **VCE** | 5 V | 5.71 V | 5.89 V | 5.98 V |

We see that the bias circuit is slightly less effective in obtaining the desired DC operating point when the 2N3904 Transistor is used. The result is probably still acceptable enough for prototyping applications, but nevertheless the calculation is quick enough that it would be worth repeating if these were the transistors to use.

Now, we use the **2N4401** transistor. First, we calculate the parameters of this transistor.



We obtain characteristic plots of the transistor by plotting IC as a function of VCE with IB as a variable parameter.



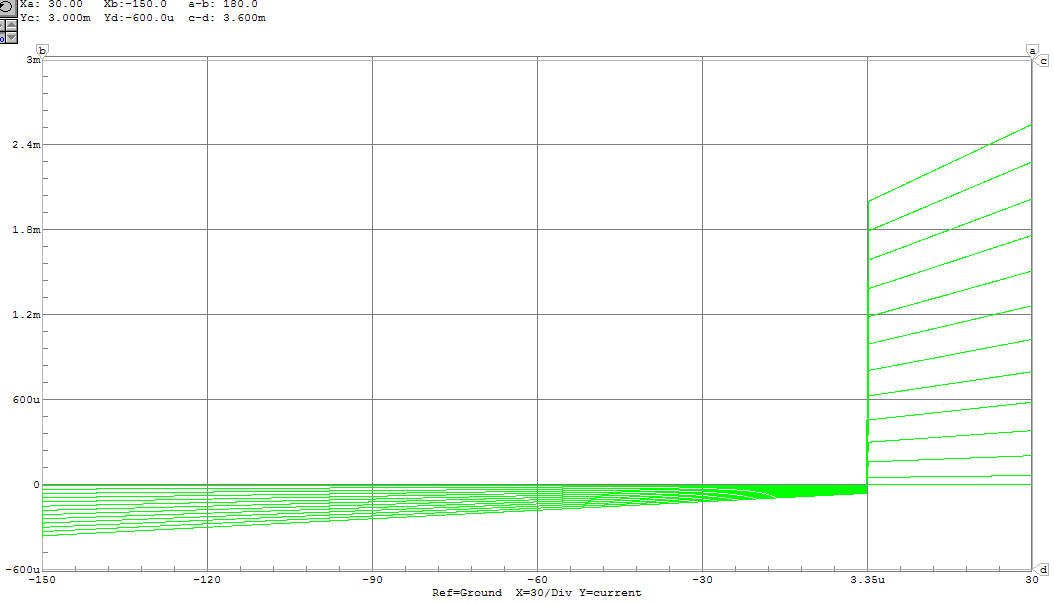
IC of the 2N4401 transistor as a function of changing VCE with IB varying from 0A to 12μA in 1μA intervals. The point at which VCE = 5V and IC = 1mA is marked.

Now we would like to calculate the small signal transistor parameters at VCE = 5V and IC = 1mA. First rπ is determined.

IB is selected based on the characteristic curve that contains VCE = 5V and IC = 1mA. This point is marked on the above figure. It corresponds to IB = 7 μA.

We determine rπ from VT/IB. At room temperature, VT is approximately 25 mV, therefore:

ϐ is determined next. In this case, it is equal to IC/IB. Therefore:

Finally rO is determined. First, we find the early voltage by extrapolating the characteristic curves backwards.

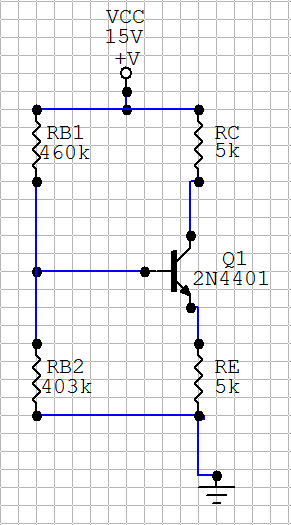
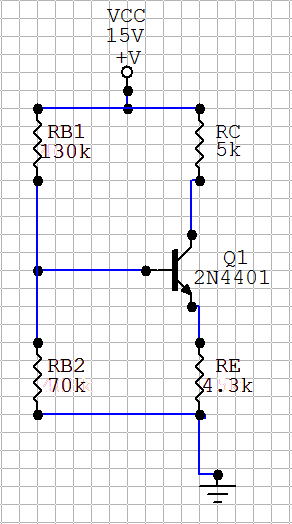
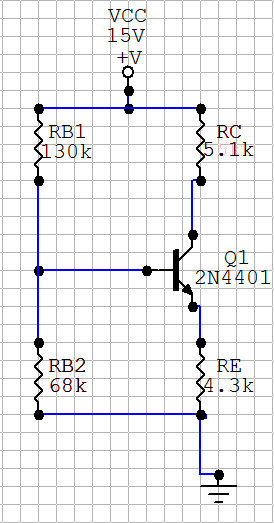
From this plot, we see that Since we can determine that:

Finally, we can determine gm.

In summary:

|  |  |  |  |
| --- | --- | --- | --- |
|  | **ϐ** | **rπ** | **ro** |
| **2N2222A** | 166.7 | 4167 | 110,000 |
| **2N3904** | 117.6 | 2941 | 100,000 |
| **2N4401** | 142.9 | 3571 | 105,000 |

This transistor is inserted into the bias circuits developed for the 2N2222A transistor in order to test tolerance of the biasing solution to varying transistor parameters. We expect the DC operating point of the 2N4401 to fall in between the operating points of the 2N2222A and the 2N3904, as its parameters lie in the center.

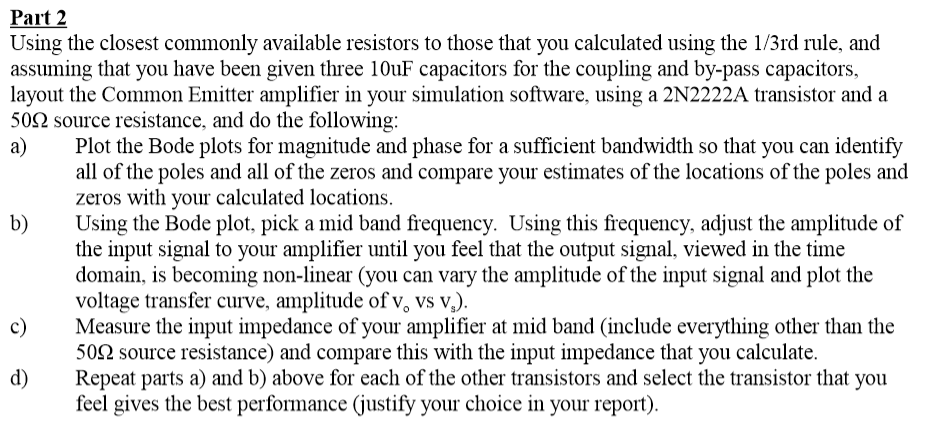


By using the multimeter feature in each of these circuits, the resulting DC operating points are returned.

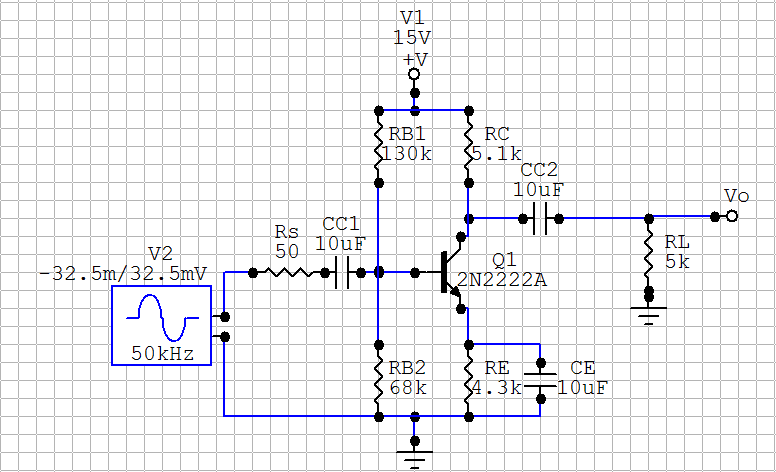
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Desired Values** | **Manual Bias** | **1/3 Rule** | **1/3 Rule w/ Commonly Available Resistors** |
| **IC** | 1 mA | 0.976 mA | 0.990 mA | 0.970 mA |
| **VCE** | 5 V | 5.21 V | 5.76 V | 5.85 V |

As expected, we see that the bias circuit is more effective at reaching our desired values for the 2N4401 than the 2N3904 transistor, but less effective for the 2N4401 than the 2N2222A, which is what the circuit is designed for.

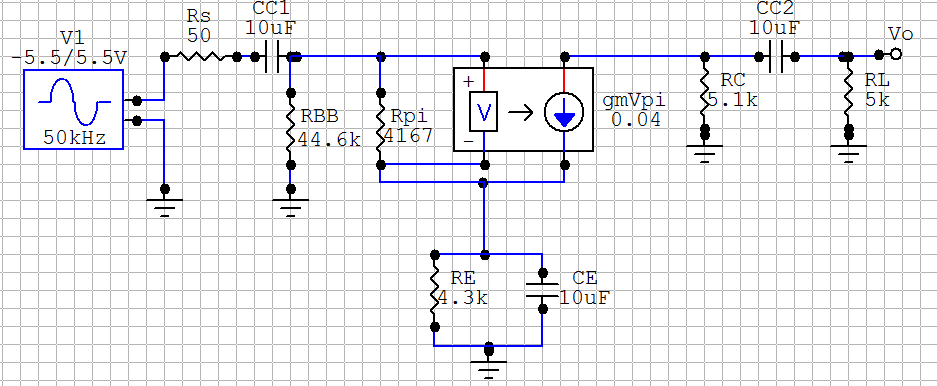
# Part II



Using the bias circuit developed earlier, a 2N2222A transistor, and three 10μF capacitors, we simulate the following common emitter amplifier. We choose an arbitrary load resistance of 5 kΩ.



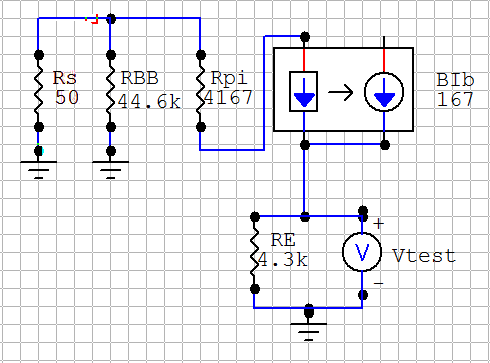
**a)**

First, the locations of the poles and zeros of this amplifier are calculated. For these calculations, we assume that ro is infinitely large for simplicity. We first examine the low frequency poles and zeros. Below is the low frequency small-signal model of this common emitter amplifier.

The low frequency pole determined by CC2 is straightforward, as it sees the current sources as independent, and is therefore decoupled from the rest of the circuit.

The short-circuit time constants are compared for CC1 and CE when calculating the other low frequency poles. The short circuit time constant for CC1 is simple, as the connection through rπ will lead straight to ground.

When finding the short-circuit time constant for CE, in order to find the resistance seen we must place a test source in place of the capacitor. We use a voltage source, and measure the current through it in order to find the resistance. (RCE = V­TEST / ITEST)

To simplify calculations, we replace the voltage-controlled current source with an equivalent current controlled current source.

As expected, we see that the total resistance seen while looking back at the base from the emitter is demagnified by 1+ϐ. From this point forward, we will use this knowledge when finding the time constants.

As expected . This is also knowledge that is assumed for the remainder of the problem set.

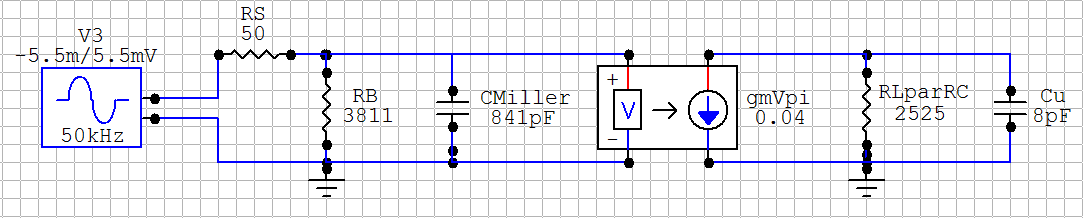
Because the pole associated with C­1 will occur at a lower frequency than the pole associated with C2, we must re-do the calculation for the time constant of C1, using an open circuit as the model for C2. Now:

The low frequency zeros due to the coupling capacitors CC1 and CC2 are equal to zero. For the third value, we need to find a value of CE such that ib­ = 0 when CC1 != 0. This is because when ib = 0, vo  = 0. This will occur when the conductance through the emitter is equal to zero.

Next, the locations of the high frequency poles are calculated. In order to model the high frequency circuit, we need to know the values of cπ and cμ. These are obtained from the datasheet used earlier.

For T = 25C: c­π=25pF and cμ=8pF.

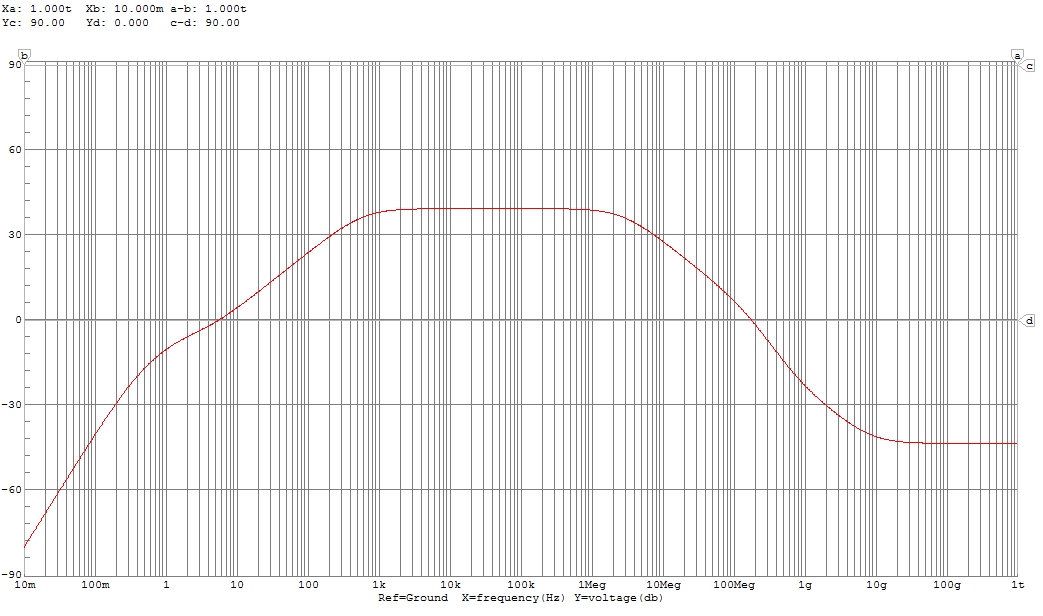
Below is the high frequency small-signal model of our common-emitter amplifier, as modelled using the Miller effect.

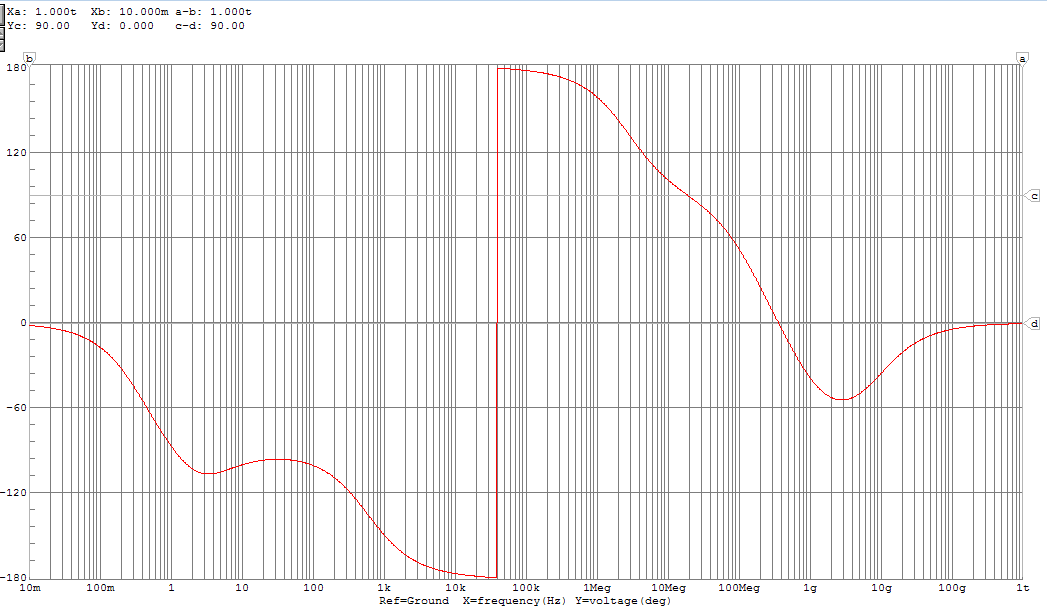


Finding the high frequency poles is straightforward:

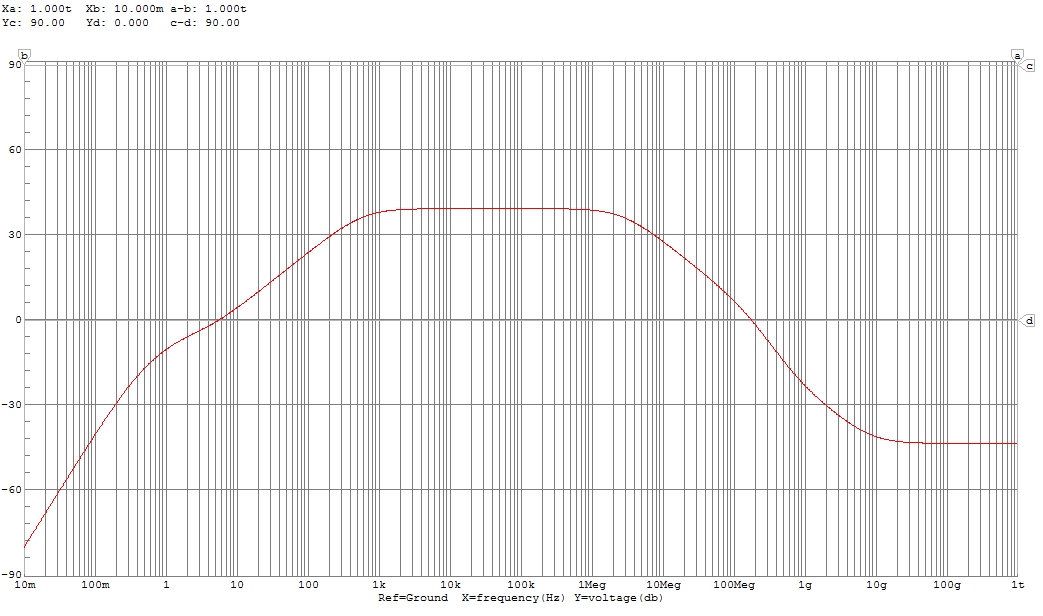
By approximation we have two high frequency zeros at infinity.

Next, we would like to compare these calculated values with values obtained from simulation generated plots. Bode plots for the magnitude and phase of the output voltage are generated from simulation.





The magnitude Bode plot is analyzed for the locations of poles and zeros. Tangent lines to the transfer function are drawn at 20\*x dB/decade. Their intersections are inferred to be poles or zeros, depending on the direction of slope change.



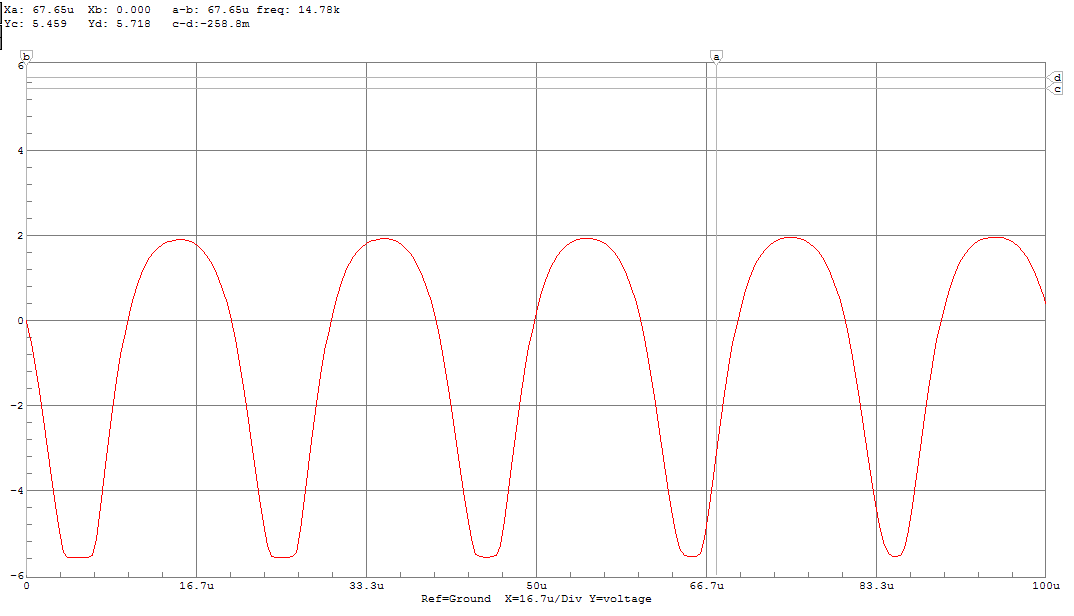
Here is a summary of part a:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **ωLP (Hz)** | **ωLZ(Hz)** | **ωHP(MHz)** | **ωHZ(MHz)** |
| **Calculated** | 0.38, 1.58, 633.9 | 0, 0, 3.70 | 3.82, 7.88 | ∞ |
| **Simulated** | 0.58, 3.3, 600 | 0, 0, 4.3 | 2.8, 210 | 900, 9000 |

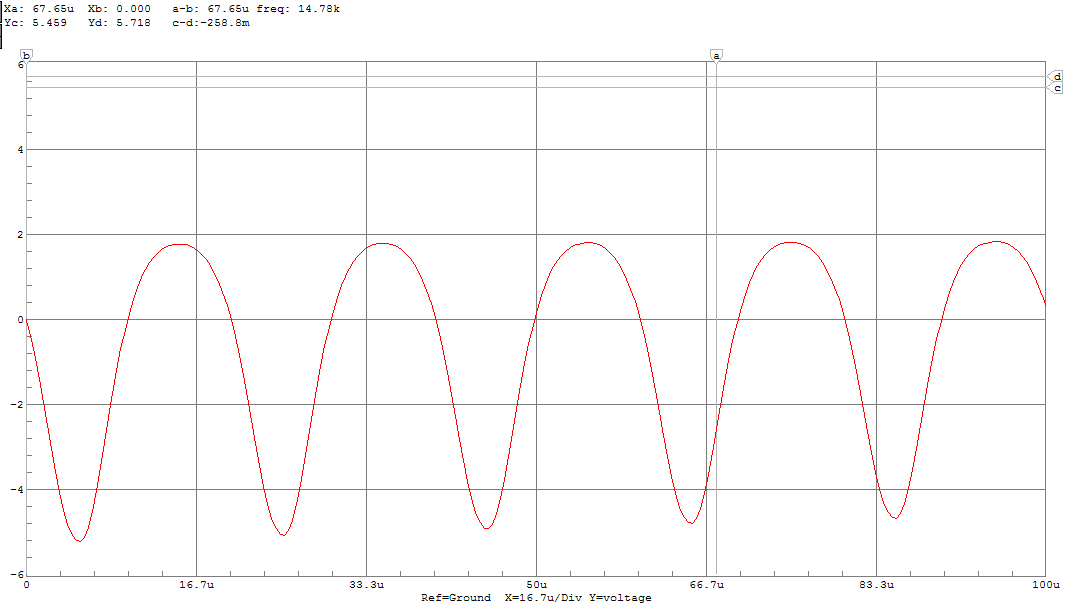
The discrepancies can be attributed to both the facts that we approximating out a resistor when performing our Miller conversion and our omission of ro.

**b)** We pick our midband frequency to be 50 kHz by consulting the magnitude bode plot and choosing a frequency unambiguous located on the midband plateau. We set this as the frequency of our small-signal generator, and vary its amplitude. The oscilloscope feature is used in the simulation to plot the output signal. When the amplifier becomes non-linear, the output signal loses its sinusoidal characteristics.

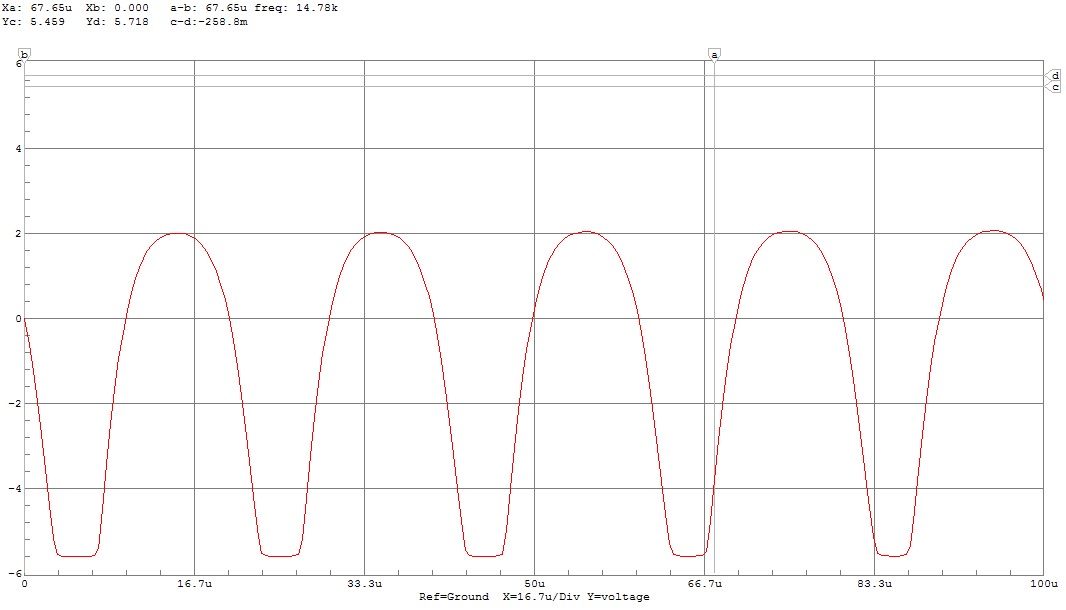
This amplitude was determined to be approximately 37.5 mV. The output signal is plotted below.



For comparison, we generate a plot with a small-signal amplitude of 32.5 mV, which is 5 mV lower and thus should be more linear.

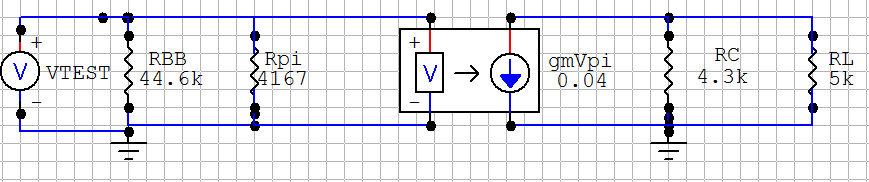


A plot with a small-signal amplitude of 42.5 mV is also plot, which should appear the least linear.



**c)** In order to measure input impedance at midband, the oscilloscope is used to obtain peak voltage and current at the input terminal of the amplifier. We used a 50 kHz frequency to remain at midband, and an amplitude 20mV less than the linear/non-linear transition.

We use the small-signal model of the amplifier at mid band, with the source impedance omitted, in order to calculate the input impedance.



**d)** We use the formulas extracted from our solutions with the 2N2222A transistor and replace the small-signal parameters to those of the new transistors in order to calculate poles and zeros. This is because the amplifier is in the same configuration, simply with a different transistor in place.

2N3904

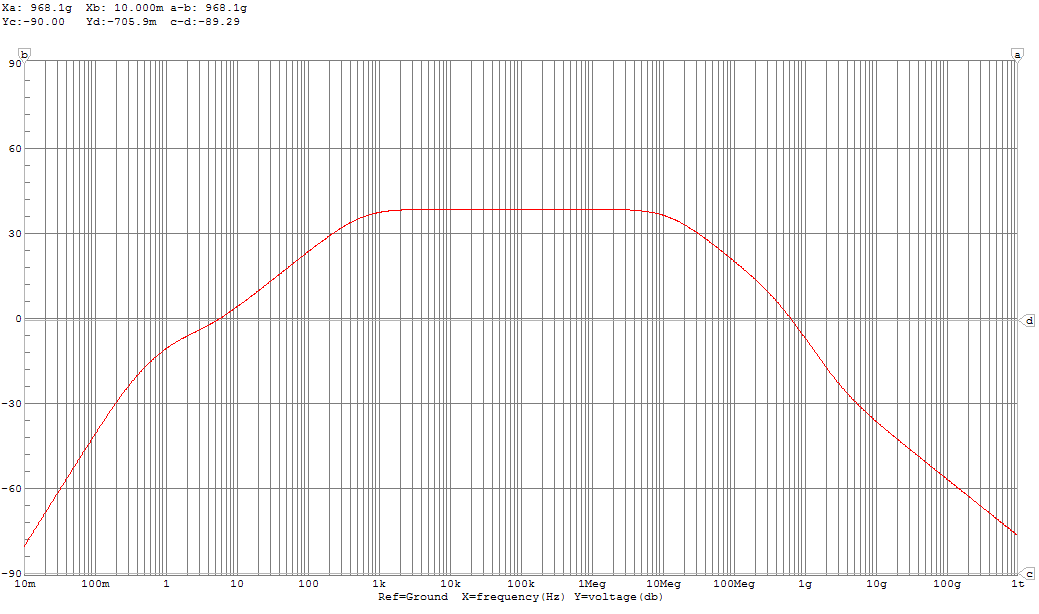
A)

ϐ = 117.6, rpi = 2941, ro = 100,000 from calculations in Part 1

cπ = 18 pF, cμ= 4 pF from <https://www.sparkfun.com/datasheets/Components/2N3904.pdf>

As for the 2N2222A capacitor, we treat ro as infinitely large in order to simplify calculations.

The magnitude Bode plot of the Common-Emitter amplifier circuit with a 2N3904 is plotted in order to graphically locate the poles.

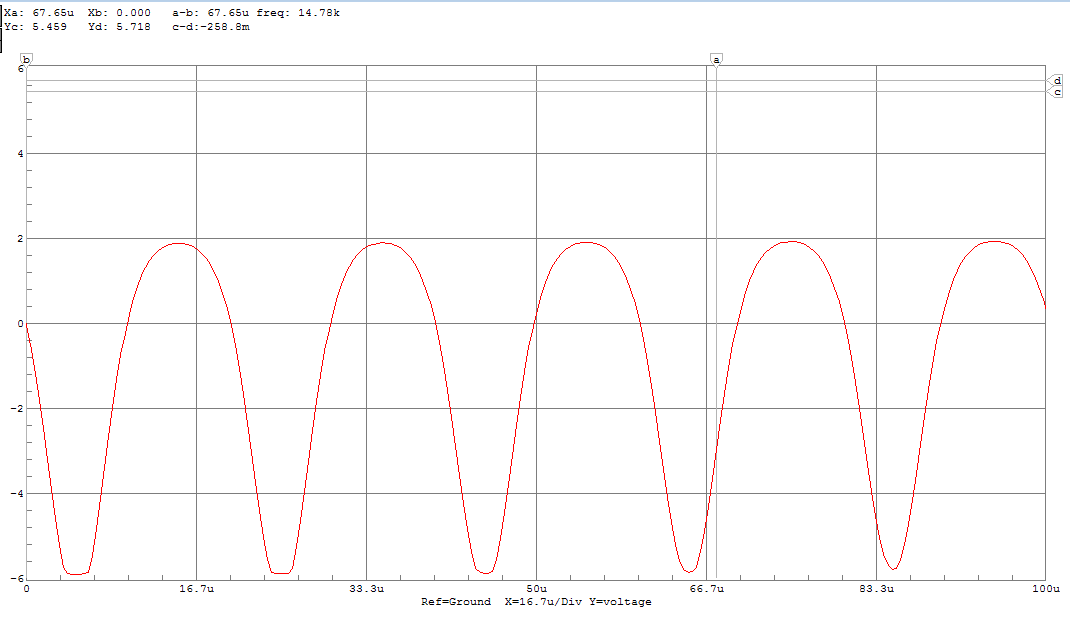


Here is a summary of part a:

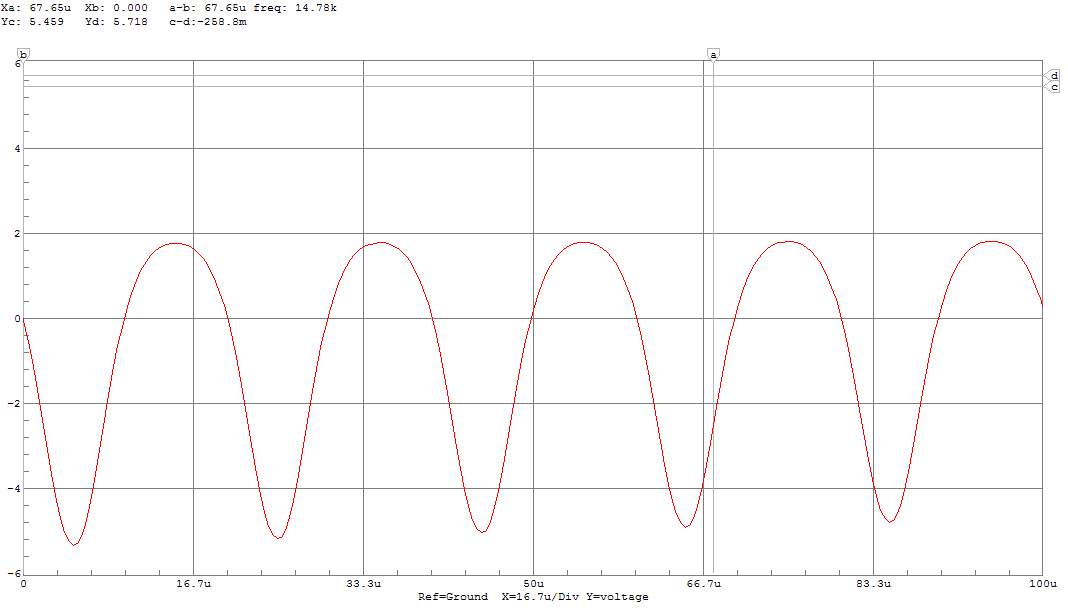
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **ωLP (Hz)** | **ωLZ(Hz)** | **ωHP (MHz)** | **ωHZ(MHz)** |
| **Calculated** | 0.39, 1.58, 634.9 | 0, 0, 3.70 | 7.61, 15.76 | ∞ |
| **Simulated** | 0.42, 3.1, 580 | 0, 0, 6.5 | 12, 510 | 3200 |

b)We pick our midband frequency to be 50 kHz, as before. The oscilloscope feature is used in the simulation to plot the output signal. When the amplifier becomes non-linear, the output signal loses its sinusoidal characteristics.

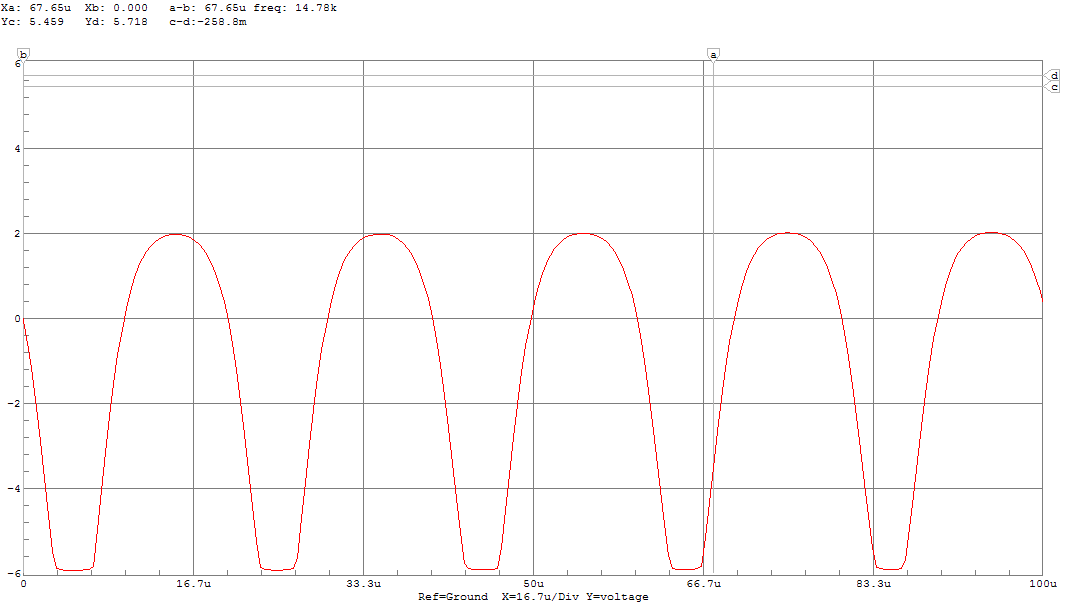
This amplitude was determined to be approximately 40.0 mV. The output signal is plotted below.



For comparison, we generate a plot with a small-signal amplitude of 35 mV, which is 5 mV lower and thus should be more linear.



A plot with a small-signal amplitude of 45 mV is also plot, which should appear the least linear.



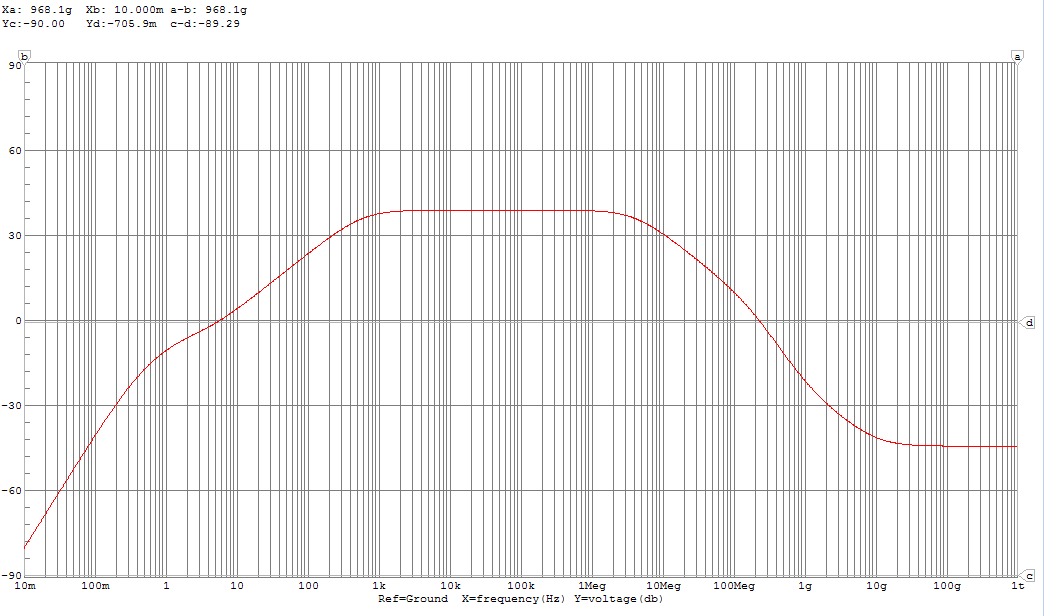
2N4401

ϐ = 143.9, rpi = 3571, ro = 105,000 from calculations in Part 1

cπ = 30 pF, cμ= 6.5 pF from <https://www.fairchildsemi.com/datasheets/2N/2N4401.pdf>

As for the other capacitors, we treat ro as infinitely large in order to simplify calculations.

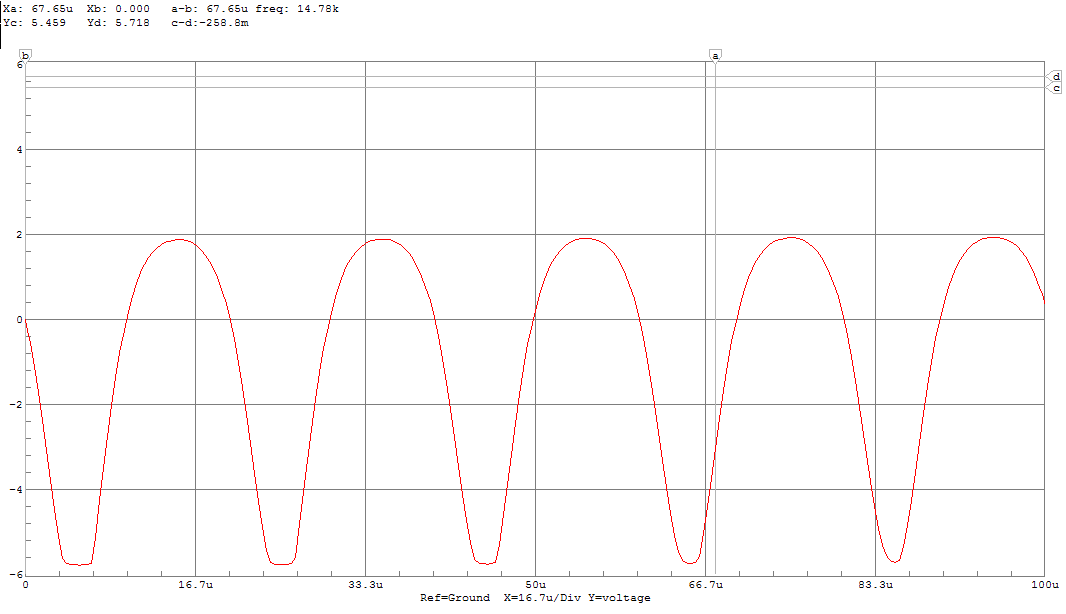
The magnitude Bode plot of the Common-Emitter amplifier circuit with a 2N4401 is plotted in order to graphically locate the poles.



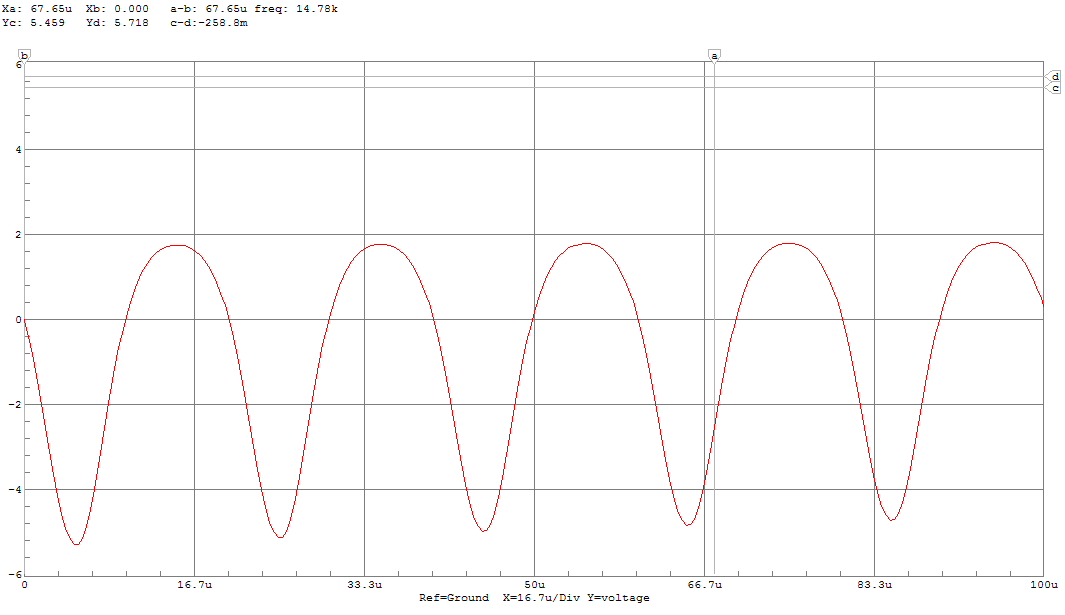
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **ωLP (Hz)** | **ωLZ (Hz)** | **ωHP (MHz)** | **ωHZ (MHz)** |
| **Calculated** | 0.38, 1.58, 640.6 | 0, 0, 3.70 | 4.66, 9.70 | ∞ |
| **Simulated** | 0.37, 2.6, 580 | 0, 0, 5.1 | 4.2, 180 | 880, 11000 |

b)We pick our midband frequency to be 50 kHz, as before. The oscilloscope feature is used in the simulation to plot the output signal. When the amplifier becomes non-linear, the output signal loses its sinusoidal characteristics.

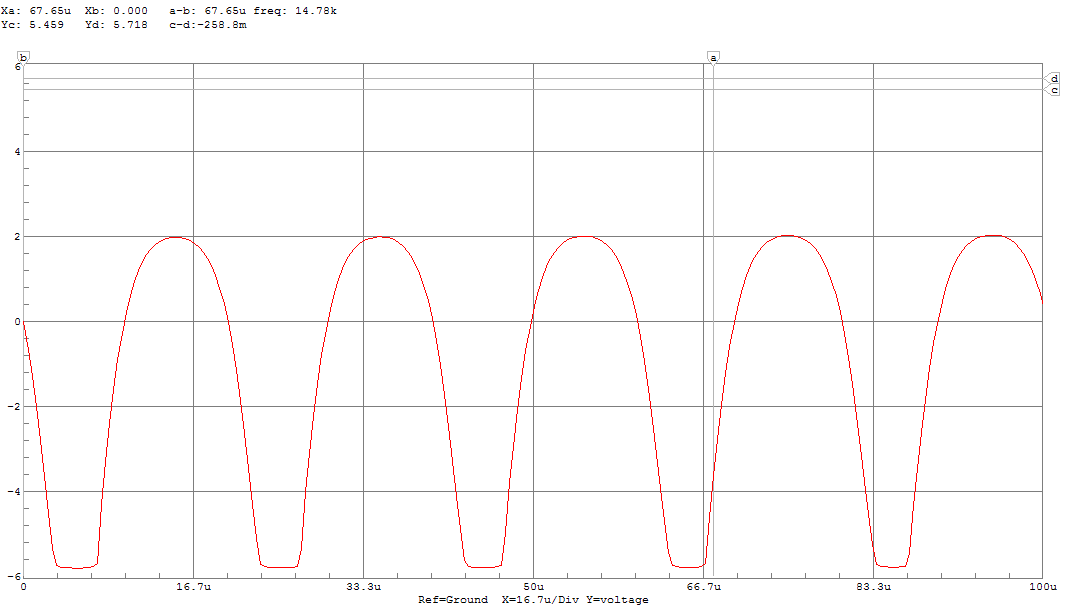
This amplitude was determined to be approximately 38.0 mV. The output signal is plotted below.



For comparison, we generate a plot with a small-signal amplitude of 33 mV, which is 5 mV lower and thus should be more linear.



A plot with a small-signal amplitude of 43 mV is also plotted, which should appear the least linear.

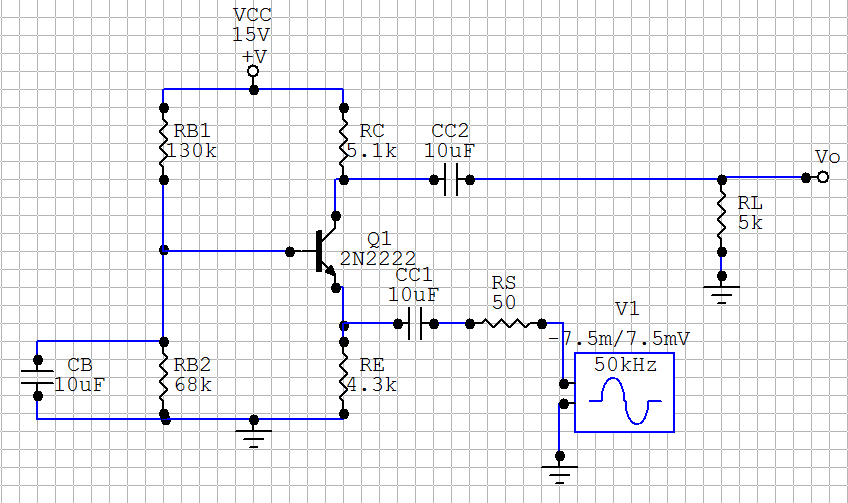


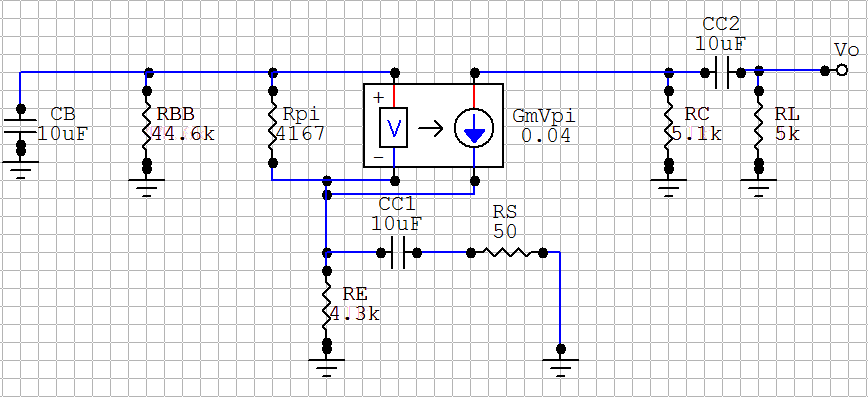
The transistor that gives the best performance is the **2N3904** transistor. It provides the widest midband, so it will be the most forgiving when developing a device in the prototyping stage. From this stage, physical measurements can be made to give us a better sense of the circuit and allow us to maybe choose a transistor providing a narrower midband but higher gain. It could be argued that the 2N2222A will provide more reliable performance at the manufacturing stage, as the circuit was biased to reach the correct DC operating point under the assumption that these were to be used.

# Part III

Using the bias circuit developed earlier, a 2N2222A transistor, and three 10μF capacitors, we simulate the following common base amplifier. We choose an arbitrary load resistance of 5 kΩ.

**a)**

First, the locations of the poles and zeros of this amplifier are calculated. For these calculations, we assume that ro is infinitely large for simplicity. We first examine the low frequency poles and zeros. Below is the low frequency small-signal model of this common base amplifier.



The low frequency pole determined by CC2 is straightforward, as it sees the current sources as independent, and is therefore decoupled from the rest of the circuit.

As we have determined previously, resistances seen by looking from the base to the emitter are magnified by (1+ϐ) while resistances seen by looking from the emitter across to the base are demagnified by (1+ϐ). We expect that the low-frequency pole determined by CC1 will be the dominant low frequency pole, as it will see a demagnified resistances and thus require lower capacitance to reach any given pole location.

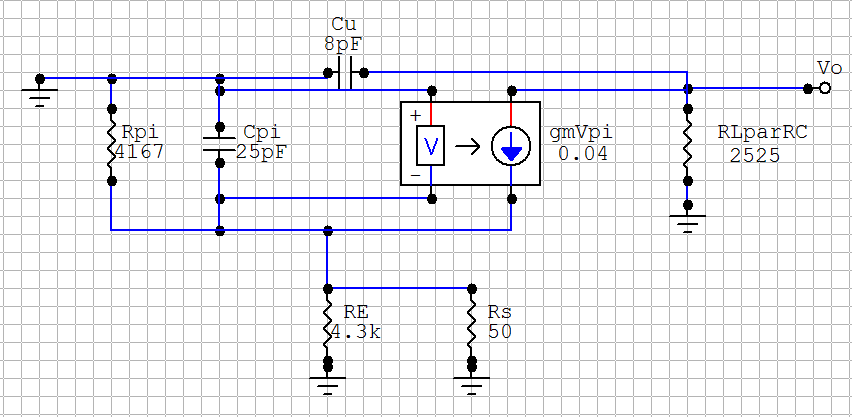
Therefore, we treat CB as a short circuit when analyzing CC1 and we treat CC1 as an open circuit when analyzing CB­.

The low frequency zeros due to the coupling capacitors CC1 and CC2 are equal to zero. For the third value, we need to find a value of CB such that ib­ = 0 when CC1 != 0. This is because when ib = 0, vo  = 0. This will occur when the conductance through the emitter is equal to zero.

Next, the locations of the high frequency poles are calculated. In order to model the high frequency circuit, we need to know the values of cπ and cμ. These are obtained from the datasheet used earlier.

For T = 25C: c­π=25pF and cμ=8pF.

Below is the high frequency small-signal model of our common-base amplifier.

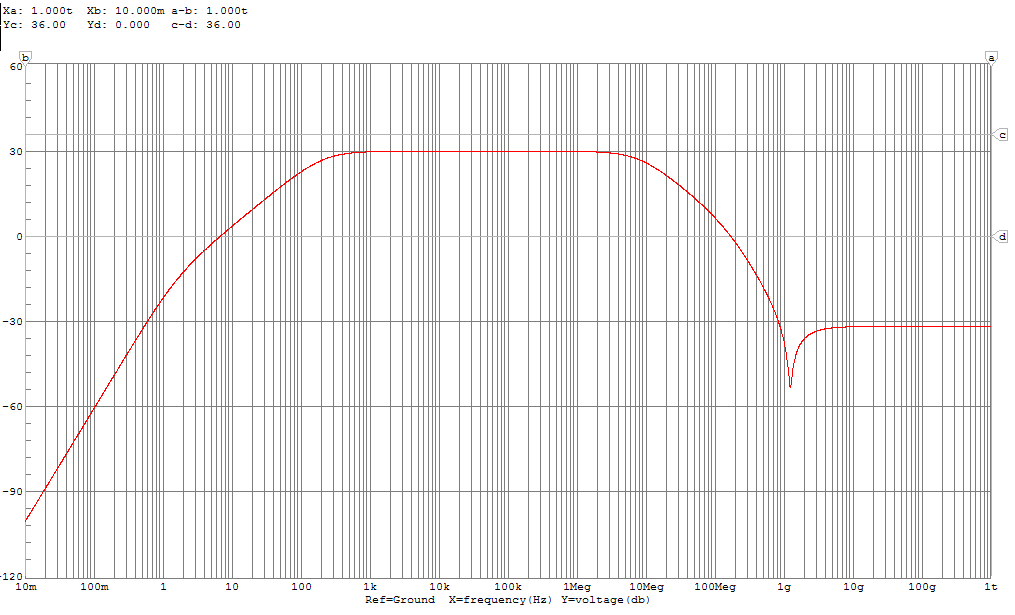
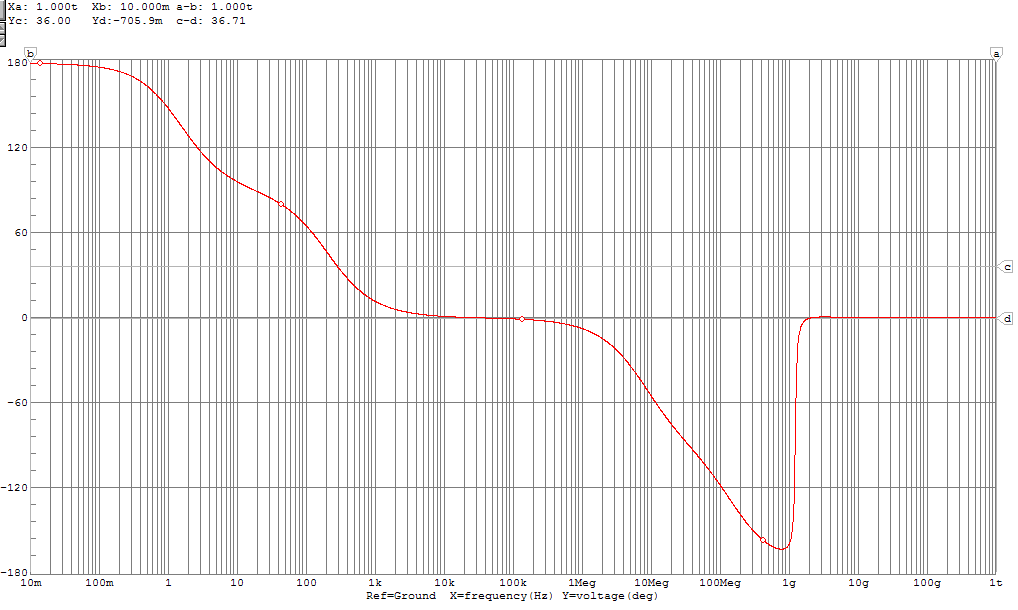


Since cμ is connected to ground on its base side, we can think of it as being in parallel with the load resistance, and thus decoupled from the rest of the circuit. The pole caused by cμ is therefore easy to find.

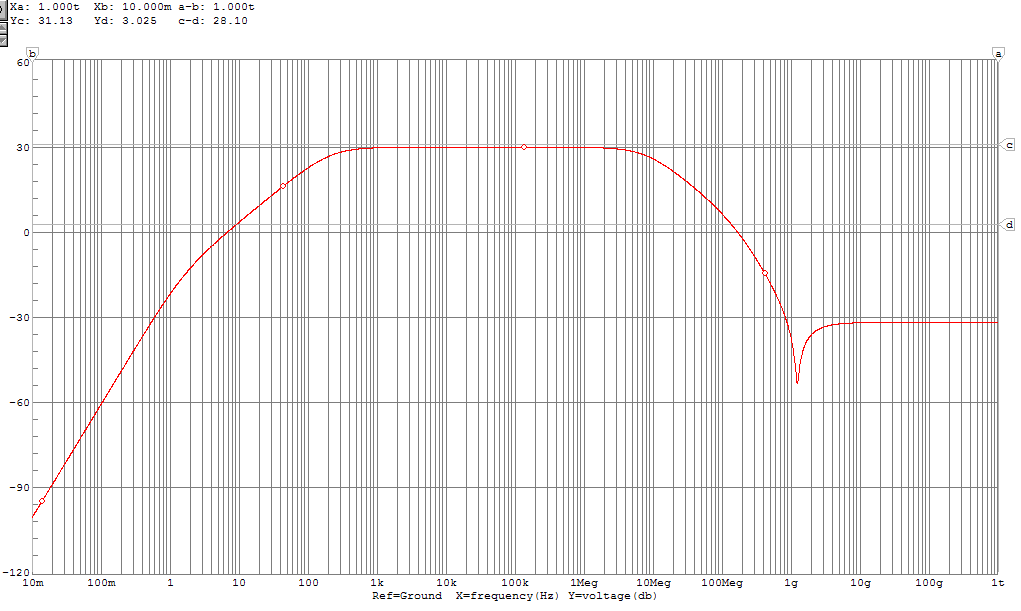
Though rπ is demagnified by 1+ϐ when looking into the emitter, there is no change in cπ. We can therefore calculate the pole cause by cπ as follows.

By approximation we have two high frequency zeros at infinity.

Next, we would like to compare these calculated values with values obtained from simulation generated plots. Bode plots for the magnitude and phase of the output voltage are generated from simulation.



The magnitude Bode plot of the Common-Base amplifier circuit with a 2N2222A is plotted in order to graphically locate the poles.

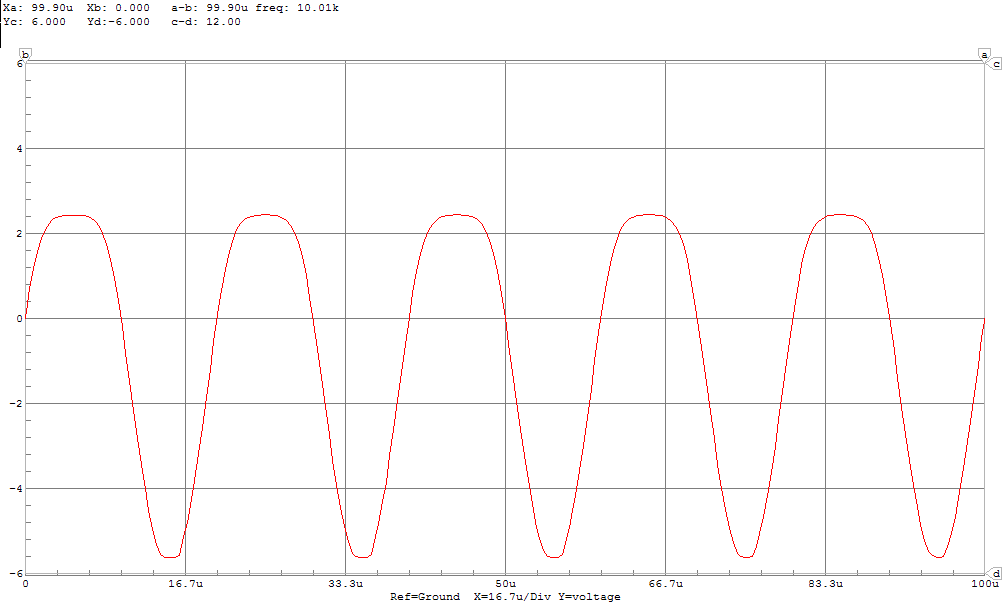


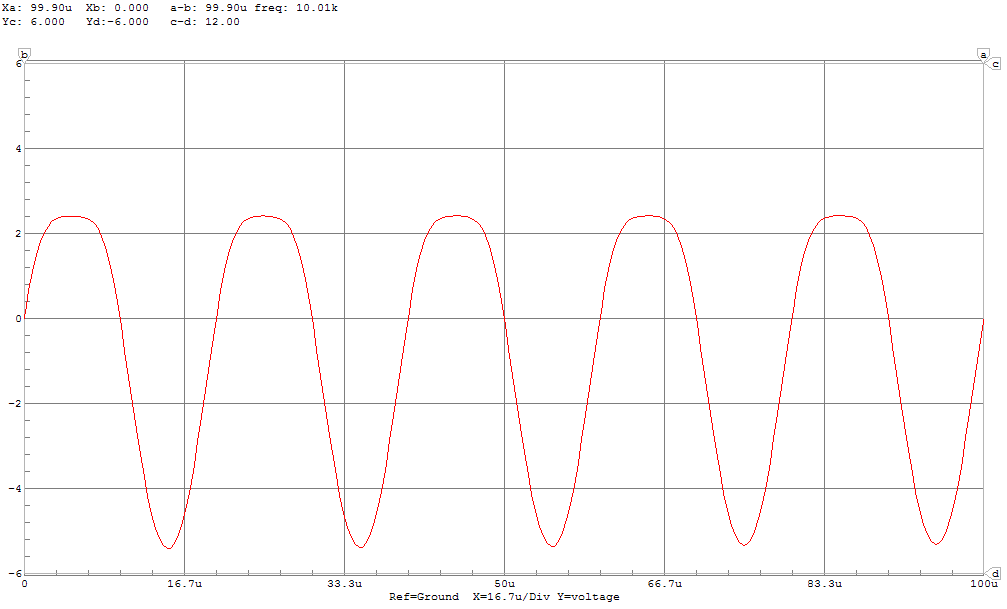
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **ωLP (Hz)** | **ωLZ (Hz)** | **ωHP (MHz)** | **ωHZ (MHz)** |
| **Calculated** | 1.58, 0.38, 212.8 | 0, 0, 0.36 | 7.88, 383.88 | ∞ |
| **Simulated** | 1.7, 210 | 0, 0 | 7, 150, ? | ? |

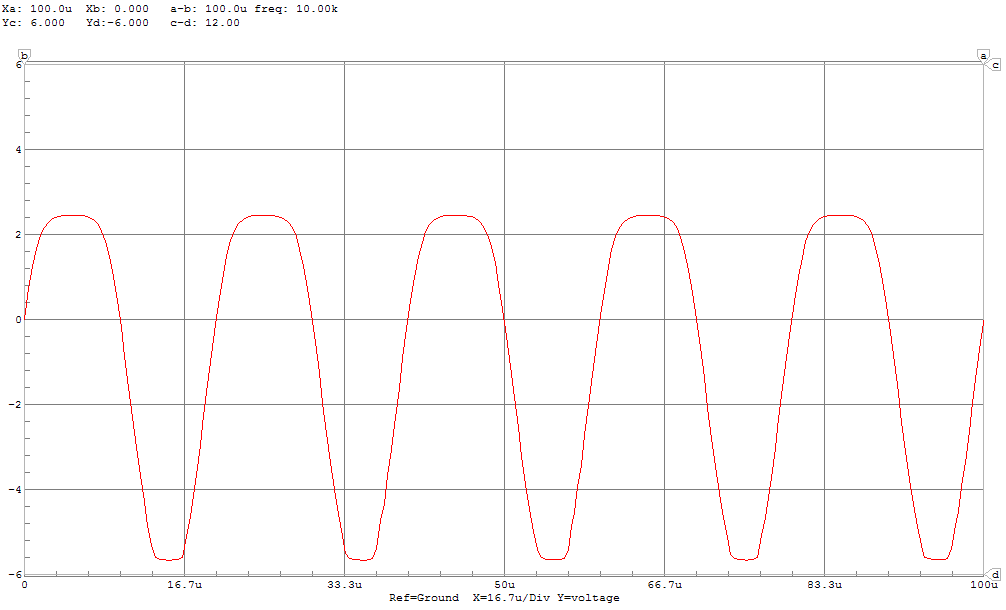
Due to the high-frequency behavior, we are unable to all of extract the high-frequency poles and zeros form the Bode plot. This is okay, because we won’t be working at frequencies as high as 1 GHz. One of the low frequencies poles and one of the low frequency zeros cannot be discriminated due to their close proximity. Their changes to the Bode plot effectively cancel each other out.

**b)** We pick our midband frequency to be 50 kHz by consulting the magnitude bode plot and choosing a frequency unambiguous located on the midband plateau. We set this as the frequency of our small-signal generator, and vary its amplitude. The oscilloscope feature is used in the simulation to plot the output signal. When the amplifier becomes non-linear, the output signal loses its sinusoidal characteristics.

This amplitude was determined to be approximately 150 mV. The output signal is plotted below.

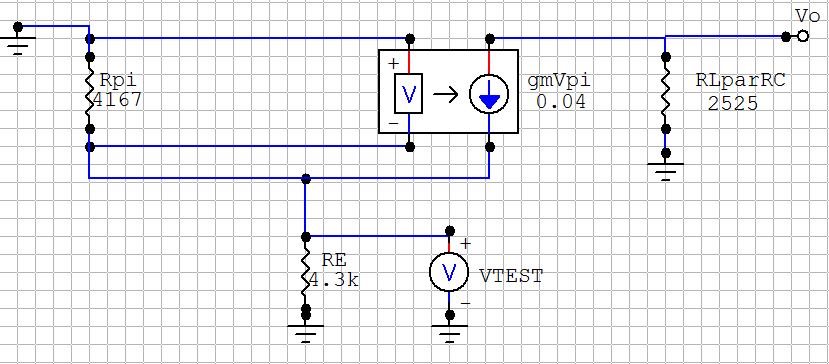


For comparison, we generate a plot with a small-signal amplitude of 140 mV, which is 10 mV lower and thus should be more linear.

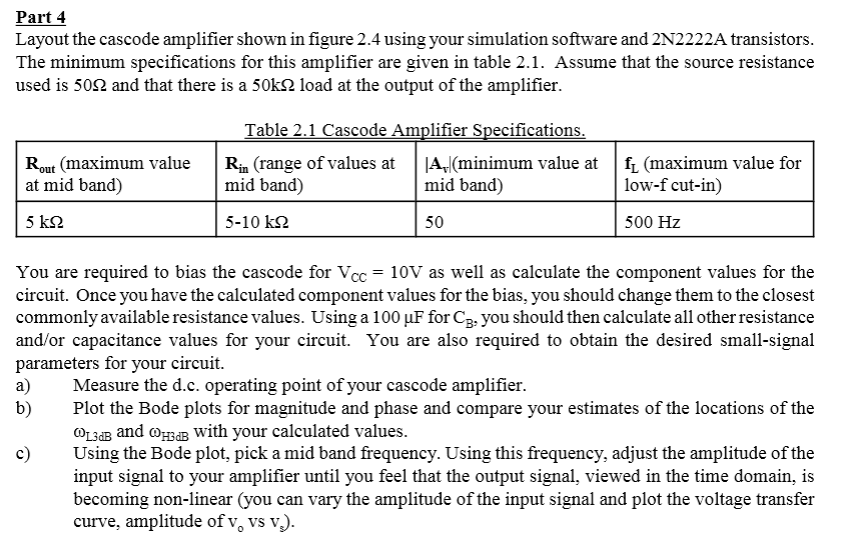
A plot with a small-signal amplitude of 160 mV is also generated. This should appear to be the least linear.

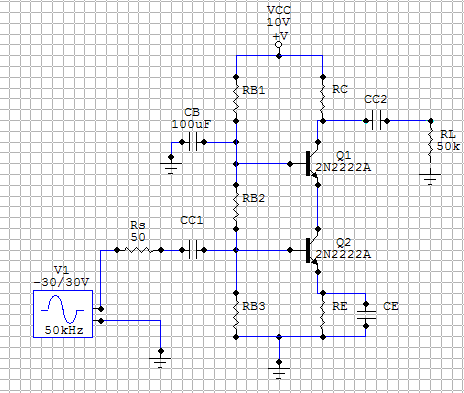
**c)** In order to measure input impedance at midband, the oscilloscope is used to obtain peak voltage and current at the input terminal of the amplifier.

We use the small-signal model of the amplifier at mid band, with the source impedance omitted, in order to calculate the input impedance.



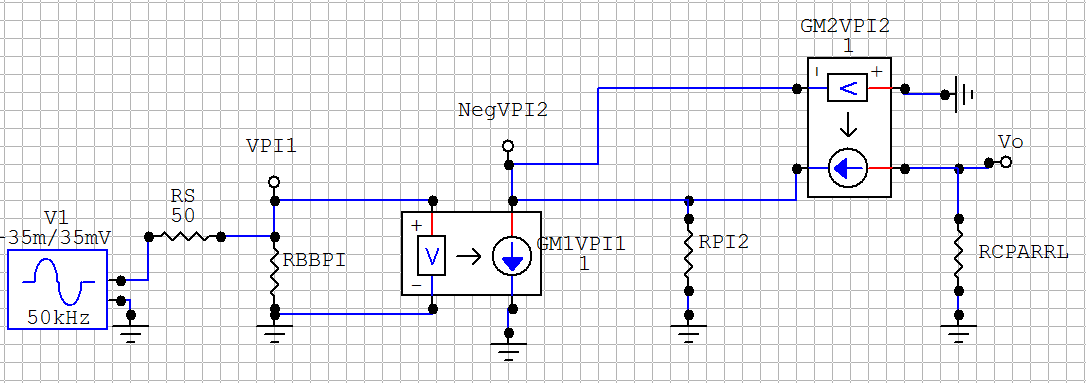
# Part 4



Here is the complete cascode circuit:

Our first step is to find the values of the bias resistors. We must design the circuit to fit the problem specifications. By using these in conjunction with a ¼ rule, we can ensure active mode operation.

The ¼ rule provides relationships between the bias resistances that are likely to provide a good amplifier. First though, we must ensure that the resistances we pick meet the requirements. These will provide bounds on our bias resistances. To find these relationships, we examine the mid-band hybrid-pi model of the circuit.



Output impedance is found first. This value is specified as a maximum value of 5kΩ at midband. From the mid-band hybrid-pi model at mid-band we see that the voltage at the output stage has no effect on the dependent current source. Therefore, we can treat the output stage to be decoupled from the rest of the circuit such that the load only sees RC.

To simplify further computation, we first establish a relationship between vπ1 and vπ2.

from our arrangement of transistors, we can now say that

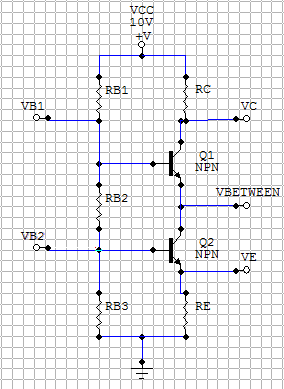
We next establish a relationship for mid-band gain to ensure that it is greater in magnitude than our specified minimum gain. From the midband small signal model we see that:

We now perform some algebraic manipulation to simplify the problem.

we can say that Therefore:

We now have a range for RC. We choose a value at the high end of this range in order to limit IC and maximize input impedance, then use our ¼ rule to complete biasing the amplifier.

Here is our bias circuit:

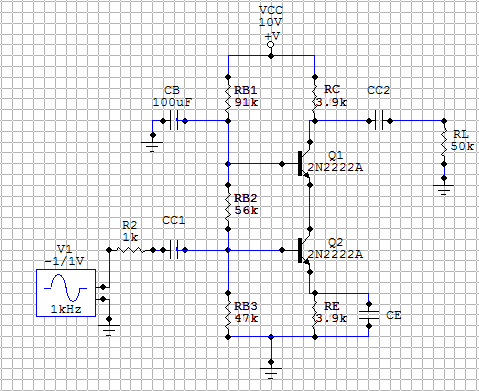
Our ¼ rule states:

With these values known, and the knowledge that VB = VE + 0.7, we can extrapolate further circuit parameters.

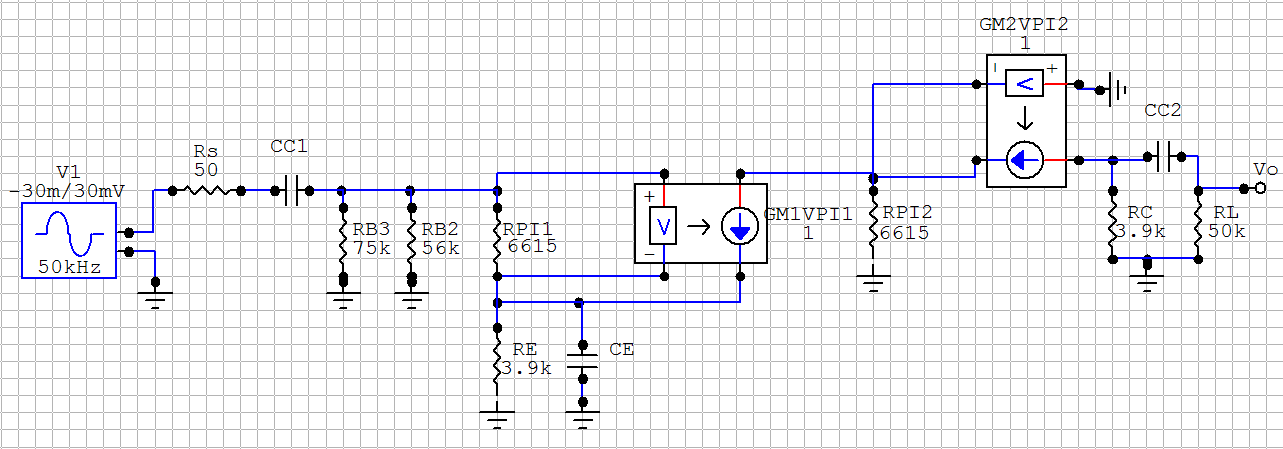
With this knowledge, we can find the values of all bias resistors. First we choose a standard desired value for IE, 1 mA.

Now, we can use this knowledge to establish all of the bias resistances.

With consultation from, <http://ecee.colorado.edu/~mcclurel/resistorsandcaps.pdf>, we replace these calculated resistances with commonly available resistors.

We place these resistance values into our full cascode model.

The next step is to find the unknown capacitance values. Since we are given the maximum value for the low-frequency cutoff frequency we can find a range for the capacitor of the dominant pole, then select it and the other coupling capacitors accordingly. In order to find these time constants, we need the low frequency hybrid-pi model. We treat CB simply as a short circuit to ground, as we know that it is a very large capacitance and will not be responsible for the dominant low-frequency pole.

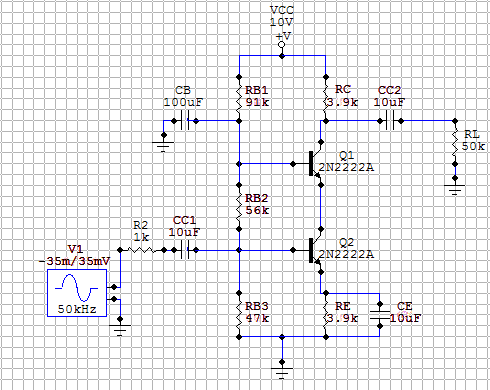


Since CE sees a demagnified resistance, most likely it will require a very high capacitance if it is not the capacitor responsible for the dominant pole. Therefore, the open circuit time constant of CE is taken, and limited as to provide a dominant low-frequency pole within the specified range. First, rπ1 is calculated, as IB for the first transistor is known.

We can now calculate the short-circuit time constant for CE.

The pole responsible caused by CE is now computed to ensure that it falls in the required specification.

A value of CE = 10μF is chosen conservatively and to simplify calculations. CC1 and CC2 can be the same, as their apparent resistances are higher and thus will conduct first and be non-dominant low-frequency poles.

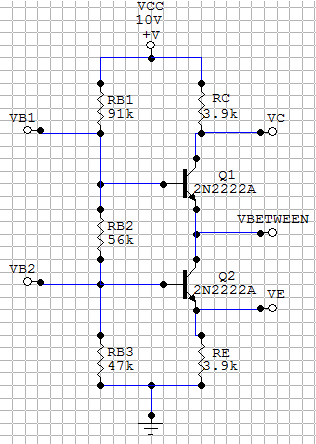
The final, full cascode model follows.

We have already proven that the requirements are met for R­out, Av, and fL. We would like to confirm that the requirements are also met for Rin. It is clear from the midband hybrid-pi model that the input stage is decoupled from the rest of the circuit such that the source only sees R­­BBπ:

This must be in the range between 5-10 kΩ at midband. As we can see, our values satisfy this requirement.

Now that our cascode amplifier has been developed, we continue with the rest of the problem.

**a)**

The bias circuit is simulated in order to obtain the DC operating point.

From the multimeter feature:

IC1 = 0.42 mA

IC2 = 0.43 mA

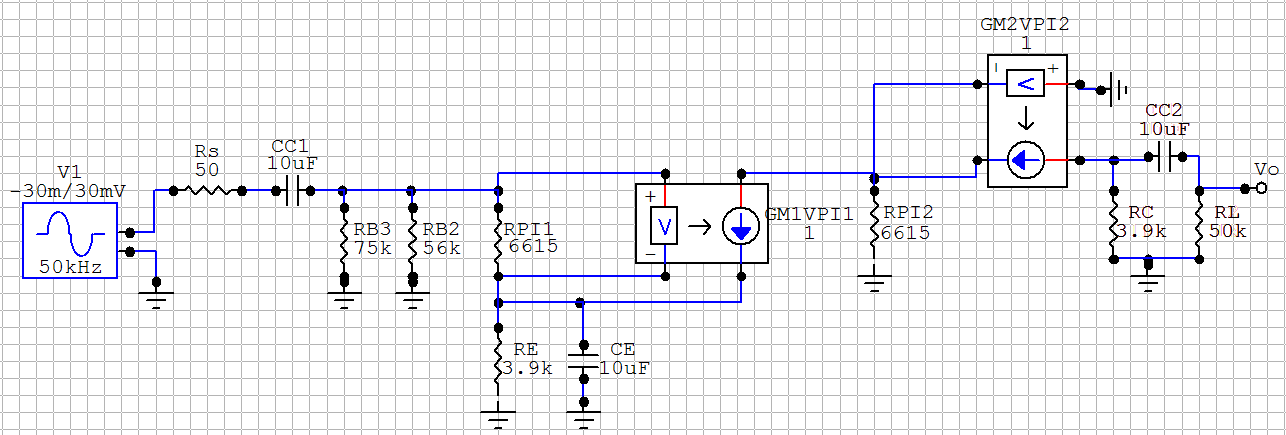
V­CE1 = 8.343 – 4.530 = 3.81 V

VCE2 = 4.530 – 1.679 = 2.85 V

VBE1 = 5.109 – 4.530 = 0.58 V

VBE2 = 2.258 – 1.679 = 0.58 V

**b)** First, estimates for ω3dBL and ω3dBH are calculated. We do this by calculating an estimate for all poles and zeros, then using the quadratic equation. The low frequency poles are examined first. For this, we use the low frequency Hybrid-Pi model.



We already know that our dominant pole, determined by CE is

The low-frequency pole determined by CC2 is straightforward.

With the magnifying effect in mind, we can easily find the low-frequency pole determined by CC1 – considering CE to be an open circuit.

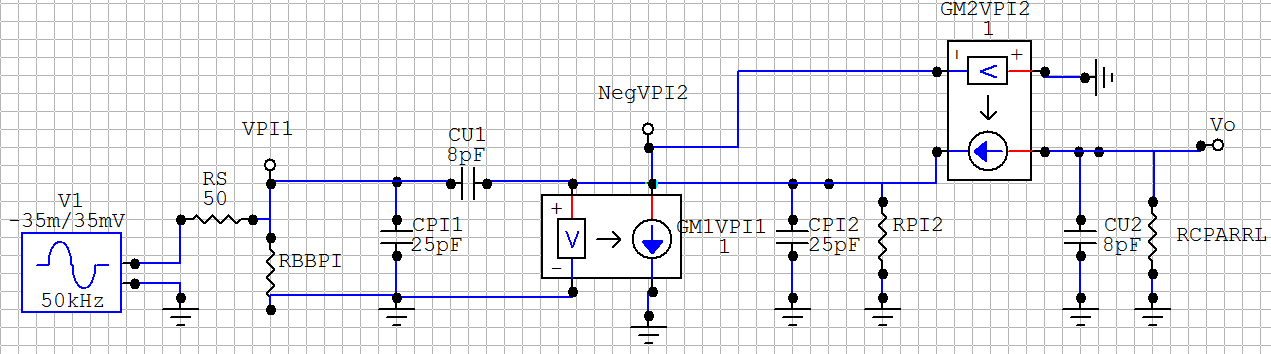
We expect the pole generated by CB to be so low that it has a negligible effect on ω3dBL, therefore we ignore it.

CC1, CC2, and CB will have zeros at zero. CE however, will be responsible for a zero when the admittance of the first emitter network equals zero.

We now estimate ω3dBL as follows:

Now we examine the high frequency poles and zeros. For this, the high-frequency hybrid-pi model is used. In order to model the high frequency circuit, we need to know the values of cπ and cμ. These are obtained from the datasheet used earlier.

For T = 25C: c­π=25pF and cμ=8pF.

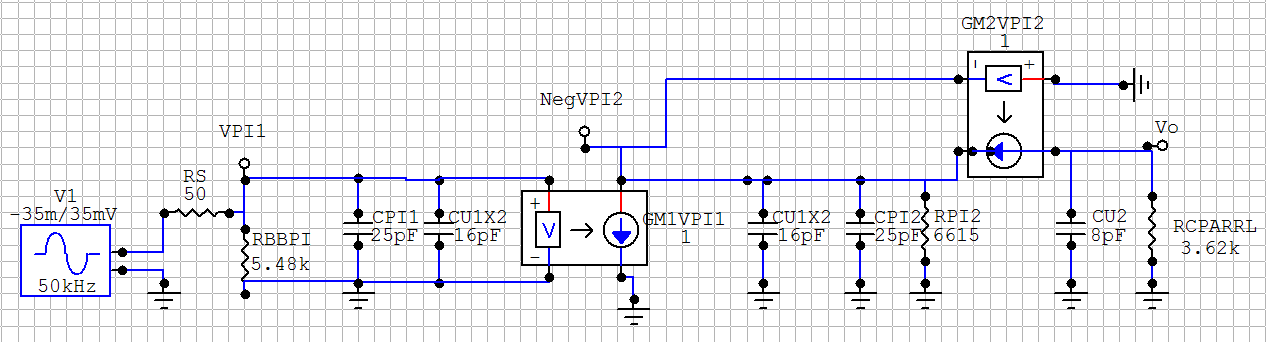


Miller’s theorem is used across C­μ1. This will split up the high-frequency hybrid-pi model into three, single capacitor, decoupled circuits. Once this approximation is complete, location of the poles is trivial.

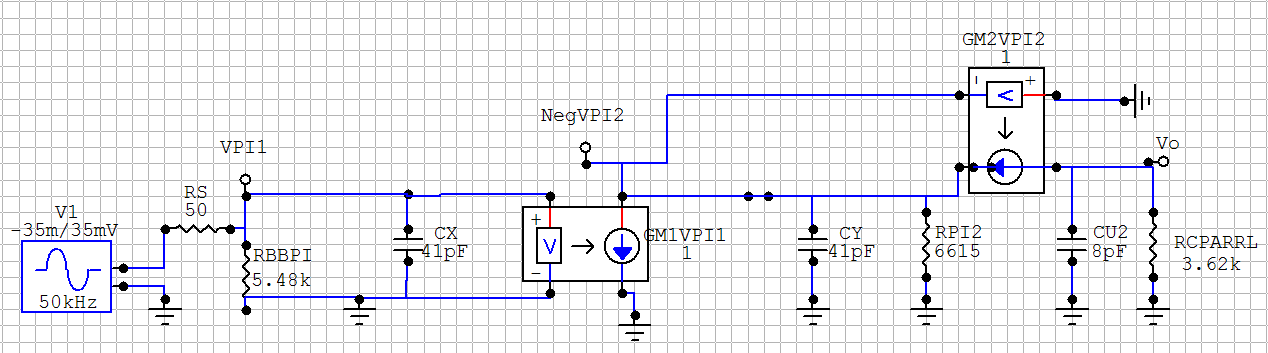
As established earlier:

This implies a Miller Gain k = -1, as vπ1 terminates at ground while vπ2 originates at ground. By using the following equations, we are able to simplify the circuit.

This allows us to build the following equivalent three decoupled circuits:



Which can be simplified to:

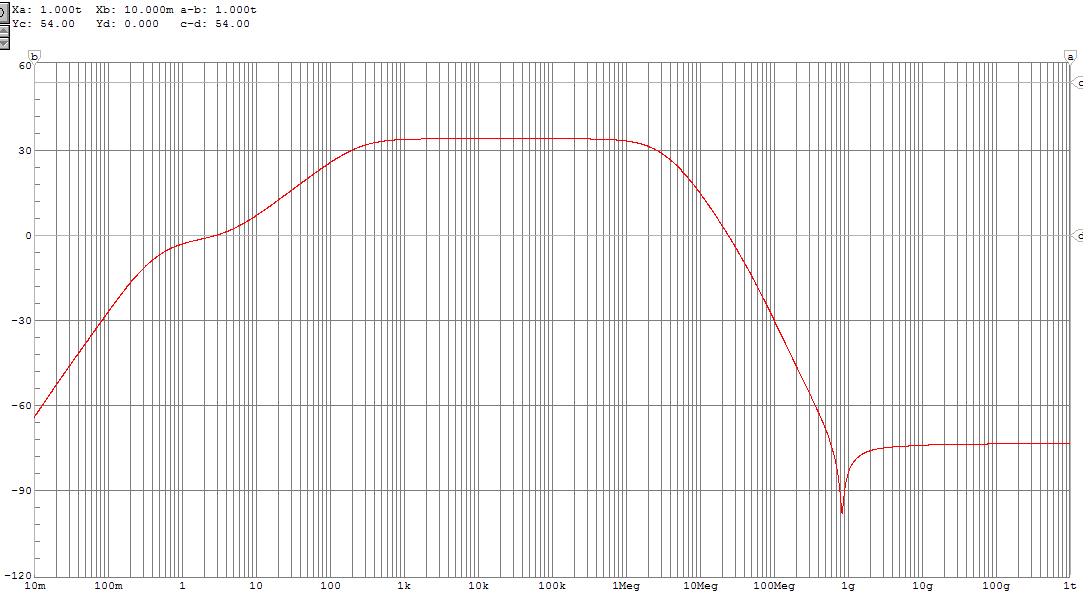


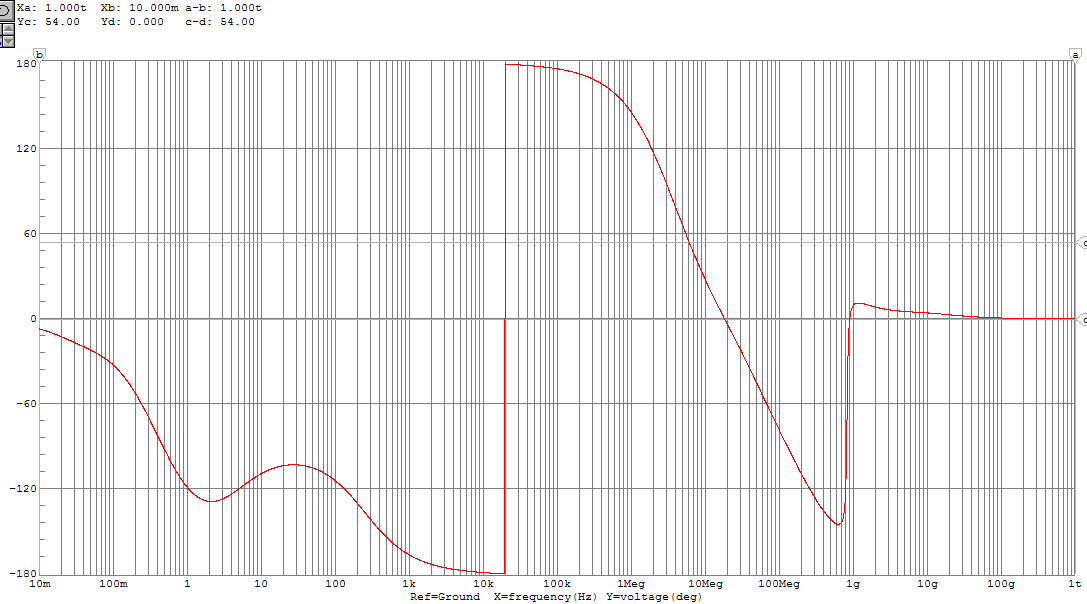
The high-frequency poles generated by CX and Cμ are straightforward to calculate.

For the pole generated by CY, it must be observed that due to the current source rπ2­ is demagnified by 1+ϐ. It can now be calculated.

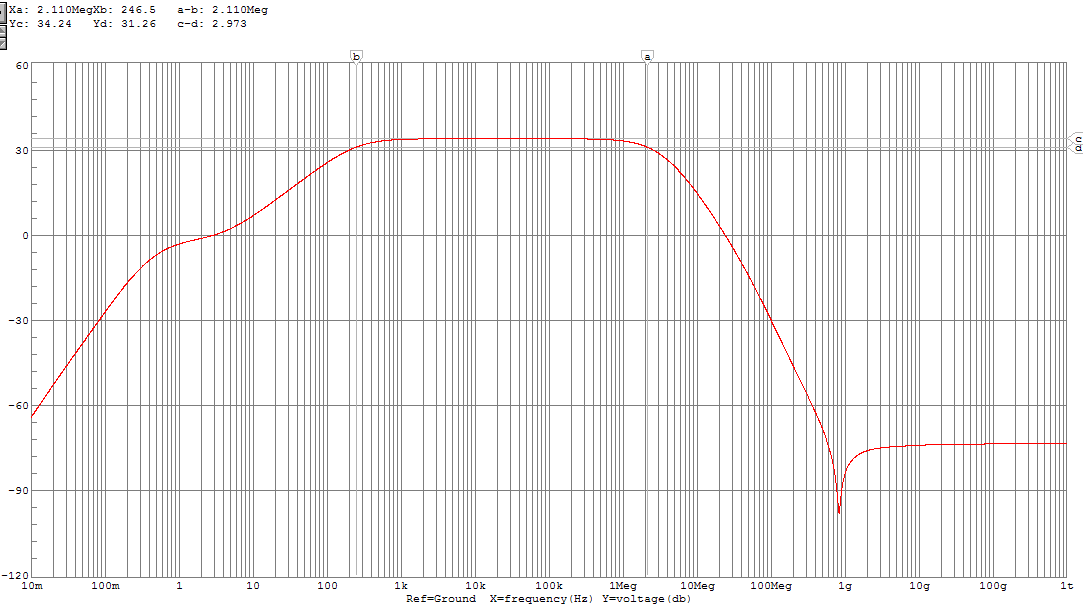
We now estimate ω3dBH as follows:

The cascode amplifier is now simulated to find values for comparison. Below are the magnitude and phase bode plots.





We examine the magnitude bode plot to graphically estimate the 3dB frequencies. One horizontal probe is place along the midband gain, while the other is placed 3dB below this. The points at which this second line intersects with the transfer function corresponds to the 3dB frequencies.

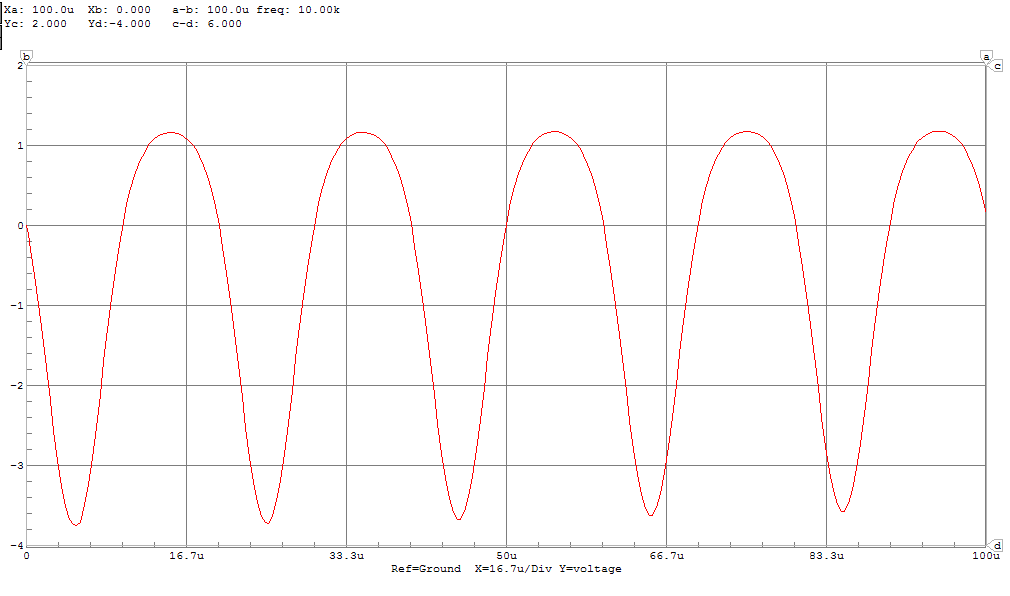


Here is a summary of part b:

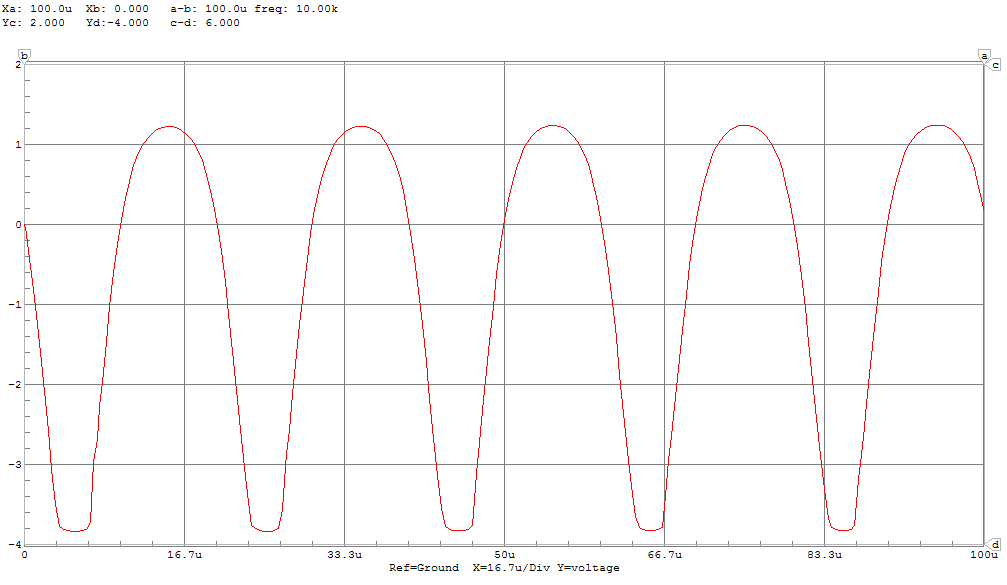
|  |  |  |
| --- | --- | --- |
|  | **ω3dBL (Hz)** | **ω3dbH(Hz)** |
| **Calculated** | 404.5 | 5.47M |
| **Simulated** | 246.5 | 2.11M |

**c)** We pick our midband frequency to be 50 kHz by consulting the magnitude bode plot and choosing a frequency unambiguous located on the midband plateau. We set this as the frequency of our small-signal generator, and vary its amplitude. The oscilloscope feature is used in the simulation to plot the output signal. When the amplifier becomes non-linear, the output signal loses its sinusoidal characteristics.

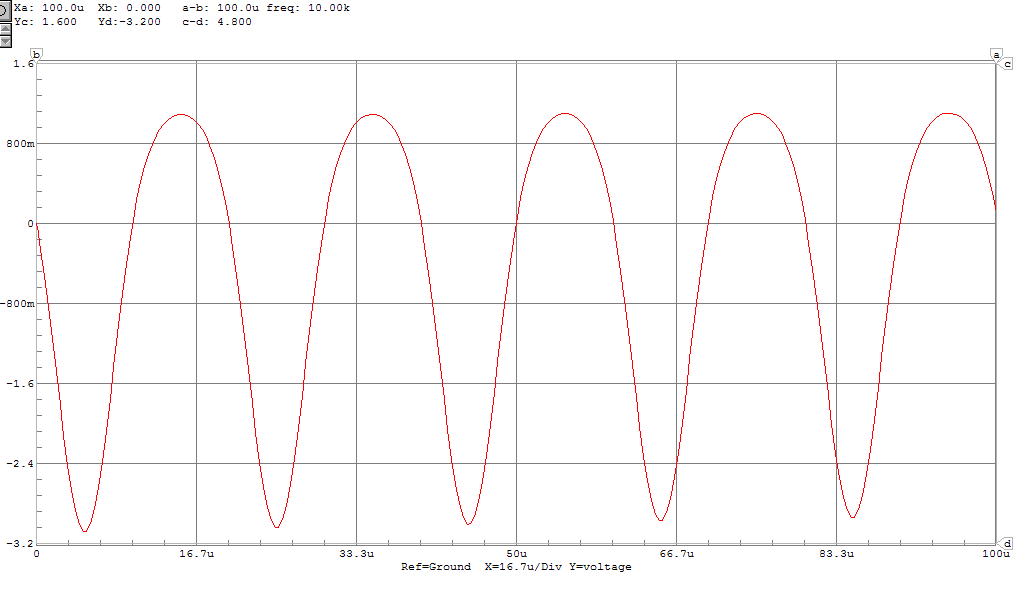
This amplitude was determined to be approximately 40 mV. The output signal is plotted below.



For comparison, the output signal was also plotted at 45 mV. As expected, this appears non-linear.



The output signal was also plotted at 35 mV. As expected, this appears the most linear.



**d)** In order to measure input impedance at midband, the oscilloscope is used to obtain peak voltage and current at the input terminal of the amplifier.

From our process in biasing the transistor, we determined the input impedance at midband.

Excluding the source resistor, we have:

Which is very close to what we see in simulation.

**e)**

2N3904

Parts b) and c) are now repeated for the 2N3904 transistor. We use the same bias circuit as for the 2N2222A transistor.

b)

Since we are using the same circuit, the same equations that we derived when using the 2N2222A transistor are used for the high and low frequency poles. As determined in Part 1: ϐ for this transistor is equal to 117.6. Therefore:

We now have enough information to calculate the low-frequency poles and zeros.

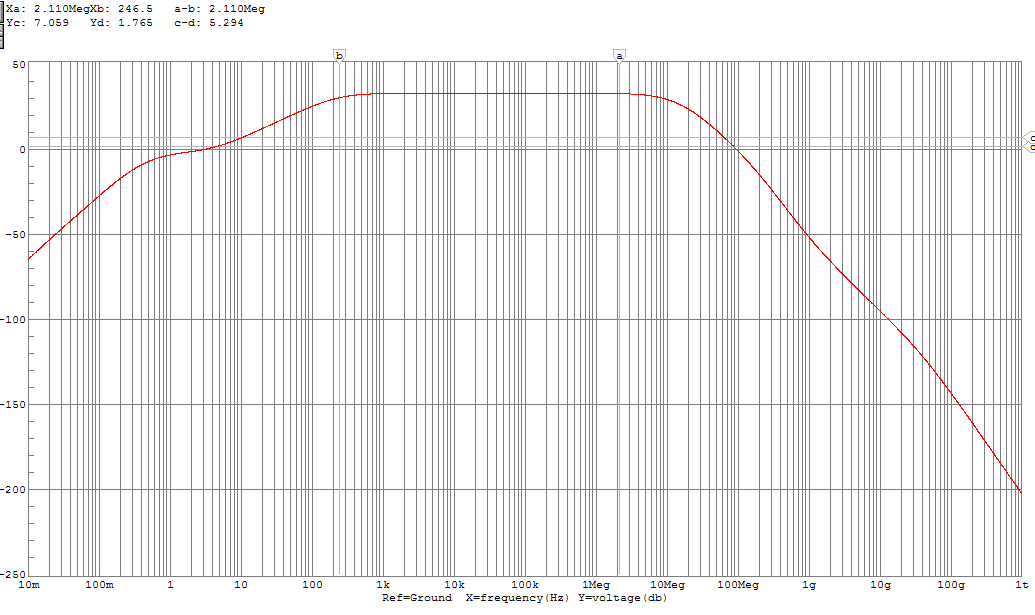
We now estimate ω3dBL as follows:

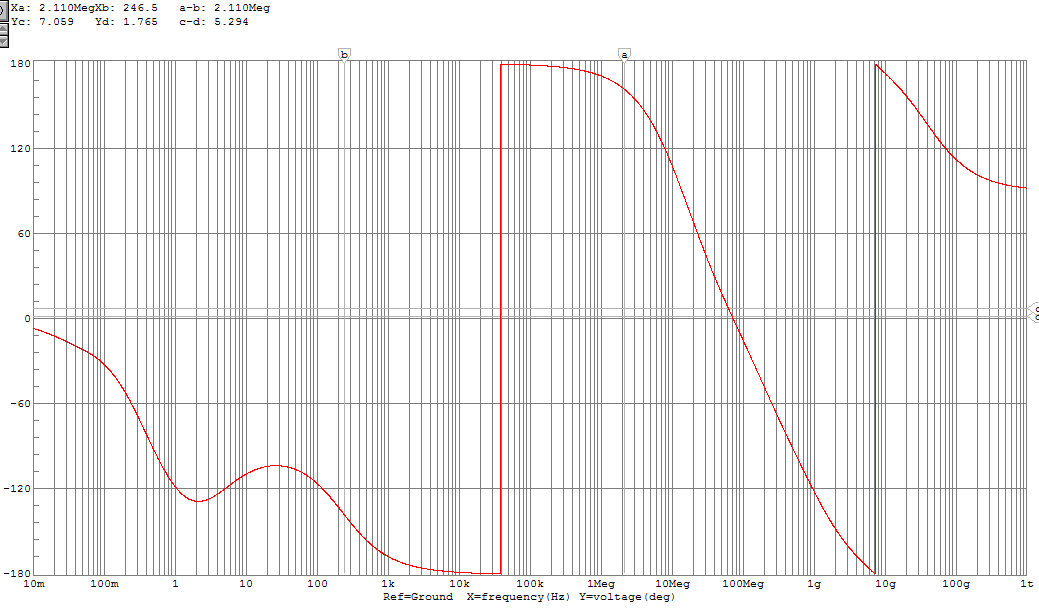
Which, as expected, is nearly indistinguishable from the circuit with the 2N2222A transistor. Now we examine the high frequency poles and zeros. In order to use the equations derived earlier, we need to know the values of cπ and cμ for the 2N3904 transistor. These are obtained from the datasheet used earlier.

For T = 25C: cπ = 18 pF, cμ= 4 pF

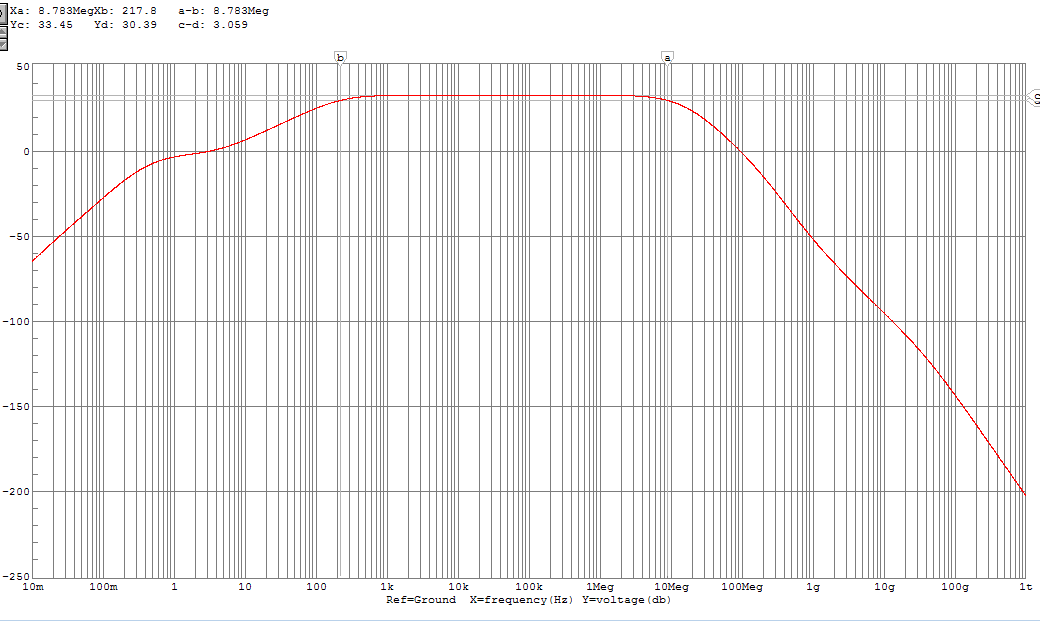
We now estimate ω3dBH as follows:

The cascode amplifier with 2N3904 transistors is now simulated to find values for comparison. Below are the magnitude and phase bode plots.





We examine the magnitude bode plot to graphically estimate the 3dB frequencies. One horizontal probe is place along the midband gain, while the other is placed 3dB below this. The points at which this second line intersects with the transfer function corresponds to the 3dB frequencies.

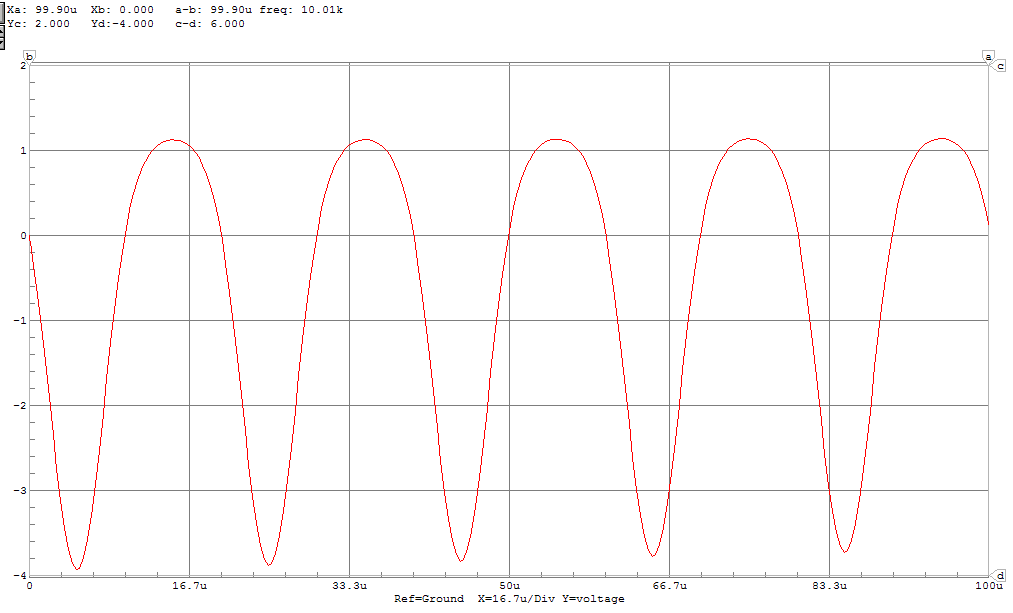


Here is a summary of part b:

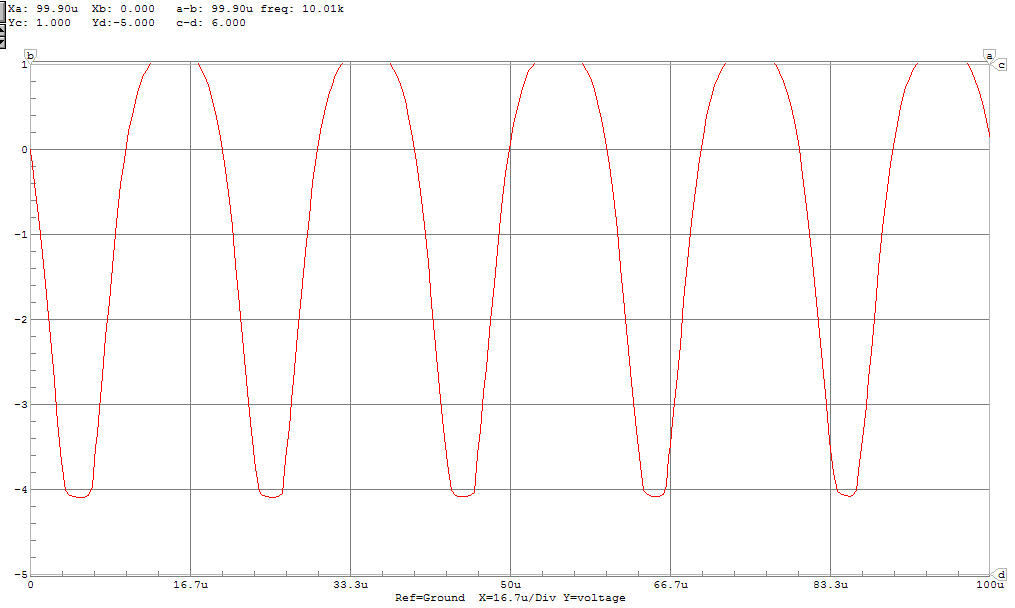
|  |  |  |
| --- | --- | --- |
|  | **ω3dBL (Hz)** | **ω3dbH(Hz)** |
| **Calculated** | 404.21 | 10.93M |
| **Simulated** | 217.8 | 8.78M |

c)We pick our midband frequency to be 50 kHz by consulting the magnitude bode plot and choosing a frequency unambiguous located on the midband plateau. We set this as the frequency of our small-signal generator, and vary its amplitude. The oscilloscope feature is used in the simulation to plot the output signal. When the amplifier becomes non-linear, the output signal loses its sinusoidal characteristics.

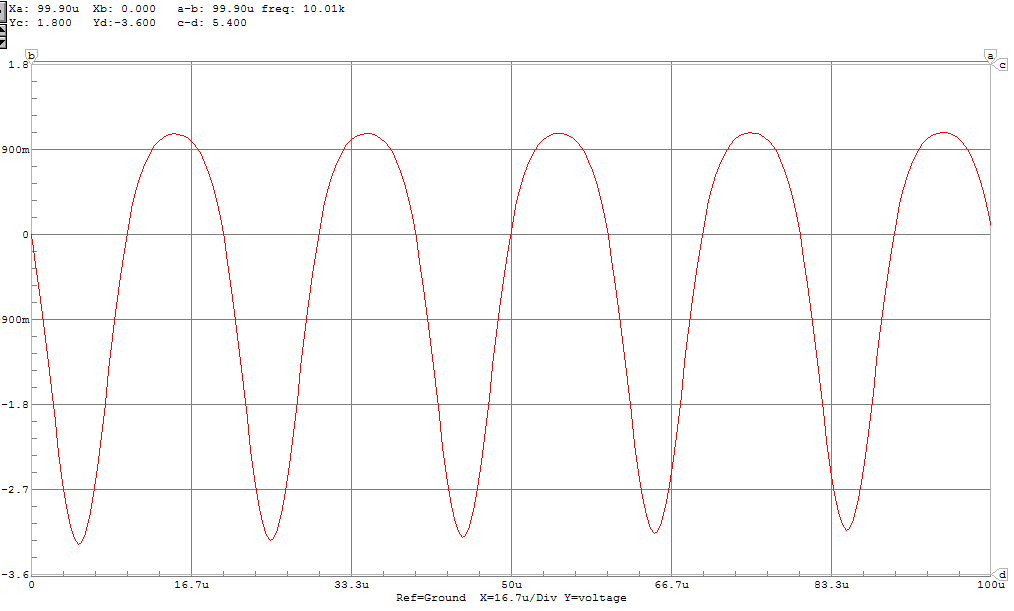
This amplitude was determined to be approximately 45 mV. The output signal is plotted below.



For comparison, the output signal was also plotted at 50 mV. As expected, this appears non-linear.



The output signal was also plotted at 40 mV. As expected, this appears the most linear.



2N4401

Parts b) and c) are now repeated for the 2N4401 transistor. We use the same bias circuit as for the 2N2222A transistor.

b)

Since we are using the same circuit, the same equations that we derived when using the 2N2222A transistor are used for the high and low frequency poles. As determined in Part 1: ϐ for this transistor is equal to 142.9. Therefore:

We now have enough information to calculate the low-frequency poles and zeros.

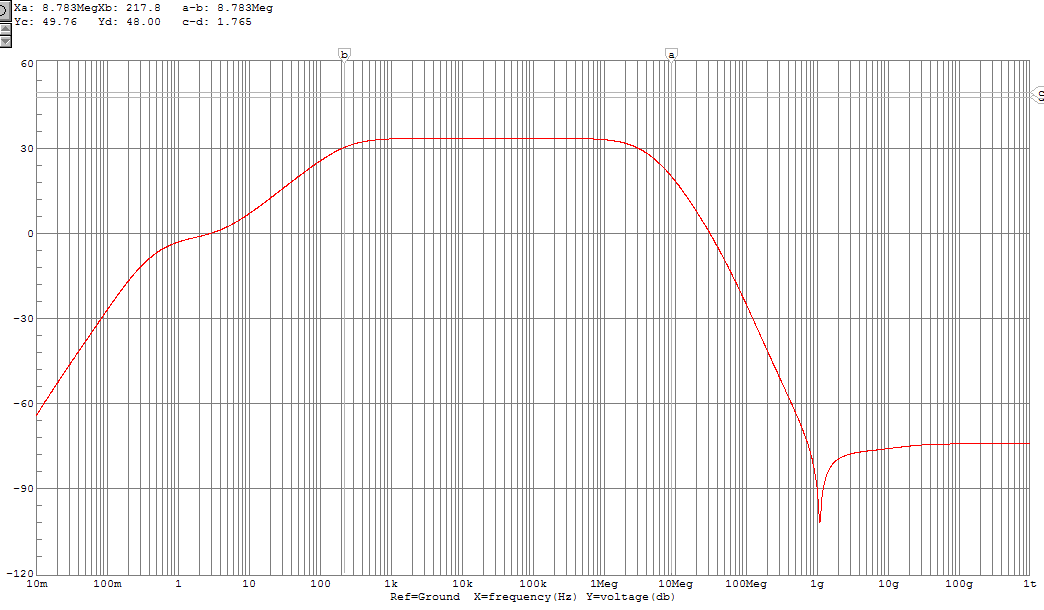
We now estimate ω3dBL as follows:

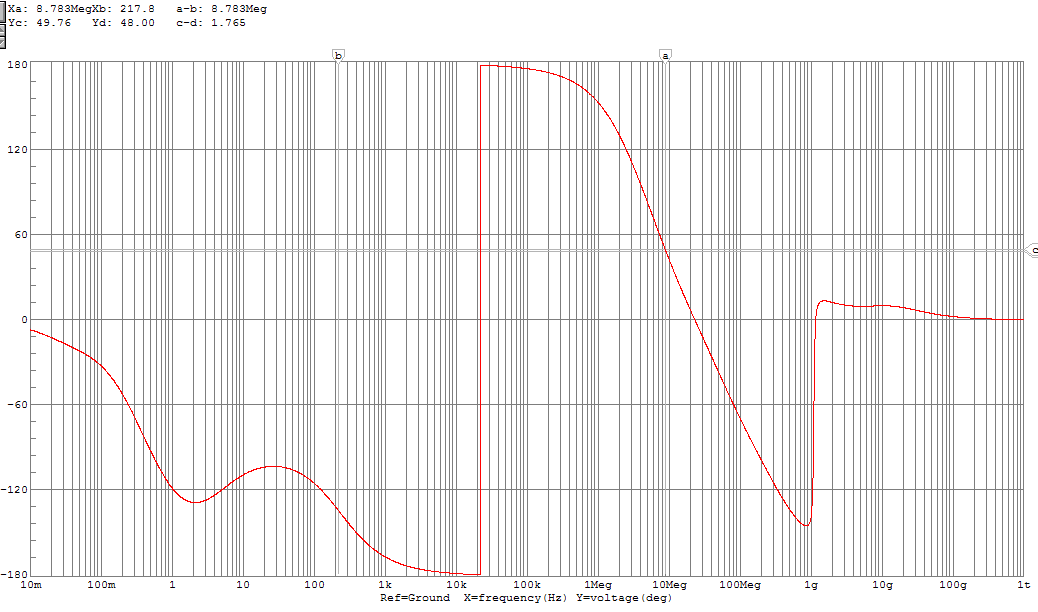
Which, as expected, is nearly indistinguishable from the circuit with the 2N2222A on the 2N3904 transistor. Now we examine the high frequency poles and zeros. In order to use the equations derived earlier, we need to know the values of cπ and cμ for the 2N4401 transistor. These are obtained from the datasheet used earlier.

For T = 25C: cπ = 30 pF, cμ= 6.5 pF

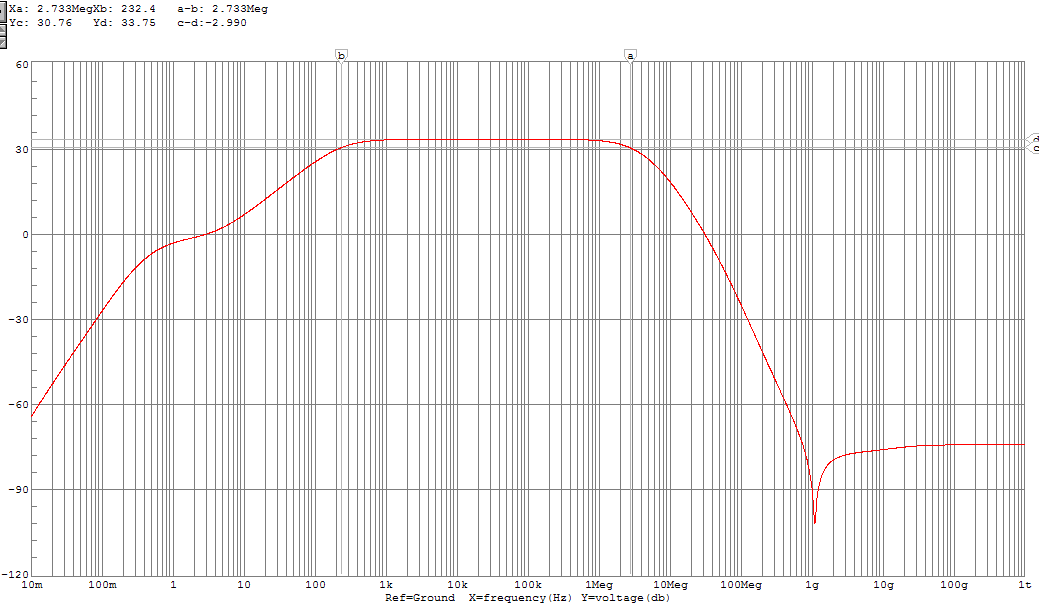
We now estimate ω3dBH as follows:

The cascode amplifier with 2N4401 transistors is now simulated to find values for comparison. Below are the magnitude and phase bode plots.





We examine the magnitude bode plot to graphically estimate the 3dB frequencies. One horizontal probe is place along the midband gain, while the other is placed 3dB below this. The points at which this second line intersects with the transfer function corresponds to the 3dB frequencies.

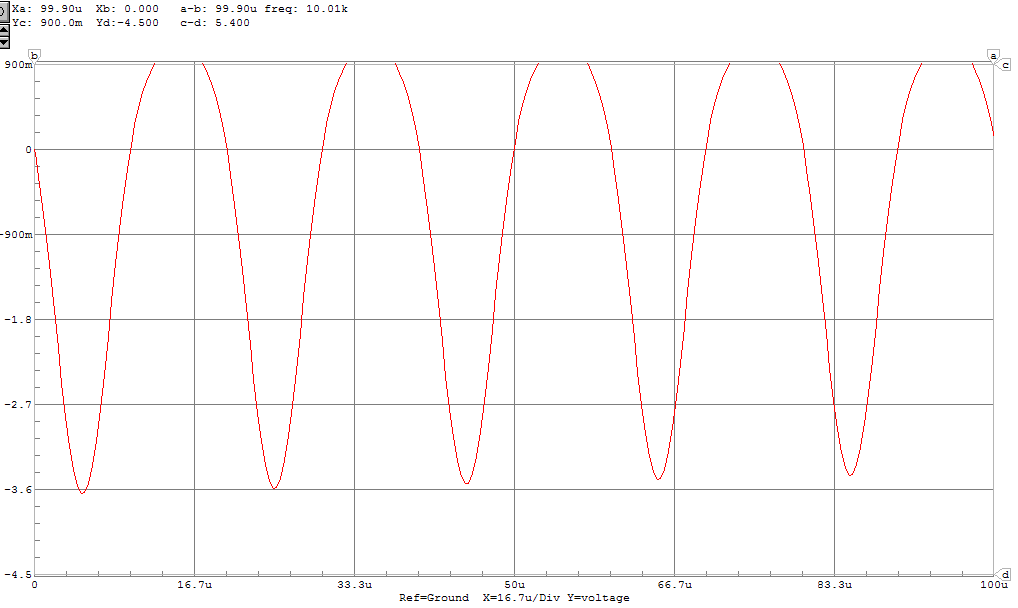


Here is a summary of part b:

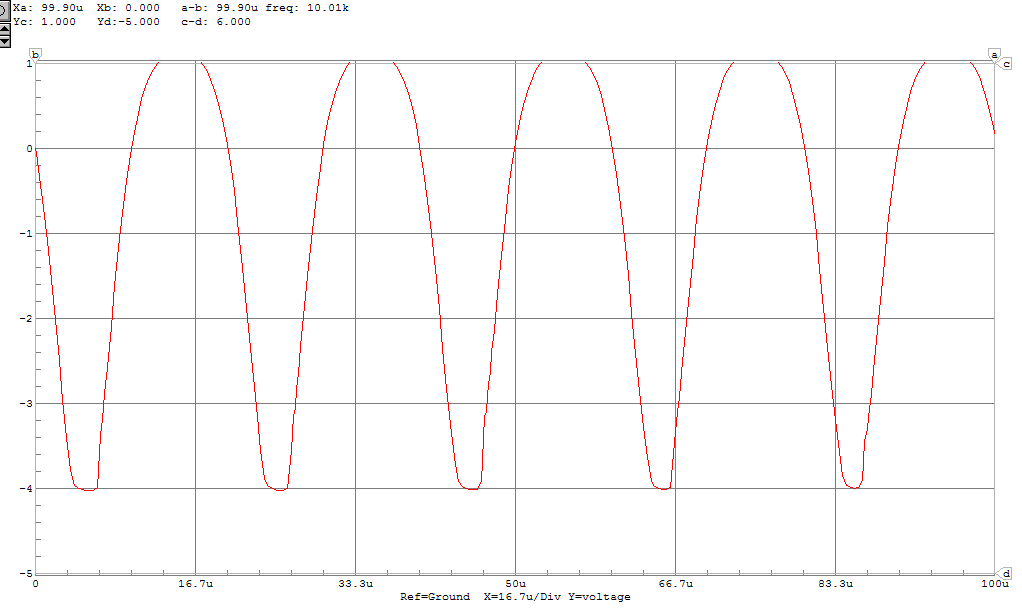
|  |  |  |
| --- | --- | --- |
|  | **ω3dBL (Hz)** | **ω3dbH(Hz)** |
| **Calculated** | 404.21 | 6.72M |
| **Simulated** | 232.4 | 2.73M |

c)We pick our midband frequency to be 50 kHz by consulting the magnitude bode plot and choosing a frequency unambiguous located on the midband plateau. We set this as the frequency of our small-signal generator, and vary its amplitude. The oscilloscope feature is used in the simulation to plot the output signal. When the amplifier becomes non-linear, the output signal loses its sinusoidal characteristics.

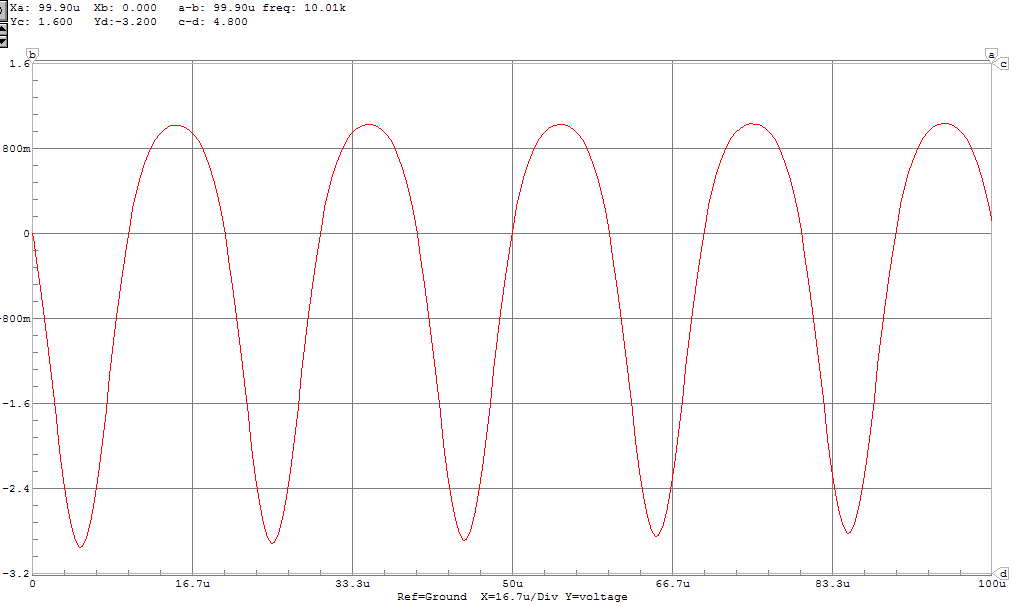
This amplitude was determined to be approximately 40 mV. The output signal is plotted below.



For comparison, the output signal was also plotted at 45 mV. As expected, this appears non-linear.



The output signal was also plotted at 35 mV. As expected, this appears the most linear.



In this cascode amplifier, the **2N2222A** tra­­­­nsistor gives the best performance.

The 2N3904 transistor is immediately eliminated, due to the fact that in this circuit it does not meet input impedance specifications. This is because input impedance is always less than rπ, and for the 2N3904 cascode amplifier circuit rπ = 4.67kΩ which is less than the specified input impedance at midband of 5-10kΩ.

From simulation, it can also be seen that the cascode circuit consisting of 2N4401 transistors also does not meet input impedance specifications. This is an expected result, as we initially biased our circuit with the assumption of using 2N2222A transistors.