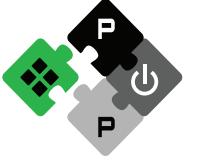


OpenPiton + Ariane   :

The First Open-Source SMP Linux-booting RISC-V System Scaling From One to Many Cores

Jonathan Balkind, Michael Schaffner, Katie Lim, Florian Zaruba, Fei Gao,
Jinzheng Tu, Luca Benini, David Wentzlaff

Princeton University, ETH Zurich

openpiton.org

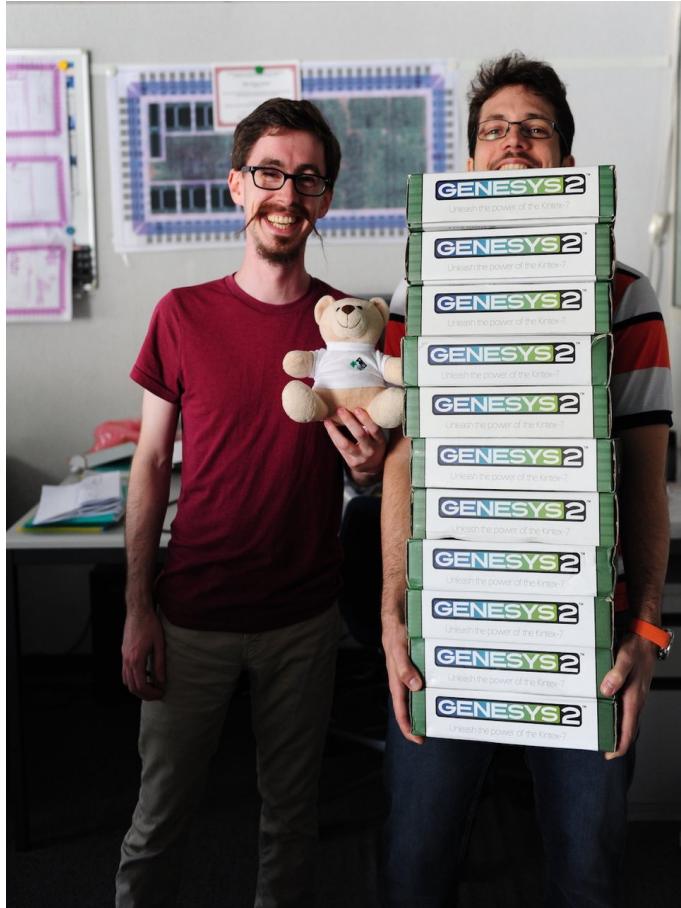


pulp-platform.org

ETH zürich

Who are we?

- Jonathan Balkind
 - Lead architect of OpenPiton
- OpenPiton Team
 - Led by Prof. David Wentzlaff
 - Princeton Parallel Research Group
 - Open source HW since 2015
 - 13 PhD students
 - 1 Postdoc
 - N undergraduates



- Michael Schaffner
 - Responsible for OpenPiton+ Ariane integration
- PULP Team
 - Led by Prof. Luca Benini
 - ETHZ / Università di Bologna
 - Open source HW since 2013
 - Leaders in RISC-V development
 - Ariane dev: Florian Zaruba, Michael Schaffner and others

Support



FONDS NATIONAL SUISSE
SCHWEIZERISCHER NATIONALFONDS
FONDO NAZIONALE SVIZZERO
SWISS NATIONAL SCIENCE FOUNDATION



Horizon 2020
European Union funding
for Research & Innovation



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Project Overview

- Collaboration between Princeton University and ETH Zurich
- Goal is to develop a permissively licensed, Linux capable manycore research platform based on RISC-V
 - Based on mature, extensible designs
 - Booted SMP Linux in <6 months
 - **The world's first open-source, SMP Linux-booting, RISC-V manycore**
- Ariane 
 - RV64GC Core (with extensions)
 - Linux capable
- OpenPiton
 - Manycore research platform
 - Distributed cache coherence and NoC

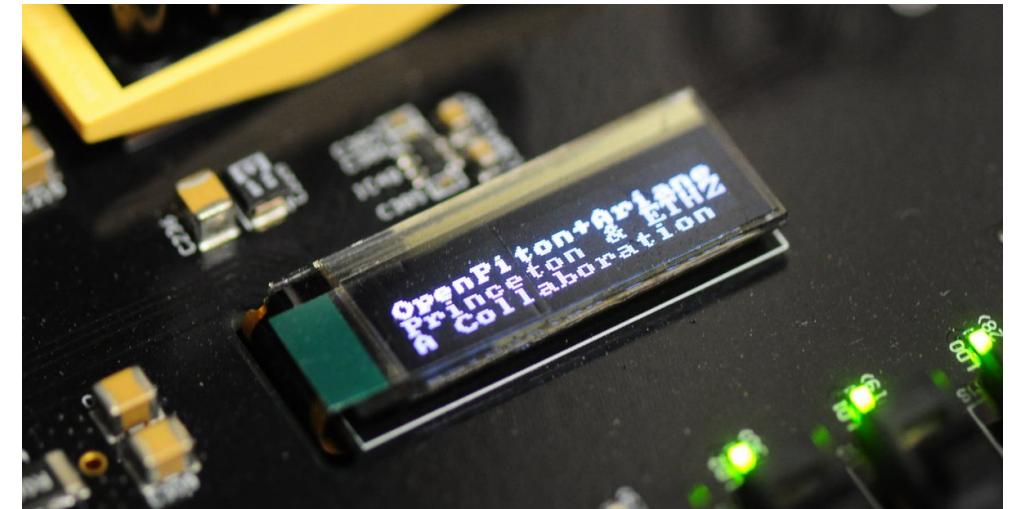
```
processor : 0
hart     : 0
isa      : rv64imac
mmu     : sv39
uarch   : eth, ariane

processor : 1
hart     : 1
isa      : rv64imac
mmu     : sv39
uarch   : eth, ariane

processor : 2
hart     : 2
isa      : rv64imac
mmu     : sv39
uarch   : eth, ariane

processor : 3
hart     : 3
isa      : rv64imac
mmu     : sv39
uarch   : eth, ariane

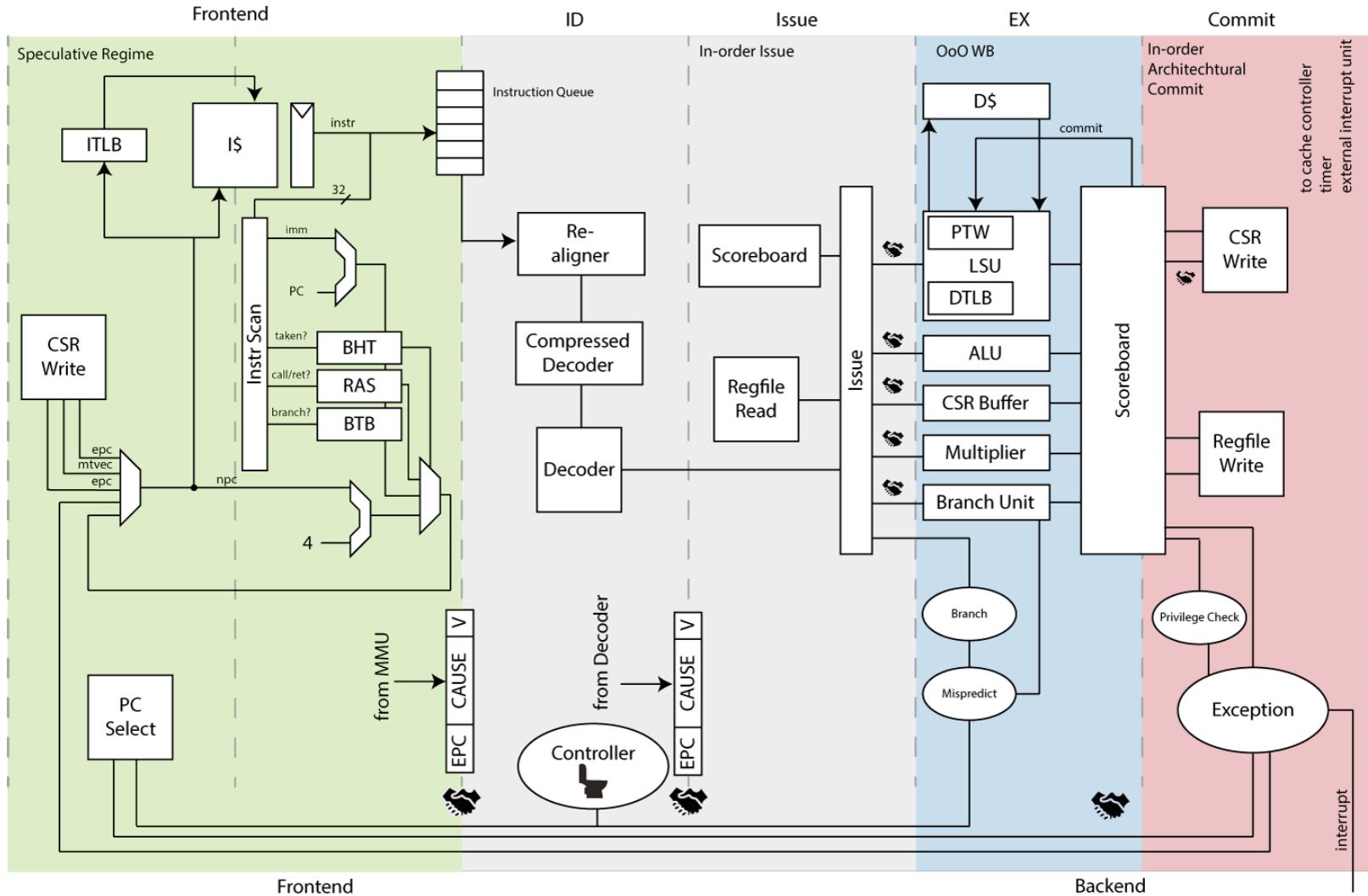
# cd /
```



Ariane RV64GC Core

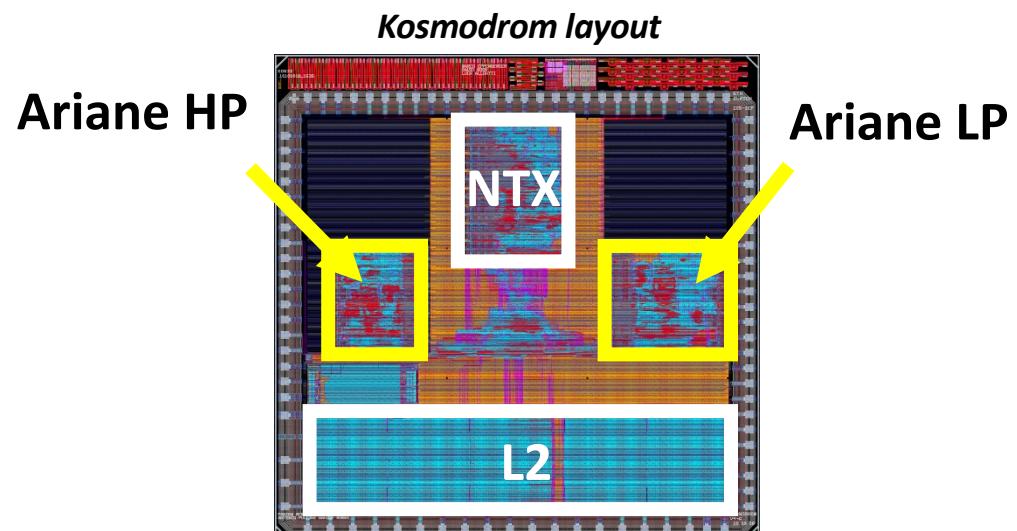
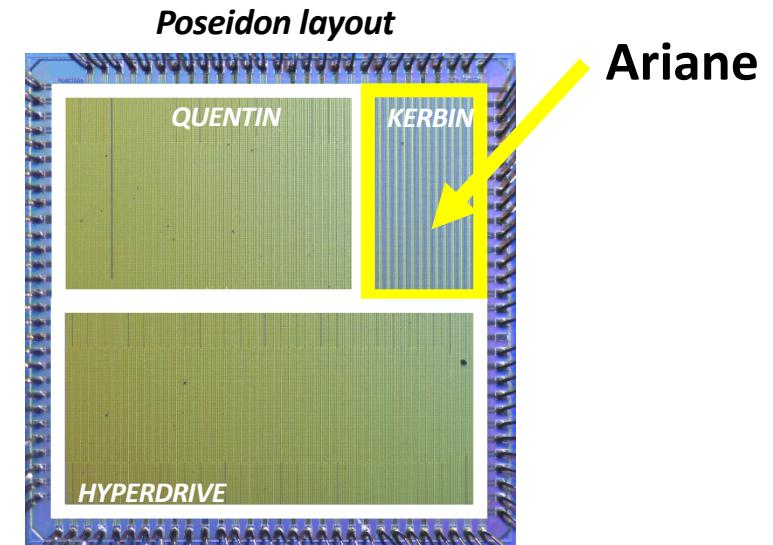
- Application class processor
 - Written in SystemVerilog
- Linux Capable
 - Tightly integrated D\$ and I\$
 - M, S and U privilege modes
 - TLB, SV39
 - Hardware PTW
- Optimized for performance
 - Frequency: 1.5 GHz (22 FDX)
 - Area: ~ 175 kGE
 - Critical path: ~ 25 logic levels
- Scoreboarding
- 6-stage pipeline
 - In-order (single) issue
 - Out-of-order write-back
 - In-order commit
- Designed for extensibility
- Branch-prediction
 - Return Address Stack (RAS)
 - Branch Target Buffer (BTB)
 - Branch History Table (BHT)

Ariane



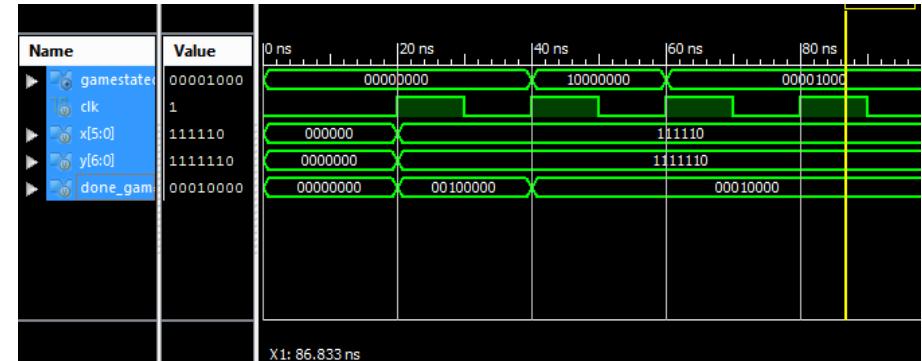
Silicon Proven Designs: Ariane

- Ariane taped-out in **GlobalFoundries 22nm FDX** twice
- 16kB instruction and 32kB data caches
- Poseidon:
 - Area: 0.23 mm² - 175 kGE
 - 0.2 - 1.7 GHz (0.5 V - 1.15 V)
- Kosmodrom:
 - RV64GCxsmallFloat, Transprecision / Vector FPU
 - **Ariane HP**
 - 8T library, 0.8V, 1.3 GHz
 - 55 mW @ 1 GHz
 - **Ariane LP**
 - 7.5T ULP library, 0.5V, 250 MHz
 - 5 mW @ 200 MHz

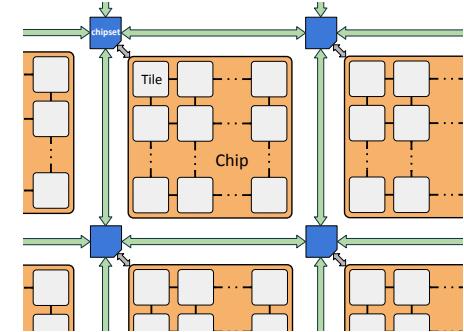


OpenPiton

- Open source manycore
- Written in Verilog RTL
- P-Mesh coherence scales to $\frac{1}{2}$ billion cores
- Configurable core, uncore
- Simulation in VCS, ModelSim, Incisive, Verilator, Icarus
- Includes synthesis and back-end flow
- ASIC & FPGA verified
- ASIC power and energy fully characterized [HPCA 2018]
- Runs full stack multi-user Debian Linux
- Used for Architecture, Programming Language, Compilers, Operating Systems, Security, EDA research

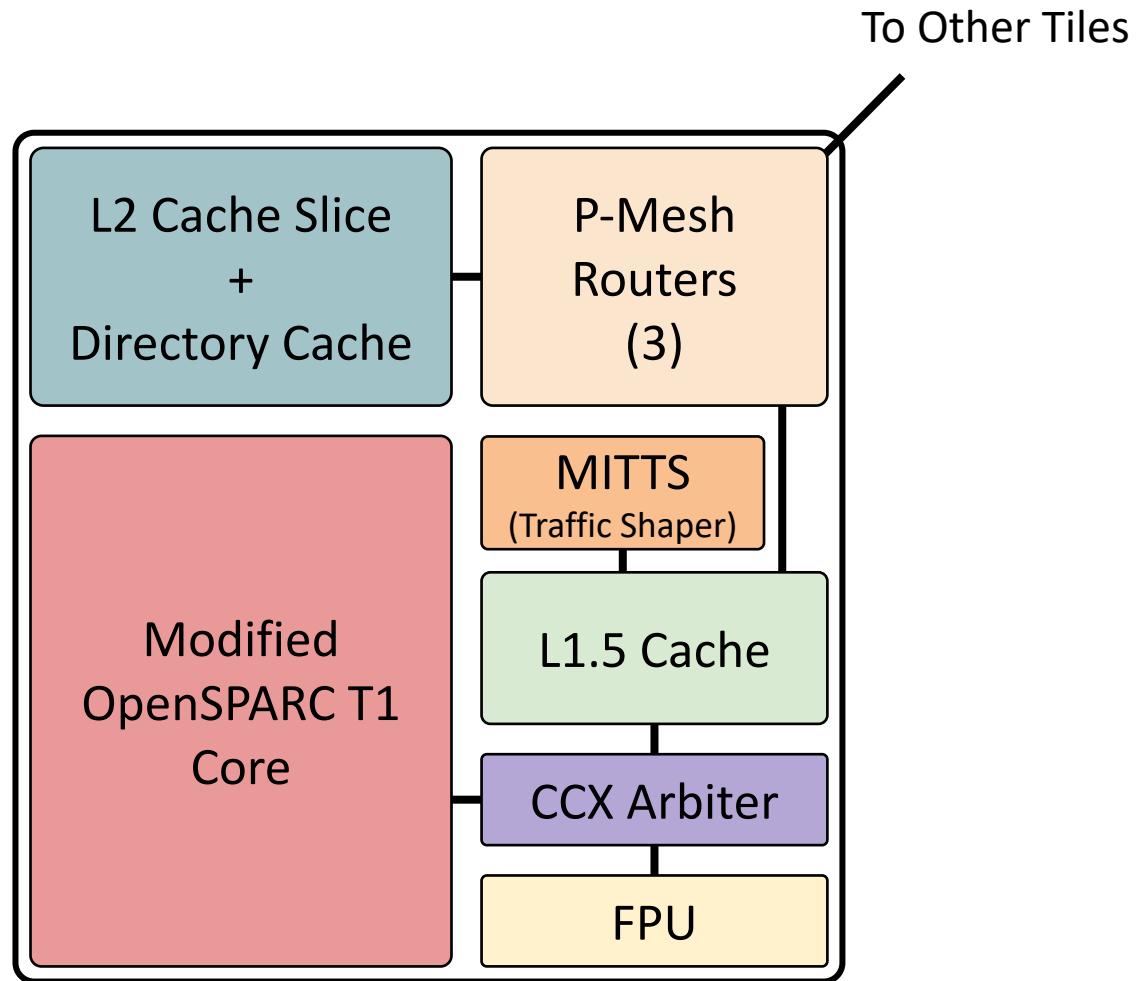


debian



XILINX®

OpenPiton Tile

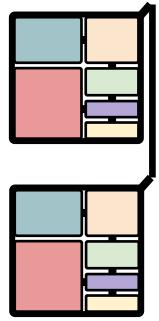


System Overview

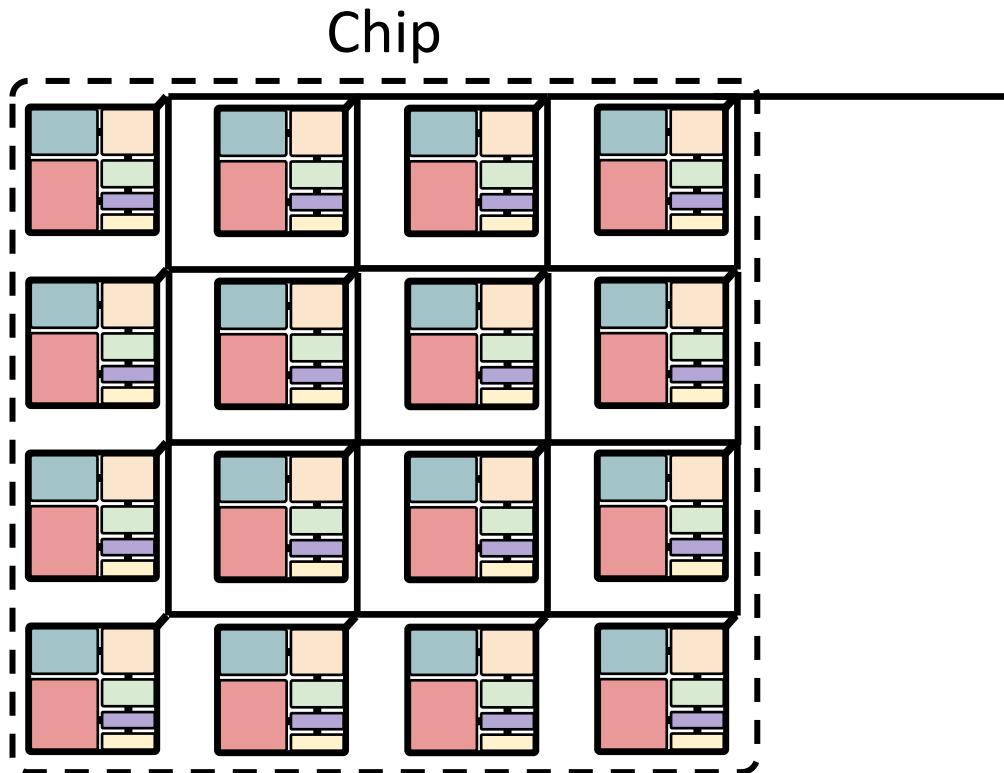
Tile



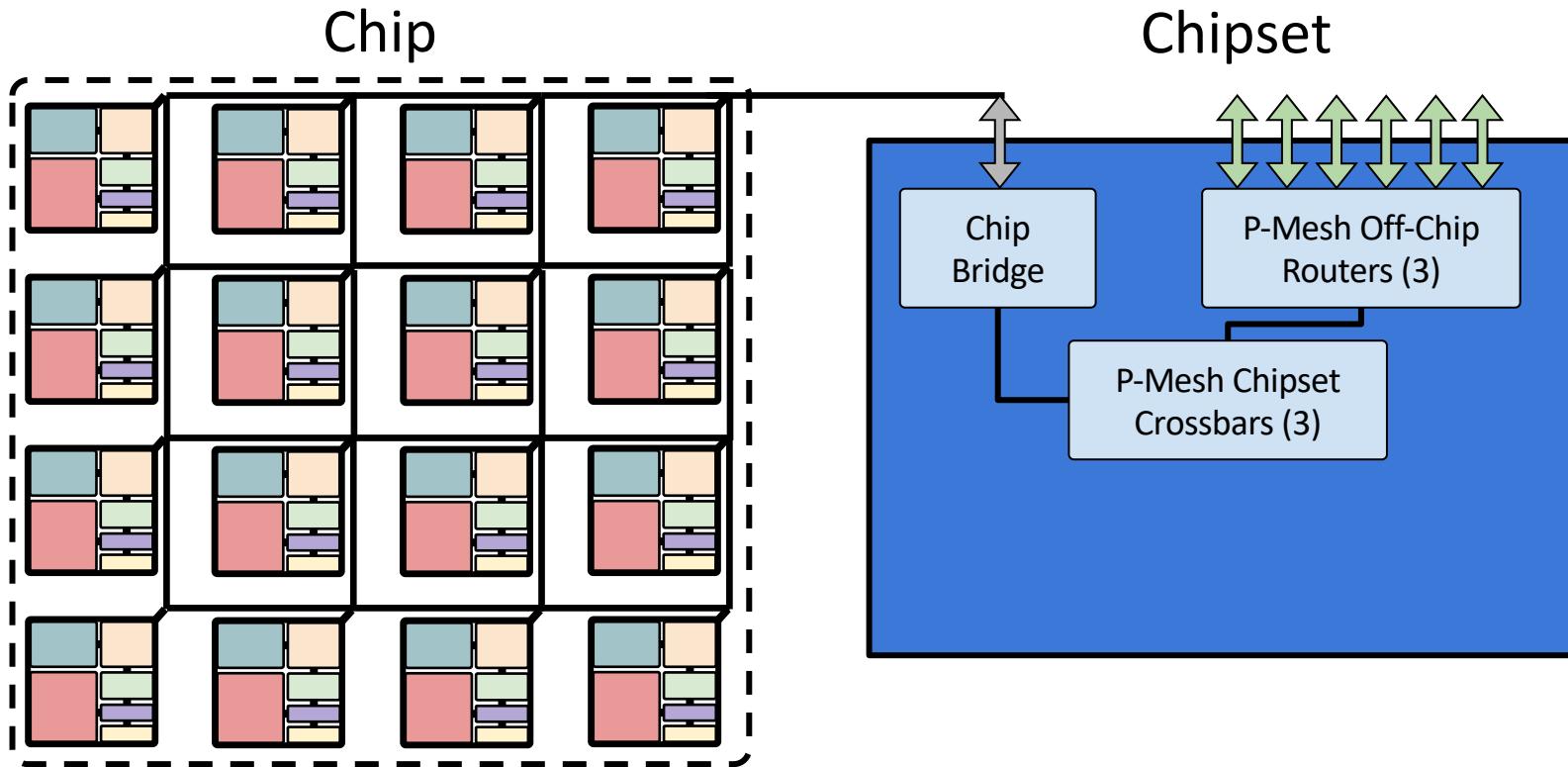
System Overview



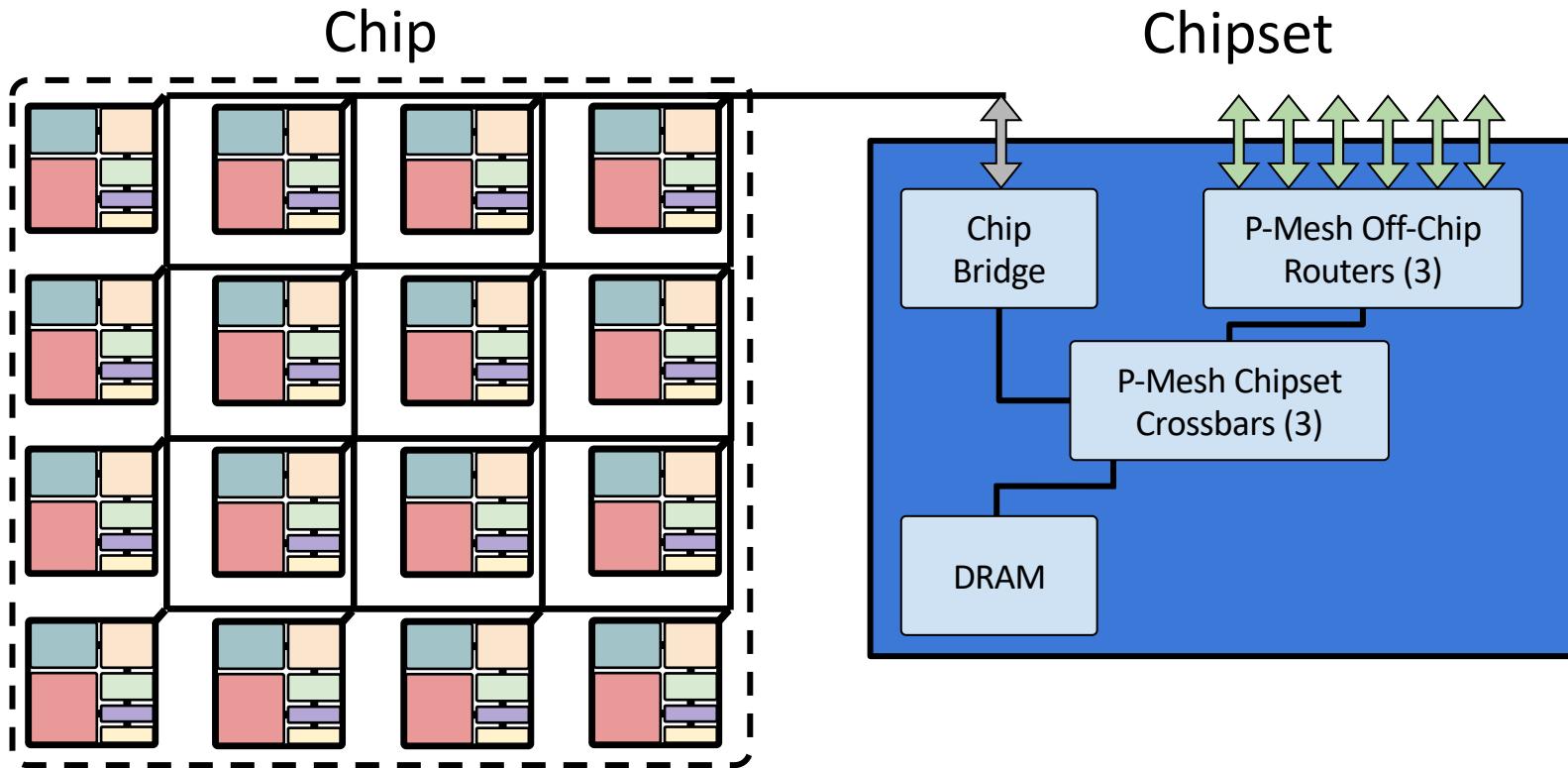
System Overview



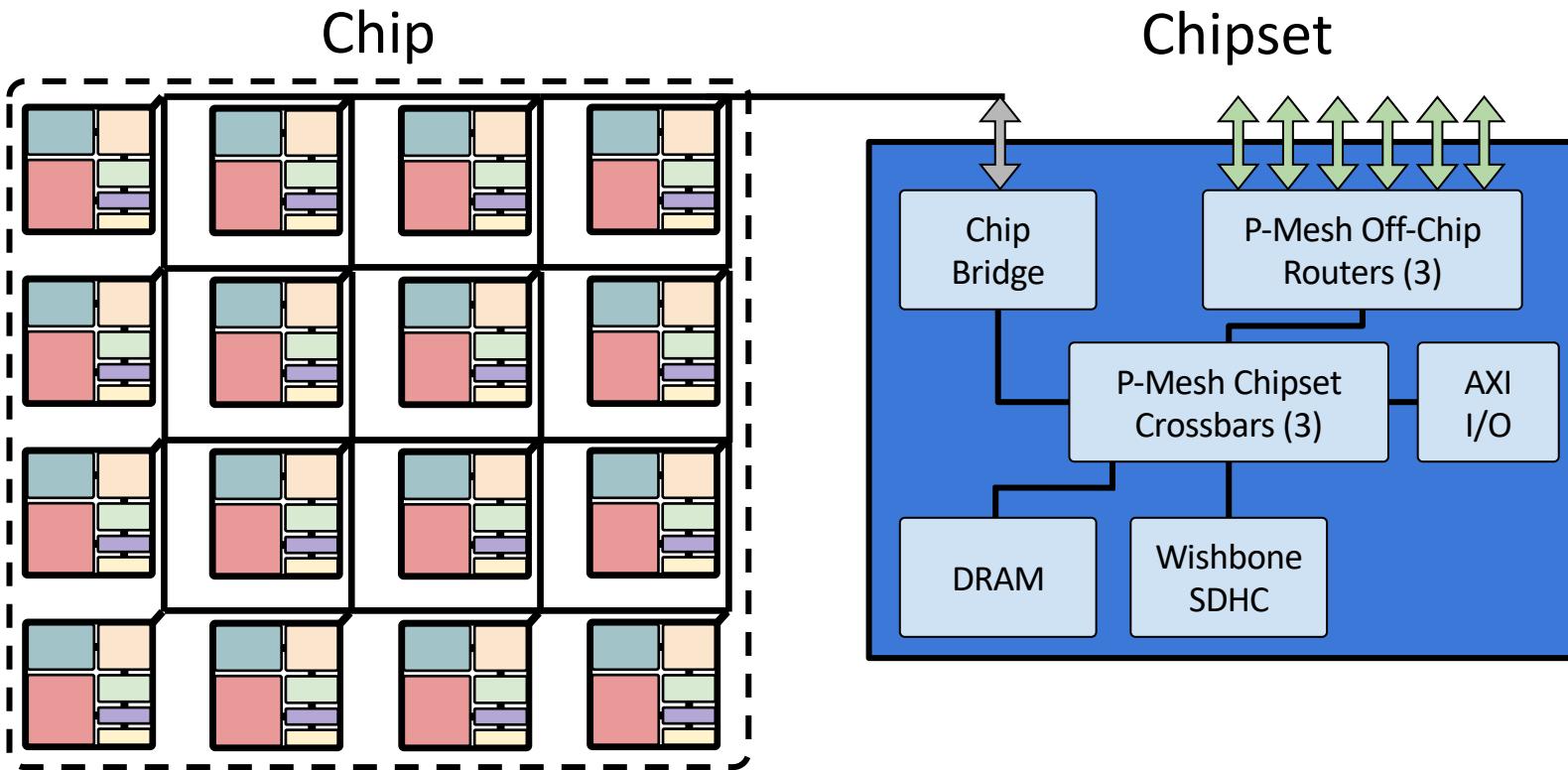
System Overview



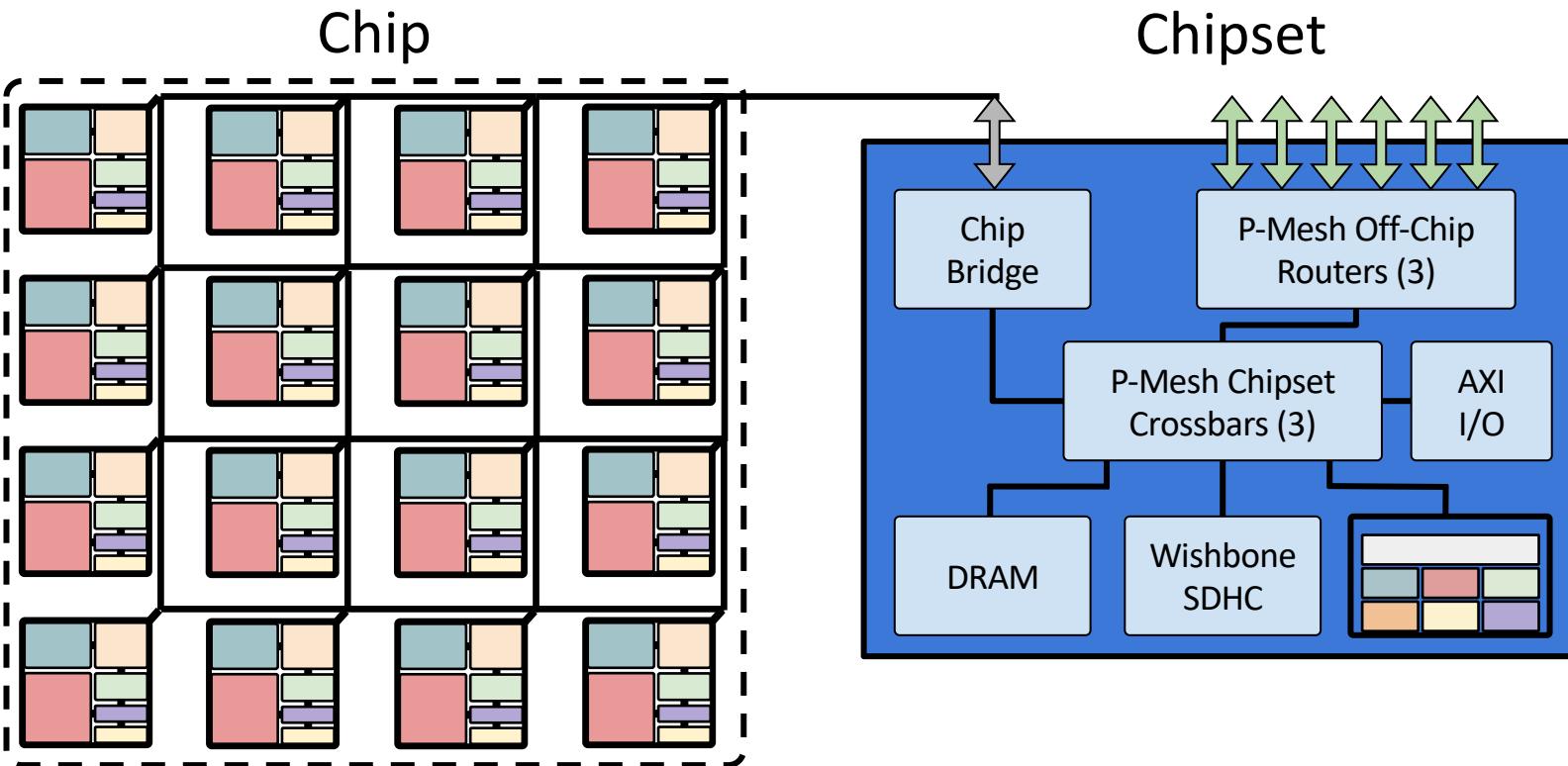
System Overview



System Overview

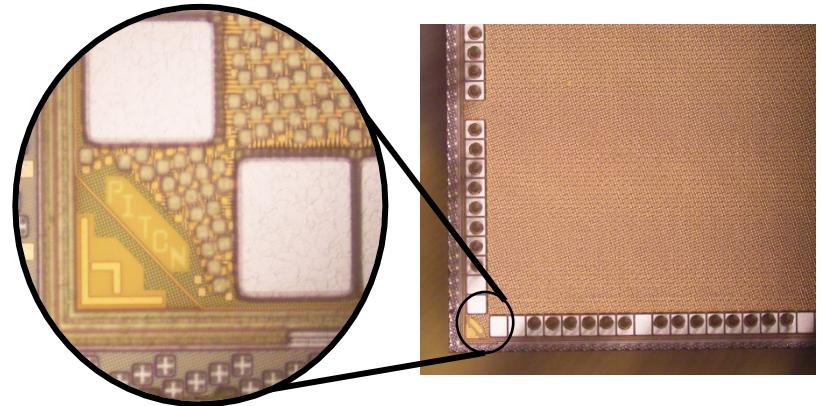
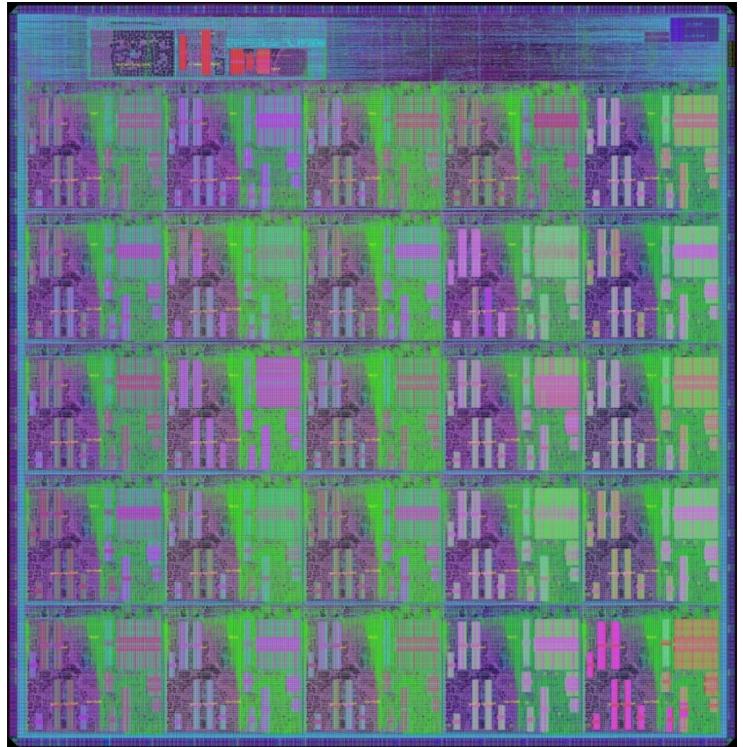


System Overview

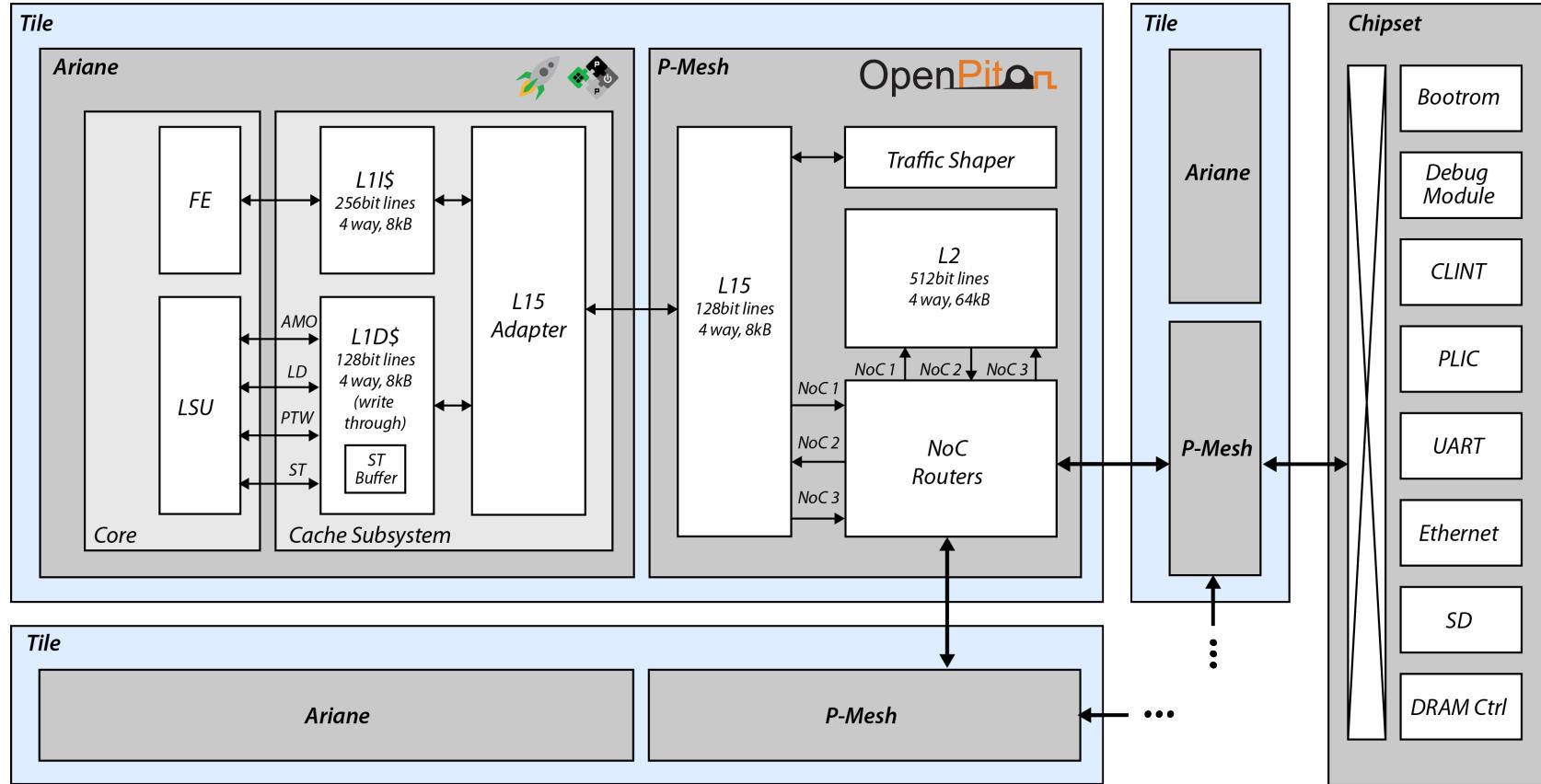


Silicon Proven Designs: Piton

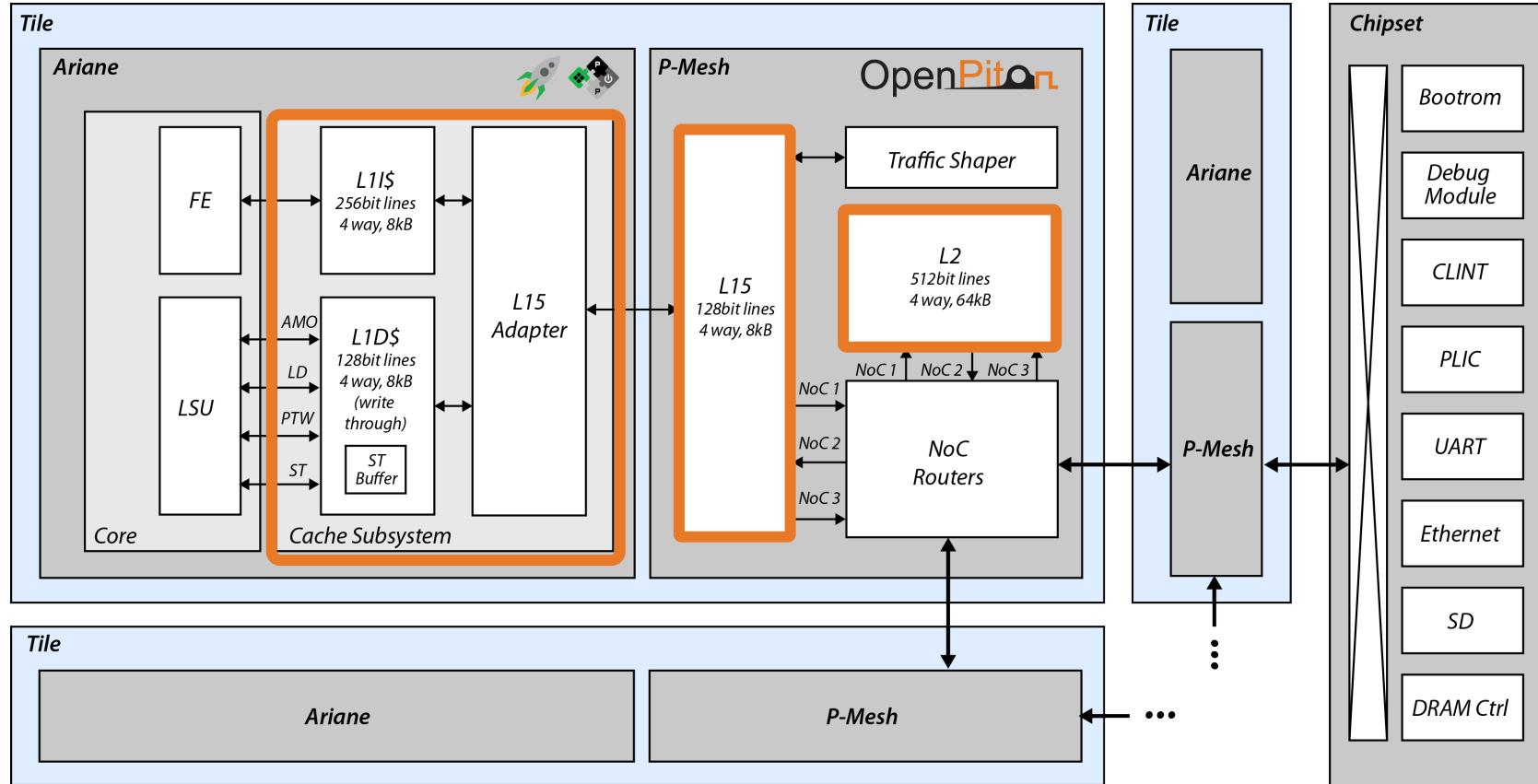
- 25-core
 - 2 Threads per core
 - Modified 64 bit OpenSPARC T1 Core
- 3 P-Mesh NoCs
 - 64 bit, 2D Mesh
 - Extend off-chip enabling multichip systems
- P-Mesh Directory-Based Cache System
 - 64kB L2 Cache per core (Shared)
 - 8kB L1.5 & L1 Data Caches
 - 16kB L1 Instruction Cache
- IBM 32nm SOI Process
 - 6mm x 6mm
 - 460 Million Transistors - Among largest chips built in academia
- Target: 1 GHz Clock @ 900 mV
- Received silicon and runs full-stack Debian in lab



OpenPiton+Ariane

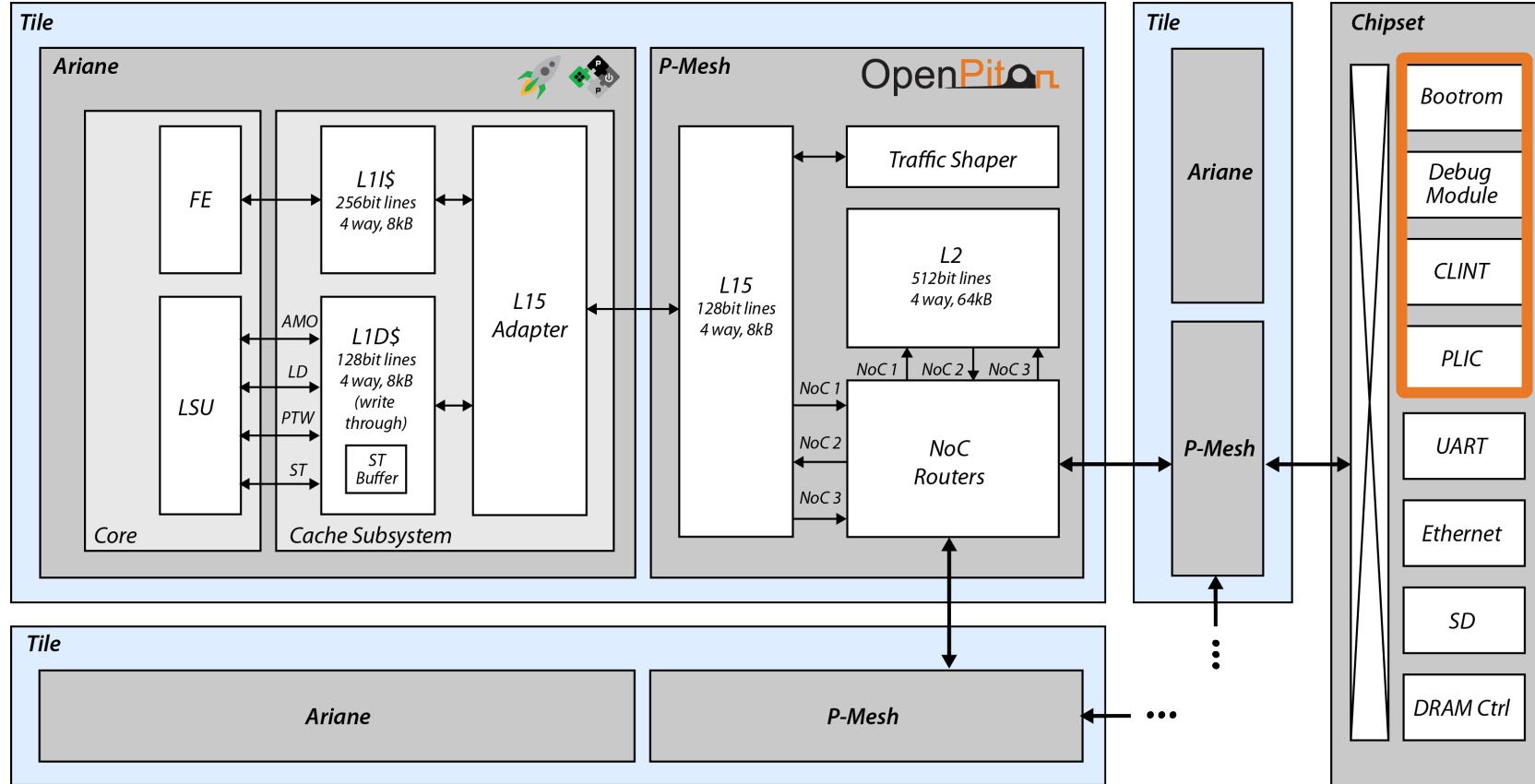


OpenPiton+Ariane Cache Modifications



- New write-through cache subsystem with invalidations and the TRI interface
- LR/SC in L1.5 cache
- Fetch-and-op in L2 cache

OpenPiton+Ariane Platform Support



- Bootrom auto-generated with device tree from configuration
- RISC-V Debug
 - OpenOCD + GDB
 - Bootloading
- CLINT
- PLIC
 - lowRISC rv_plic

Configurability Options

Component	Configurability Options	
Cores (per chip)	Up to 65,536	
Cores (per system)	Up to 500 million	
Core Type	OpenSPARC T1	Ariane 64 bit RISC-V
Threads per Core	1/2/4	1
Floating-Point Unit	FP64, FP32	FP64, FP32, FP16, FP8, BFLOAT16
TLBs	8/16/32/64 entries	Number of entries (16 entries)
L1 I-Cache	Number of Sets, Ways (16kB, 4-way)	
L1 D-Cache	Number of Sets, Ways (8kB, 4-way)	
L1.5 Cache	Number of Sets, Ways (8kB, 4-way)	
L2 Cache	Number of Sets, Ways (64kB, 4-way)	
Intra-chip Topologies	2D Mesh , Crossbar	
Inter-chip Topologies	2D Mesh, 3D Mesh, Crossbar, Butterfly Network	
Bootloading	SD/SDHC Card, UART, RISC-V JTAG Debug	

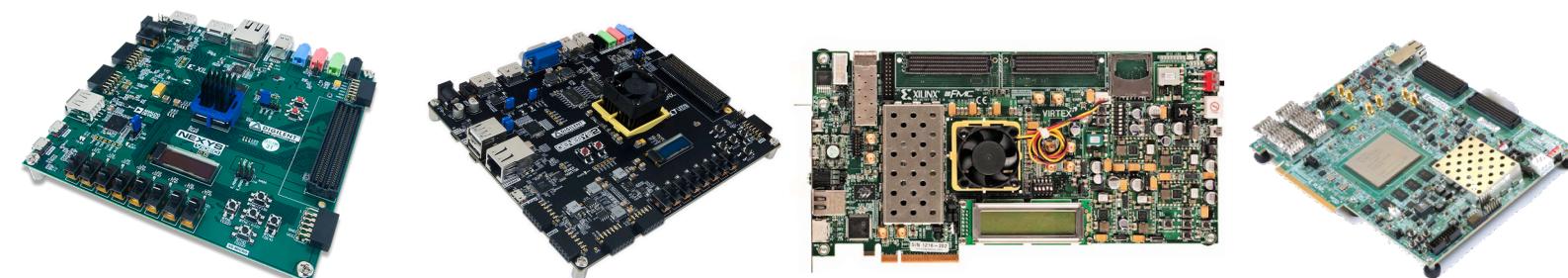
FPGA Prototyping Platforms

Available:

- Digilent Genesys2
 - \$999 (\$600 academic)
 - 1-2 cores at 66MHz
- Xilinx VC707
 - \$3500
 - 1-4 cores at 60MHz
- Digilent Nexys Video
 - \$500 (\$250 academic)
 - 1 core at 30MHz

In progress:

- Xilinx VCU118, BittWare XUPP3R
 - \$7000-8000
 - >100MHz
- Amazon AWS F1
 - Rent by the hour
 - 1-N cores
 - Live demo at tomorrow's tutorial!



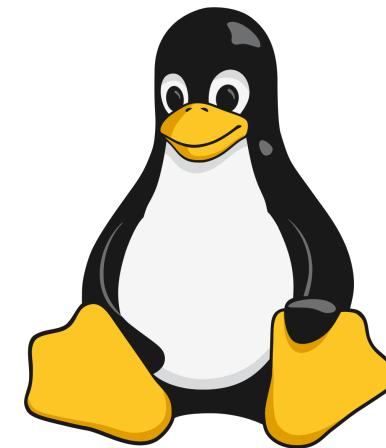
Roadmap

- Testing:
 - Memory consistency testing with litmus/herd/diy
 - Randomised testing with riscv-torture, RISC-V DV
- Bootloading:
 - OpenSBI
 - U-Boot/Coreboot/...
- Debian/Fedora Linux distro
- Performance enhancements
 - Multi-level TLBs
 - Branch Prediction improvements*
 - Increasing TRI/L1.5 line size
 - Multi-issue Ariane*
- Open backend flow for Ariane
- Tapeouts!

* GSoC project with FOSSi Foundation

Boot SMP Linux Today!

- Clone from:
 - <https://github.com/PrincetonUniversity/openpiton>
 - Simulation with Modelsim, VCS, Verilator
 - FPGA implementation with Vivado 2018.2 or newer
 - RV64GC Demo
 - 2 cores on Genesys2 at 66MHz
 - Play Tetris, browse the web!
 - Tutorial tomorrow afternoon! (in this room)
 - Hands-on with Verilator simulation
 - Boot SMP Linux on FPGA
 - http://openpiton.org/ISCA19_tutorial.html



```
processor      : 0
hart          : 0
isa           : rv64imac
mmu           : sv39
uarch         : eth, ariane

processor      : 1
hart          : 1
isa           : rv64imac
mmu           : sv39
uarch         : eth, ariane

processor      : 2
hart          : 2
isa           : rv64imac
mmu           : sv39
uarch         : eth, ariane

processor      : 3
hart          : 3
isa           : rv64imac
mmu           : sv39
uarch         : eth, ariane

# cd /
# ./tetris
```

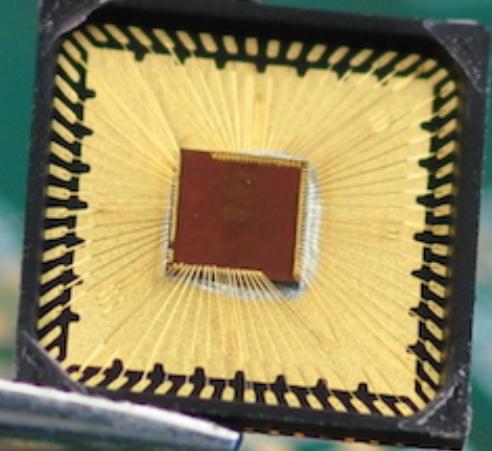
Score
000136

Level
00

Lines
001

Next

QUESTIONS?



@pulp_platform

<http://pulp-platform.org>



@OpenPiton

<http://openpiton.org>

Board Name / FPGA Type	Clock [MHz]	Config $X \times Y$	Core Type	FPU [y/n]	LUTs [k]	Registers [k]	RAM Tiles [#]	DSPs [#]
Digilent NexysVideo Artix 7 7a200tsbg484	30	1×1	Ariane	no	95 (71%)	72 (27%)	66 (18%)	16 (2%)
	30	1×1	Ariane	yes	110 (82%)	75 (28%)	66 (18%)	27 (4%)
	30	1×1	OpenSPARC T1	yes	115 (86%)	96 (36%)	59 (16%)	13 (2%)
Digilent Genesys2 Kintex 7 7k325tffg900-2	67	1×1	Ariane	no	86 (42%)	72 (17%)	66 (15%)	16 (2%)
	67	1×1	Ariane	yes	99 (49%)	75 (18%)	66 (15%)	27 (3%)
	67	1×1	OpenSPARC T1	yes	105 (52%)	91 (22%)	59 (13%)	16 (2%)
Xilinx VC707 Virtex 7 7vx485tffg1761-2	67	2×1	Ariane	no	141 (69%)	113 (28%)	124 (28%)	16 (4%)
	67	2×1	Ariane	yes	167 (82%)	120 (30%)	124 (28%)	54 (6%)
	67	2×1	OpenSPARC T1 [†]	yes	160 (79%)	137 (33%)	112 (25%)	32 (4%)
Xilinx VCU118 Virtex US+ xcvu9pflga2104-2L	60	1×1	Ariane	no	99 (33%)	73 (12%)	63 (6%)	16 (<1%)
	60	1×1	Ariane	yes	114 (37%)	77 (13%)	63 (6%)	27 (1%)
	60	1×1	OpenSPARC T1	yes	119 (39%)	97 (16%)	53 (5%)	16 (<1%)
Xilinx VCU118 Virtex US+ xcvu9pflga2104-2L	60	2×2	Ariane	no	284.1 (94%)	202 (33%)	237 (23%)	64 (2%)
	60	3×1	Ariane	yes	268 (88%)	169 (28%)	179 (17%)	81 (3%)
	60	3×1	OpenSPARC T1 [†]	yes	255 (84%)	208 (34%)	158 (15%)	48 (2%)
Xilinx VCU118 Virtex US+ xcvu9pflga2104-2L	100	1×1	Ariane	no	90 (8%)	81 (3%)	88 (4%)	19 (<1%)
	100	1×1	Ariane	yes	103 (9%)	84 (4%)	89 (4%)	30 (<1%)
	100	1×1	OpenSPARC T1	yes	108 (9%)	100 (4%)	79 (4%)	19 (<1%)
Xilinx VCU118 Virtex US+ xcvu9pflga2104-2L	100	4×4	Ariane	no	923 (78%)	704 (30%)	963 (45%)	259 (4%)
	100	4×2	Ariane	yes	583 (49%)	399 (17%)	495 (23%)	219 (3%)

[†] Without Coherence Domain Restriction [8] in caches.