CSCE-312 SP 2016 Quiz 7 (25 points)

Student Name ……..**Student ID** ……

Question 1. [10 points, 2 points each] Please answer the following questions for a 5-stage pipeline with IF, ID, EX, MEM, and WB stages.

a. **Describe in 1-2 sentences the function of each stage above.**

1) FETCH: Instruction Fetch, Increment PC

2) DECODE: Instruction Decode, Read Registers

3) EXECUTE:
Mem-ref: Calculate Address
Arith-log: Perform Operation

4) Memory:
Load: Read Data from Memory
Store: Write Data to Memory

5) Writeback: Write Data Back to Register

b. **If each stage is 1 clock cycle, calculate the number of clock cycles to execute a code stream of 10 instructions in a non-pipelined (i.e. sequential) fashion?**

= 10* 5 = 50

c. **Repeat part b, assuming the instructions are executed in a pipelined fashion.**

= 5+ 9 = 14

d. **What are the latency and throughput of the pipeline assuming no overheads, stalls, or flushes?**

Latency = 5 and Throughput = 1 per cycle

e. **If pipeline register CLK-Q delay is 30ps and Setup time is 20ps, what stage delay must be designed to achieve a pipeline frequency of 2GHz?**

Answer: 450ps because 2Ghz frequency translates to clock period of 500ps from which we take out the overhead of 50ps resulting in stage delay of 450ps.

Question 2. [5 points] Please put Yes or No for each entry of the table of data dependencies between instructions below in a 5-stage pipeline. The meaning of instructions are shown inline below.

I1: LD R1, MEM(324) /* Load content of MEM(324) into Register R1 */
I2: ADD R1, R2 /* Add R1 to R2 and store result in R1 */
I3: SUB R2, R4 /* Subtract R4 from R2 and store result in R2 */
I4: MUL R3, R2 /*Multiply R3 and R2 and store result in R3 */
I5: ST MEM(324), R1 /* Store contents of R1 into MEM(324) */

	Read After Write (RAW)	Write after Read (WAR)	Write after Write (WAW)
I1 -> I2	X		X
I1 -> I3			
I2 -> I3		X	
I2 -> I5	X		
I1 -> I5	X	X	

Question 3. [10 points] Use the following code fragment in a hypothetical assembly language. Explanations for instructions are given inline:

LD R1, MEM(R2) ***/*Loads contents of Memory location pointed by R2 into R1 */***
ADD R1, R2 ***/* Adds R1 and R2 and stores the result in R1*/***
ST MEM(R2), R1 ***/*Stores contents of R1 into Memory location pointed by R2 */***
ADD R2, 4 ***/* Adds R2 and immediate constant 4 and stores the result in R2 */***
SUB R3, R2 ***/* Subtract R2 from R3 and store result in R3 */***

Assumption: The registers can be written and read in the same cycle, during the write register stage. Also assume that all stages are same length and there is no overhead between stages.

Notation: Pipestages F, D, A, M, W refer to Fetch, Decode, ALU, Memory, Write Register. S refers to Stall. Fill in the table below using this letter notation.

NOTE: The numbers in the first row show clock cycle advancement. The entries for first two instructions are already filled in the table to show pipeline chart. Write S for any given clock cycle where the pipestage is stalled.

Cycle#>>	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
LD	F	D	E	M	W												
ADD		F	S	S	D	E	M	W									
ST					F	S	S	D	E	M	W						
ADD								F	D	E	M	W					
SUB									F	S	S	D	E	M	W		